

Ultra Low Power (ULP) Challenge in System Architecture Level : New architectures for 45- nm, 32-nm era

Sato, Toshinori
System LSI Research Center, Kyushu University

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Ultra Low Power (ULP) Challenge in System Architecture Level

- New architectures for 45-nm, 32-nm era -

ASP-DAC 2007 Designers' Forum
9D: Panel Discussion: Top 10 Design Issues

Toshinori Sato (Kyushu U)



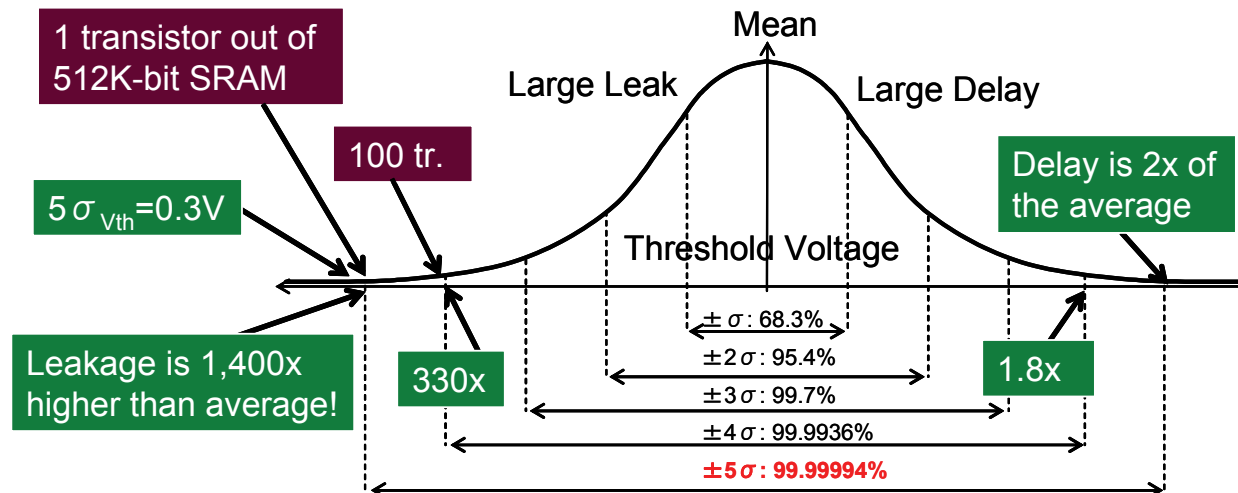
Global View Helps ULP Design

- Only to reduce power is not enough
 - Variation tolerance,
 - Soft error tolerance, and still
 - High performance
- High-level consideration of power reduction is required
 - Software optimization increases flexibilities of design
 - Speculation can create new frontiers for optimizations
 - Architecture selection can change characteristics of circuits
- Variation-aware (VA) ULP design examples



VA ULP Cache Architecture

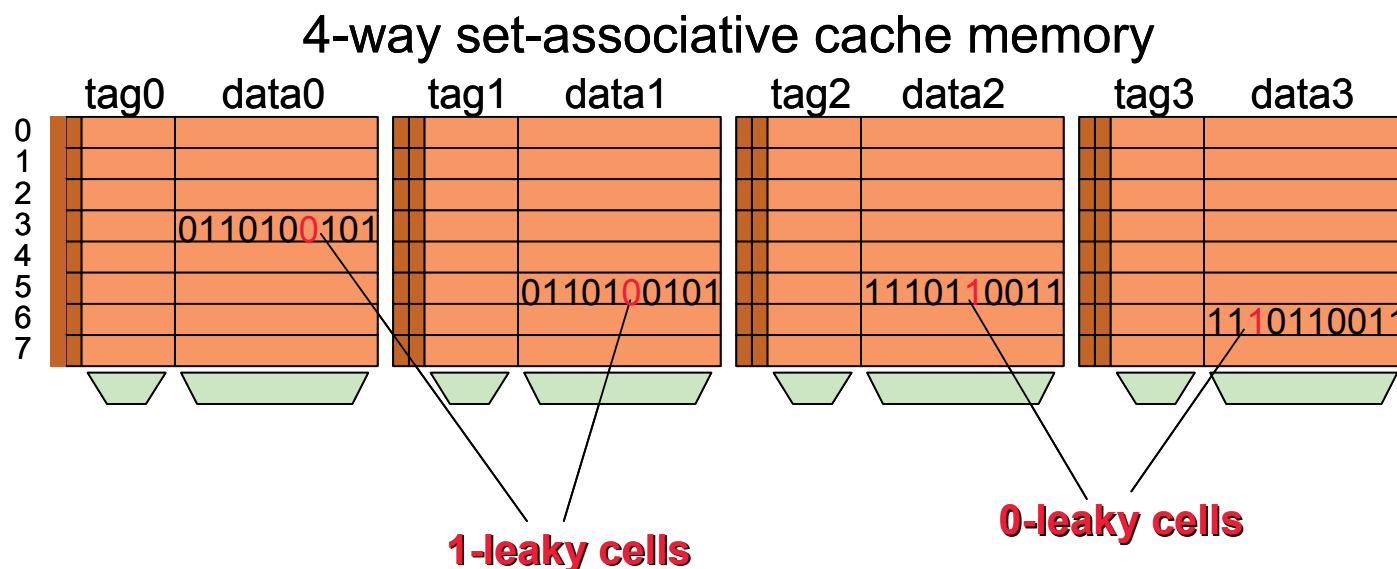
- Process variations create ultra leaky transistors
 - Fortunately, leakage current of an SRAM cell depends on the logic value stored





VA ULP Cache Architecture

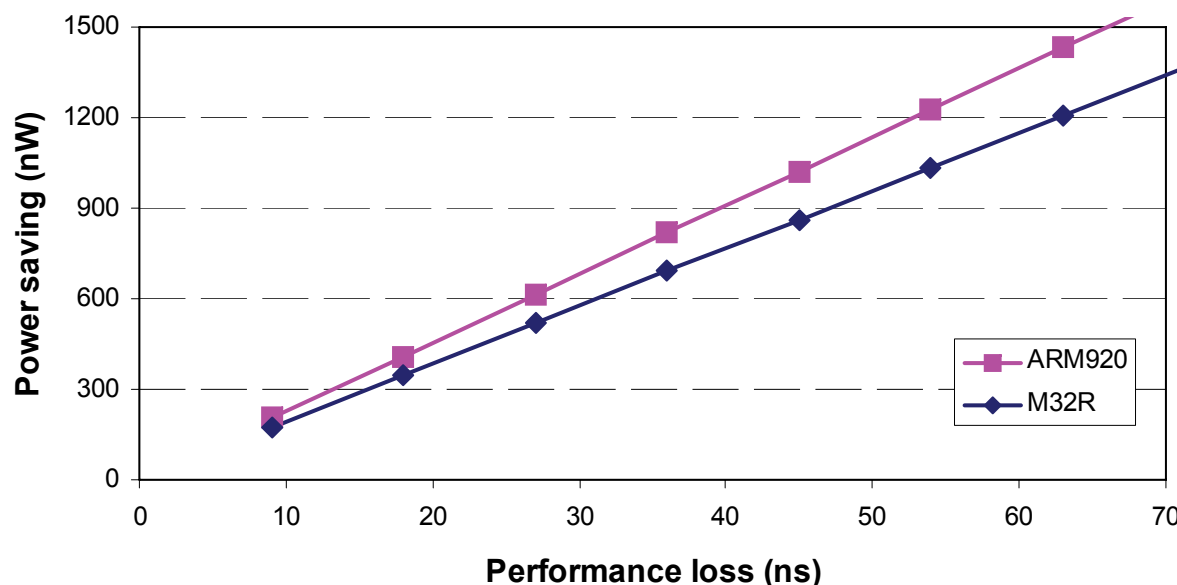
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- Store leakage-safe values on entering into standby mode





VA ULP Cache Architecture

- Process variations create ultra leaky transistors
 - Fortunately, leakage current of an SRAM cell depends on the logic value stored
- Store leakage-safe values on entering into standby mode
- Power saving with negligible performance penalty

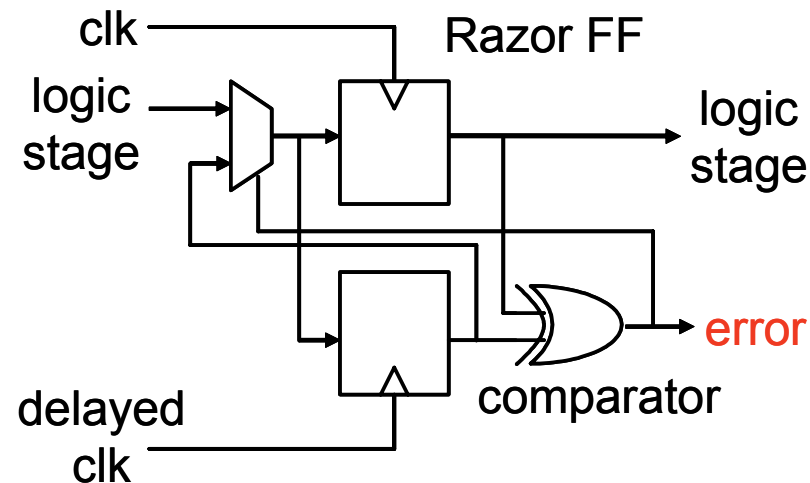
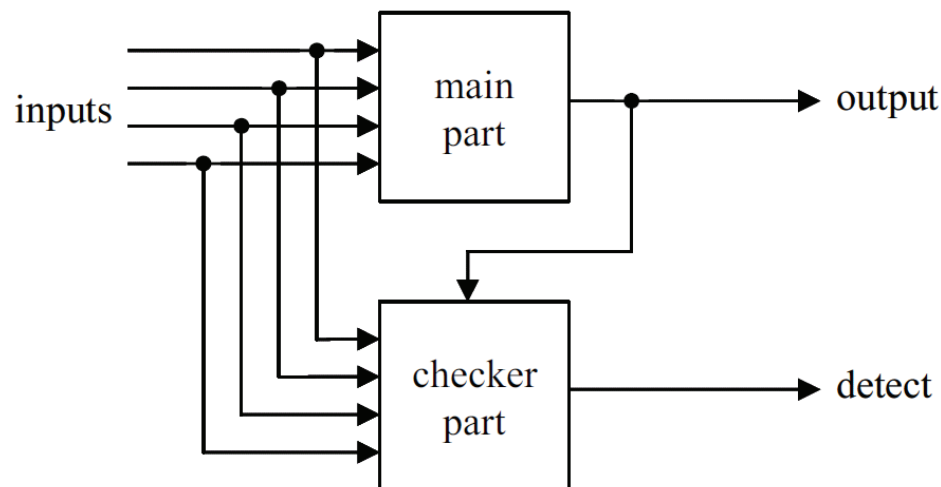


M. Goudarzi: A Software Technique to Improve Yield of Processor Chips in Presence of Ultra-Leaky SRAM Cells Caused by Process Variation, Session 9A @Room 411+412, just NOW.



VA ULP Logic Architecture

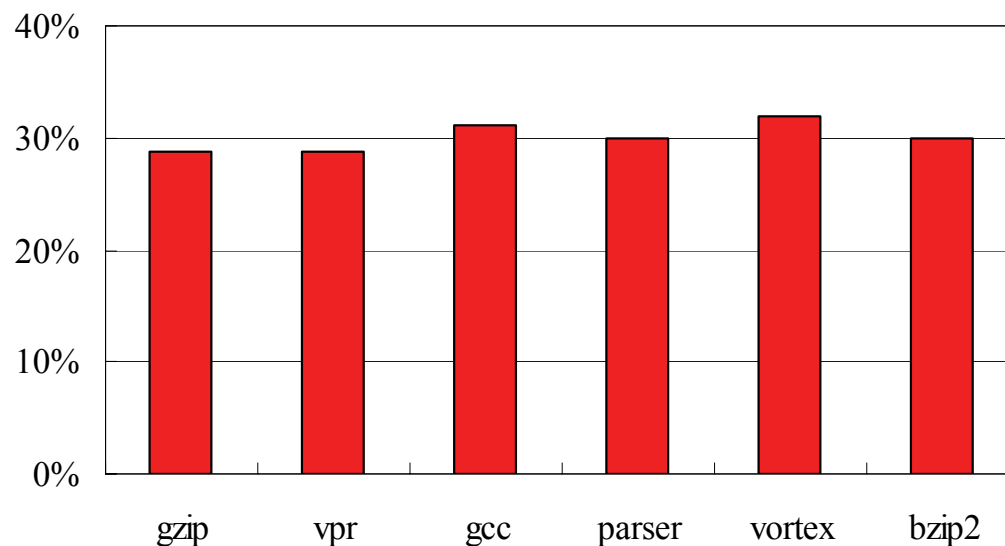
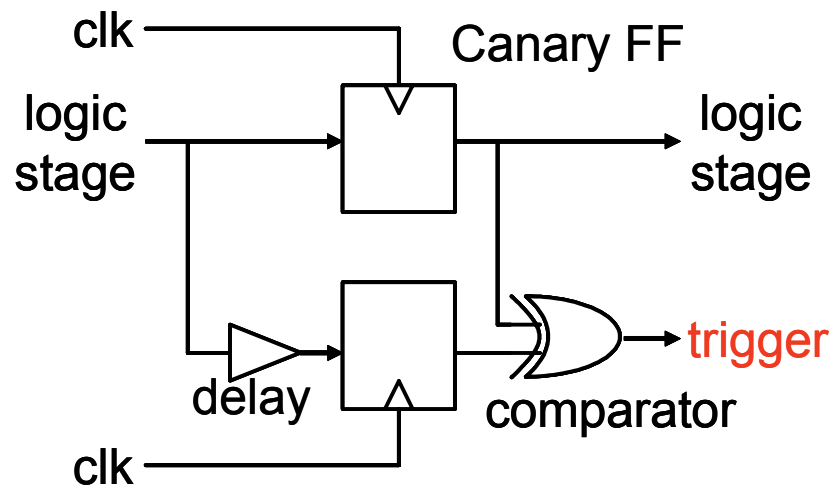
- Typical-case design
 - Optimizing not for worst cases but for typical cases
 - Combination of two circuits
 - Main for power reduction
 - Checker for correctness
- Examples
 - Razor FF





VA ULP Logic Architecture

- Typical-case design
 - Optimizing not for worst cases but for typical cases
 - Combination of two circuits
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 - Checker for correctness
- Examples
 - Razor FF
 - Canary FF
- Potential of over 30% of energy reduction
- Ltd. soft error tolerance





VA ULP CMP Architecture

- Statistical characteristics of circuit delay
 - As the number of critical paths increases, the mean delay increases and **the standard deviation decreases**
- CMP with simple CPU cores
 - reduces critical path delay, and increases the number of critical paths
 - is more variation-tolerant

