QUBE : A Practical Education Program for System LSI Designers

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https://qube. slrc.kyushu-u.ac.jp/

Outline

- QUBE (Q–shu University hardware/software Borderless system design Education program)
- Education Program for
  - SoC Engineers
    - System Designers
    - Hardware (Logic) Engineers
    - Embedded Software Engineers
  - Engineers in industry

Hardware Design   HW/SW Co-design   Embedded Software Design

- July, 2005 to March, 2010
- QUBE developed in 2005
  - A curriculum for SoC Designers
  - Exercise centric course materials

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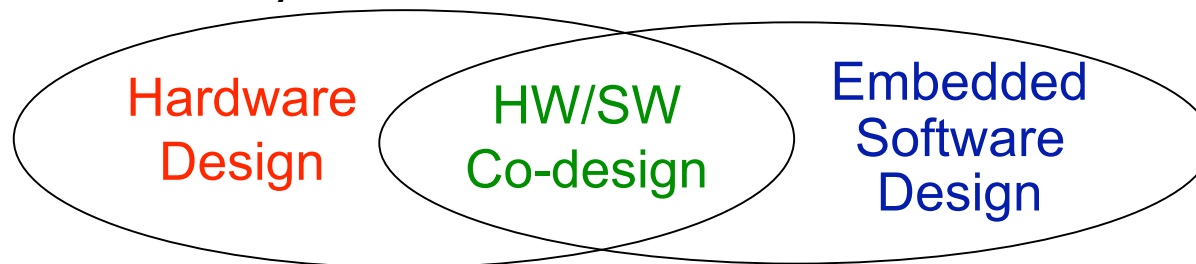
Motivation

- Difficult to design SoCs considering aspects of:
  - Hardware
  - Software
  - Whole of System
  - Business
- Universities dose not provide lectures to understand whole of system in Japan
  - individual technologies only
- Industries under heavy cost competitions cannot use big budgets for educating engineers
- It is not cost effective to develop course materials which should be improved in each industries or universities
- Technologies are improved vecy quickly.

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Mission

- **Educate SoC Designers**
  - Hardware Engineers
  - Embedded Software Engineers
  - System (HW/SW codesign) Engineers
- **QUBE provides practical classes:**
  - invites top professors / industrial engineers of individual technical domain
  - Exercise Centric

QUBE System

- Funded by Ministry of Education, Culture, Sports, Science and Technology, Japan.
- A Curriculum Committee consists of All of Lecturers of QUBE.
- QUBE provides classes according to the curriculum committee's decision.
- QUBE obtains questionnaire from students and lecturers for feedback to the curriculum and classes.

Curriculum Committee

Classes

Questionnaire

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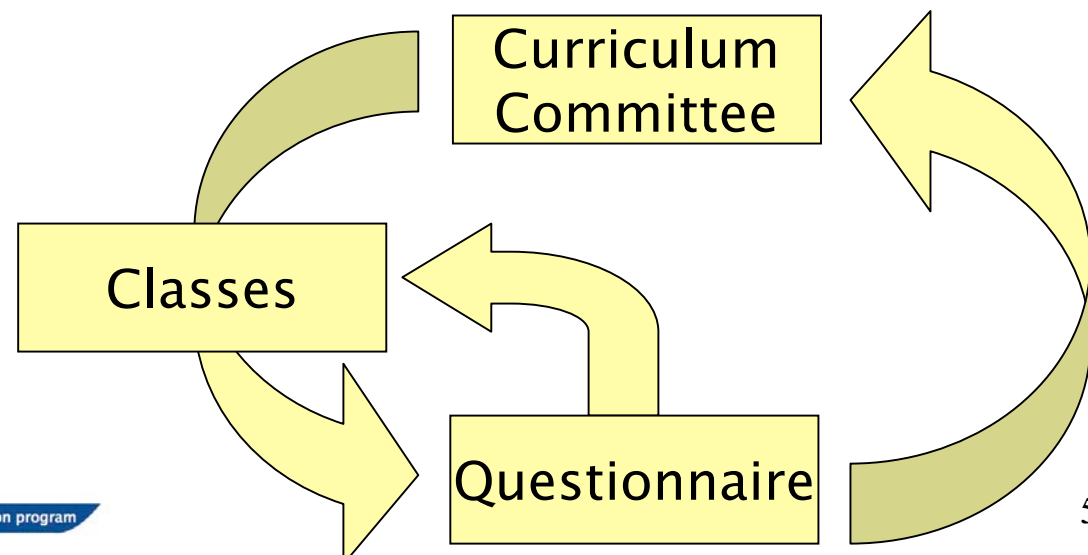
QUBE System

- We have a plan to form a advisory committee
  - The curriculum committee is too big to discuss and revise the curriculum appropriately.
  - The advisory committee consists of someone from industries and someone from universities.
  - To obtain opinions from industries.
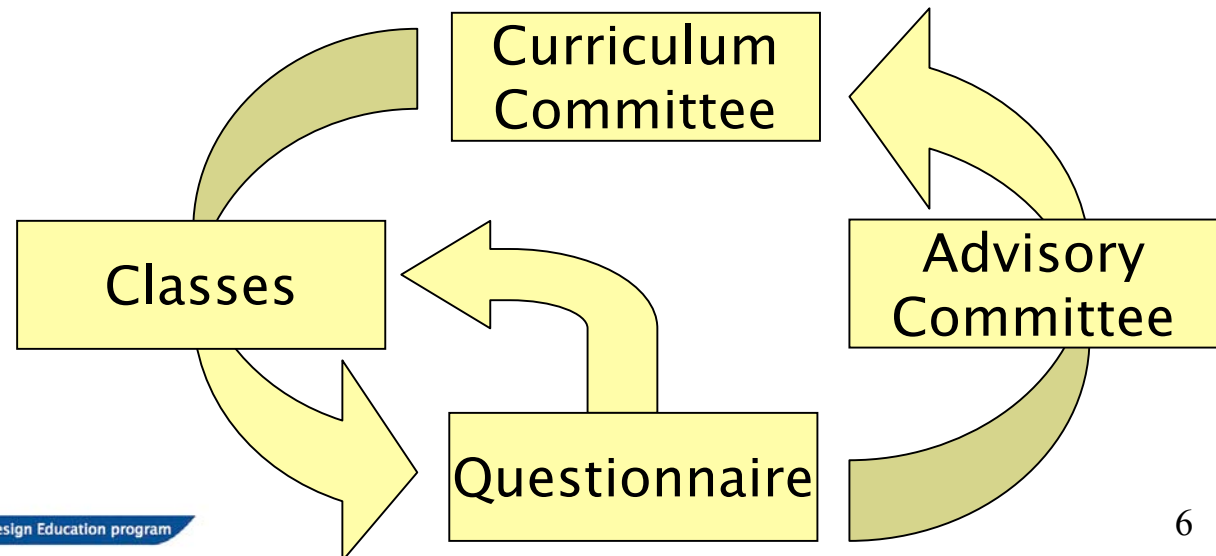
Curriculum

System LSI Design Training Program

- long-term class
- Project Based Learning

System LSI Design Course

- System LSI Design Training (2005 -)
- Software Product Lines Training (2006 -)
- Production Chip Evaluation (2006 -)

Advanced Design Technology Program

- Educating deeply professional design technologies
- short-term classes (average 2day)

Hardware Design Technology Course

noise, power/signal integrity, RF, large-scaled design

Embedded Software Design Technology Course

development methodologies, test, RTOS, middleware

HW/SW Co-Design Technology Course

ASIP, C-based design and low-power design

Technology Management Knowledge Course

intellectual properties, management of technology

SLD: System LSI Design Training Class

- Motivation
  - Educate System LSI Design knowledge and skills to hardware, embedded software, and co-design engineers
  - Educate practical design and implementation skills
- Originally developed
- Party-Exercise:
  - Leader: HW/SW co-design architects (1 person)
  - hardware engineers (2 or more person)
  - embedded software engineers (2 or more person)
  - engineers who belong to different industry
- HW/SW Co-design:
  - Lectures
  - Tutorials
  - Exercise using processor embedded FPGA board

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SLD: Course Plan

- Lecture (1st, 2nd day am)
  - What is System LSI?
  - Basics of HW/SW development
    - basics of hardware design for software engineers
    - basics of software development for hardware engineers
  - System LSI and Costs
  - HW/SW Co-Design
  - Low-power system development
- Tutorials (1st, 2nd day pm)
  - familiarize students with development environment and board
- Exercise (3rd – 8th day)
  - Gives a target system spec and some IPs.
  - A team designs:
    - HW/SW partitioning
    - write documents
  - A team implement a target system according to the documentations.

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The Target System of Exercise

Multimedia (Sound & Whiteboard) Phone

Call Target List
1: xxxx-xxxx
2: yyyy-yyyy
:

Call Target List
1: zzzz-zzzz
2: xxxx-xxxx
:

Whiteboard Sharing

Talk by Mic & Speaker

| 1 | 2 | 3 | 4 | 5 | < | > | R |

| 1 | 2 | 3 | 4 | 5 | < | > | R |

Call Target Selection

Exchanger
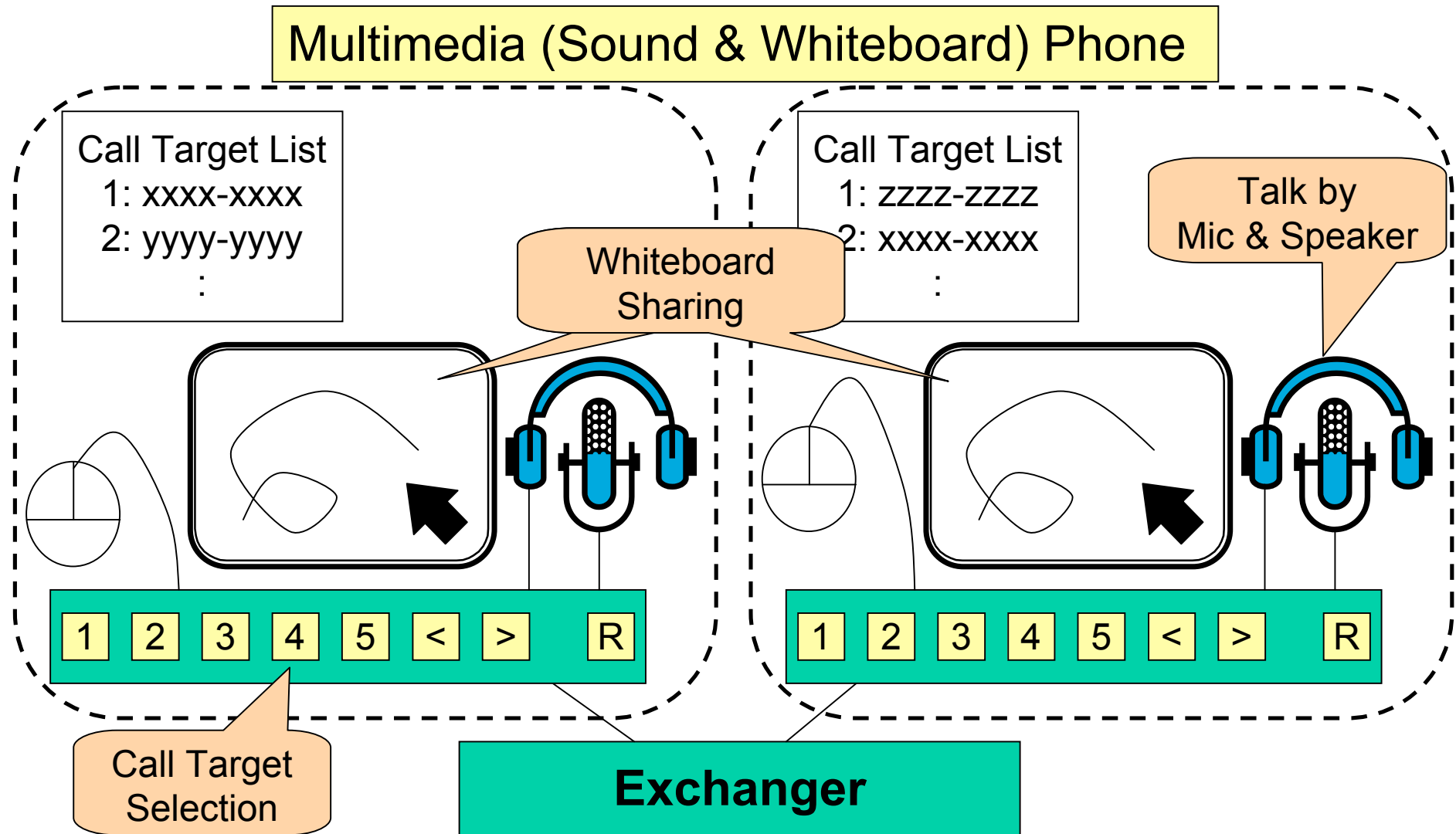
SLD: Environment

Multimedia Phone Emulator

Talk

White Board Shareing
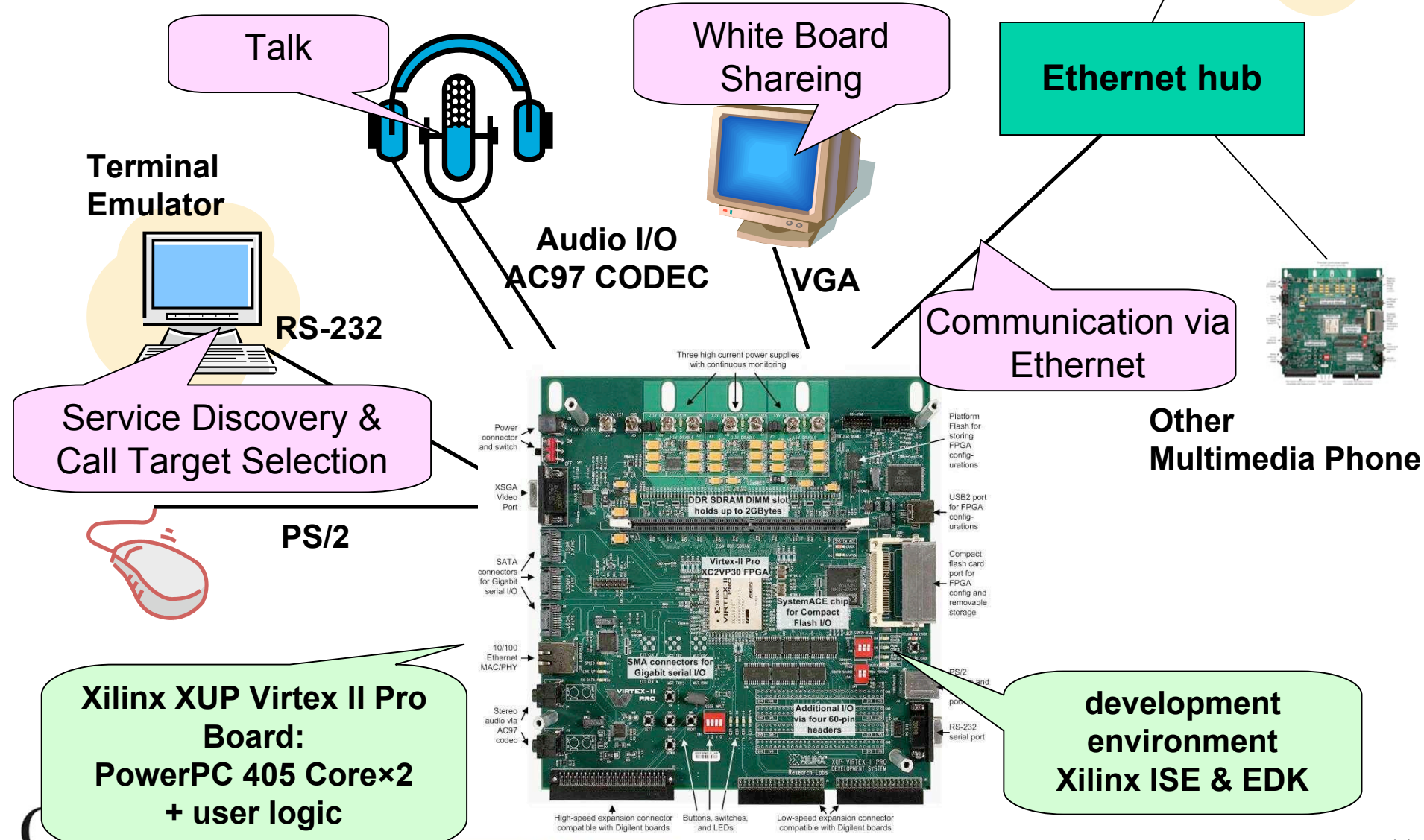
Ethernet hub

Terminal Emulator

Audio I/O AC97 CODEC

VGA

RS-232

Service Discovery & Call Target Selection
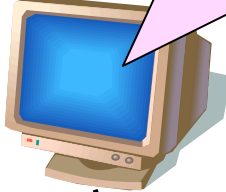
Communication via Ethernet

Other Multimedia Phone

PS/2

Xilinx XUP Virtex II Pro Board: PowerPC 405 Core×2 + user logic

development environment Xilinx ISE & EDK

Three high current power supplies with continuous monitoring

Power connector and switch

Platform Flash for storing FPGA configurations

XSGA Video Port

DDR SDRAM DIMM slot holds up to 2GBytes

USB2 port for FPGA configurations

SATA connectors for Gigabit serial I/O

Virtex-II Pro XC2VP30 FPGA

Compact flash card port for FPGA config and removable storage

SystemACE chip for Compact Flash I/O

10/100 Ethernet MAC/PHY

SMA connectors for Gigabit serial I/O

PS/2 keyboard and mouse port

Stereo audio via AC97 codec

Additional I/O via four 60-pin headers

RS-232 serial port

VIRTEX-II PRO

XUP VIRTEX-II PRO DEVELOPMENT SYSTEM Research Labs

High-speed expansion connector compatible with Digilent boards

Buttons, switches, and LEDs

Low-speed expansion connector compatible with Digilent boards

Q-shu University hardware/software Borderless system design Education program
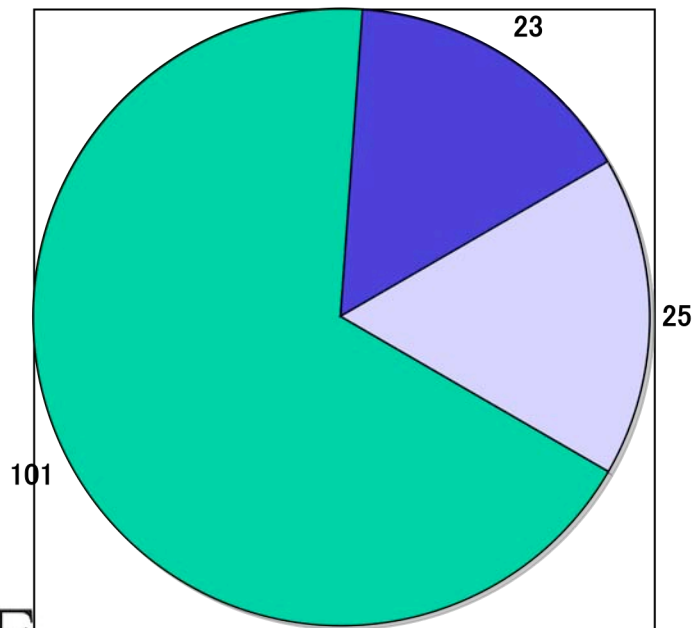
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1st run at 1st – 10th, March 2006

- Students
  - 5 students from industry
    - CO: 1, HW: 2, SW: 2
  - 2 students from university
    - SW: 2, (HW: 1 from staff)
- Course
  - Lecture / Tutorials (2 days)
  - Design (2.5 days)
    - eUML
    - PLUS (Product Lines)
  - Implementation (3 days)
    - implement MMP in software only
  - Presentation (0.5 days)
    - Peer review

- Questionnaire
  - Industry wants system design courses.
  - They wants a course for newcomer (this course too difficult for newcomer)
  - too short to implement whole of system in 8 days
  - Development Methodologies
- Now, we tackles:
  - To develop course materials for beginner
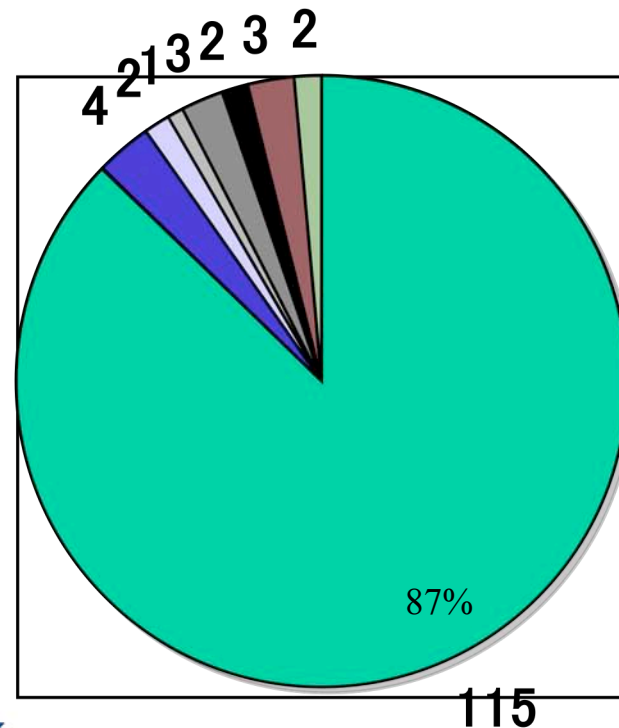 - To develop a course including development process

Project activities in 2005

- 16 classes (35 days) in 18 weeks
- 40 organizations / 106 registered applicants
- 149 applicants (8.3 per class)
- 80% applicants comes from industrial or research org
- Most of applicants comes from Fukuoka area
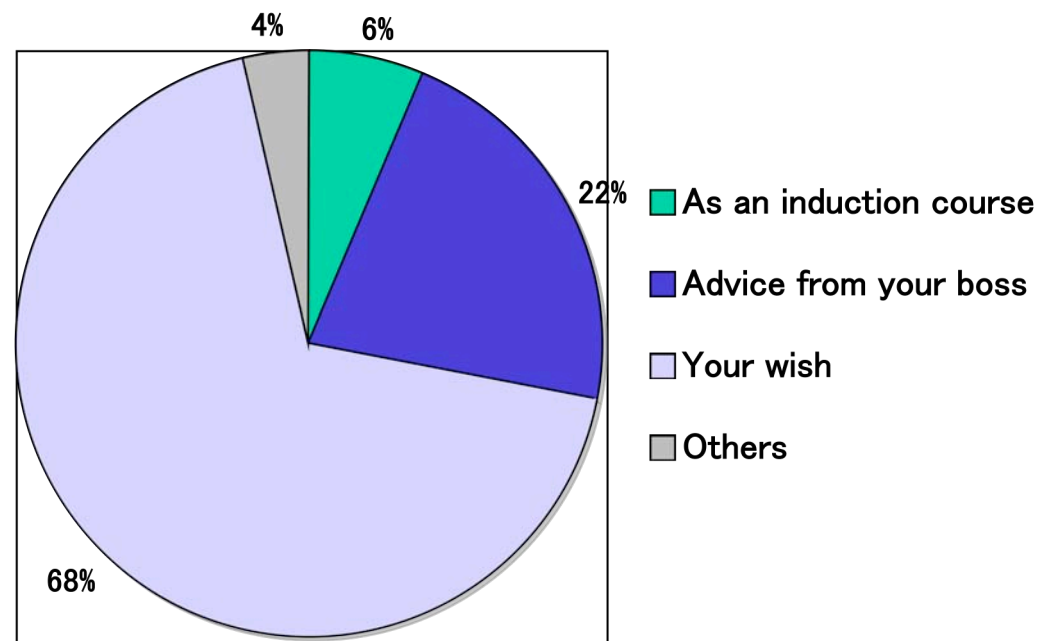

# of Applicants

# of Applicants of each area

23
25
101

4 2 1 3 2 3 2
87%
115

Fukuoka
Saga
Oita
Hyougo
Osaka
Aichi
Kanagawa
Tokyo

Industries Non-Industries Students

Project activities in 2005

- Most of motivations to take QUBE class is applicants' wish
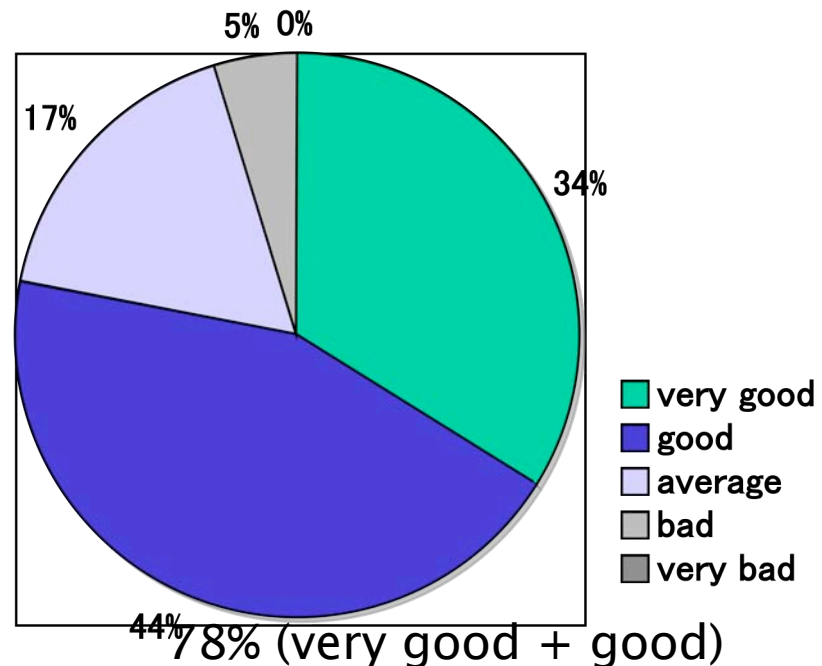- Engineers in industry have motivations to educate themselves

What occasion did you take this class?

4%   6%

22% ▢ As an induction course

     ▢ Advice from your boss

     ▢ Your wish

     ▢ Others

68%

Project activities in 2005

- Students feels good to our classes
- Publicity of the QUBE is not enough
  - But... applicants are registered half of capacity in average (8.3 applicants / class)
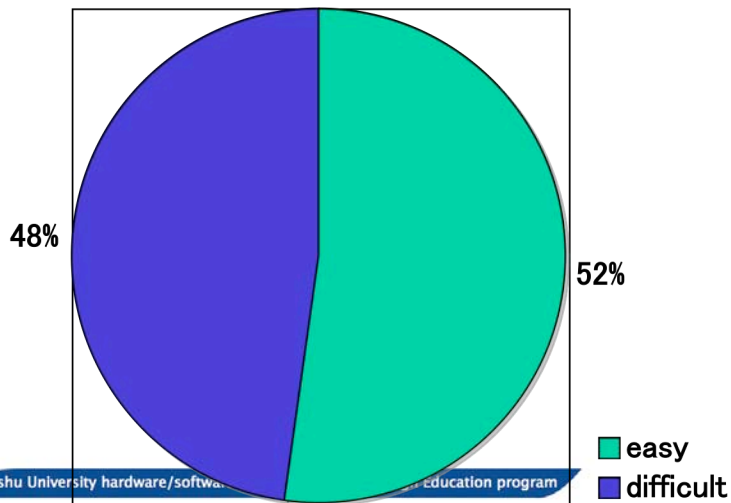
How was you satisfied with your prospect?

5% 0%

17%

34%

☐ very good
☐ good
☐ average
☐ bad
☐ very bad

44% 78% (very good + good)

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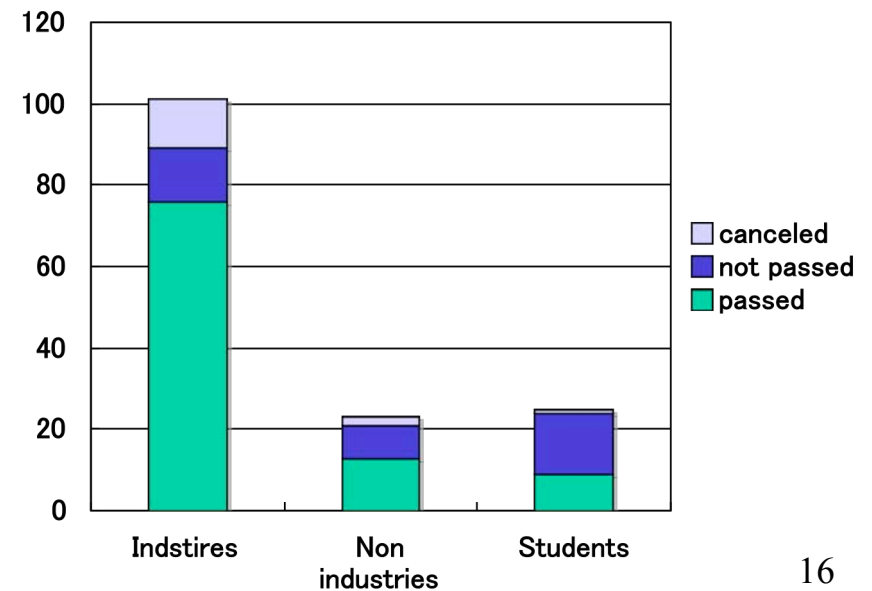
However ...

- Pass ratio: Average: 74% (Non-students 82%, Students 38%)
  - 10% applicants canceled or absent classes due to business accident
  - Not passed: 34 students
    = 22 students attend but not submit their reports+ absentee 12 students
  - Why they do not submit reports?
- Level of some classes is too high
  - pass ratio of some class is lower than 50%
  - Some students luck basic knowledge to understand lecutres.
  - to improve pass ratio
    - We should show course required levels explicitly.
    - We should provide pre-learning materials in some couse.

How did you feel about level of the lecture?

48% 52%

□ easy
■ difficult

Statistics of Applicants

120
100
80
60
40
20
0

Indstires   Non industries   Students

□ canceled
■ not passed
■ passed

Applicants' Statistics of Classes in 2005

	Total			Pass	Questionnaire	
	Registered	age	passed	Ratio		
Total	149	33.3	98	74%	109	83%
SLD-HW : Hardware Design Training	3		2		2	
SLD-SW : Embedded Software Training	4	30.7	4	100%	3	86%
SLD-CD : HW/SW Co-Design Training	1		1		1	
A-HW1 : Noise problems in SoC	9	33.0	4	44%	7	78%
A-HW2 : A/D・D/A Converter in SoC	8	35.3	6	86%	6	86%
A-HW3 : EDA Algorithms	3	35.3	3	100%	3	100%
A-HW4 : Power/Signal Integrity Problems	14	31.1	7	58%	11	92%
A-HW5 : RF Analog Circuit Design for Wireless System	15	32.4	5	36%	9	64%
A-HW6 : Test Design for LSI	4	29.5	4	100%	4	100%
A-HW7 : Large-Scaled High-Performance System LSI Design	4	30.7	3	100%	3	100%
A-SW1 : Embedded Software Development Methodology	9	32.7	7	78%	6	67%
A-SW2 : Software Test Methodology	12	31.4	9	90%	7	70%
A-SW3 : Realtime OS and Middleware	9	31.8	7	88%	7	88%
A-CD1 : HW/SW Co-Design	11	31.4	4	44%	6	67%
A-CD2 : LSI Design using C Language	10	35.9	4	57%	7	100%
A-CD3 : Low-Power Design	10	31.1	8	89%	9	100%
A-MG1 : Intellectual Properties in Business	7	35.9	6	86%	6	86%
A-MG2 : Design Process and Management of Technologies	16	40.4	14	100%	12	86%

Sumarry

- QUBE (<u>Q</u>-shu <u>U</u>niversity hardware/software <u>B</u>orderless system design <u>E</u>ducation program)
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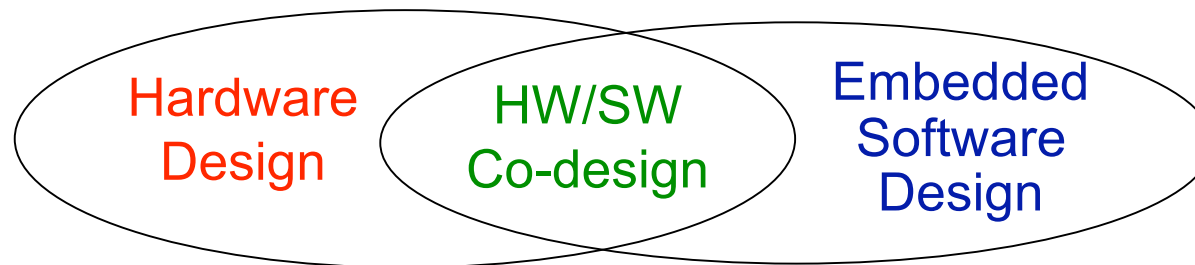
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Thank you for your attention!