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Development of PPRAM-Link Interface (PLIF) IP Core for High-Speed Inter-SoC Communication

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Abstract— We are proposing "PPRAM-Link": a new high-speed communication standard for merged-DRAM/logic SoC architecture. PPRAM-Link standard is composed of physical/logical layers and an API for the upper software layer, which are standardized by PPRAM Consortium. We developed a PPRAM-Link Interface IP family, or 'PLIF Core" that realizes logical protocols necessary for subaction-level communications, and it can be applied to various applicatioss. In addition, we designed an FPGA-based PCI-to-PPRAM-Link board for inter-PC/WS communications.

I. Introduction

Parallel Processing RAM (PPRAM) is an architectural framework for ASSPs (Application-Specific Standard Products) of any size, any function, or any performance according to the request of applications. DRAM or other memory, MPU or application-specific logic, and a network interface which based on "PPRAM-Link" standard can be integrated into a PPRAM chip. Goals of PPRAM, and the paradigm shift (see Fig.1) that PPRAM architecture brings are summarized below:

1. *Goals of merged-DRAM/logic SoCs:*
   Improve the performance by exploiting high on-chip memory bandwidth and low on-chip memory latency.
   Reduce the power consumption by reducing the necessity to drive off-chip buses. Optimize on-chip memory-path.
   Reduce off-chip memory traffic and EMI.

2. *Goals of parallel/distributed processing:*
   Overcome the limit of instruction-level parallel processing by means intra/inter-chip multiprocessing.
   Give system scalability to SoC by allowing them to scale with application size.
   Ease to design and test and improve reliability.

3. *Goals of high-speed inter-SoC communication standard:*
   Ease to interconnect and inter-operate PPRAM chips provided by different vendors.
   Ease to guarantee the portability of communication software over various PPRAM-based system.
   Ease of design by means of allowing us to focus on the design of parts other than inter-chip communication.

Since 1997, PPRAM Consortium has been making a continuous effort to develop open standard specifications for inter-chip communication, or PPRAM-Link. Foundation of PPRAM-Link logical layer is mainly Scalable Coherent Interface (SCI, IEEE standard 1596-1992). Besides, some modifications are done in the flow-control, initialization protocols and packet formats.

In verify performance of PPRAM-Link standard, and to promote the utilization, it is indispensable to develop a general-purpose logic circuit that realizes minimum logical protocols necessary for subaction-level communications. Besides that, its estimation environment and additional interface logics are also needed. Hence, in this paper, we propose the development of PPRAM-Link Interface IP "PLIF Core" and its PCI bus edition utilizable for the functional estimation.

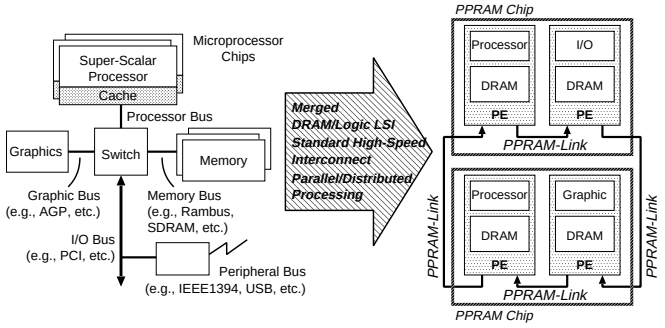

Fig. 1. PPRAM paradigm shift. System designers can construct various computer systems, just by choosing the required PPRAM chips, and by interconnecting them though PPRAM-Link.

II. Digest of PPRAM-Link

PPRAM chips are connected to each other by a one to one single way serial or parallel link, or PPRAM-Link network. The PPRAM-Link standard consists of a logical layer, a physical layer, and an Application Programming Interface (API) for software development, as shown in Fig.2 .

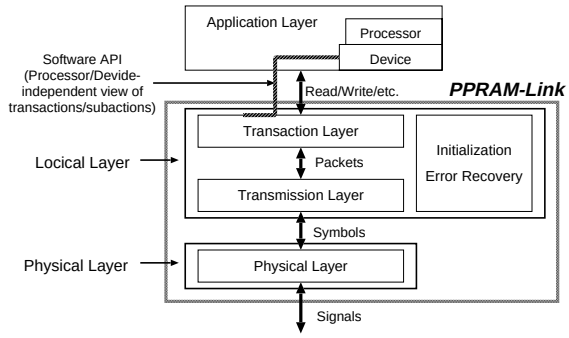

Fig. 2. PPRAM-Link protocol stack. The logical layer also contains bandwidth allocation, queue allocation, and realtime transmission protocols.

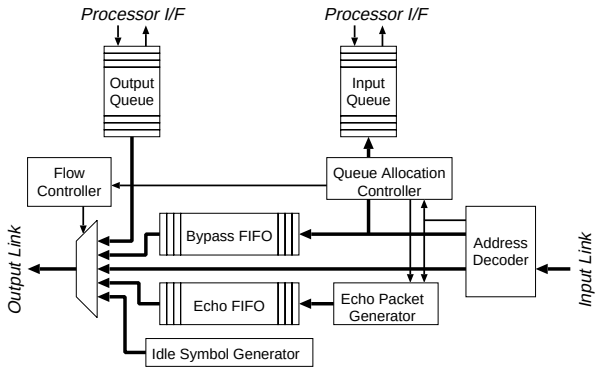

Fig. 3. Organization of PLIF Kernel

The physical layer compensates undistorted and smooth transmissions. It bears the roles that passes electrical/physical signals to the logical layer of its own node as pairs of 16 bit-width symbol and 1 bit-width flag. On the other hand, a set of communication protocols is provided at the logical layer. It possesses a transmission layer, transaction layer, and initialization/error processing protocol. The transmission Layer bears a role of packet-flow control to guarantee the right packet transmission. And at the transaction layer, one transaction instructed by its upper layer is interchanged to two pairs of packet exchange. We define a ringlet as the basic topology, and it is a vertex of the PPRAM-Link network. Each PPRAM node has their own node ID of 16bit-width which is assigned at the ringlet initialization phase. Finally, the application layer corresponds with processor/DMACs by means of data transmission at PPRAM-Link network.

III. PLIF Core

PLIF Core is a hardware realization of PPRAM-Link logical layer, and it conforms to the latest PPRAM-Link standard (version 1.1). It is written in synthesizable VHDL, so it is useful for its functional simulations/estimations and FPGA/ASIC implementations. If the user try to put PPRAM-Link to practical use, an appropriate physical layer should be applyed to it.

PLIF Core is distributed under the GNU General Public License which means that its entire source code is freely-distributed and available to the general public.

Basic block of PLIF Core is called the kernel (see Fig.3), and the following lineup is provided:

TABLE I
Implementation of PLIF PCI Bus Edition

HDL synthesis	Synopsys DesignCompiler
Target Device	Altera FLEX10K100
Mapping tool	Altera MAX+PLUS II
Logic Size	4818 cells (including several SRAM cells)
Internal Clock	33.3MHz (validated)
Platform	Windows98 PC with a PCI card that mounts one FLEX10K100. Two or more PCs are inter-connected uni-directionally through each own PCI-FPGA card.

PLIF Core kernel : It has ringlet input/output ports of 17 bit-width, and simple processor-side I/F. The control logic has function/protocols as follows, subaction-level communication control, node ID assignment at single-ringlet, bandwidth allocation, and primitive-level error detection.

PCI bus edition : PLIF Core kernel + interface logic of PCI bus. The PCI bus logic is connected to the processor-side I/F of the kernel. The PCI bus edition can be implemented to recent FPGA/PLD-mounted PCI boards for purposes of software development. This implementation is outlined in Table 1.

IBM CoreConnect edition : PLIF Core kernel + IBM CoreConnect [1] logic as its processor-side interface. It enable us to interconnect PPRAM chips that are composed of CoreConnect-based IPs.

IV. Summary and Conclusions

In this paper, the development of PPRAM-Link interface (PLIF) IP Core and the PCI bus edition for functional evaluations are proposed. We are now promoting PPRAM-Link and PLIF Core to various fields, and also planning to enrich the PLIF Core lineup. PLIF Core and more PPRAM-Link informations can be obtained from our WWW site [2].

Through these PLIF designs, we are recognizing some problems of packet transmission performance and interface circuit size. So, we have just started to discuss how resolve such problems, and then, to develop new standard that includes to use switch-based and ringlet-based interconnections together.

References

[1] Murakami, K., Shirakawa, S., and Miyajima, H., "Parallel Processing RAM Chip with 256Mb DRAM and Quad Processors", 1997 IEEE International Solid-State Circuits Conference, pp.228–229, Feb. 1997.

[2] PPRAM Project of Kyushu University,
`http://ppram.csce.kyushu-u.ac.jp/`

[3] PPRAM Consortium,
`http://www.ppram.or.jp/`

[1] IBM CoreConnect bus architecture is interface standard that eases the integration and reuse of processor, system, and peripheral cores within standard product and custom SoC designs.