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<https://hdl.handle.net/2324/7443189>

出版情報 : pp.2530-2536, 2024-05-02. IEEE

バージョン :

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Abstract— In recent years, using SiC devices for fast switching have led to the miniaturization of power modules. However, due to the high di/dt of fast switching, false triggering and parallel oscillation caused by high di/dt have become an issue. A method for extracting equivalent circuits, including parasitic inductance, is essential to solve these issues. In power modules, multiple devices are often connected in parallel to meet the demand for high power density. Therefore, complex mutual coupling between wirings makes it challenging to determine the equivalent circuit, including parasitic inductance. In this paper, we propose an equivalent circuit extraction method for power modules that focuses on current loops instead of focusing on the wiring section as in previous studies. The proposed method can extract the effective inductance considering the mutual coupling between wires with fewer measurements than the conventional method. We first summarize the concept of inductance and explain the advantages of the extraction method, focusing on current loops. Next, the equivalent circuit, including the parasitic inductance of a double-pulse test circuit board with SiC-MOSFETs connected in parallel, is extracted using the proposed method. To confirm the validity of the proposed method, a double resonance system was constructed using the test circuit board wiring, and the frequency characteristics of the actual measurement and the simulation based on the extracted parasitic inductance were compared.

Keywords—Power Module, Parasitic Inductance, SiC-MOSFET, Mutual Coupling, parallel oscillation.

I. INTRODUCTION

In recent years, SiC devices, which are wide bandgap semiconductors (WBGs), have attracted much attention[1][2]. SiC devices are being applied to power modules for automotive applications due to their fast switching capability, low on-resistance, and heat resistance compared to conventional Si-

based devices. In particular, fast switching enables miniaturization of passive components such as capacitors and inductors.

However, one of the problems with fast switching is that its high di/dt increases the influence of parasitic inductance[3]. Furthermore, current commercial power modules have a planar structure using direct bond copper (DBC) and wire bonding. While these structures are superior in terms of heat dissipation and ease of manufacturing, they tend to have large parasitic inductance. Therefore, there is concern that parasitic inductance may cause voltage overshoot and device degradation.

In addition, power modules using SiC devices are multi-parallelized to reduce current stress and meet the demand for high power conversion in practical applications. However, parallel oscillation has been pointed out as a problem of multi-chip power modules[4]–[6]. In a previous study [4][5], equivalent circuit analysis was performed to suppress parallel

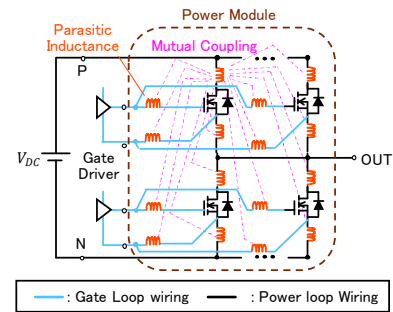


Fig.1. Parasitic parameter in typical a multi-parallel Half-Bridge power module.

oscillation, and it was clarified that the oscillation condition could be avoided by appropriately designing the ratio of parasitic inductance and parasitic capacitance. However, to realize these suppress guidelines in practical designs, underlying technology to extract parasitic elements in the power module wiring precisely is essential.

In general, extracting the equivalent circuit of a power module containing parasitic inductance is difficult. The first reason is a complex network of mutual coupling between the wires of each part of a multichip power module. This coupling becomes more significant as the devices become smaller and the wiring distances become closer. The second reason is that the parasitic inductances of the power modules are smaller than those of magnetic components, such as transformers for power converters[7]. Therefore, the influence of parasitic elements, such as the measurement cables and terminals, could not be ignored. The Third reason is that it is difficult to extract an equivalent circuit considering mutual coupling. The equivalent circuit, including mutual coupling shown in Fig. 1, is too complex and challenging to handle when analyzing parallel oscillation. Therefore, an equivalent circuit extraction method using effective inductance that considers the effect of mutual inductance, as shown in [8], is essential.

Several studies have proposed methods for extracting the parasitic inductance of power converters and power modules. The extraction of parasitic inductance of power modules can be classified into 1) simulation-based methods and 2) measurement-based methods.

1) simulation-based methods, analysis by Ansys® Q3D Extractor® or partial element equivalent circuit (PEEC) is commonly used [8][9][10][11]. In [8][9], the inductance matrix of a wiring segment is extracted using Q3D Extractor. However, in [8][9], only the coupling between power loops is discussed, not the coupling to the gate drive circuit. In addition, if inductance matrices were defined for all branches or sections of multiply-parallel power module wiring, the number of orders of inductance matrices and measurements would be enormous. In addition, in 1) simulation-based methods, the accuracy of the extraction results depends on how precisely the internal wiring structure can be reproduced. However, circuit designers cannot always obtain precise geometry data on the internal structure of power modules. Notably, a measurement method is still needed to evaluate the validity of the simulation results.

2) There are two types of methods based on measurement: a) methods focusing on the time domain and b) methods focusing on the frequency domain.

A typical example of a) methods focusing on the time domain is time domain reflectometry (TDR)[12][13]. TDR requires the measurement target to be an L and C ladder network and cannot consider mutual coupling. In addition, it is necessary to connect microstrip lines to the target, and accurate measurement is difficult when the measurement target is a complex circuit network.

b) Methods focusing on the frequency domain include those using impedance analyzers and vector network analyzers (VNA). In particular, several papers have proposed two-port s-parameter approaches using VNA [3][14][15]. In these methods, the s-parameter is first measured using VNA. Next, the measured s-parameters are converted to z-parameters, and then the parasitic parameters of each section are derived. Unlike the [Z], [Y], and

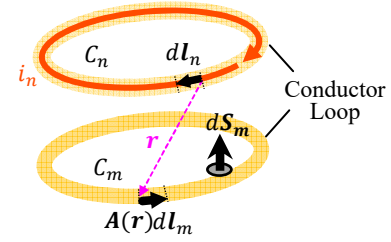


Fig.2. The induced voltage generated by time rate of change of the vector potential $A(r)$ due to the current i on the conductor loop.

[H] parameters, measurement using the S-parameters is an effective measurement method for objects that cannot be in an "open" or "short" state[15]. However, it is known that in measurements using the S-parameter, the further away from the reference impedance (50Ω), the lower the measurement accuracy is.

In this study, we propose a method to extract a network of parasitic inductances by determining the inductance matrix between loop currents in the power module instead of the conventional method of determining the inductance of each segment. In this method, the inductance of a segment is defined as the mutual inductance between each loop instead of the inductance between two points on the wiring.

This paper consists of the following five chapters. Chapter 1 describes the background, issues, and objectives of this paper. In Chapter 2, we propose a method for extracting parasitic inductance. Chapter 3 introduces the measurement setup to realize the proposed method. In Chapter 4, experiments are proposed to verify the validity of the proposed method. Finally, Chapter 5 presents the conclusion.

II. PROPOSED METHOD

A. Review of self-inductance and mutual-inductance

In this section, we first review the concept of inductance to extract equivalent circuit considering magnetic coupling. As shown in (2.1), inductance is the coefficient of the magnetic flux Φ when a current i_n flows through the conductor loop.

$$\Phi = L i_n \quad (2.1)$$

Consider where loops C_n and C_m are arranged, as shown in Fig. 2, When current i_n flows, the magnetic flux interlink to can be expressed as in (2.2).

$$\Phi_{mn} = \oint_{C_m} \mathbf{A}_n \cdot d\mathbf{l}_m \quad (2.2)$$

Where $\mathbf{A}$ is the vector potential created by i_n and dl_m is the minute length of C_m . Substituting (2.2) into (2.1), the inductance can be expressed as (2.3). Furthermore, by differentiating (2.2), Faraday's law expressed in terms of proximity effect can be obtained as in (2.4).

$$L = \frac{1}{i_n} \oint_{C_m} \mathbf{A}_n \cdot d\mathbf{l}_m \quad (2.3)$$

$$V = \oint_{C_m} \frac{\partial \mathbf{A}_n}{\partial t} \cdot d\mathbf{l}_m \quad (2.4)$$

From (2.3), it can be interpreted that the time rate of change of the vector potential behaves as an electric field and generates

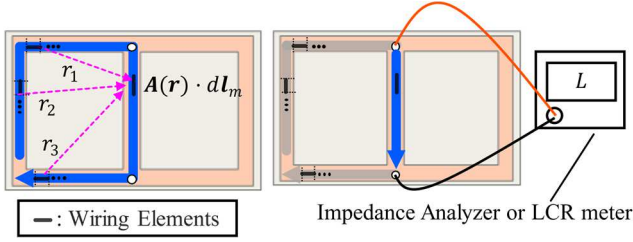


Fig. 3. Requirements for measurement considering mutual coupling. (a) Induced voltage generated by the vector potential created by the currents outside the measurement segment (b) Measurement between two points.

an induced voltage on the wiring. Induced voltage can be classified into 1) voltage generated on a conductor through which a current flow and 2) voltage generated on another conductor loop. In other words, from (2.2) and (2.3), self-inductance can be regarded as the coefficient when the current generates an induced voltage on its conductor via a vector potential. Mutual inductance can be regarded as the coefficient when the current generates an induced voltage on another conductor loop via a vector potential.

B. Previous Study : Section-Based Method.

Next, the requirements for measurement based on the above definition of inductance are explained. First, as shown in Fig. 3(a), the vector potential at a given point is determined by the influence of all current elements in the current loop. Therefore, the inductance is also affected by all current elements on the current loop. In other words, inductance cannot be determined by a simple measurement between two points, as shown in Fig. 3(b). This fact is true not only for actual measurements but also for simulations.

Many previous studies have also modeled the parasitic inductance of power modules, considering this mutual coupling[8][9]. Almost previous studies have focused on wiring sections and defined an inductance matrix consisting of self and mutual inductances. These methods divide wiring loops into physical sections. Hereafter, methods focusing on wiring sections are referred to as section-based methods. However, one problem with the section-based method is that it requires many measurements to determine the inductance matrix. In the section-based method, the number of sections corresponds to the number of self-inductances.

In the section-based method, when the number of sections is n , the number of measurements N to determine the inductance matrix is given by (2.5)

$$N = \sum_{k=1}^n k = \frac{n(n+1)}{2} \quad (2.5)$$

For example, as shown in Fig. 1 and [8][9], four parasitic inductances per leg express a typical half-bridge power loop. If six legs are in parallel, the number of measurements becomes 300. This number is the case when only the power loop coupling is considered. So, the number of measurements becomes enormous when the coupling with the gate drive circuit is considered. Therefore, when modeling power modules that consider magnetic coupling in multi-parallel devices, the method that focuses on intervals becomes more difficult as the number of legs increases.

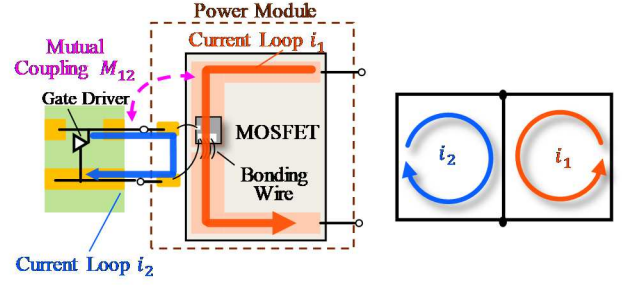


Fig. 4. Definition of current loop(a) the case of one gate loop and one power loop (b) graph of (a).

C. Proposed Method: Loop Based Method.

In the previous section, we outlined section-based parasitic inductance extraction. This section proposes a loop-based method for extracting parasitic inductance instead of the section-based method. The proposed method consists of three steps: 1) definition of current loops, 2) determination of the inductance matrix, and 3) conversion to effective inductance.

1) Definition of Current Loops

In this paper instead of focusing on the wiring section, we propose a method that defines an inductance matrix between current loops. For simplicity, we use the case of one gate loop and one power loop, as shown in Fig. 4. First, current loops are defined in the network. (2.3) based on graph theory gives the number of current loops, N_{loop} , where m is the number of branches and n is the number of nodes.

$$N_{loop} = m - n + 1 \quad (2.6)$$

Fig. 4(b) shows a graph of the circuit in Fig. 4(a). In this graph, $m=3$ and $n=2$, and N_{loop} is 2. The advantage of the loop-based method is that it requires fewer measurements and enables modeling that considers mutual coupling. In the loop-based method, the number of self-inductances equals the number of current loops. So, the order of the inductance matrix in the loop-based method is smaller than that of the inductance matrix in the section-based method. The more complex the network of circuits to be measured, the larger this difference becomes. Therefore, the loop-based method can model parasitic in multi-parallel power modules with fewer measurements than the section-based method.

2) Determination of the inductance matrix

Next, determine the inductance matrix for the current loops defined in 1). The inductance matrix between the current loops shown in Figure 3(a) is as in (2.7).

$$\mathbf{L} = \begin{bmatrix} L_{11} & M_{12} \\ M_{21} & L_{22} \end{bmatrix} \quad (2.7)$$

Here, L_{11} , and L_{22} are the self-inductances of current loops 1 and 2, respectively. M_{12} and M_{21} are the mutual inductances of current loops 1 and 2. Here, since the reciprocal theorem holds for the mutual inductance, the following (2.8) holds. In (2.8), two self-inductances and one mutual inductance must be used to determine the inductance matrix in this example. The

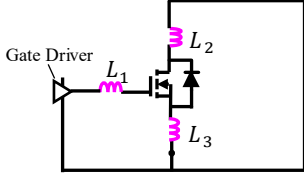


Fig. 5 Equivalent circuit of effective inductance converted from the inductance matrix.

inductance matrix is a complex number, and the imaginary component can be used to determine the parasitic resistance of the wiring section.

$$M_{12} = M_{21} \quad (2.8)$$

3) conversion to effective inductance.

The inductance matrix obtained in 2) represents the coupling between current loops, but it is unsuitable for circuit analysis. Therefore, the inductance matrix obtained in 2) is converted to an effective inductance that considers mutual coupling as shown in Fig. 5. Here, The power module consists of wiring loops placed on a flat surface on an aluminum heat sink. This heat sink significantly reduces the magnetic field created by the current in the power module. Therefore, in the power module, the mutual inductance of current loops at remote locations that do not have a common part can be neglected.

All branches of a network can be classified into two types: a) a branch with two current loops and b) a branch with only one current loop.

First, we consider the effective inductance of a) a branch with two current loops. Parasitic inductance, which exists in the common section of the different loops, causes the current in one loop to induce an induced voltage in the other loop. This behavior is the very definition of mutual inductance described in A. In other words, The effective inductance of a) a branch with two current loops can be defined as the mutual inductance between the different loops.

Next, Define the effective inductance of b) a branch with only one current loop. Here, b) a branch with only one current loop is the component of self-inductance that is induced only in its current loop. In other words, b) a branch with only one current loop can be defined as the leakage inductance between different current loops. Given the above, the inductance matrix shown in (2.7) can be transformed as follows.

$$L_1 = L_{22} - M_{12} \quad (2.8)$$

$$L_2 = L_{11} - M_{12} \quad (2.9)$$

$$L_3 = M_{12} \quad (2.10)$$

III. MEASUREMENT OF INDUCTANCE MATRIX

In the previous chapter, we discussed the extraction of parasitic inductance considering mutual coupling by focusing on the wiring loops of a power module. To realize the proposed method, it is essential to precisely extract the self and mutual inductances of the wiring loops. In this chapter, we propose a measurement method that can precisely measure wiring loops' self-inductance and mutual inductance.

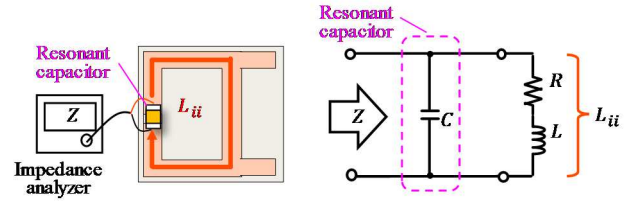


Fig. 6. Measurement principle of self-inductance using parallel resonance.

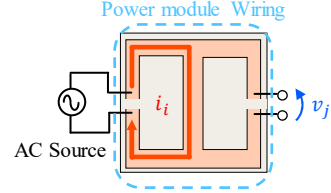


Fig. 7. Measurement principle of mutual inductance between different current loops.

A. Principle of self-inductance measurement

This section explains a method for measuring the self-inductance of a power module. Based on the concept of self-inductance explained in previous chapter, the self-inductance of an arbitrary loop can be obtained by measuring the current in the wiring loop and the voltage generated by the vector potential on its conductor. However, measuring the inductance of power module wiring is difficult. As indicated in the introduction, the parasitic inductance of a power module is minimal, so the induced voltage is relatively small, making it difficult to measure with measurement equipment accurately. To address this issue, we employ a self-inductance measurement method using parallel resonance, as shown in Fig. 6. The advantage of this method is that the measurement equipment can measure a significant impedance than when directly measuring self-inductance. Therefore, the induced voltage is also larger, resulting in a higher S/N ratio and improved measurement accuracy. In this method, a capacitor with a known value is connected in parallel to the wiring loop. An impedance analyzer is also connected in parallel with the capacitor to measure the frequency characteristics, including the resonance peak. When the resonant capacitor is ideal, the resonant frequency is f_{peak} , and the capacitance of the resonant capacitor is C_r . The self-inductance is given by (3.1).

$$L_{ii} = \frac{1}{(2\pi f_{peak})^2 C_r} \quad (3.1)$$

The actual capacitor has parasitic capacitances such as ESL and ESR, so the actual resonance peak position is different from (3.1). Therefore, the self-inductance is obtained by fitting the theoretical frequency dependence to the measured results, considering the parasitic elements of the capacitor.

B. Principle of self-inductance measurement

This section explains a method for measuring the mutual inductance between different wiring loops of a power module. Based on the concept of mutual inductance explained in the

previous section, mutual inductance can be obtained by measuring the current flowing in one loop and the induced voltage in the other conductor by the vector potential. Therefore, as shown in Fig. 7, an AC source is connected to one loop, current i_i is applied, and the induced voltage v_j in the other loop is measured. If the phase difference between the v_j and i_i is θ , the mutual inductance M_{ij} can be obtained from (3.2).

$$M_{ij} = \frac{v_j}{2\pi f i_i} \sin \theta \quad (3.2)$$

IV. EXPERIMENTAL VALIDATION

In Chapter 2, the proposed method was explained using the case of two simple wiring loops as an example. This chapter extracted parasitic inductance by applying the proposed method to a test circuit board with a complex wiring loop consisting of SiC-MOSFETs connected in parallel. In addition, inductance validation experiments using a multi-resonant system were conducted to confirm the validity of the proposed method.

A. Extraction of parasitic inductance of test Circuit board

Fig. 8(a) shows a test circuit board to verify the validity of the proposed method. This board is a double-pulse test circuit with two SiC-MOSFETs connected in parallel. This chapter applies the proposed method to test the circuit board to determine the equivalent circuit, including parasitic inductance. Fig. 8(b) shows the current loops determined based on the proposed method. The inductance matrix Figure 8(b) is shown in (4.1).

$$\mathbf{L} = \begin{bmatrix} L_{d1d1} & M_{d1d2} & M_{d1g1} & M_{d1g2} & M_{d1d} \\ M_{d2d1} & L_{d2d2} & M_{d2g1} & M_{d2g2} & M_{d2d} \\ M_{g1d1} & M_{g1d2} & L_{g1g1} & M_{g1g2} & M_{g1d} \\ M_{g2d1} & M_{g2d2} & M_{g2g1} & L_{g2g2} & M_{g2d} \\ M_{dd1} & M_{dd2} & M_{dg1} & M_{dg2} & L_{dd} \end{bmatrix} \quad (4.1)$$

Here, as shown in Chapter 2, the mutual inductance of power modules that do not have a common section of the current loop can be neglected. Therefore, the inductance matrix can be approximated as in (4.2).

$$\mathbf{L} = \begin{bmatrix} L_{d1d1} & M_{d1d2} & M_{d1g1} & 0 & M_{d1d} \\ M_{d2d1} & L_{d2d2} & M_{d2g1} & M_{d2g2} & 0 \\ M_{g1d1} & M_{g1d2} & L_{g1g1} & M_{g1g2} & M_{g1d} \\ 0 & M_{g2d2} & M_{g2g1} & L_{g2g2} & M_{g2d} \\ M_{dd1} & 0 & M_{dg1} & M_{dg2} & L_{dd} \end{bmatrix} \quad (4.2)$$

Next, the inductance matrix is converted to the effective inductance. Defining the parasitic inductance of each section as shown in Fig. 10, the effective inductance of each section can be expressed as follows.

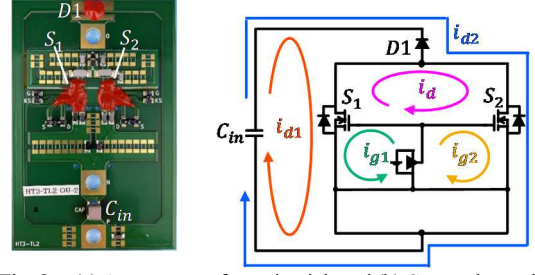


Fig. 8. (a) Appearance of test circuit board (b) Current loops defined on test circuit board

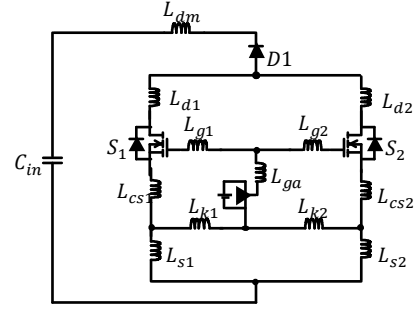


Fig. 9. (a) Circuit diagram of test circuit board including effective inductance determined by the proposed method

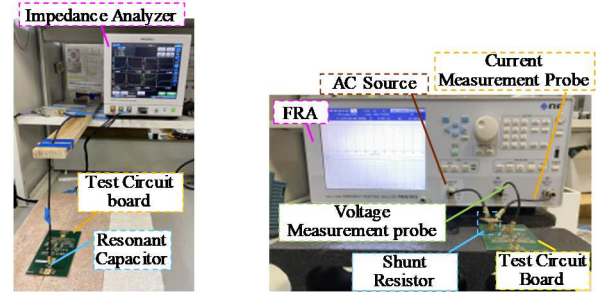


Fig. 10. (a) Circuit diagram of test circuit board including effective inductance determined by the proposed method

$$L_{dm} = M_{d1d2} \quad (4.3)$$

$$L_{d1} = M_{d1d} \quad (4.4)$$

$$L_{d2} = M_{d2d} \quad (4.5)$$

$$L_{g1} = M_{g1d} \quad (4.6)$$

$$L_{g2} = M_{g2d} \quad (4.7)$$

$$L_{cs1} = M_{d1g1} \quad (4.8)$$

$$L_{cs2} = M_{d2g2} \quad (4.9)$$

$$L_{k1} = L_{g1g1} - M_{g1d} - M_{g1g2} - M_{d1g1} \quad (4.10)$$

$$L_{k2} = L_{g2g2} - M_{g2d} - M_{g1g2} - M_{d2g1} \quad (4.11)$$

TABLE 1. INSTRUMENTS EMPLOYED FOR THE EXPERIMENT

Instrument	Model (Manufacturer)
Frequency Response Analyzer (FRA)	FRA51615,(NF Corp.)
Impedance Analyzer	(IM7581, HIOKI E.E. Corp.)

TABLE 2. LIST OF CIRCUIT ELEMENTS OF MEASUREMENT SET UP

C_r	Resonant Capacitor (C1206C561FCGAC7800, KEMET Corp.)
R_2	Shunt Resistor :1 Ω (Y16061R00000B9W, Vishay Intertechnology, Inc.)

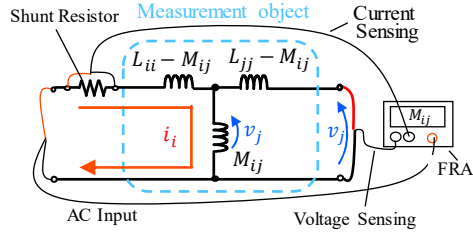


Fig. 11. (a) Circuit diagram of test circuit board including effective inductance determined by the proposed method

$$L_{s1} = L_{d1d1} - M_{d1d} - M_{d1g1} - M_{d1d2} \quad (4.12)$$

$$L_{s2} = L_{d2d2} - M_{d2d} - M_{d2g2} - M_{d1d2} \quad (4.13)$$

Fig. 10 shows the setup based on the self-inductance and mutual inductance measurement principles explained in the previous section. TABLE.1 shows the instruments employed for the experiment. TABLE.2 shows the list of circuit elements of measurement set up. In measuring mutual inductance, measuring the induced voltage and AC input at two different ports is necessary. Therefore, the measurement method using parallel resonance, which is used for self-inductance, cannot be applied. Therefore, in this paper, the mutual inductance measurement was performed using a frequency response analyzer (FRA). The measurement system using the FRA is shown in Fig. 11. FRA generally has greater voltage sensitivity than a typical oscilloscope and can be calibrated accurately. Next, TABLE 3 shows the effective inductance values obtained from (4.3) to (4.12) based on the components of the measured inductance matrix.

B. Validation using multi-resonant circuits

In the previous section, we extracted the equivalent circuit, including the parasitic inductance of the test circuit board, using the proposed method. In this section, we verify the validity of the extracted equivalent circuits. As a verification approach, this paper uses a multi-resonant circuit to validate. Fig. 12 shows the circuit diagram of the validation experiment using a multi-resonant circuit. In this experiment, three resonant capacitors are first connected to a test circuit board, as shown in Fig. 12. Next, the frequency characteristics of the multi-resonant circuit are measured using an impedance analyzer.

TABLE 3. EFFECTIVE INDUCTANCE OBTAINED BY PROPOSED METHOD

Effective Inductance / Parasitic Resistance	L [nH]	R[m Ω]
L_{dm}	58.0	8.2
L_{d1}	1.03	3.0
L_{d2}	1.01	3.0
L_{cs1}	-0.271	3.5
L_{cs2}	-0.276	2.8
L_{g1}	6.46	17.9
L_{g2}	6.44	18.9
L_{ga}	15.2	50.7
L_{k1}	2.86	152.9
L_{k2}	1.94	142.5
L_{s1}	10.9	51.4
L_{s2}	10.9	51.7

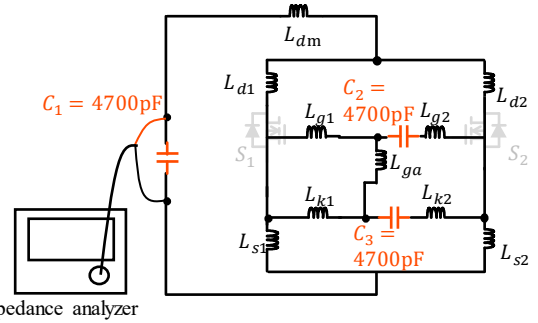


Fig. 12. (a) Circuit diagram of test circuit board including effective inductance determined by the proposed method

This multi-resonant circuit has three resonance peaks determined by the parasitic inductance in the wiring and the three resonant capacitors. Next, using the values of resonant capacitors and the parasitic inductance of the test circuit board extracted in the previous section, a multi-resonant circuit is constructed in a SPICE simulation, and the frequency characteristics are measured. The validity of the proposed method is confirmed by comparing the positions of the resonance peaks in the measured and simulated multi-resonant circuits based on the proposed method.

Fig. 13 shows the results of the validation experiment using the multi-resonant circuit. LTspiceXVII[®] was used as the SPICE simulator. Figure 13 shows that the three resonance peaks of the double-resonant system are in good agreement. TABLE 4 compares the peaks of the multi-resonant circuit in the measurement and the simulation based on the proposed method. The relative error of the three resonance peaks is within 3.6%. This result confirms the validity of the equivalent circuit, including parasitic inductance extracted by the proposed method.

V. CONCLUSION

In recent years, the increasing switching speeds of power modules have caused problems such as false triggering and parallel oscillation due to parasitic inductance in the wiring. In addition, the miniaturization of power modules increases the

influence of mutual coupling between wiring. Therefore, extracting an equivalent circuit, including parasitic inductance, becomes more difficult. In addition, the number of measurements required for the section-based method, which is a previous study, is enormous. Therefore, it is difficult to model the coupling with the gate drive circuit for the multi-parallel

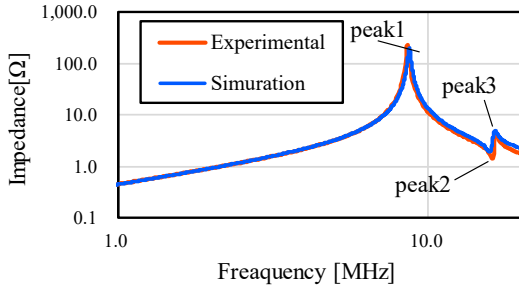


Fig.13. (a) Circuit diagram of test circuit board including effective inductance determined by the proposed method

TABLE 4. EFFECTIVE INDUCTANCE OBTAINED BY PROPOSED METHOD

	Peak1	Peak2	Peak3
Experimental [MHz]	8.55	16.1	16.7
Simulation [MHz]	8.7	15.6	16.1
relative error [%]	1.75	3.1	3.59

power modules in the previous studies.

In this paper, we propose an equivalent circuit extraction method for power modules that focuses on current loops instead of focusing on wiring sections. Compared to the conventional method, the proposed method can extract the effective inductance considering the magnetic coupling between wires with fewer measurements.

In this paper, verification experiments are conducted to confirm the validity of the proposed method. As a result, the proposed method is promising for extracting the parasitic inductance of power module wiring. Therefore, the proposed method can contribute to the malfunction suppression guidelines based on the design of parasitic inductance values proposed in previous studies and clarify the parallel oscillation of power modules connected in parallel.

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