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A Novel Soft-Switching Inverter using Auxiliary Power Supply for Capacitive Load High Voltage and High Frequency Applications

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***Abstract*—In recent years, the trend toward higher switching frequency in inverters has been advancing, and there is a growing demand for applications involving high voltage. In particular, there is a need to develop inverters for special industrial applications where PWM control is possible, and the load is capacitive. In this application, enormous turn-on switching loss occurs due to the energy of the output capacitance, even though the load current is not flowing. This paper proposes a novel soft-switching inverter to reduce this switching loss not only the main switch but also the auxiliary switch. The proposed inverter can attain soft-switching conditions for the main switch turn-on under zero-voltage switching (ZVS). Also, the auxiliary switch operates under zero-current switching (ZCS) turn-on using an auxiliary power supply of lower voltage than the main power supply. These features were successfully verified by the prototype of a small power experiment.**

Keywords—high-frequency inverter, PWM inverter, soft-switching, capacitive load

I. INTRODUCTION

In recent years, the rise of wide-bandgap semiconductors has accelerated the trend toward higher switching frequencies in inverters[1]~[3], and there is a growing demand for applications involving high voltage. In the future, the development of half-bridge inverter with PWM control is required to arbitrarily change the load voltage. This application requires the design of an inverter operating under capacitive load conditions (No current flow during itching) at 10kV and 1MHz.

The switching inverters for high frequency applications tend to suffer from enormous switching loss. In particular, the energy stored in the output capacitance is large[4]. This energy results in enormous losses during turn-on, even though load current is not flowing. In other words, even if zero-current switching (ZCS) under high voltage is achieved at turn-on, enormous loss still occur.

Recently, many soft switching inverters have been proposed to reduce switching loss. Some of these soft-switching inverters utilize full resonance to achieve soft switching[5]~[7]. These topologies generally rely on the resonance phenomenon of passive components. As a result, the achievable soft-switching frequency is limited. This limitation prevents PWM control.

To achieve soft switching in PWM control, it is necessary to use partial resonance, which resonates only during switching. Partial resonance methods can be classified into two main categories: DC link[8]~[13], and AC link[14]~[18] methods. The first method, DC link, involves adding an auxiliary circuit between the power supply and the inverter. These methods achieve zero voltage switching(ZVS) turn-on of the main switch by temporarily setting the link voltage of the inverter to 0V. However, because a period is required to keep the link voltage at 0V, the dead time becomes longer. This means that the dead time becomes longer relative to the switching period. For this reason, the DC link method is impractical for high frequency applications. To solve this problem, the second method, AC-link, enables ZVS turn-on of the main switch without varying the link voltage. These methods allow for a shorter dead time. However, because the auxiliary switch performs ZCS under high voltage, enormous loss occur in the auxiliary switch.

To address this problem, the novel AC-link method is required. In this method, the auxiliary switch archives ZCS when a voltage lower than the power supply voltage is applied. The purpose of this paper is to propose such a novel soft-switching inverter for high voltage and high frequency applications. The proposed inverter can attain soft-switching conditions for the main switch turn-on under ZVS and turn-off under ZVS. Also, the auxiliary switch operates under ZCS turn-on using an auxiliary power supply of lower voltage than the main power supply and under ZVS and ZCS turn-off. In addition, the control pulses for the auxiliary switch can be generated with a pulse width similar to that of the main switch.

The following discussion consists of three sections. Section II presents the proposed soft-switching inverter as well as its operating principle. Section III presents the small power experiment to evaluate the operating principle and resultant loss reduction. Finally, section IV gives conclusions.

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II. PROPOSED INVERTER

A. Circuit Topology

Figure 1 illustrates the proposed soft-switching inverter. The proposed inverter consists of two switches S_1 and S_2 as the main circuit, two auxiliary power supplies V_{a1} and V_{a2} that are lower than the input power V_{in}, two inductors L_{a1} and L_{a2}, two switches S_{a1} and S_{a2}, two diodes D_{a1} and D_{a2}, four diodes D_{a3} to D_{a6} for recovery measures.

D_{a3} and D_{a5} are snubber diodes for the recovery current generated by D_{a1} and D_{a2}, respectively. D_{a4} and D_{a6} are snubber diodes for S_{a1} and S_{a2}. Therefore, the losses due to the anti-recovery diodes are considered to be small.

B. Operating Principles

Figures 2 and 3 show the operating waveforms and current patterns of these operating modes. The proposed inverter charges the magnetic energy of the inductor by operating . By discharging this energy during the turn-on process of , it discharges the electrostatic energy of the output capacitance of the output capacitance of . This circuit realizes the ZVS of .

The operation of the first half of the switching cycle consist of 5 operating modes. The operation of the latter half is the same as that in the first half except that the current flows in the opposite direction. main switches S_1 and S_2 are replaced by S_2 and S_1. S_{a1}, S_{a2}, D_{a1}, D_{a2}, L_{a1}, and L_{a2} are replaced by S_{a2}, S_{a1}, D_{a2}, D_{a1}, L_{a2}, and L_{a1}.

In order to simplify the description of the proposed converter, the following assumptions are made:

1) main switches S_1, S_2 ,and auxiliary switches S_{a1}, S_{a2} have output capacitance ($C_{oss(main)}$, $C_{oss(auxiliary)}$), zero on-state resistance, infinite off-state resistance, zero input capacitance, and reverse capacitance.

2) Other semiconductor devices are ideal.

3) All energy storage components have no parasitic elements and are thus free of loss.

4) The load is assumed to be unloaded because no current flows during switching transitions in this application.

Mode0 [Fig. 3(a)] ($t_0 < t < t_1$): Main switch S_1 kept at the on-state, whereas S_2 is kept at the off-state. Auxiliary switch S_{a1}, S_{a2} is in the off-state, and there is no current flowing anywhere in the circuit.

Mode1 [Fig.3(b)] ($t_1 < t < t_2$): This mode is activated when S_{a1} is turned on. The current flows through auxiliary diode D_{a1} to supply the current to auxiliary inductor L_{a1}. The current of L_{a1} increases linearly supplied with V_{a1} voltage. L_{a1} inductor current $i_{La1}(t)$ of this mode is as follows:

$$i_{La1}(t) = \frac{V_{a1}}{L_{a1}}(t - t_1) \tag{1}$$

At this time, Because the current rise speed of S_{a1} is restricted by L_{a1}, S_{a1} achieves the ZCS turn-on. Furthermore, the loss due to output capacitance at turn-on of the auxiliary switch is expressed by the following equation:

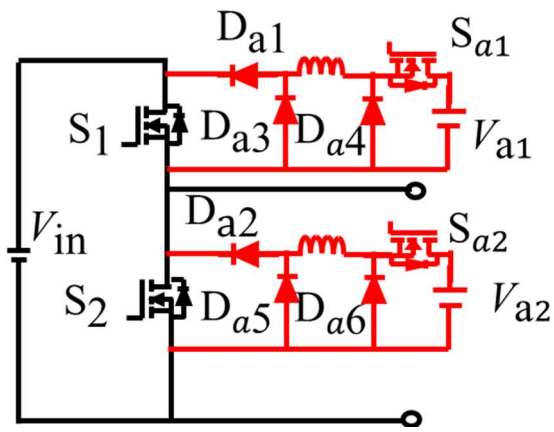


Fig. 1. Proposed soft-switching inverter

$$P_{oss} = \int_0^{V_{a1}} C_{oss(auxiliary)} v dv \times f \tag{2}$$

At this time, f represents the frequency.

Therefore, the energy of the output capacitance is reduced by turn-on when a low voltage is applied.

After the current in L_{a1} exceeds the magnetic energy to charge the energy in the output capacitance of S_1 and discharge the energy in the output capacitance of S_2, the operation steps into the next mode.

Mode2 [Fig.3(c)] ($t_2 < t < t_3$): Main switch S_1 is turn-off, whereas S_2 are still kept in the off-state to make the dead time. L_{a1} inductor current is represented as a resonance phenomenon of the output capacitance of La1 and the sum of S1 and S2 with the initial current at the end of Mode2. L_{a1} inductor current $i_{La1}(t)$ of this mode is as follows:

$$i_{La1}(t) = \sqrt{\frac{2C_{oss(main)}}{L_{a1}}} V_{a1} \sin\left(\omega_r (t - t_2)\right)$$

$$+ i(t_2) \cos\left(\omega_r (t - t_2)\right) \tag{3}$$

At this time, $\omega_r = \sqrt{\frac{1}{2L_{a1} C_{oss(main)}}}$

Furthermore, the drain-source voltage of S_1 and S_2 $v_{S1}(t)$, $v_{S2}(t)$ of this mode is as follows:

$$v_{S2}(t) = V - v_{S1}(t) = V - V_{a1}\left(1 - \cos\left(\omega_r (t - t_2)\right)\right)$$

$$- \sqrt{\frac{L_{a1}}{2C_{oss(main)(er)}}} i(t_2) \sin\left(\omega_r (t - t_2)\right) \tag{4}$$

At this time, the drain-source voltage of S_1 rises slowly due to resonance phenomenon, thus achieving ZVS turn-off.

After charging and discharging the output capacitance, when $v_{S2}(t)$ reaches 0V, the operation steps into the next mode.

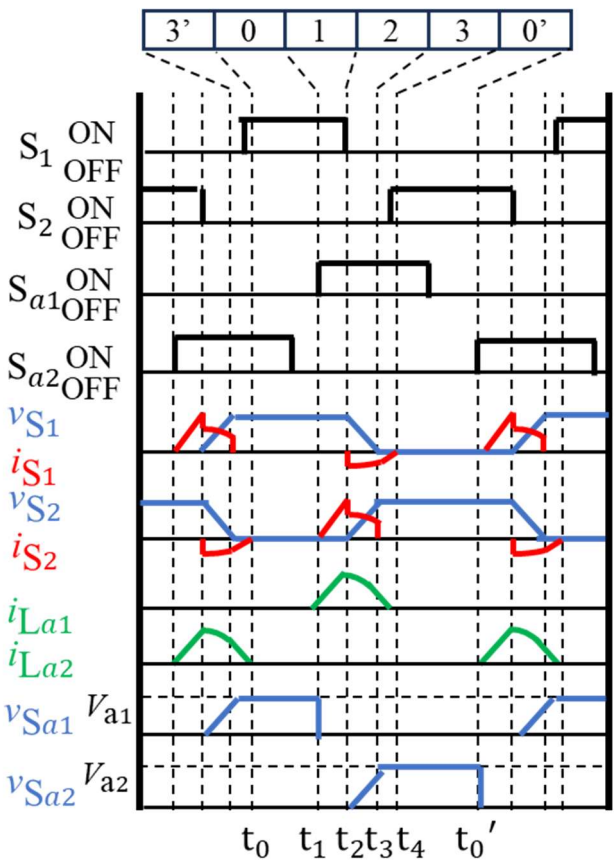


Fig. 2. Operating waveforms of proposed inverter

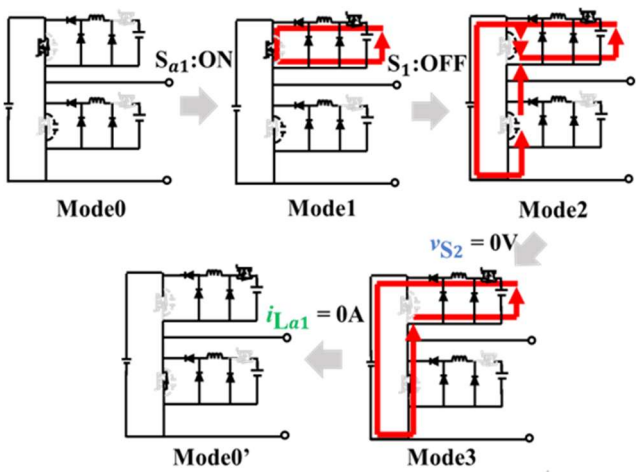


Fig. 3. Current patterns of proposed inverter

Mode3 [Fig.3(d)] ($t_3 < t < t_4$): because $v_{S2}(t)$ is 0V, S_2 conducts the body diode. By placing S_2 in the on-state at this mode, S_2 can achieve ZVS turn-on. The current of L_{a1} decreases linearly supplied with V_{in} - V_{a1} voltage with the initial current at the end of mode 3. L_{a1} inductor current $i_{La1}(t)$ of this mode is as follows:

$$i_{La1}(t) = i_{La1}(t_3) - \frac{V_{in} - V_{a1}}{L_{a1}} t \tag{5}$$

when $i_{La1}(t)$ reaches 0A, the operation steps into the next mode.

Mode0' [Fig3(e)] ($t_4 < t < t_5$): because $i_{La1}(t)$ is 0A, there is no current flowing anywhere in the circuit. By placing S_{a1} in the of-state at this mode, S_{a1} can achieve ZCS turn-off. Moreover, ZVS turn-off can be achieved at the same time because the drain-source voltage of S_{a1} does not increase.

As we have seen above, all the semiconductor switches achieve soft-switching. Main switches S_1 and S_2 achieve ZVS turn-on and ZVS turn-off, auxiliary switches S_{a1} and S_{a2} achieve ZCS turn-on using low voltage and ZVS and ZCS turn-off. Therefore, the proposed soft-switching inverter is effective for switching loss suppression due to output capacity short circuit.

C. Design of Auxiliary Circuit

To achieve soft switching, the drain-source voltage of S_2 must be 0V at the end of Mode3. In this case, transforming equation (4) into the equation of the equilibrium between magnetic energy and electrostatic energy, it is expressed as follows:

$$\frac{1}{2} L_{a1} i^2(t_2) = \frac{1}{2} 2 C_{oss(Smain)(er)} V_{in}(V_{in} - 2V_{a1}) \tag{6}$$

The auxiliary power supply and inductor must be designed to satisfy this condition. At this time, during Mode2, both S_1 and S_{a1} must be in the ON state. Therefore, the current $i_{La1}(t_2)$ is constrained by the pulse width of the main switch and will not exceed the minimum pulse width $t_{\min}$ of the main switch. Therefore, the circuit should be designed so that when the main switch operates at its minimum pulse width $t_{\min}$, the peak resonant voltage plus the auxiliary power supply matches the input voltage. Therefore, when Mode 2 is equal to the minimum pulse width, as can be seen by substituting into equation (1), once the value of the auxiliary power supply is determined, the value of the auxiliary inductor is dependently determined.

The auxiliary power supply should be determined such that the conduction loss occurring between Mode 2 and Mode 4, due to the on-resistance of the main switch S_1 and the auxiliary switch S_{a1}, is equal to the output capacitance loss of the auxiliary switch P_{oss}. Therefore, Va1 must be chosen to satisfy the following equation:

$$\int_0^{V_{a1}} C_{oss(Sa1)}(v) v dv = R_{on(main)} \int_{t_1}^{t_2} i_{La1}{}^2(t) dt$$

$$+ R_{on(auxiliary)} \int_{t_1}^{t_4} i_{La1}{}^2(t) dt \tag{7}$$

D. Control of Auxiliary Switches

In high-frequency operation, it is difficult to precisely control the auxiliary switch with a pulse width that differs significantly from that of the main switch. Therefore, the auxiliary switch should either be controlled by phase shifting the main switch or have some margin in the timing of its

transition to the on-state or off-state

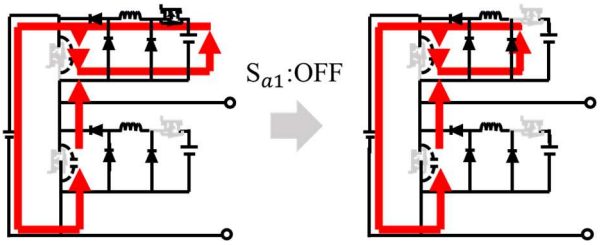


Fig. 4. Current path when S_{a1} is turn-off during mode 2

In the proposed inverter, the auxiliary switch can be allowed to turn on earlier than the appropriate Mode 2 period, even though this increases conduction loss. The appropriate timing for transitioning to the OFF state is between Mode 0' and the next turn-on of S1, providing a wide permissible range.

Additionally, as shown in Figure 4, even if the auxiliary switch turns off during the Mode 2 period, the conduction path shifts from Va1 and Sa1 to Da4, making the operation acceptable. Therefore, it is possible to operate the auxiliary switch with a duty cycle similar to that of the main switch with a short pulse width, making it suitable for high-frequency operation.

E. Voltage Stress on Auxiliary Semiconductor Device

According to Fig.3, auxiliary switch S_{a1} is applied in mode3 with the voltage of auxiliary voltage V_{a1}. Similarly, auxiliary switch S_{a2} is applied in mode3' with the voltage of auxiliary voltage V_{a2}. (Auxiliary switches S_{a1} and S_{a2} have equal or smaller voltage stress in the other mode than in their off-state of mode3 or mode3'.) Consequently, auxiliary switches S_{a1} and S_{a2} experience the voltage stress identical to auxiliary power supplies.

According to the current pattern in mode0, D_{a2} is applied with V_{in} - V_{a2}. Similarly, D_{a1} is applied in mode0' with V_{in} - V_{a1}. (Auxiliary diodes D_{a1} and D_{a2} have equal or smaller voltage stress in the other mode than in their off-state of mode0' or mode0.) Consequently, auxiliary diodes D_{a1} and D_{a2} experience the voltage stress identical to input voltage V_{in}.

According to the current pattern in mode3, D_{a3} is applied with V_{in} Similarly, D_{a5} is applied in mode3' with V_{in}. According to the current pattern in mode1, D_{a4} is applied with V_{a1}. Similarly, D_{a6} is applied in mode1' with V_{a2}. (Auxiliary diodes D_{a3} ~ D_{a6} have equal or small voltage stress in the other mode.) Consequently, recovery measures diodes D_{a3} and D_{a5} experience the voltage stress identical to input voltage V_{in}. However, D_{a4} and D_{a6} experience the voltage stress identical to auxiliary power supplies.

III. EXPERIMENT

A small power experiment was carried out to verify the operating principle as well as the power loss reduction by the proposed soft-switching inverter. The operating principle was evaluated by measuring the voltage and current waveforms of the prototype. The power loss was evaluated by multiplying voltage and current

TABLE I. SPECIFICATIONS OF PROTOTYPE

Parameter	Specification
Input voltage (V_{in})	100V
Operating frequency	400kHz
Main switch S_1, S_2	C2M0045170D
Auxiliary switch S_{a1}, S_{a2}	BSC520N15NS3_G
Resonant inductance L_{a1}	1.96uH
Resonant inductance L_{a2}	1.98uH
Auxiliary diode D_{a1}, D_{a2}	SBR1U150SA
Recovery measure diode D_{a3} ~ D_{a6}	DMA10IM1600UZ-TUB
Auxiliary voltage V_{a1}, V_{a2}	12V (SCWN03E-12)

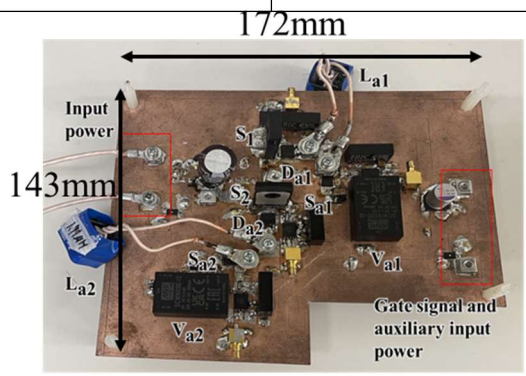


Fig. 5. Photograph of prototype of proposed inverter

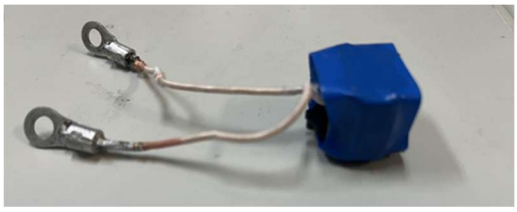


Fig. 6. Photograph of the auxiliary inductor

TABLE II. SPECIFICATIONS OF AUXILIARY INDUCTORS

Parameters	L_{a1}	L_{a2}
Magnetic core	PC-200/RM-8	PC200/RM-80
Winding	ELEKTRISOLA P155p 1000×0.04mm	ELEKTRISOLA P155p 1000×0.04mm
Turns	3T	3T
Gaps	0.4mm	0.4mm
AC resistance (400kHz)	86mΩ	78mΩ
Self-inductance	1.96uH	1.98uH

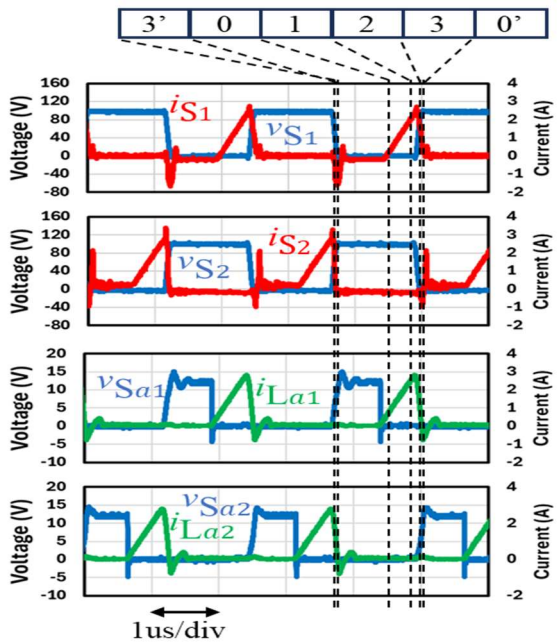
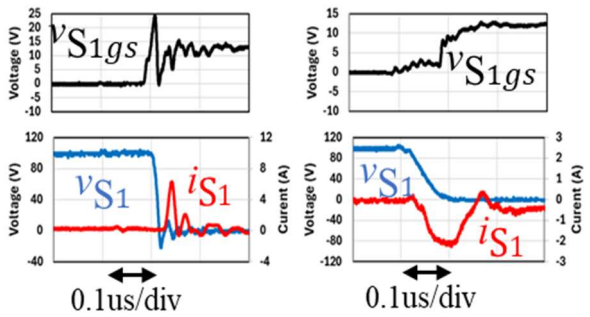
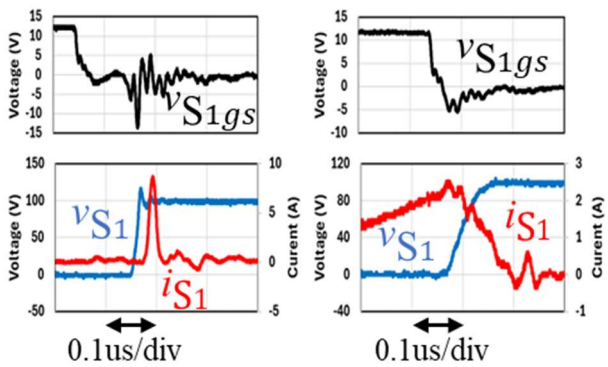


Fig. 7. Operating waveforms of the proposed inverter in prototype



(a)Conventional inverter (b)Proposed inverter

Fig. 8. Turn-on waveforms of the main switch S_1



(a)Conventional inverter (b)Proposed inverter

Fig. 9. Turn-off waveforms of the main switch S_1

A. Experimetal Setup

Table I shows the specifications of the prototype. Figure 5 shows the photograph of the prototype. Main switches S_1 and S_2 operate at the same duty cycle with a dead time of 100ns. the voltage stress identical to auxiliary power supplies. A low switching frequency (400kHz) and a low voltage (100V) was chosen for this experiment to easily observe the current and voltage waveforms with the oscilloscope. As for the prototype of the conventional inverter, we disconnected the auxiliary inductor from the prototype of the proposed inverter.

The auxiliary power supplies V_{a1} and V_{a2} were set to 12V. In the prototype, the 5V power supply selected for the control circuit is boosted to 12V by an isolated power supply. Figure 6 shows the photograph of auxiliary inductor L_{a1}. L_{a1} and L_{a2} is made of the Lits wire wound on the ferrite cores. Specifications of the structures of these magnetic devices, including the core materials and the Lits wire, are presented in Table II. In the prototype, auxiliary switches S_{a1} and S_{a2} are operated with the same duty cycle of the main switches S_1 and S_2 with a mode2 period of 590ns.

B. Evaluation Result of Operating Waveforms

Figure 7 shows the voltage and current waveforms of the proposed soft-switching inverter during one switching period. The measured waveforms were found to be consistent with those of the theoretical waveforms presented in Fig.3. The small L_{a1} and L_{a2} current $i_{La1}(t)$, $i_{La2}(t)$ was found to flow in opposite direction throughout recovery measures diodes.

Figure 8 and Figure 9 show the comparison result of the turn-on and turn-off switching waveforms of main switch S_1 between the proposed and conventional inverters. As can be seen in the figure, it can be seen that the conventional inverter has a high voltage at the transition to the on-state of S_1. On the other hand, in the proposed inverter, the output capacitance is discharged before the on-state of S_1, resulting in a drain-source voltage of 0V. This confirms that ZVS turn-on is successfully achieved. Furthermore, in the conventional inverter, even after S_1 transitions to the off-state, the drain-source voltage does not rise during the dead

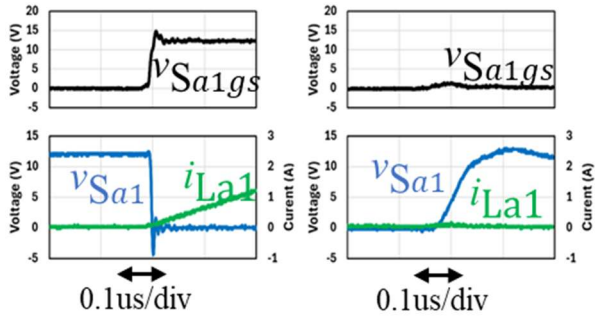
time, achieving both ZVS and ZCS turn-off. On the other hand, in the proposed inverter, the voltage rise was suppressed at the turn-off of S_1 indicating the zero-voltage turn-off. This result indicates that all of the main switches achieve the zero-voltage turn-on and the zero-voltage turn-off because of the symmetry between S_1 and S_2.

Figure 10 shows the turn-on and turn-off switching waveforms of auxiliary switch S_{a1}. These waveforms indicate the zero-current turn-on, using auxiliary power supply V_{a1} (12V) as is consistent with the theory. The turn-off waveforms were consistent with the zero-current zero-voltage turn-off.

Consequently, the operating waveforms were found to support the operating principle.

C. Evaluation Result of Power Loss

We compared the total power loss between the proposed and conventional inverters. Because the prototype operates under no-load conditions, the total power loss is the input power loss at the conventional inverter. Therefore, power loss were evaluated by measuring the input voltage and input current using a digital multimeter and a shunt resistor, then calculating their product. In the proposed inverter, in addition to the input power, the output power of the isolated power supply for V_{a2} is measured using the same method as the input power. This value is then doubled to determine power loss in the auxiliary circuit.



(a)Turn-on (b)Turn-off

Fig. 10. Switching waveforms of the main switch S_{a1}

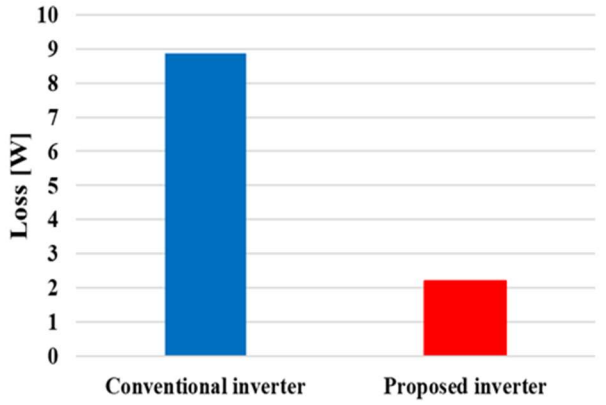


Fig. 11. Loss comparison

Figure 11 shows the measured power loss of the prototypes. As can be seen in the figure, the power loss is reduced by the auxiliary circuit. Consequently, this experiment was found to support the effectiveness of the proposed soft-switching inverter.

IV. Conclusions

In recent years, the rise of wide-bandgap semiconductors has accelerated the trend toward higher switching frequencies in inverters, and there is a growing demand for applications involving high voltage. If zero-voltage switching is not possible due to the load current, excessive losses may occur due to switching losses caused by the output capacitance of the semiconductor switching device.

To address this issue, this paper proposed an inverter that achieves ZVS or ZCS at a lower voltage than input voltage for all switches, including auxiliary switches. The small power experiment verified the soft-switching capability as well as the total power loss reduction owing to reduction in the switching loss.

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