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Hayashi, Takuto

Graduate School of Environmental, Life, Natural Science and Technology, Okayama University

Umetani, Kazuhiro

Graduate School of Environmental, Life, Natural Science and Technology, Okayama University

Ishihara, Masataka

Graduate School of Environmental, Life, Natural Science and Technology, Okayama University

Sakai, Hiroto

ROHM Research & Development Center, ROHM Co., Ltd.

他

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Improvement Turn on Loss Simulation Accuracy by Nonlinear Voltage Dependence Modeling of Gate Source Capacitance

Takuto Hayashi
Graduate School of
Environmental, Life, Natural
Science and Technology
Okayama University
Okayama, Japan
p6pm98sx@s.okayama-u.ac.jp

Kazuhiro Umetani
Graduate School of
Environmental, Life, Natural
Science and Technology
Okayama University
Okayama, Japan
umetani@okayama-u.ac.jp

Masataka Ishihara
Graduate School of
Environmental, Life, Natural
Science and Technology
Okayama University
Okayama, Japan
masataka.ishihara@ec.okayama-
u.ac.jp

Hiroto Sakai
ROHM Research & Development
Center
ROHM Co., Ltd.
Kyoto, Japan
hiroto.sakai@rohm.co.jp

Yuta Okawauchi
ROHM System Solutions Engineering
Headquarters
ROHM Co., Ltd.
Kyoto, Japan
Yuta.Okawauchi@mnf.rohm.co.jp

Kotaro Kobashi
Graduate School of Environmental, Life,
Natural Science and Technology
Okayama University
Okayama, Japan
pctz02ec@s.oakayama-u.ac.jp

Eiji Hiraki
Graduate School of Environmental, Life,
Natural Science and Technology
Okayama University
Okayama, Japan
hiraki@okayama-u.ac.jp

Abstract— This paper discusses the importance of accurately modeling the gate-source parasitic capacitance of semiconductor devices to estimate the switching losses required to optimize heat dissipation components. We focus on the gate-source voltage dependence of gate-source capacitance, which has not received much attention in the past, and measure for the first time its characteristics at high drain voltages. The proposed measurement method revealed a significant difference in characteristics with and without drain voltage. By applying the model incorporating this new knowledge to SPICE simulations, we succeeded in accurately estimating the Turn on switching losses and verified the effectiveness of the proposed method.

Keywords— switching device, SPICE simulation, gate-source capacitance, switching loss

I. INTRODUCTION

Switching devices such as MOSFETs are used in a wide range of fields, from consumer and industrial equipment to in-vehicle devices, including electronic devices, factory automation equipment, power circuits (DC-DC converters, etc.), and motor drive inverters. [1]. In recent years, the emergence of next-generation switching devices such as SiC-MOSFETs [2],[3] and GaN-HEMTs [4], which are capable of operating at high speeds, has led to a shift towards higher frequencies in power conversion circuits. The increased driving frequency of these circuits allows for the reduction of the volume of passive components like inductors and capacitors, thereby minimizing the overall size of the circuit. However, operating at higher frequencies also increases the losses generated in switching devices, necessitating additional heat-dissipating components to manage cooling, which can impede miniaturization efforts. This issue is particularly pronounced in inverters that handle large

amounts of power, where heat-dissipating components often occupy more volume than passive components. Thus, an effective heat dissipation design is crucial for the miniaturization of the entire circuit. To optimize the design of heat-dissipating components, accurate calculations of switching losses based on voltage and current waveforms during switching are required. Measuring these waveforms directly in actual circuits poses challenges due to the influence of parasitic components in measurement equipment probes and the limitations of probe size. Consequently, there is a need to estimate waveforms through simulation using a circuit simulator.

Accurate modeling of the parasitic capacitance of switching devices is crucial for simulating switching waveforms. The parasitic capacitances of switching devices exhibit nonlinear characteristics with respect to the applied voltage. Among them, the gate drain capacitance C_{gd} and the drain source capacitance C_{ds} show significant dependence on the applied voltage, and numerous detailed models have been reported for tuning these parameters [5],[6],[7]. However, there are few reports focusing on the voltage dependence of the gate-source capacitance C_{gs} . In many manufacturer-supplied models, C_{gs} is represented as a constant ideal capacitor, disregarding its variability. This is due to two main factors.

Firstly, C_{gs} has a small dependence on the drain voltage V_{ds} and gate voltage V_{gs} , and its capacitance fluctuation has been considered negligible compared to the other two parasitic capacitances. Especially in FETs for low power applications, C_{gs} itself is very small, and its dependency can be ignored. However, recent advancements have led to the development of devices with higher current capabilities for handling high power. Generally, to achieve higher current handling, the chip size

needs to be increased for better wiring and heat dissipation. This increase in chip size also increases the parasitic capacitance of the device. Consequently, the previously negligible dependence may now result in significant changes in capacitance values.

Secondly, it has been impossible to measure the gate-source capacitance versus gate-source voltage characteristic ($C_{gs} - V_{gs}$ characteristic) with an applied drain voltage. While there are instances where the $C_{gs} - V_{gs}$ characteristic has been measured[8] and simulations have been conducted using models incorporating this characteristic[9],[10], these measurements were performed with no drain voltage applied ($V_{ds} \cong 0V$). This is because, beyond the threshold value, the drain-source interface becomes short-circuited, causing excessive drain current flow when the drain voltage is applied. Therefore, there have been no actual measurements of the $C_{gs} - V_{gs}$ characteristic with an applied drain voltage.

However, the voltage dependence of C_{gs} is a critical factor in estimating switching losses. Fig.1 illustrates the relationship among the drain current I_{ds} , drain-source voltage V_{ds} , and gate-source voltage V_{gs} during the turn-on switching of a device with an inductive load. During turn-on switching, V_{gs} rises while V_{ds} is applied to the device. When V_{gs} reaches the threshold voltage V_{th} , I_{ds} begins to flow, but V_{gs} continues to rise. The plateau voltage V_p increases with the current flowing through the device, making V_p significantly higher than V_{th} in high-current applications. The drop in V_{ds} begins when I_{ds} equals the load current. Therefore, during the period indicated in blue in Fig.1, charge is accumulated in C_{gs} while V_{ds} is applied. If C_{gs} exhibits V_{gs} voltage dependence during this period, the time to reach V_p changes, and consequently, the slope of I_{ds} changes. Additionally, the $C_{gs} - V_{gs}$ characteristic may vary significantly when the drain voltage is applied versus when it is not, greatly affecting switching loss estimation. Hence, it is necessary to measure the $C_{gs} - V_{gs}$ characteristic with an applied drain voltage.

The purpose of this paper is to measure the voltage dependence of the gate-source parasitic capacitance C_{gs} beyond the device threshold under high drain voltage conditions and to verify its effect on improving the accuracy of switching waveform predictions.

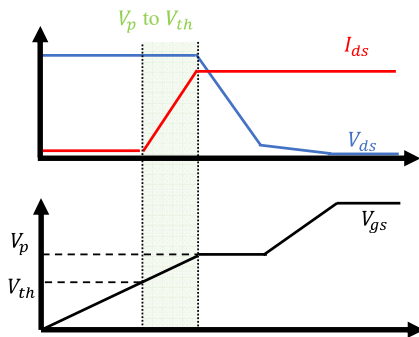


Fig.1 Turn on switching waveforms

II. METHOD OF MEASURING $C_{gs} - V_{gs}$ CHARACTERISTICS WHEN DRAIN VOLTAGE IS APPLIED

It is not easy to measure the $C_{gs} - V_{gs}$ characteristics after the threshold with drain voltage applied. Generally, dedicated devices such as curve tracers are used to measure the voltage dependence of parasitic capacitances of devices, but it is impossible to measure the $C_{gs} - V_{gs}$ characteristics with the drain voltage applied in these devices. This is because if the device is always turned on, an excessive drain current continues to flow, leading to damage to both the device and the measurement equipment. Additionally, it is difficult to keep the drain voltage applied while the device is turned on.

Therefore, in this study, a capacitance measurement method using a double-pulse test circuit was considered. A combination of a high-frequency AC voltage for capacitance measurement and a pulse voltage to turn on the device for a short period is applied between the gate and source of the switching device. We propose a method to determine the C_{gs} capacitance from the amplitude and phase of the AC component of the gate-source voltage V_{gs} and the gate current I_g . This method is described below.

Fig.2 shows the $C_{gs} - V_{gs}$ voltage dependence measurement circuit: C_{in} is connected to a DC voltage source V_{in} to supply an arbitrary voltage to be applied between the drain source of switch S_1 . The drain terminal of S_1 is connected to the source part of switch S_2 and an inductor L . The inductor L should have a large enough inductance to keep the drain current flowing through S_1 during switching. the gate of S_1 is connected to the power supply V_{pul} to apply pulse voltage through resistor R_1 and to the AC voltage source V_{ac} through shunt resistor R_{snt} for current measurement and DC cut capacitor C_1 . ac is connected to the AC voltage source V_{ac} . The AC voltage source V_{ac} supplies an AC current with frequency f_{ac} , which is detected by the voltage at both ends of R_{snt} .

The waveforms of each operation in this circuit are shown in Fig.3. This circuit inputs two pulses with different peak values of V_{pul} . The first pulse of V_{pul} is a voltage sufficient to turn the device fully on, while the second pulse is a double pulse with a peak value corresponding to the V_{gs} voltage whose dependence is to be measured. the period t_1 is when switching S_1 turns on completely and the inductor current rises. By adjusting the time

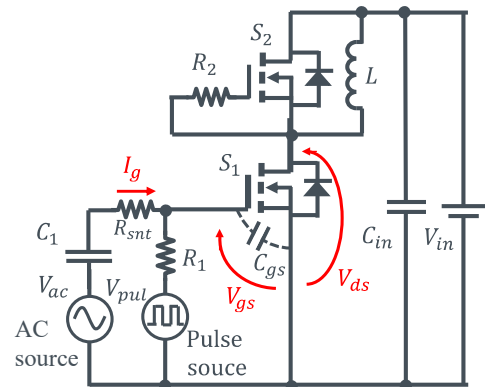


Fig.2 $C_{gs} - V_{gs}$ measurement circuit

of t_1 , the inductor current is increased to the maximum withstand current of the device. During the period t_2 , the inductor current is maintained by the return current through the body diode of S_2 . As a result, during the period t_3 , the inductor current is maintained at a level larger than the drain current that the device tries to flow due to the applied V_{gs} . As the inductor current continues to return, the voltage at both ends of S_2 becomes the forward voltage of the body diode, allowing the gate voltage V_{gs} after the threshold can be applied in a pulsed manner without V_{ds} dropping.

To eliminate the effects of parasitic inductance and measure only the parasitic capacitance, the frequency of the AC voltage source V_{ac} should be as low as possible. However, to maintain measurement accuracy, the frequency should be set so that several cycles of AC voltage are applied within the on period of the second pulse. The amplitude of this AC voltage V_{ac} is superimposed on the pulse wave V_{pul} . Therefore, the AC amplitude component must be as small as possible to obtain the dependence on V_{gs} . Additionally, for the measurement, the values of R_1 , C_1 , and R_{snt} need to be changed according to the measurement target. R_1 should remain constant during the second pulse of V_{pul} , and the impedance seen from the AC power source should be sufficiently larger the impedance of C_{gs} at the frequency f_{ac} so that the component of C_{gs} dominates. C_1 must cut the voltage supplied from the pulse power supply, but the AC amplitude must be measurable at t_3 . Therefore, the capacitance value of C_1 should be sufficiently smaller that of C_{gs} . Similarly, R_{snt} should be kept at the same level as the impedance of C_{gs} so that the AC amplitude can be measured at t_3 .

Ultimately, during the period t_3 , the AC amplitude v_{gs} of the gate-source voltage V_{gs} , the AC amplitude i_g of the current through R_{snt} , and their phase difference θ are measured. From these measurements, C_{gs} can be determined according to (1). When a high drain voltage is applied, the parasitic capacitance

C_{gd} becomes sufficiently small compared to C_{gs} . Therefore, the $C_{gs} - V_{gs}$ characteristic can be obtained from the DC component of the simultaneously measured V_{gs} voltage.

$$C_{iss} \cong C_{gs} = \frac{i_g}{2\pi f_{ac} v_{gs}} \sin \theta \quad (1)$$

III. CGS-VGS CHARACTERISTIC MEASUREMENT EXPERIMENT

This chapter reports the results of evaluating the $C_{gs} - V_{gs}$ characteristics of Si and SiC-MOSFET devices using the $C_{gs} - V_{gs}$ characteristics measurement method described in Chapter II. Commercially available 4-terminal package MOSFETs were used for the measurements. The six types of MOSFETs used in the measurements are shown in TABLE 1. Fig.4 shows the measurement setup for the $C_{gs} - V_{gs}$ characteristics. In this experiment, an AC voltage source V_{ac} and a pulse voltage V_{pul} were supplied using a function generator and amplifier. f_{ac} was set at 2 MHz, and the turn-on time of the second pulse of V_{pul} was 18 μ s. The amplitude of V_{ac} was measured at several hundred mV. The AC current I_g and AC voltage V_{gs} were measured simultaneously using an oscilloscope, and their amplitudes and phase differences were obtained by Fourier series expansion. The circuit elements used in the measurements are shown in TABLE 2. The switching devices were evaluated by shaking the wave height of the second pulse within the measurable range according to (1), and the results are shown in Fig.5 as the $C_{gs} - V_{gs}$ characteristics. Fig.5 also presents the characteristics at a drain voltage of 0 V and a measurement frequency of 100 kHz, obtained using a curve tracer (B1505).

Fig.5 shows that for all devices, the results obtained with the curve tracer at $V_{ds}=0$ V and the results obtained using the proposed method with drain voltage applied are significantly different. The capacitance value increases around the threshold when a voltage is applied, and especially for Fig. 5 (a) and (b) with $V_{gs}=0$ V and large C_{gs} , the maximum capacitance value increases by more than 50%. Therefore, incorporating this characteristic into the model is expected to significantly alter the

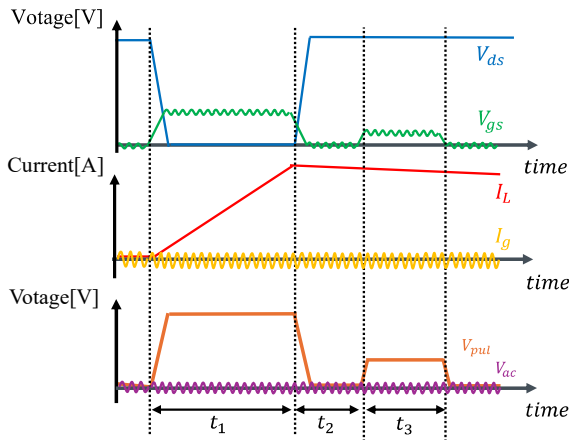


Fig. 3 waveforms of each operation

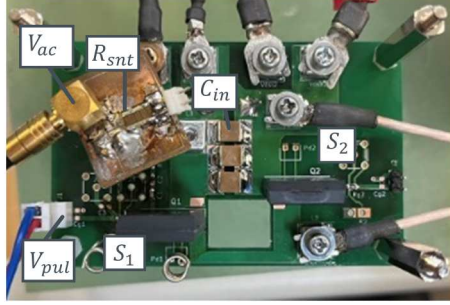
TABLE 1. Devices listed

Number	Manufacturer
S4611MFFCZTA	ROHM
FCH023N65S3L4	ON semiconductor
STW70N60DM6	STMicro
G3R20MT12K	GeneSiC
MSC015SMA070B4	Microchip
C3M0025065K	Wolfspeed(Cree)

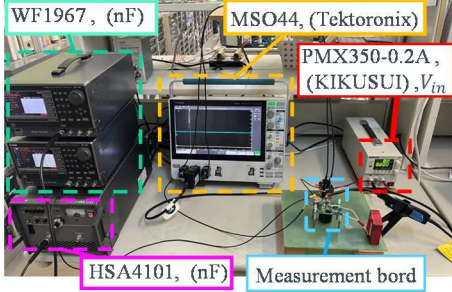
TABLE 2. $C_{gs} - V_{gs}$ Measurement Parameters

Symbols	Values (Manufacturer)
R_{snt}	5 Ω
L	109 μ H
C_{in}	1643 μ F
C_1	200 pF ~ 700 pF
R_1	100 Ω ~ 200 Ω
R_2	100 Ω

slope of the gate-source voltage during switching. Additionally, as shown in Fig. 5 (c), some devices exhibited constant capacitance values even when drain voltage was applied. This indicates that the manner in which the $C_{gs} - V_{gs}$ characteristic changes with applied drain voltage varies from device to device. This confirms the necessity of measuring the $C_{gs} - V_{gs}$ characteristic under applied drain voltage.



(a) Test circuit board to measure to $C_{gs} - V_{gs}$



(b) Photographs of test circuit
Fig.4 $C_{gs} - V_{gs}$ Measurement setup

IV. PREDICTION OF SWITCHING WAVEFORMS

This chapter compares the switching waveforms and switching losses at three different switching speeds by using SPICE simulations with the measured waveforms. A device exhibiting a particularly large variation in capacitance, S4611MFFCZTA, was used for these simulations. Two types of simulations are used: a conventional tuning that includes only the $C_{gs} - V_{gs}$ characteristics at $V_{ds}=0V$ measured with a curve tracer and a proposed tuning that includes the $C_{gs} - V_{gs}$ characteristics at high drain voltage, which were measured in Chapter III. The effect of including the $C_{gs} - V_{gs}$ characteristic at high drain voltage is discussed.

A. Switching Waveform Comparison

Fig. 6 shows the double pulse test circuit used in the simulation. The inductances L_{g1} , L_{g2} , L_d , L_{cs1} , and L_{cs2} in the circuit are parasitic to the substrate and package, and were measured using an impedance analyzer IM7581 (Hioki) and FRA51615 (NF Corp.) using the methods in the previous studies [11],[12]. Fig. 7 shows the actual double-pulse measurement environment. The measured waveforms were drain voltage V_{ds} , drain current I_d , and gate voltage V_{gs} of the low-side switch, which were measured at turn-on and turn-off, respectively. TABLE 3 shows the values of the circuit elements used in both the measurements and the simulations.

Comparison of simulated and measured waveforms at gate resistances of 100Ω , 33Ω , and 10Ω are shown in Fig. 8, Fig. 9, and Fig.10, respectively. In each figure, the timing at which the low-side gate voltage V_{gs} begins to fall for turn-off and the

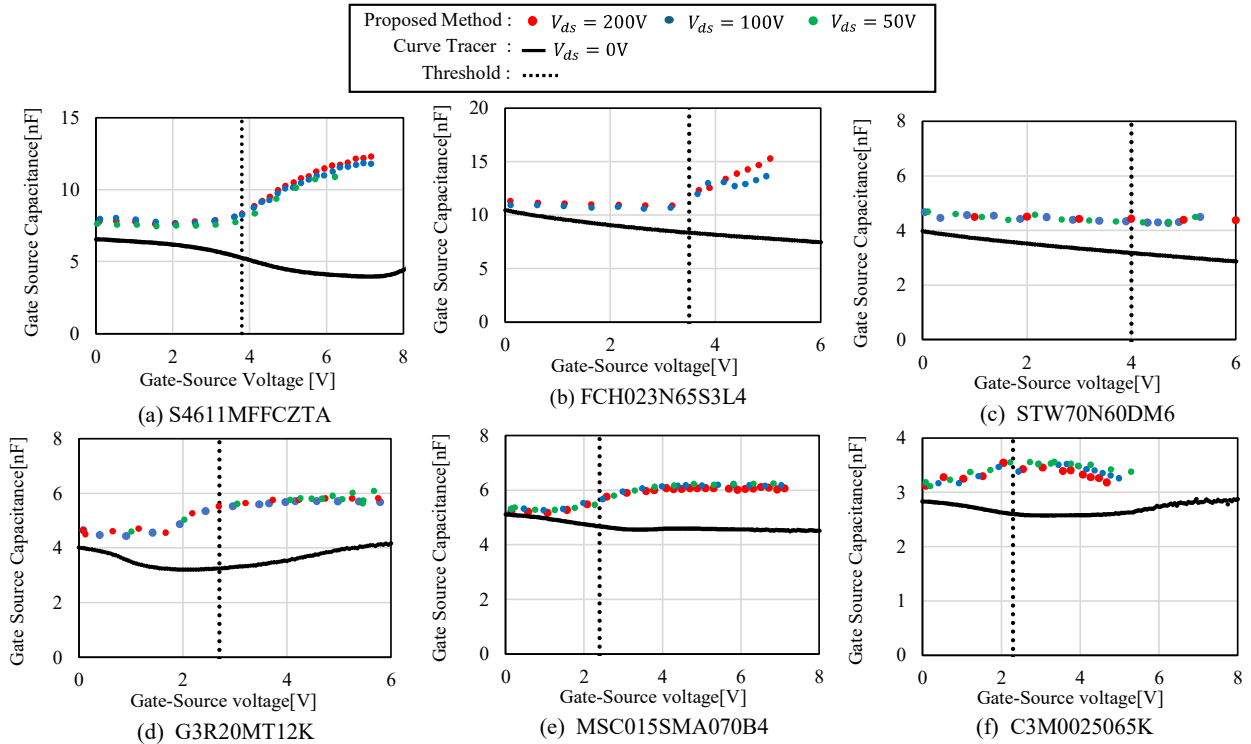


Fig.5 Measurement $C_{gs} - V_{gs}$ characteristics.

timing at which v_{gs} begins to rise for turn-on overlap between the actual measurement and the simulation.

As shown in the turn-on switching in Fig.8(a), Fig.9(a), and Fig.10(a), the slope of the low-side gate voltage waveform V_{gs} changes after the threshold at which drain current begins to flow for both the proposed and conventional tuning. This suggests that an increase in C_{gs} after the threshold value also occurs in the actual switching waveform. Moreover, the change in gate voltage waveforms shows that the time up to the plateau voltage matches the actual measurement, and the slope of I_d is much improved compared to the conventional tuning. On the other hand, in Fig.8(a) and Fig.9(a), the slope when V_{ds} is falling from 200V deviates from both simulations and measurements. This is thought to be due to the deviation of the parasitic capacitance C_{gd} . The period between the peak drain current and the drain voltage becoming almost 0 V corresponds to the mirror period, and this time varies depending on the magnitude of C_{gd} . The reason why the deviation of V_{ds} can hardly be confirmed in Fig.10(a) is because the mirror period is short due to the extremely fast switching speed, and the difference is not readily apparent in the waveform. This is because the mirroring period is short due to the very high switching speed, and the difference is not easily seen in the waveform. Generally, C_{gd} of SiC-MOSFET becomes much smaller when drain voltage is applied than when no drain voltage is applied. In fact, the device used in this study was measured to have $C_{gd}=15\text{pF}$ at $V_{ds}=200\text{V}$, and individual differences in devices and errors in capacitance measurement can easily increase the value. As a future issue, accurate estimation of C_{gd} during switching is required.

In the turn-off switching shown in Fig.8(b) and Fig.9(b), the slope of the falling gate voltage V_{gs} after the plateau voltage changes in a consistent manner, while the slope of the drain current deviates from the plateau voltage. The drain current deviation differs from the cause of the turn-on waveform deviation, and the drain voltage is constant during the period when the drain current deviates, indicating that it is not due to the effect of the feedback current due to C_{gd} . Reading the threshold value from the measured waveform, it can be confirmed that the characteristic actually changes from 4.7V during turn-on to 5.2V during turn-off. Since the waveforms from this simulation have a threshold of 4.7V for both turn-on and turn-off, it can be said that the cause of the drain current deviation is the change in the $I_d - V_{gs}$ characteristic only during turn-off in the actual measurement. However, since no threshold fluctuation occurs in Fig.10(b), it can be inferred that this phenomenon occurs in accordance with the switching speed.

TABLE 3. LIST OF EXPERIMENTAL AND SIMULATIONS INSTRUMENTS FOR DPT

Symbols / Parameters	Values
Rg1	Gate resistance of S1 side
Rg2	Gate resistance of S2 side
L load	Load inductor
Cdc	Input Capacitor
Ld	Drain parasitic inductance
Lg1	Gate parasitic inductance of S1 side
Lg2	Gate parasitic inductance of S2 side
Lcs1	Common source inductance of S1 side
Lcs2	Common source inductance of S2 side
	10Ω or 33Ω or 100Ω
	10Ω
	89.1μH
	683μF
	31nH
	22nH
	8.5nH
	417pH
	281pH

Since the difference in the slope of the drain current causes a shift in the period during which the switching loss is accounted for, it can be assumed that the simulation predicts a larger loss than the actual measurement for the waveforms with 33Ω and 100Ω gate resistors.

In general, the slope of the gate voltage waveform was greatly improved by modifying the capacitance values for both the turn-on and turn-off waveforms by considering the $C_{gs} - V_{gs}$ characteristics. It was also confirmed that this had a significant effect on the timing of the rise and fall of the drain voltage and the slope of the drain current.

B. Switching Loss Comparison

Next, the switching losses obtained from the switching waveforms are compared between the conventional and proposed tuning. the switching loss is calculated from the

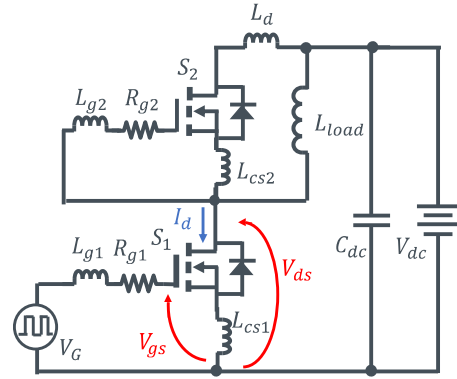
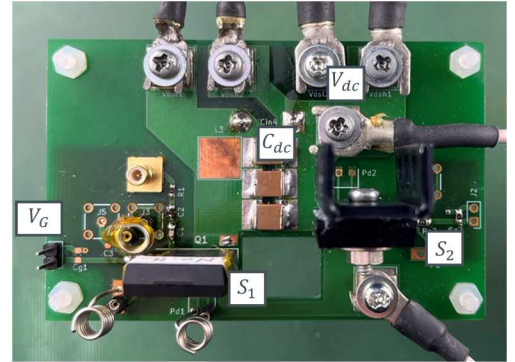
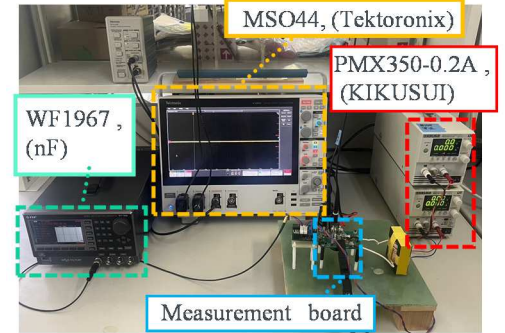


Fig. 6 Double pulse test simulation circuit.



(a) Measurement board



(b) Photographs of test circuit

Fig. 7 Double pulse Measurement setup

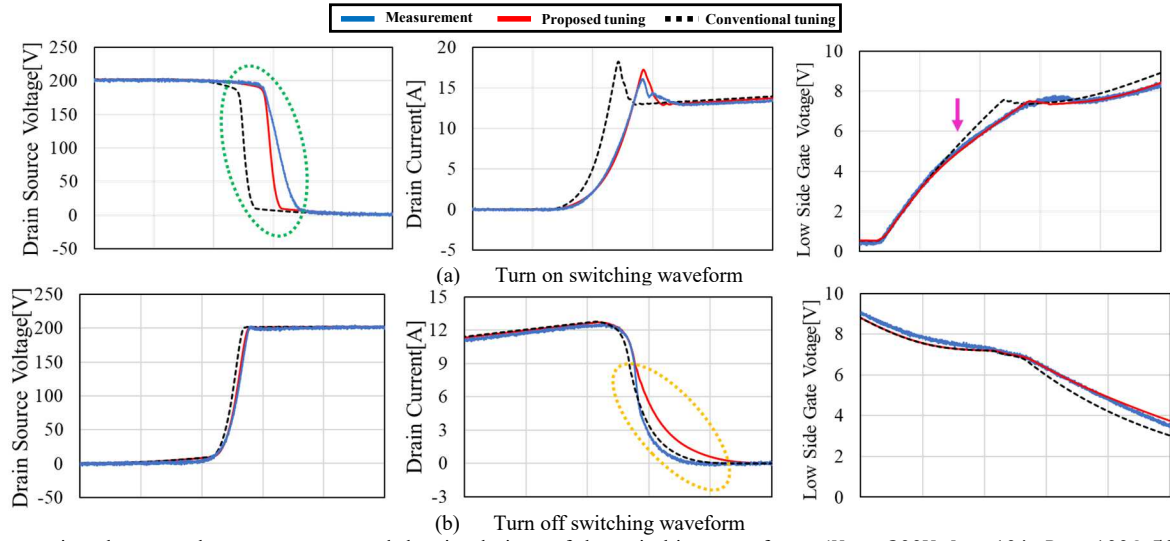


Fig. 8 Comparison between the measurement and the simulations of the switching waveforms ($V_{ds} = 200V$, $I_d = 10A$, $R_g = 100\Omega$, 50ns/div)

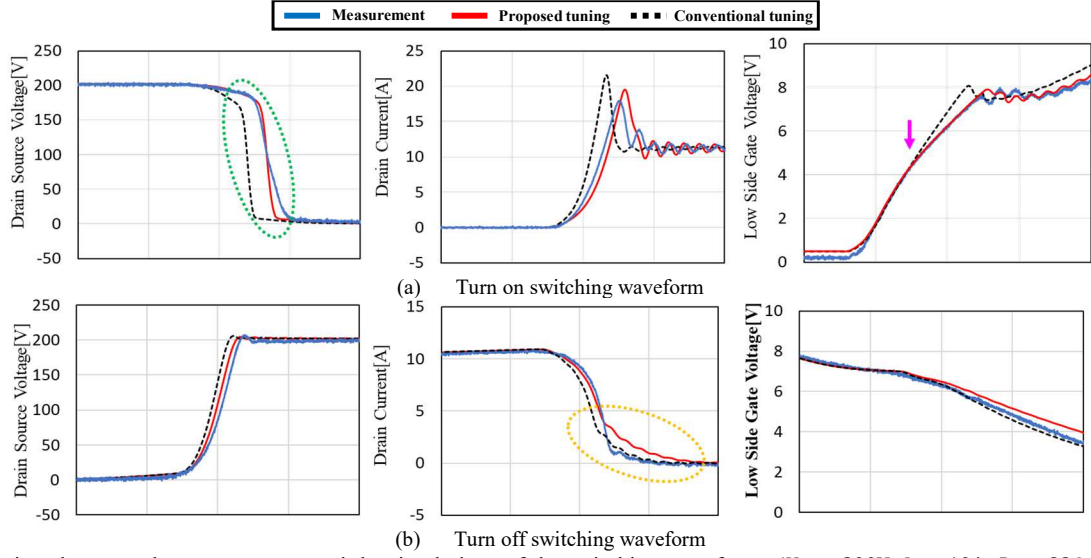


Fig. 9 Comparison between the measurement and the simulations of the switching waveforms ($V_{ds} = 200V$, $I_d = 10A$, $R_g = 33\Omega$, 100ns/div)

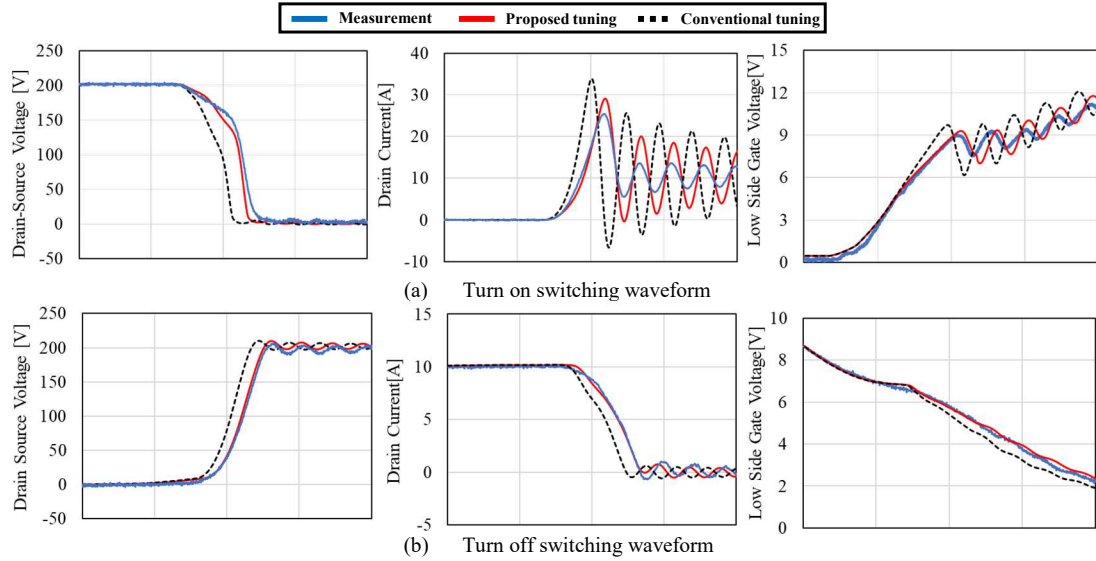


Fig. 10 Comparison between the measurement and the simulations of the switching waveforms ($V_{ds} = 200V$, $I_d = 10A$, $R_g = 10\Omega$, 50ns/div)

beginning of the rise of I_d until V_{ds} becomes zero. Fig. 11 shows the comparison results of switching loss obtained from the waveforms shown in Section A. Fig. 11(a) shows that the proposed tuning is more than 15% better than the conventional tuning in terms of turn-on loss at all switching speeds, and the prediction is accurate within 20% error rate. Therefore, the addition of the $C_{gs} - V_{gs}$ characteristic to the model was shown which to be effective in estimating turn-on loss. However, in the turn-off loss shown in Fig. 11(b), the proposed tuning deviates from the actual measurement by nearly a factor of 2 when the gate resistance is 33 and 100Ω. On the other hand, when the gate resistance is 10Ω, the switching loss is very consistent and within 10% of the error rate. From the above, it can be said that the deviation of the turn-off loss is caused by the deviation of the drain current as described in Section A. Therefore, the deviation of the drain current is the cause of the deviation of the turn-off loss. Therefore, by identifying the cause of the drain current deviation, we can eliminate the excessive deviation from the actual measurement and confirm the additional influence of the $C_{gs} - V_{gs}$ characteristic on the simulation model.

These results confirm that the addition of the $C_{gs} - V_{gs}$ characteristic to the model when drain voltage is applied greatly improves the prediction accuracy of the turn-on loss. Although no improvement in prediction accuracy could be demonstrated for turn-off loss, we were able to confirm the issues in switching loss estimation.

V. CONCLUSION

In this paper, we proposed a measurement method to extract the dependence of the parasitic capacitance C_{gs} after the

threshold on the gate-source voltage V_{gs} when a high drain voltage is applied. By applying the proposed method to several commercial Si and SiC-MOSFET, we actually measured the characteristics after the threshold when a high drain voltage was applied and found that the capacitance value changed. Furthermore, by comparing the switching losses using simulation, it was shown that adding the $C_{gs} - V_{gs}$ characteristics under the condition of applied drain voltage to the simulation model is effective in estimating the turn-on switching losses. Although we could not show an improvement in the prediction accuracy of the turn-off loss, we were able to confirm the issues in the estimation of the switching loss.

REFERENCES

- [1] Renesas Electronics Corp : 「Power MOSFET Application Note」 , Application Note, R07AN0007EJ0110, pp2, (2022)
- [2] F. Jiang, S Yang and K Sheng: "Comparative study on temperature-dependent characteristic parameters of SiC MOSFET", Journal of Power Supply., Vol. 16, NO. 6, pp. 143-151, (2018)
- [3] Ryota Maeno, Hideki Omori, Hisato Michikoshi, Noriyuki Kimura, and Toshimitsu Morizane, : "A 3kW Single-Ended Wireless EV Charger with a Newly Developed SiC-VMOSFET," IEEE 2th Int. Conf. on Renewable Energy Research and Applicat, (ICRERA), 2018.
- [4] Alex Lidow et al., "GaN Transistor for Efficient Power Conversion", Wiley, pp.1-2 (2020)
- [5] D. Johannesson, M. Nawaz, "Analytical PSpice model for SiC MOSFET based high power modules", Microelectronics J., vol. 53, pp. 167–176, Jul. 2016
- [6] K. Chen, Z. Zhao, L. Yuan, T. Lu and F. He, "The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET," in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 333-338, Feb. 2015
- [7] F. -J. Hsu, C. -C. Hung, K. -T. Chu, L. -S. Lee and C. -Y. Lee, "A Dynamic Switching Response Improved SPICE Model for SiC MOSFET with Non-linear Parasitic Capacitance," 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, 2020, pp. 1-4
- [8] R. Stark, A. Tsibizov, I. Kovacevic-Badstuebner, T. Ziemann and U. Grossner, "Gate Capacitance Characterization of Silicon Carbide and Silicon Power mosfets Revisited," in IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 10572-10584, Sept. 2022
- [9] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda and H. Tanigawa, "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior Over Wide Voltage and Current Ranges," in IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7314-7325, Sept. 2018
- [10] Z.Wang, X. Yang, Y. Ding and J. Wang, "An Improved SPICE Model of SiC MOSFET by Output Nonlinear Capacitor Optimization," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 2020, pp. 3132-3137
- [11] K. Umetani, K. Aikawa, and E. Hiraki: "Straightforward Measurement Method of Common Source Inductance for Fast Switching Semiconductor Devices Mounted on Board", IEEE Trans. Ind. Electron, Vol.64, No. 10 pp. 8258 - 8267 (2017)
- [12] K. Umetani ,Keisuke Yagyu ,Eiji Hiraki : "A Design Guideline of Parasitic Inductance for Preventing Oscillatory False Triggering of Fast Switching GaN-FET",IEEJ Trans 11(S2): S84–S90 (2016)

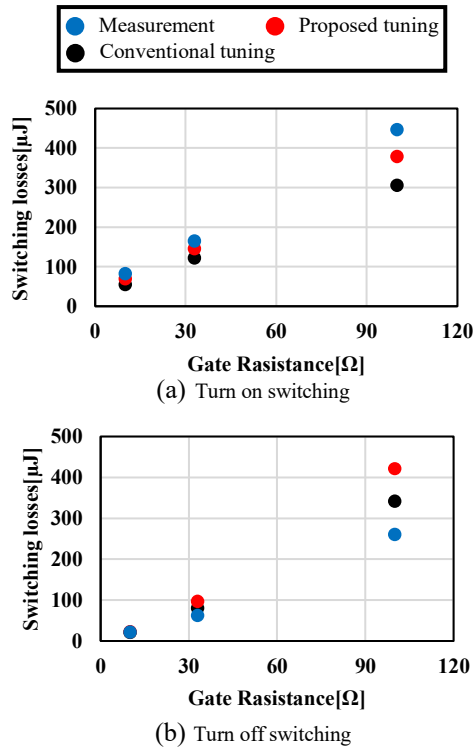


Fig.11 Comparison of switching losses