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Equivalent Capacitance of Nonlinear Capacitance in GaN-FET for Improving Accuracy in Suppressing Conditions of Oscillatory False Triggering

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Abstract— While GaN-FET enables the miniaturization and increased efficiency of power modules, its low threshold voltage increases the likelihood of malfunctions. Additionally, the occurrence of oscillatory false triggering has been reported. This phenomenon is caused by oscillations in the gate-source voltage due to parasitic capacitors of GaN-FET and wiring inductors. These issues hinder the practical application of GaN-FETs. An existing method to suppress this involves adjusting the wiring inductance, a component of the parasitic oscillator, to match the parasitic capacitance, thereby avoiding oscillation conditions. However, this method does not sufficiently consider the nonlinear characteristics of the parasitic capacitance, which varies with voltage. This leads to discrepancies between the calculated and measured values of the wiring inductance required to suppress oscillatory false triggering. Therefore, the objective of this study is to propose a method for deriving the equivalent capacitance of nonlinear capacitance in oscillatory states to improve the suppression accuracy of oscillatory false triggering.

Keywords—GaN-FET, false turn-on, oscillatory false triggering, nonlinear capacitance

I. INTRODUCTION

The next-generation switching device, GaN-FET, enables high-speed switching and low on-resistance compared to conventional Si semiconductors. These characteristics contribute to the miniaturization and increased efficiency of power modules [1]-[4]. However, despite its excellent performance, GaN-FET has a low threshold voltage, making it tend to malfunction due to noise generated during switching. Additionally, high-speed switching devices like GaN-FET occur oscillatory false triggering, caused by oscillation in the gate-source voltage [5]-[13]. Once initiated, this phenomenon continues to cause unintended turn-ons, resulting in substantial switching losses and potentially damaging the device or PCB. To ensure the stable operation of GaN-FET, it is crucial to prevent oscillatory false triggering.

Oscillatory false triggering can be suppressed by reducing noise generated in the gate circuit. Previous studies have proposed inserting a gate resistor to lower the Q-factor of the gate loop, thereby suppressing oscillatory false triggering [6]-[8]. However, this method reduces switching speed, hindering high-speed operation and diminishing the advantages of GaN-FET. Hence, there is a need for techniques to suppress oscillatory false triggering without relying on resistors.

Oscillatory false triggering occurs when a parasitic oscillator formed by parasitic capacitors of the GaN-FET and parasitic inductors of the circuit wiring meets the oscillation conditions [5][10]. Therefore, by appropriately adjusting the wiring inductance relative to the parasitic capacitance to avoid oscillation conditions, suppression of this phenomenon can be achieved [10]. This method focuses on the circuit components causing noise, constructs a linear circuit based on these components, and derives suppression conditions for oscillatory false triggering by analyzing the oscillation conditions.

However, the parasitic capacitance of the switching element has a nonlinear characteristic that changes with the drain-source voltage. This characteristic appears during switching when the drain-source voltage changes rapidly. Thus, when analyzing switching phenomena using a linear circuit, it is necessary to consider this nonlinear characteristic and use an appropriate equivalent capacitance. In a suppression method [10], a single value read from the C-V characteristics of the parasitic capacitance at the power supply voltage applied during turn-off was used as the equivalent capacitance value for the nonlinear capacitance. Given that oscillatory false triggering are oscillation-induced malfunctions, the drain-source voltage oscillates rather than remains constant when they occur. Therefore, it is thought that the equivalent capacitance of the nonlinear capacitance during oscillatory false triggering should be determined from the perspective of oscillation rather than as a single value. Moreover, verification experiments in this study

showed that oscillatory false triggering were suppressed at a wiring inductance different from that calculated using the suppression conditions derived from a single value. This suggests the existence of a more appropriate equivalent capacitance for nonlinear capacitance during oscillatory false triggering.

In this way, the nonlinear capacitance makes it difficult to design wiring inductance for preventing oscillatory false triggering. In research on the suppression of oscillatory false triggering, SPICE simulations are often used for circuit design [11]-[13]. A feature of this method is that it takes time to construct the simulation circuit and search for optimal inductance conditions. Thus, by analytically determining the equivalent capacitance of the nonlinear capacitance, it is possible to calculate the wiring inductance that suppresses oscillatory false triggering without using simulations.

A common method for calculating the equivalent capacitance of a nonlinear capacitance involves deriving the equivalent capacitance from the perspective of total charge and electrostatic energy [14]-[16]. These methods derive an equivalent capacitance from the behavior of the capacitor in that phenomenon. In oscillation phenomena, the nonlinear capacitors is distributed in the feedback circuit of the oscillator and plays the role of the reactance of the feedback circuit. Therefore, the equivalent capacitance of the nonlinear capacitance in oscillation phenomena needs to be considered from its reactance. By using the equivalent capacitance derived from this consideration, it is possible to improve the accuracy of suppression conditions for oscillatory false triggering.

Therefore, this study proposes a method for deriving the equivalent capacitance of nonlinear capacitance from the perspective of reactance to improve the suppression accuracy of oscillatory false triggering. Additionally, a comparison is made between the prediction accuracy of existing equivalent capacitance derivation methods and the proposed method to evaluate the superiority of the proposed method.

II. SUPPRESSION CONDITION OF OSCILLATORY FALSE TRIGGERING

A suppression principle of oscillatory false triggering outlined in prior research [10] is demonstrated. Oscillatory false triggering arise due to parasitic capacitors of GaN-FETs and wiring parasitic inductors during switching. To derive

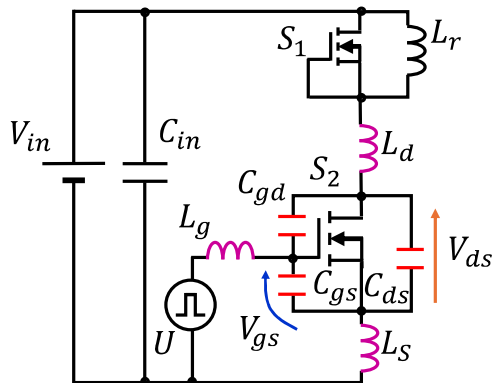
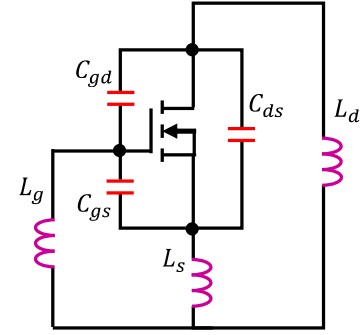
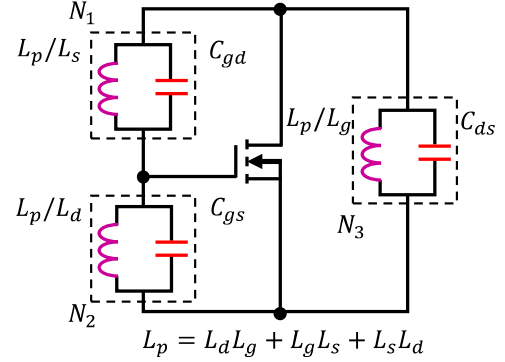


Fig. 1. Double pulse test circuit



(a) Circuit by parasitic components



(b) Oscillator of parasitic components

Fig. 2. Equivalent circuit in oscillatory false triggering

suppression conditions, analysis is conducted using the circuit shown in Fig. 1. The circuit is a double-pulse test circuit that takes parasitic components into account. In the figure, L_d and L_g represent the wiring inductors in the power loop and gate loop, respectively. L_s is a source inductor existing in the common part of the power loop and the gate loop. C_{ds} , C_{gd} and C_{gs} denote the parasitic capacitors of the GaN-FET between drain-source, gate-drain, and gate-source, respectively. Also, the parasitic capacitances express the linear capacitance during oscillatory false triggering. Other circuit symbols denote the input voltage V_{in} , input capacitor C_{in} , and load inductor L_r .

For simplification of the analysis, the following equivalent circuit transformations are carried out. First, oscillatory false triggering occur during the turn-off of the low-side, thus the high-side GaN-FET is conducting between drain and source, effectively short-circuiting. Then, given the high oscillation frequency of oscillatory false triggering, C_{in} can be treated as a short circuit, and L_r can be considered as an open circuit. Finally, since oscillatory false triggering are caused by parasitic components, it is considered as a circuit that extracts only these components. As a result, an equivalent circuit such as Fig. 2(a) is obtained. Performing a Y- Δ transformation on the wiring inductances results in Fig. 2(b). It becomes clear that this circuit in the diagram as a Barkhausen oscillator.

Oscillation conditions of this circuit can be determined from the open-loop gain of the gate-source voltage. Solving this, the reactance conditions for subcircuits $N_1 \sim N_3$ that meet the oscillation conditions are as shown in Fig. 3. These oscillators

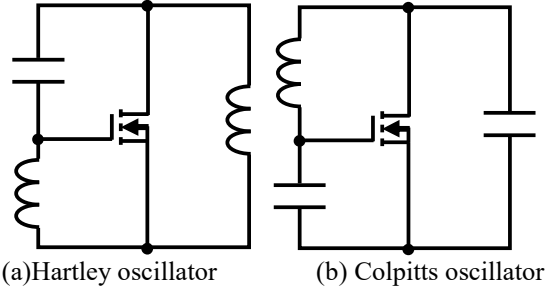


Fig. 3. Oscillator meeting oscillation condition

compose typical Hartley and Colpitts oscillators. Suppression of oscillatory false triggering occurs when the circuit in Fig. 2 does not form a circuit like the one in Fig. 3. Therefore, the frequency characteristics of the reactance of the subcircuits are examined. Since the subcircuits are LC parallel circuits, they exhibit inductive characteristics in the frequency range below the resonant frequency and capacitive characteristics in the higher frequency range. Let the resonant frequencies of subcircuits $N_1 \sim N_3$ be $f_1 \sim f_3$. Thus, the conditions for the resonant frequencies to suppress oscillatory false triggering can be expressed as follows.

$$f_2 < f_1 < f_3 \cup f_3 < f_1 < f_2 \quad (1)$$

Furthermore, the resonant frequencies $f_1 \sim f_3$ can be expressed by the following equations.

$$f_1 = \frac{1}{2\pi\sqrt{C_{gd} \cdot L_p/L_s}} \quad (2)$$

$$f_2 = \frac{1}{2\pi\sqrt{C_{gs} \cdot L_p/L_d}} \quad (3)$$

$$f_3 = \frac{1}{2\pi\sqrt{C_{ds} \cdot L_p/L_g}} \quad (4)$$

By substituting and rearranging equations (2) to (4) into (1), these are expressed as following equation.

$$\frac{L_d}{C_{gs}} < \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} \cup \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} < \frac{L_d}{C_{gs}} \quad (5)$$

Therefore, the design method for wiring inductances to suppress oscillatory false triggering can be achieved by adjusting the ratio between wiring inductances and parasitic capacitances, as indicated in (5).

III. EQUIVALENT CAPASITANCE OF NONLINEAR CAPACITANCE

A. Constructing the analysis model

From the suppression conditions for oscillatory false triggering, the equivalent capacitance of the nonlinear capacitance should be determined based on the resonant

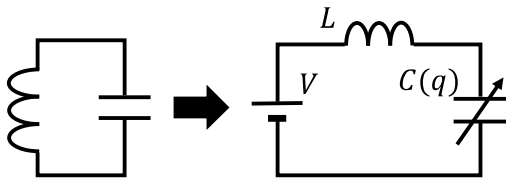


Fig. 4. Analysis model of LC resonant of nonlinear capacitance

frequency. For the analysis of the resonance frequency due to the nonlinear capacitance, an analysis model is obtained as shown in Fig. 4, derived from the subcircuit in Fig. 2(b). In the Fig.4., $C(q)$ represents the nonlinear capacitance and the voltage source V represents the power supply voltage (input voltage). For the subsequent analysis, the nonlinear capacitance is expressed as a function of the accumulated charge q rather than as a function of the voltage V .

B. Derivation of the equivalent capacitance

The resonant frequency can be obtained as the reciprocal of the resonant period. Therefore, subsequent analysis use analytical mechanics to derive the resonant period.

By regarding the accumulated charge q of the capacitor as a generalized coordinate, the Lagrangian Λ of the circuit in Fig. 4 is expressed as follows, as it is the energy due to the time derivative of the accumulated charge q minus the potential energy of the accumulated charge.

$$\Lambda = \frac{1}{2}L\dot{q}^2 - E_c(q) + qV \quad (6)$$

$E_c(q)$ represents the electrostatic energy stored in the nonlinear capacitor. Also, $\dot{q}$ is the time derivative of q . From (6), the Hamiltonian H is expressed as

$$H = \frac{\phi^2}{2L} + E_c(q) - qV \quad (7)$$

ϕ is the generalized momentum of q and it is expressed as follows

$$\phi = L\dot{q} \quad (8)$$

Since the above Hamiltonian doesn't include the function of time t , so the Hamilton-Jacobi equation is obtained by considering the principal function S

$$\frac{1}{2L} \left(\frac{\partial S(q)}{\partial q} \right)^2 + E_c(q) - qV = E \quad (9)$$

E represents the energy of the resonant system. Furthermore, S can be expressed as follows using the function $S(q)$ and E :

$$S = -Et + S(q) \quad (10)$$

By transforming (9), $S(q)$ is expressed as:

$$S(q) = \pm \int \sqrt{2L(E - E_c(q) + qV)} dq \quad (11)$$

By taking the appropriate sign of $S(q)$ and partial differentiating both sides of (10) with respect to E ,

$$\frac{\partial S}{\partial E} = \frac{\partial S(q)}{\partial E} - t = \int \frac{\sqrt{L}dq}{\sqrt{2(E - E_c(q) + qV)}} - t = t_0 \quad (12)$$

Since the energy of the system is conserved, the value obtained by differentiating the principal function S with respect to energy E is constant value, and this value is denoted as t_0 . From (12), the motion of the charge q is solved in the time domain for LC resonance due to the nonlinear capacitance. The charge q during resonance can take the minimum value q_α to the maximum value q_β within one period. These two values

correspond to the charge where the potential energy is minimum or maximum, and can be determined from the following equation

$$E = E_C(q) - qV \quad (13)$$

The resonance period T can be considered as twice the period during which the charge transitions from q_α to q_β . Expressed in formula form, it is as follows

$$T = 2 \int_{q_\alpha}^{q_\beta} \frac{\sqrt{L} dq}{\sqrt{2(E - E_C(q) + qV)}} \quad (14)$$

From the above, the equivalent capacitance C_{eq} of the nonlinear capacitance based on the resonance period can be derived by comparing the resonance period ($T = 2\pi\sqrt{LC_{eq}}$) as follows

$$C_{eq} = \frac{1}{2\pi^2} \left\{ \int_{q_\alpha}^{q_\beta} \frac{dq}{\sqrt{2(E - E_C(q) + qV)}} \right\}^2 \quad (15)$$

When considering the switching time, since the input voltage is applied to the nonlinear capacitance, V is set as the input voltage, and $E = 0$ is set because resonance starts from the initial charge $0[C]$ and initial current $0[A]$. The electrostatic energy $E_C(q)$ can be derived by converting the C-V characteristic to the V-Q characteristic and integrating it. In this study, the parasitic capacitors C_{gd} and C_{ds} with large variations based on the C-V characteristic were applied to this equation. The capacitor C_{gs} was considered constant since its variation relative to the initial value is small with respect to voltage.

IV. EXPERIMENTAL VERIFICATION

A. Purpose

The purpose of this experiment is to investigate the occurrence and suppression of oscillatory false triggering under suppression conditions obtained from various calculation methods for the equivalent capacitance used in the suppression condition (5). The equivalent capacitances were determined using the calculation method shown in the previous chapter, along with the single value obtained from the C-V characteristic and the equivalent capacitance based on the total charge [16]. The equivalent capacitance C_Q based on the total charge is calculated using the following equation, where $C(V)$ is the C-V characteristic of the nonlinear capacitance expressed as a function of the voltage V :

$$C_Q = \frac{\int_0^{V_{in}} C(V) dv}{V_{in}} \quad (16)$$

B. Experimental details

In the experiment, a printed circuit board as shown in Fig. 5 was made, and a double pulse test was conducted. The circuit diagram is shown in Fig. 1. The PCB was designed to allow for an adjustment of L_s by changing the length of the wiring, thereby adjusting the inductance as shown in Fig. 6. The adjustment method allows the length to be varied by using 0Ω resistors or copper sheets on each side of the PCB. This allows L_s to be adjusted from a minimum of 436 pH to a maximum of 1930 pH. During the adjustment of L_s , the inductances L_d and L_g of the wiring slightly changed because the length of the

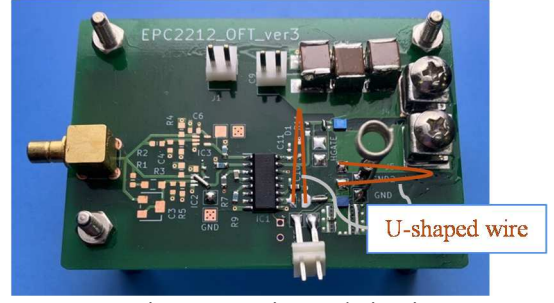


Fig. 5. Experimental circuit

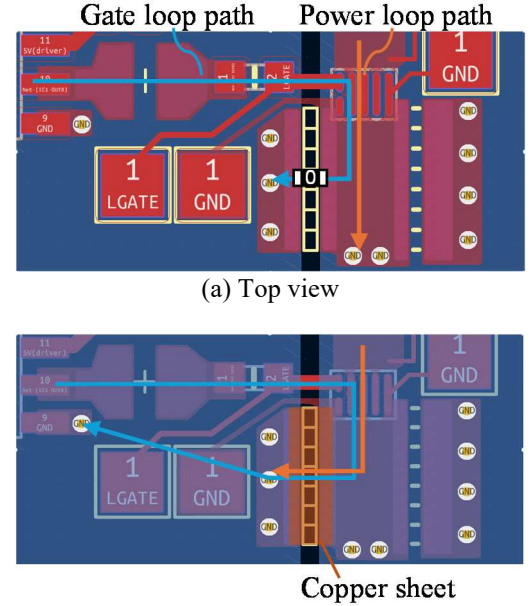


Fig. 6. Adjustment of source inductance



Fig. 7. U-shaped wire

common part of the power loop and gate loop was altered. To approximately maintain L_d and L_g at 35.0 nH and 35.1 nH respectively, U-shaped wires as shown in Fig. 7 were created and inserted at the positions shown in Fig. 5 (power loop and gate loop). The values of L_d and L_g are such that the range in which oscillatory false triggering occur falls within the adjustable range of L_s .

L_s was measured by using previous research [17]. Additionally, L_d and L_g were measured by using resonance with an external capacitor, as described in the Appendix [18].

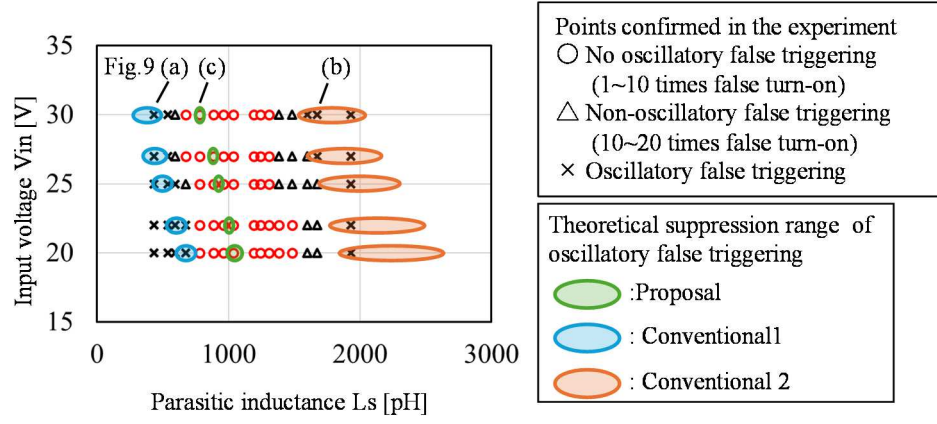


Fig. 8. Range of false triggering suppression in each input voltage comparison conventional with proposed method

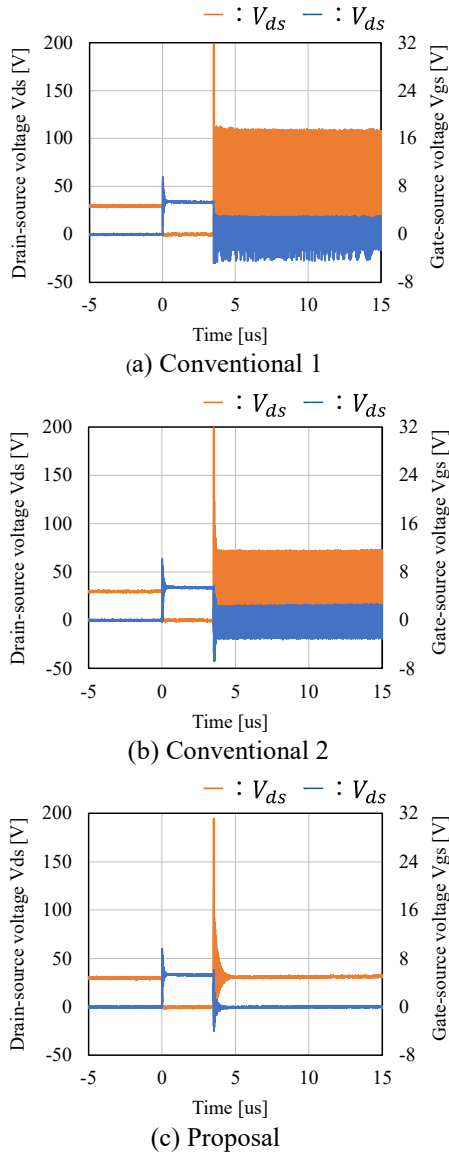


Fig. 9. Measured waveforms at the points where oscillatory false triggering was predicted to be suppressed for each equivalent capacitance value

For the details of the experiment, S_2 was kept turn-on until the load inductor L_r reached 15 A, and then S_2 was turned off. The gate-source voltage and drain-source voltage were observed.

To examine the changes in suppression conditions due to the nonlinearity of parasitic capacitance, the input voltage was varied at five levels (20V, 22V, 25V, 27V, 30V) in the voltage range where the capacitance fluctuates sharply in the C-V characteristic of the GaN-FET used in the experiment. Also, The components used in the experiment corresponding to Fig. 1 are listed in Table 1.

C. Result

The experimental results are shown in Fig. 8. This figure indicates the presence or absence of oscillatory false triggering caused by L_s with respect to the input voltage. Instances where the number of malfunctions after turn-off was less than 10 were considered to have suppressed oscillatory false triggering, and instances with 20 or more malfunctions were considered oscillatory false triggering. Malfunctions occurring 10 to 20 times were classified as non-oscillatory malfunctions. Since oscillation continues periodically without damping, the number

Table1. Components used in the experiment

Symbols / Elements / Model numbers	
S_1, S_2	GaN-FET EPC2212 (EPC Corp.)
C_{in}	Ceramic capacitor, 22 μ F $\times$ 3 pcs., CKG57NX7S1H226M500J (TDK Corp.)
L_r	Inductor, 7.0 μ H, B65686A0000R027 (TDK)
U	Gate driver, 2EDF7275FXUMA2 (Infineon Technologies)

Table2. Calculation Values of parasitic capacitance

Input voltage [V]	Conventional 1		Conventional 2		Proposal	
	Cds [pF]	Cgd [pF]	Cds [pF]	Cgd [pF]	Cds [pF]	Cgd [pF]
20	321	6.37	476	25.3	356	10.5
22	293	5.28	460	23.5	346	9.69
25	276	4.37	439	21.3	329	8.68
27	271	4.02	427	20	321	8.13
30	265	3.69	411	18.4	308	7.43

of malfunctions was used to determine oscillatory false triggering.

The three shaded areas in the figure represent the range of L_s values that suppress oscillatory false triggering, calculated using the equivalent capacitance of the three types of nonlinear capacitances. The values in Table 2 represent the equivalent capacitance of C_{ds} and C_{gd} used in the calculations. In the table, "conventional 1" refers to the single value from the C-V characteristic, "conventional 2" refers to the equivalent capacitance based on the total charge, and "proposal" refers to the equivalent capacitance derived from the proposed method. Additionally, the C_{gs} value was the typical value of 335 pF from the C-V characteristic.

From Fig. 8, it shows for all input voltages, oscillatory false triggering was suppressed within the suppression range obtained using the proposed method. On the other hand, within some ranges obtained using the two conventional methods, oscillatory false triggering was not suppressed. Fig. 9 shows the measured waveforms obtained in the region meeting the oscillatory false triggering suppression conditions calculated by each method for an input voltage of 30V. In the waveform within the range calculated using the proposed equivalent capacitance (Fig. 9(c)), the number of malfunctions is minimized, and oscillatory false triggering are also suppressed. However, oscillatory false triggering occurred within the ranges calculated using the conventional methods (Fig. 9(a) and Fig. 9(b)). From these results, the calculations using the proposed equivalent capacitance are superior to the conventional ones in suppressing oscillatory false triggering.

D. Consideration

The reason why the suppression conditions derived from the proposed method were superior to the conventional methods is discussed, as shown in the suppression distribution of oscillatory false triggering in Fig. 8. The measured and calculated oscillation frequencies of oscillatory false triggering are compared. A method for calculating the oscillation frequency was derived from the frequency conditions of the oscillation conditions analyzed in a previous study [10].

Table 3 compares the measured oscillation frequencies and the calculated oscillation frequencies for an input voltage of 20V and L_s of 436 pH. The numbers in parentheses in the table represent the relative errors between the measured and calculated frequency values. From the same table, it is inferred that the proposed method's equivalent capacitances are most suitable for oscillation, as they exhibit the smallest relative error in calculation.

Table3. Comparison of measured and calculated oscillation frequencies

	Conventional 1	Conventional 2	Proposal	Mesurement
Oscillation frequency [MHz]	45.7 (10.4%)	37.7 (-8.94%)	44.1 (6.52%)	41.4

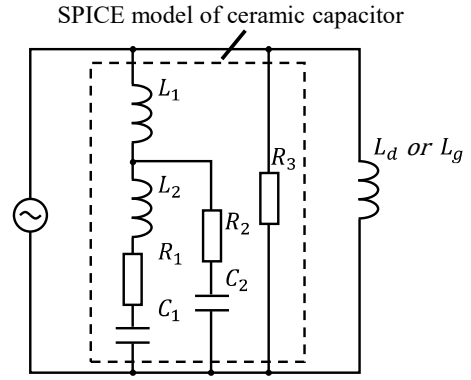


Fig. 10. Simulation model

V. CONCLUSION

The practical application of GaN-FETs is hindered by oscillatory malfunctions known as oscillatory false triggering. A method to suppress these involves adjusting the wiring inductance relative to its parasitic capacitance to prevent the occurrence of oscillatory false triggering. However, due to a nonlinear characteristic of the parasitic capacitance, there is a risk of discrepancies between the calculated and measured values of the wiring inductance needed to suppress oscillatory false triggering. Therefore, we propose a method to derive an equivalent capacitance of the nonlinear capacitance. As a result, using the proposed method improves the suppression accuracy of oscillatory false triggering compared to conventional equivalent capacitance methods.

APPENDIX

A. Measuring Method of Parasitic Inductance L_g and L_d

Parasitic inductances L_d and L_g exist in the power loop and gate loop, respectively. To measure their values, external ceramic capacitors which is C0603C222F5GAC7867 are attached in parallel to each loop on unmounted PCB. Resonant frequencies of the LC parallel circuits in each loop are then measured experimentally using an impedance analyzer.

These resonant frequencies encompass resonances that include parasitic components such as ESL and dielectric losses within the ceramic capacitors. Therefore, taking these effects into consideration, fitting of the parasitic inductances using simulations is conducted. Fig. 10 is a simulation circuit that includes parasitic components inside the ceramic capacitors. In this figure, values of resistance components R_1 to R_3 , inductor components L_1 to L_2 , and capacitor components C_1 to C_2 in the figure utilize SPICE models provided by KEMET Corporation.

The inductance values of L_d and L_g were calculated to match the resonant frequency of this circuit with the experimentally measured resonant frequency.

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