九州大学学術情報リポジトリ
Kyushu University Institutional Repository

Optimization of Common Source Inductance and Gate-Drain Capacitance for Reducing Gate Voltage Fluctuation after Turn-off Transition

Hatakenaka, Yusuke
Graduate School of Natural Science and Technology, Okayama University

Umetani, Kazuhiro
Graduate school of engineering, Tohoku University

Ishihara, Masataka
Graduate School of Natural Science and Technology, Okayama University

Hiraki, Eiji
Graduate School of Natural Science and Technology, Okayama University

https://hdl.handle.net/2324/7442731

出版情報：pp.3155-3162, 2020-10-30. IEEE
バージョン：
権利関係：© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

KYUSHU UNIVERSITY

Optimization of common source inductance and gate-drain capacitance for reducing gate voltage fluctuation after turn-off transition

Yusuke Hatakenaka *, Kazuhiro Umetani**, Masataka Ishihara*, and Eiji Hiraki*

*Graduate school of natural science and technology
Okayama University
Okayama, Japan

**Graduate school of engineering
Tohoku University
Sendai, Japan

Published in: 2020 IEEE Energy Conversion Congress and Exposition (ECCE)

© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

DOI: 10.1109/ECCE44975.2020.9236428

Optimization of Common Source Inductance and Gate-Drain Capacitance for Reducing Gate Voltage Fluctuation after Turn-off Transition

Yusuke Hatakenaka
Graduate school of natural science and technology
Okayama University
Okayama, Japan
pc7x61kj@s.okayama-u.ac.jp

Kazuhiro Umetani
Graduate school of engineering
Tohoku University
Sendai, Japan
kazuhiro.umetani.e1@tohoku.ac.jp

Masataka Ishihara
Graduate school of natural science and technology
Okayama University
Okayama, Japan
p4wv0vf6@s.okayama-u.ac.jp

Eiji Hiraki
Graduate school of natural science and technology
Okayama University
Okayama, Japan
hiraki@okayama-u.ac.jp

***Abstract*— Next-generation switching devices as GaN-FETs are recently emerging as promising switching devices capable of extremely high-speed switching. High-speed switching enables the high-frequency operation of the power converters, which can reduce the size of the passive components. However, high-speed switching can induce the resonance between the parasitic capacitance of the switching device and the parasitic inductance of the circuit board wiring, which appears as the gate voltage fluctuation at the switching. Particularly, GaN-FETs tend to have comparatively low gate threshold voltage and therefore are susceptible to the false turn-on, which is caused by the gate voltage fluctuation in the switching device just after the turn-off transition. For preventing this phenomenon, this paper analytically investigates the design requirement of these parasitic parameters to reduce the gate voltage fluctuation after the turn-off transition. As a result, the optimal ratio of the gate-drain capacitance and the common source inductance is elucidated to be the key to minimize the gate voltage fluctuation. The simulation and the experiment supported that the optimal design of this ratio can reduce the gate voltage fluctuation, supporting the usefulness of this novel insight for preventing the false turn-on.**

Keywords*— *common source inductance, GaN-FET, false triggering, parasitic capacitance, self-turn-on, switching noise

I. Introduction

The recent development of semiconductor technology has given rise to the next generation switching devices as GaN-FETs. In addition to their low on-resistance, these new devices are reported to exhibit higher switching speed than the conventional Si-based counterparts [1][2]. High-speed switching is not only effective for improving the power conversion efficiency by reducing the switching loss but also for enabling the high-frequency operation of the power converters, which can reduce the size of the passive components such as inductors, transformers, and capacitors. [3]-[7]

Despite these attractive benefits, however, the high-speed switching can cause the undesired triggering of the switching device called the false triggering, which is a disastrous event for the switching power converters. The high-speed switching entails the rapid change of the current in the circuit and therefore can generate the large voltage induction at the parasitic inductance of the printed circuit board (PCB) wires. This voltage induction excites the parasitic LC resonance comprised of the parasitic capacitance of the switching device and the parasitic inductance of the PCB wires [8][9]. This resonance is called as the switching noise and is the major cause of the gate voltage fluctuation of the switching device. Large gate voltage fluctuation can result in the false triggering and therefore should be reduced for practical application of the next generation switching devices.

Among various types of false triggering, GaN-FETs tend to be particularly susceptible to the false turn-on [10]-[15] because many GaN-FETs have a comparatively low gate threshold voltage. Thus, the false turn-on is known to be one of the typical but practically important problems for the power converters using GaN-FETs. The false turn-on of a switching device can be triggered by the switching noise just after the turn-off transition of this device or triggered during the off-state of this switching device by the switching noise generated by another switching device. However, in both of the cases, the switching device erroneously turns on due to the gate voltage fluctuation in its off-state. This paper focuses on this type of false triggering and investigates the design instruction for preventing the false turn-on by analyzing the gate voltage fluctuation just after the turn-off transition of a switching device

Because the parasitic capacitance of the switching device and the parasitic inductance of the PCB wires take an essential role of the gate voltage fluctuation, effective reduction of the gate voltage fluctuation may lie in the optimal design of these parasitic parameters. As for the special type of false triggering called the oscillatory false triggering [15]-[18], which is the self-sustaining repetitive false triggering caused by the parasitic oscillator circuit formed of the switching device and the parasitic inductance, recently-published studies [17][18] have elucidated that the optimal design of the parasitic inductance and the parasitic capacitance can effectively prevent this phenomenon. Hence, it seems natural to suppose that there also may be a design instruction of these parasitic parameters preveinting the aforementioned false turn-on.

The following discussion consists of four sections. Section II analyzes the gate voltage fluctuation based on the high-frequency equivalent circuit model of the switching noise and

XXX-X-XXXX-XXXX-X/XX/$XX.00 ©20XX IEEE

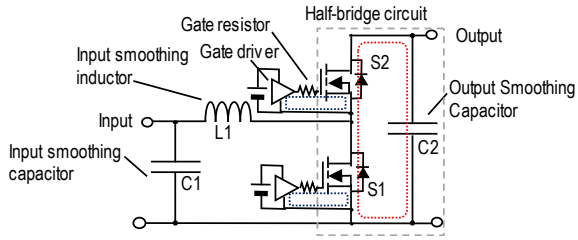


Fig. 1. Bidirectional boost chopper circuit under consideration

derives the design instruction for minimizing the gate voltage fluctuation. The high-frequency equivalent circuit model was constructed based on the switching device including the parasitic capacitance of the device and the parasitic inductance of the PCB wiring, similarly as in the preceding studies [17][18]. However, for straightforwardly calculating the gate voltage fluctuation, this paper transforms this circuit model into a novel equivalent circuit. Sections III and IV present the simulation and the experiment, respectively, which were performed to verify the proposed design instruction. Finally, section V gives the conclusions.

II. Design Requirement for Reducing Gate Voltage Fluctuation After Turn-off Operation

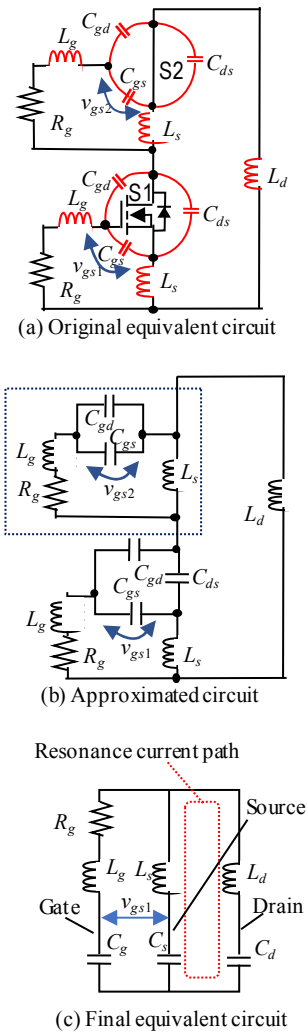
A. Model Construction

For analyzing the gate voltage fluctuation, this subsection constructs the high-frequency equivalent circuit model of the switching noise in a switching power converter. Certainly, there have been reported a large variation of the switching power converter topologies in literature. However, the majority of the switching power converter topologies are made by combining one or more half-bridge circuits. Because the high-frequency current of each half-bridge circuit is generally decoupled by the smoothing capacitor (or the snubber capacitor) installed in the half-bridge circuit, the switching noise can be discussed by analyzing a single half-bridge circuit without the loss of generality. Therefore, this section hereafter analyzes the switching noise based on the bidirectional boost chopper circuit shown in Fig. 1, which contains only a single half-bridge circuit.

The bidirectional boost chopper can operate both in the boost mode, in which the power flows from the input to the output, and the buck mode, in which the power flows from the output to the input. The inductor current path changes according to the turn-on and turn-off operations of S1 in the boost mode and to those of S2 in the buck mode. This change in the inductor current path causes the parasitic resonance, which appears as the switching noise. The switching noise can overlap the gate voltage of the switching devices in both the on-sate and the off-state. However, this paper discusses the gate voltage fluctuation of the switching device in the off-state considering that this device is susceptible to the false turn-on due to the low gate threshold voltage of GaN-FETs.

The discussion of this section hereafter considers the gate voltage fluctuation of S1 just after the turn-off transition of S1 when the bidirectional boost chopper operates in the boost mode, as a typical case of the false turn-on. Nonetheless, the same discussion stands in the other cases of the false turn-on, in which the switching noise overlaps the gate voltage of the switching device during the off-state of this device.

In the boost mode operation, switch S2 is in the on-state after the turn-off transition of S1. For simplifying the analysis,



(a) Original equivalent circuit

(b) Approximated circuit

(c) Final equivalent circuit

Fig. 2. High-frequency equivalent circuits of switching noise for analysis

switch S2 is therefore regarded as the short circuit for constructing the high-frequency equivalent circuit model of the switching noise. Furthermore, the gate drivers of S1 and S2 are also regarded as the short circuit because the output of the gate driver can be regarded as the voltage source with small output resistance. (This output resistance is included in the gate resistor.)

Besides, the switching noise generally has a far higher frequency than the switching frequency. Therefore, the output smoothing capacitor and the input smoothing inductor are simply regarded as the short and open circuits, respectively, because of their extremely small and large impedance at the frequency of the switching noise. Meanwhile, as discussed in the preceding studies [17][18], the parasitic capacitance of the switch in the off-state, as well as the parasitic inductance of the PCB wires should not be ignored.

Consequently, we can construct the high-frequency equivalent circuit of Fig. 1 as shown in Fig. 2(a), where C_{gd}, C_{gs}, and C_{ds} are the gate-drain capacitance, the gate-source capacitance, and the drain-source capacitance of switches S1 and S2; and L_d, L_g, and L_s are parasitic inductance of the PCB wires. L_d and L_g represent the loop wiring paths marked by the red and blue dotted lines in Fig. 1, respectively. L_s is the parasitic inductance of the source terminal of the switching

device and is called the common source inductance [9], [19], [20]. R_g is the resistance of the gate resistor.

Similarly as in the preceding studies [17][18], switch S1 of Fig. 2(a) is regarded as the current source controlled by the gate-source voltage. Nonetheless, this section analyzes the amplitude of the gate voltage fluctuation v_{gs1} under the assumption that v_{gs1} is below the level of the false triggering. Hence, switch S1 is simply regarded as the open circuit because this switch is assumed to remain in the off-state after the turn-off transition. As a result, the equivalent circuit is obtained as shown in Fig. 2(b).

Furthermore, for simplifying the discussion, the gate voltage fluctuation v_{gs2} of S2, i.e. the switch in the ON state, is not discussed because the gate resistance R_g is practically designed to be much larger than the impedance of L_g, as well as that of C_{gs}+C_{gd}, and therefore v_{gs2}, i.e. the voltage across C_{gs}, is much smaller than the voltage fluctuation at L_s. Because L_s is commonly small enough not to generate large voltage fluctuation, v_{gs2} tends to be less important than v_{gs1}. Consequently, the region surrounded by the blue dotted line is approximated simply as a short circuit, noticing this region has a far smaller impedance than L_d.

For further simplifying the calculation, the Δ-Y transformation is applied to the Δ-connection of the three parasitic capacitance of S1, i.e. C_{gd}, C_{gs}, and C_{ds} in Fig. 2(b). Consequently, the transformed equivalent circuit is obtained as shown in Fig. 2(c), where C_g, C_d, and C_s are the transformed parasitic capacitance defined as

$$C_g = C_\Delta^2 / C_{ds}, \quad C_s = C_\Delta^2 / C_{gd}, \quad C_d = C_\Delta^2 / C_{gs} \tag{1}$$

where $C_\Delta^2 = C_{gs}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{ds}$.

B. Analysis of Gate Voltage Fluctuation

The equivalent circuit Fig. 2(c) is made of the parallel-connection of three series LC resonators. Because this circuit has multiple inductors and capacitors, this circuit has more than one resonating modes. However, because R_g is assumed to have larger impedance than L_g and C_{gs}, R_g can be naturally assumed to have far larger impedance than L_s and C_s, which generally have far smaller impedance than L_g and C_{gs} in practical switching power converters. Then, Fig. 2(c) can be approximated to have only a single resonant mode with the AC current flowing along the red dotted line shown in Fig. 2(c). Therefore, the resonant frequency f_{res} of this resonant mode can be calculated as follows, under the approximation that L_d is far greater than L_s and C_{gd} is far smaller than C_{gs} and C_{ds}. (Hence, $C^2_\Delta \approx C_{gs}C_{ds}$, $L_d+L_s \approx L_d$, and $C_{gs}+C_{gd} \approx C_{gs}$.)

$$\begin{aligned} f_{res} &= \frac{1}{2\pi\sqrt{(L_d+L_s)C_dC_s/(C_d+C_s)}} \\ &= \frac{1}{2\pi\sqrt{(L_d+L_s)C_\Delta^2/(C_{gs}+C_{gd})}} \\ &\approx \frac{1}{2\pi\sqrt{L_dC_{ds}}}. \end{aligned} \tag{2}$$

The amplitude of the resonant current can be calculated by estimating the initial resonance energy. If I_L and V_{out} denote the current across the input smoothing inductor and the output voltage at the turn-off of S1, the current flowing through L_d and L_s is changed by I_L and the voltage between the drain and the source of S1 is changed by V_{out} as a result of the switching. Hence, the initial resonant energy E_{res} can be estimated as

$$\begin{aligned} E_{res} &= \frac{1}{2}(L_d+L_s)I_L^2 + \frac{1}{2}(C_d // C_s)V_{out}^2 \\ &\approx \frac{1}{2}L_dI_L^2 + \frac{1}{2}C_{ds}V_{out}^2. \end{aligned} \tag{3}$$

Hence, the amplitude I_{res} of the resonant current i_{res} is

$$\begin{aligned} &\frac{1}{2}(L_d+L_s)I_{res}^2 = E_{res} \\ &\therefore I_{res} \approx \sqrt{I_L^2 + \frac{C_{ds}V_{out}^2}{L_d}}. \end{aligned} \tag{4}$$

Next, the gate voltage fluctuation of S1, generated as a result of the resonance, is calculated. The gate voltage fluctuation is the voltage appearing between the gate and the source terminals of S1 as a result of the resonant current i_{res}. Therefore, the gate voltage fluctuation v_{gs1} is

$$\begin{aligned} v_{gs1} &\approx \frac{\left(j\omega L_s + \frac{1}{j\omega C_s}\right)\frac{i_{res}}{j\omega C_g}}{R_g + j\omega L_g + \frac{1}{j\omega C_g}} - \frac{i_{res}}{j\omega C_s} \\ &= \frac{j\omega L_s\left(1-\frac{L_gC_g}{L_sC_s}\right) - \frac{C_gR_g}{C_s}}{\left(1-\omega^2L_gC_g\right) + j\omega C_gR_g} i_{res}, \end{aligned} \tag{5}$$

where ω is the angular frequency of the resonant current defined as $\omega=2\pi f_{res}$. Consequently, the amplitude V_{gs1} of the gate voltage fluctuation can be calculated as

$$V_{gs1} \approx \sqrt{\frac{\omega^2L_s^2\left(1-\frac{L_gC_g}{L_sC_s}\right)^2 + \frac{C_g^2R_g^2}{C_s^2}}{\left(1-\omega^2L_gC_g\right)^2 + \omega^2C_g^2R_g^2}} I_{res}, \tag{6}$$

Parasitic capacitance C_{gs} and C_{ds} have the same order in many commercial switching devices. Furthermore, as a result of the effort minimizing the wiring path length of the power circuit and the gating circuit to reduce L_d and L_g, the wiring path length representing L_d and L_g are commonly confronting the restriction of the package size of the switching device, and therefore L_d and L_g also tend to have the same order in recent PCB design of the switching power converter. Consequently, L_dC_{ds} tend to be close to L_gC_{gs}, which makes $\omega L_g - 1/\omega C_{gs}$ to have far smaller impedance than L_g and C_{gs}. In this case, the following assumption can be introduced: $R_g >> \omega L_g - 1/\omega C_{gs}$. Hence, $\omega C_gR_g >> \omega^2C_gL_g - 1$. Under this assumption, (6) can be further approximated as

$$V_{gs1} \approx \sqrt{\frac{\omega^2L_s^2\left(1-\frac{L_gC_g}{L_sC_s}\right)^2 + \frac{C_g^2R_g^2}{C_s^2}}{\omega^2C_g^2R_g^2}} I_{res}, \tag{7}$$

Noticing the following relations shown in (8), V_{gs} can be rewritten as (9).

$$\frac{L_g C_g}{L_s C_s} = \frac{L_g C_{gd}}{L_s C_{ds}}, \quad \frac{C_g}{C_s} R_g = \frac{C_{gd}}{C_{ds}} R_g, \qquad \omega^2 C_g^2 R_g^2 \approx \frac{C_g^2 R_g^2}{L_d C_{ds}} \approx \frac{C_{gs}^2 R_g^2}{L_d C_{ds}}. \tag{8}$$

$$V_{gs1} \approx I_{res} \sqrt{\frac{\frac{L_s^2}{L_d C_{ds}}\left(1 - \frac{L_g C_{gd}}{L_s C_{ds}}\right)^2 + \frac{C_{gd}^2 R_g^2}{C_{ds}^2}}{\frac{C_{gs}^2 R_g^2}{L_d C_{ds}}}} = \frac{C_{gd}}{C_{gs}} I_{res} \sqrt{\frac{1}{R_g^2}\left(\frac{L_s}{C_{gd}} - \frac{L_g}{C_{ds}}\right)^2 + \frac{L_d}{C_{ds}}}, \tag{9}$$

From the result obtained in (9), two design instructions of the parasitic inductance can be extracted for reducing the gate voltage fluctuation. One is to minimize L_d, which is a well-known instruction for reducing the switching noise and therefore already considered in many practical design of the switching power converters. The other is to design L_s/C_{gd} to be equals to L_g/C_{ds}. This is a novel design instruction that can achieve further reduction of the gate voltage fluctuation. This novel instruction indicates that optimizing the ratio of the common source inductance L_s and the gate-drain capacitance C_{gd} is important for reducing the gate voltage fluctuation.

It should be noted that the continuous effort of the semiconductor industry to reduce C_{gd} is also effective to reduce the gate voltage fluctuation, according to (9). Therefore, the proposed instruction should be taken as an additional instruction that L_s should be reduced in accordance with C_{gd}. Certainly, the importance of the appropriate ratio L_s/C_{gd} has also been pointed out in [18] for the prevention of the oscillatory false triggering. However, the equation of the proposed instruction is slightly different from that of [18]. In the practical design of the switching converter. L_s can be more easily changed only by a small change in the PCB layout than C_{gd}. Therefore, the proposed instruction may be interpreted as the importance of the appropriate design of L_s.

Equation (9) can be rewritten in the following form:

$$V_{gs1} \approx \frac{I_{res}}{C_{gs}} \sqrt{\frac{L_g^2}{R_g^2}\left(\frac{L_s}{L_g} - \frac{C_{gd}}{C_{ds}}\right)^2 + \frac{L_d}{C_{ds}} C_{gd}^2} = I_{res} \sqrt{R_g^2 Q_g^4 \left(\frac{L_s}{L_g} - \frac{C_{gd}}{C_{ds}}\right)^2 + \frac{L_d}{C_{ds}} \frac{C_{gd}^2}{C_{gs}^2}}, \tag{10}$$

where Q_g is the quality factor of the parasitic resonance defined as

$$Q_g = \frac{1}{R_g} \sqrt{\frac{L_g}{C_{gs}}}. \tag{11}$$

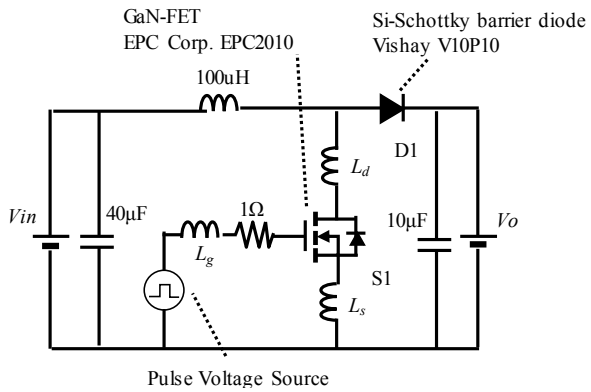


Fig. 3. Simulation model of bidirectional boost chopper circuit.

TABLE I. SIMULATION CONDITIONS OF PARASITIC PARAMETERS IN EVALUATION WITH CHANGING C_{GD}

L_g [nH]	L_g [nH]	L_s [nH]	C_{ds} [pF]	C_{gd} [pF]	M [10^{-3}]
				9	91
				20	55
				30	23
5.0	9.0	0.6	310	40	-9
				50	-41
				60	-74
				70	-106

TABLE II. SIMULATION CONDITIONS OF PARASITIC PARAMETERS IN EVALUATION WITH CHANGING L_S

L_g [nH]	L_d [nH]	L_s [nH]	C_{ds} [pF]	C_{gd} [pF]	M [10^{-3}]
	8.9	0.1			-109
	8.8	0.2			-89
	8.6	0.4			-49
5.0	8.4	0.6	310	40	-9
	8.2	0.8			31
	8.0	1.0			71
	7.8	1.2			111

Therefore, the aforementioned design instruction can be evaluated by introducing a dimensionless number M defined as

$$M = \frac{L_s}{L_g} - \frac{C_{gd}}{C_{ds}}. \tag{12}$$

According to (10), the gate voltage fluctuation is expected to take the minimum amplitude when M equals to zero.

III. SIMULATION

The circuit simulation was carried out to test the proposed design instruction for reducing the gate voltage fluctuation, derived in the previous section. In this simulation, the amplitude of the gate voltage fluctuation was evaluated at various values of L_s and C_{gd}. The circuit simulator was OrCAD Pspice ver. 17.2.

Figure 3 illustrates the simulated circuit model. In this model, L_g, L_d, and L_s were the parasitic inductance of the wiring of the PCB board, whereas the parasitic capacitance of switching device S1 and diode D1 was incorporated in the Spice model of these devices. The semiconductor devices S1 and D1 are assumed to be a GaN-FET (EPC Corp. EPC2010)

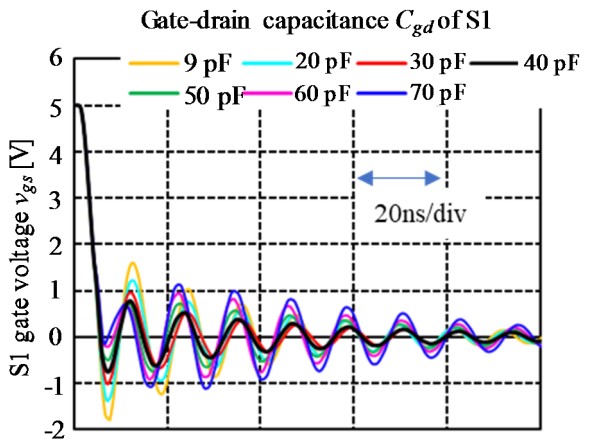


Fig. 4. Simulation results of gate-source voltage waveforms of various gate-drain capacitance C_{gd} under the conditions listed in Table I. Input and output voltage was set at V_{in}=25 V and V_o=50 V.

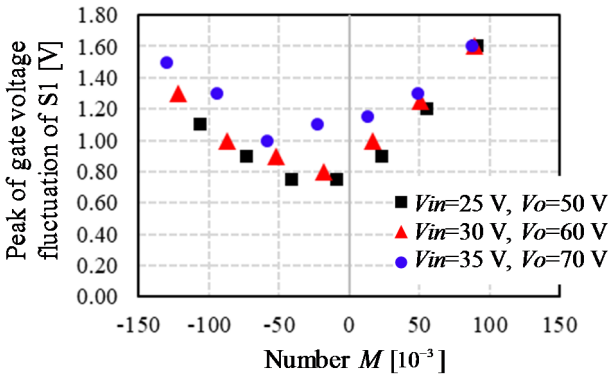


Fig. 5. Dependence of peak value of gate voltage fluctuation on number M at variuous input and output voltages. Variation in M was obtained by changing gate-drain capacitance C_{gd} according to Table I.

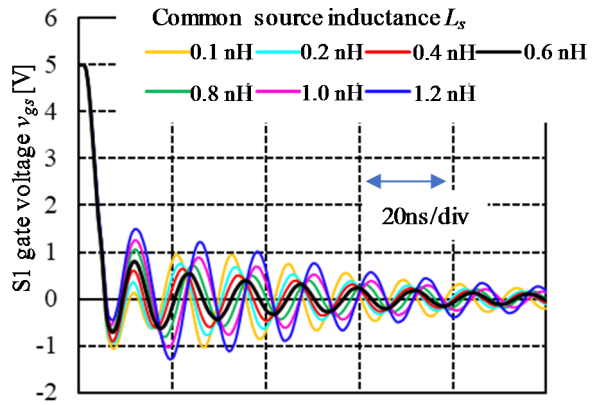


Fig. 6. Simulation results of gate-source voltage waveforms of various common source inductance L_s under the conditions listed in Table II. Input and output voltage was set at V_{in}=25 V and V_o=50 V.

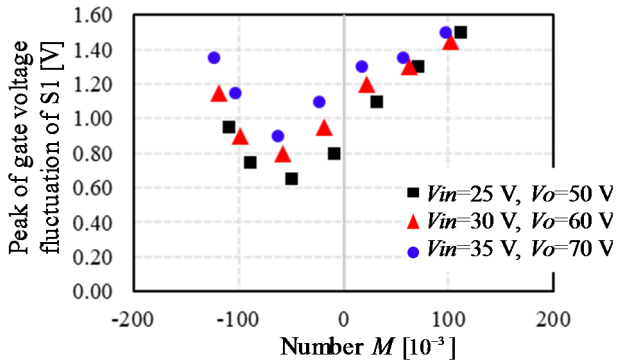


Fig. 7. Dependence of peak value of gate voltage fluctuation on number M at variuous input and output voltages. Variation in M was obtained by changing common source inductance L_s according to Table II.

and a Si-Schottky barrier diode (Vishay V10P10). Their Spice models were provided by their manufacturers.

The simulated circuit model is a unidirectional boost chopper unlike the theoretical discussion in the previous section. However, the same discussion can be applied because diode D1 is in the forward-biased state just after the turn-off of S1, which is equivalent to the on-state of S2 in Fig. 1. The reason for the difference between the simulation model and the theoretical model originates from the scope of this simulation. In this simulation, the gate voltage fluctuation of S1 at the turn-off of S1 was tested. Therefore, the false triggering of S2 is not desirable because this might slightly affect the gate voltage fluctuation of S1.

In this simulation, the gate voltage fluctuation of S1 was evaluated just after the turn-off of S1. For this purpose, the boost chopper was operated for only one cycle to test the turn-off of S1. Firstly, the switching device S1 was kept in the on-state until the inductor current reaches at 7.5A. Then, S1 was turned off to observe the gate voltage fluctuation of S1. GaN-FET S1 was driven by the pulsed voltage source via gate resistor R_g of 1Ω. This voltage source outputs the rectangular voltage pulse, whose top and bottom voltage was 5V and 0V, respectively.

The evaluation of the gate voltage fluctuation was repeated by changing the gate-drain capacitance C_{gd} and the common source inductance L_s, respectively. Table I shows the simulation conditions of the evaluation with changing C_{gd}, whereas Table II shows those with changing L_s. The values of C_{gd} was adjusted by adding a capacitor directly between the gate and drain terminals of S1. The values of the parasitic capacitance in Tables I and II are the incremental capacitance given in the datasheet [21] at the drain-source voltage of V_o, which corresponds to the average drain-source voltage of S1 after its turn-off. Furthermore, the whole evaluation process was repeated at three pairs of the input and output voltage, i.e. V_{in} and V_o: 1. V_{in}=25 V and V_o=50 V, 2. V_{in}=30 V and V_o=60 V, 3. V_{in}=35 V and V_o=70 V.

Figure 4 shows the simulation results of the gate-source voltage waveforms at various values of C_{gd} tested under the conditions listed in Table I at the input and output voltage condition of V_{in}=25 V and V_o=50 V. The result suggested the existence of the optimum value of C_{gd}, as expected by the theory: C_{gd} of 40 pF exhibited the smallest amplitude of the gate voltage fluctuation, although both larger and smaller values of C_{gd} than 40 pF resulted in the larger amplitude of the fluctuation.

This feature was also seen in the other pairs of the input and output voltage. Figure 5 shows the dependence of the peak value of the gate voltage fluctuation on the dimensionless number M varied by changing C_{gd}. Because M is the linear function of C_{gd}, the results indicate that the existence of the optimum value of C_{gd} regardless of the input and output voltage. Furthermore, the peak voltage took the minimum value at a value of M close to zero, supporting the proposed design instruction.

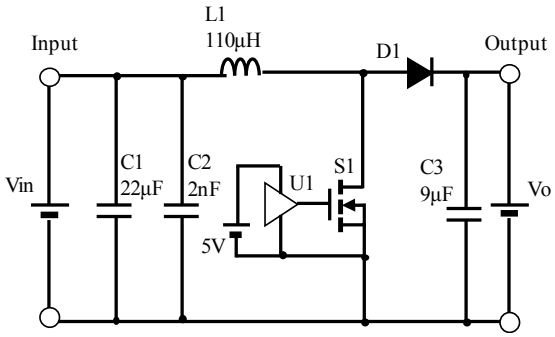


Fig. 8. Schematics of experimental boost chopper.

TABLE III. CIRCUIT ELEMENTS OF EXPERIMENTAL BOOST CHOPPER

S1	GaN-FET EPC2010 (EPC Corp.)
D1	SBD V10P10-M3/86A (Vishay Semiconductors)
C1	Ceramic Capacitor 22uF×2pcsCKG57NX7S2A226M500JH (TDK Corp.)
C2	Film Capacitor 1nF×2pcs ECWU1105KCV (Panasonic)
C3	Ceramic Capacitor 2.2uF×4pcs CKG57KX7T2E225M335JH (TDK Corp.)
L1	Inductor 27uF×4pcs 7G14A-270M (Sagami)
U1	Gate Driver LM5113SDE/NOPB (Texas instruments)

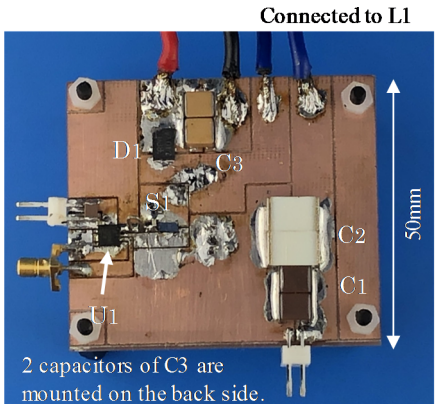
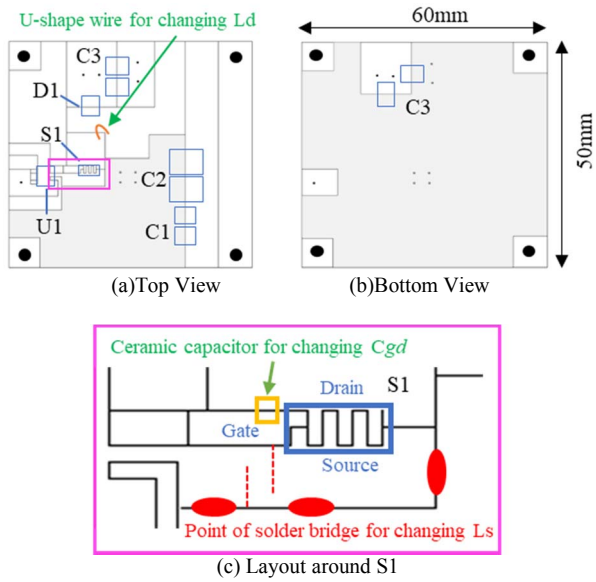


Fig. 9. Photograph of experimental boost chopper.

Next, Fig. 6 shows the simulation results of the gate-source voltage waveforms at various values of L_s tested under the conditions listed in Table II at the input and output voltage condition of V_{in}=25 V and V_o=50 V. The results revealed that L_s of 0.6nH exhibited the smallest amplitude of the gate voltage fluctuation, thus suggesting the existence of the optimum value of L_s as expected by the theory. This feature was also seen in the other pairs of the input and output voltage. Figure 7 shows the dependence of the peak value of the gate voltage fluctuation on M varied by changing L_s. The results indicate that the existence of the optimum value of L_s regardless of the input and output voltage. Furthermore, the peak voltage again took the minimum value at a value of M close to zero, also supporting the proposed design instruction. Certainly, according to the simulation results in Fig. 5 and Fig. 7, the optimum M slightly deviated from zero. The reason is not cleared in this paper. However, the optimum value of M might be slightly affected by the non-linear voltage dependence of the parasitic capacitance of the switching device, which was not considered in the theory in the previous section.

Consequently, the simulation supported that the gate voltage fluctuation can be minimized by optimizing the balance of C_{gd} and L_s according to the proposed design instruction, i.e. L_s/C_{gd} should be equal to L_g/C_{ds}, or M should be designed to be zero.



(a)Top View (b)Bottom View

(c) Layout around S1

Fig. 10. Layout of printed circuit board of experimental boost chopper.

TABLE IV. LIST OF EXPERIMENTAL INSTRUMENTS

Instrument	Model (Manufacturer)	Frequency limit
Oscilloscope	MDO3034 (Tektronix)	350MHz
Passive Probe	TPP0500B (Tektronix)	500MHz

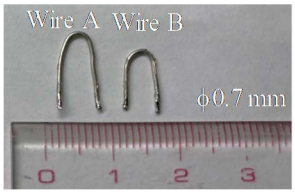


Fig. 11. Photograph of U-shaped wires for adjusting L_d.

IV. EXPERIMENT

An experiment was carried out to verify the effectiveness of the proposed design instruction. Similar to the simulation presented in the previous section, this experiment utilized the unidirectional boost chopper consisting of a GaN-FET and a Si-SBD. Figure 8 shows the circuit diagram of the experimental boost chopper; Table III shows the list of the circuit elements. The GaN-FET was driven by the gate driver LM5113 [22] without any gate resistor. According to the ratio between the DC supply voltage and the sink current of LM5113, equivalent resistance R_g, which equals to the output resistance of the gate driver, was approximately estimated as 1Ω, which was far greater than the impedance of $\omega L_g - 1/\omega C_{gs}$ at f_{res}.

Figure 9 and Fig. 10 show the photograph and the PCB layout of this experimental unidirectional boost chopper, respectively. This chopper was designed to be able to change the value of L_s and C_{gd}. The value of L_s was changed by elongating or shortening the common source path [23], which is the wiring path of the source terminal shared by the gating circuit and the power circuit. The length of the common source path was changed by the combination of two methods: 1. Selecting the point of the solder bridge to connect the ground

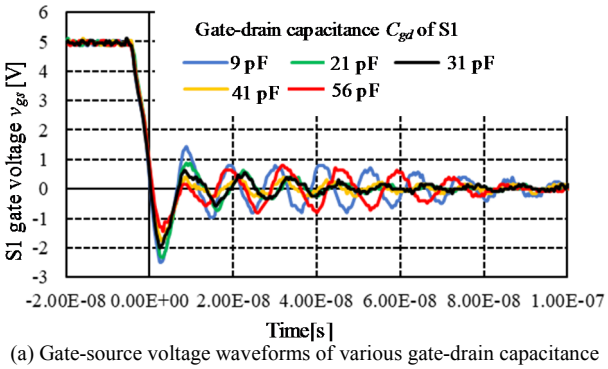
TABLE V. EXPERIMENTAL CONDITIONS IN EVALUATION OF DEPENDENCE ON C_{gd}

Vin [V]	Vo [V]	Ld [nH]	Lg [nH]	Ls [nH]	Cds [pF]	Cgd [pF]	Number M [10^{-3}]
25	50	8.8	5.9	0.58	310	9	68
						21	30
						31	-2
						41	-34
						56	-83

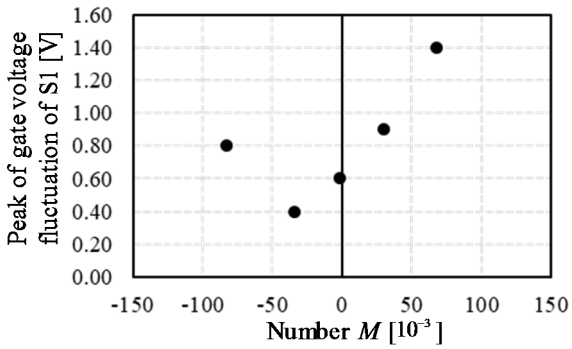
TABLE VI. EXPERIMENTAL CONDITIONS IN EVALUATION OF DEPENDENCE ON L_s

Vin [V]	Vo [V]	Cds [pF]	Cgd [pF]	Lg [nH]	Ld [nH]	Ls [nH]	Number M [10^{-3}]
25	50	310	31	6.1	14.8†	0.38	-38
				5.9	15.3†	0.58	-2
				5.5	15.0‡	1.00	82
				5.5	15.0‡	1.18	115

†U-shape wire A was attached. ‡U-shape wire B was attached.



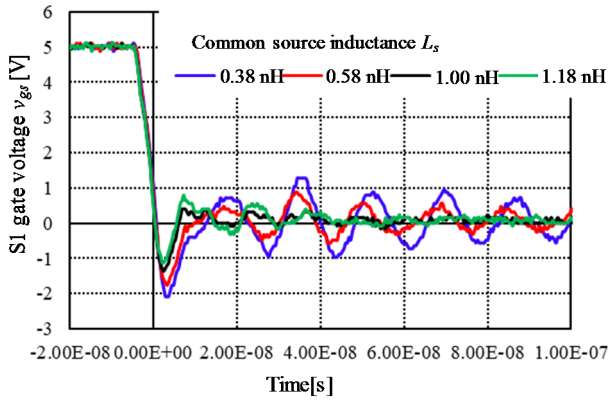
(a) Gate-source voltage waveforms of various gate-drain capacitance C_{gd}.



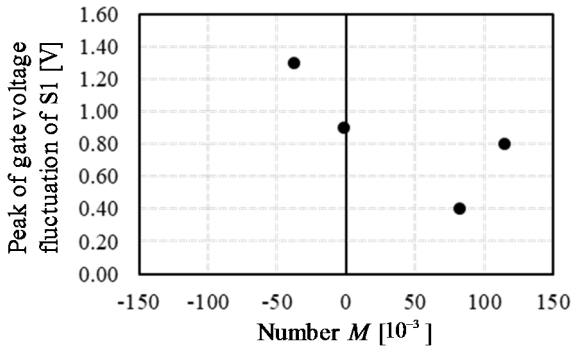
(b) Dependence of peak value of gate voltage fluctuation on number M.

Fig. 12. Evaluation results of dependence of gate voltage fluctuation of S1 on C_{gd} under the conditions listed in Table V.

of the gating circuit to the source terminal of S1, and 2. partly cutting the wiring path of the common source path. The red dots in Fig. 10(c) shows the three points for making the solder bridge, and the red dashed line shows the cut pattern for extending the common source path. As a result, four levels of L_s, ranging from 0.4nH to 1.2nH, was implemented in the PCB. The value of C_{gd} was changed by adding a small ceramic capacitor between the gate and drain terminals of S1. This ceramic capacitor was mounted just adjacent to S1. In this experiment, this additional capacitor can be almost directly attached between the gate and drain terminals because the GaN-FET under test was supplied as the flip-chip device.



(a) Gate-source voltage waveforms of various common source inductance L_s.



(b) Dependence of peak value of gate voltage fluctuation on number M.

Fig. 13. Evaluation results of dependence of gate voltage fluctuation of S1 on L_s under the conditions listed in Table VI.

This experiment evaluates the dependence of the gate voltage fluctuation on the gate-drain capacitance C_{gd} and the common source inductance L_s, respectively. For this purpose, the experimental boost chopper was operated for only one cycle to test the turn-off of S1 just the same as in the previous section. Firstly, the switching device S1 was kept in the on-state until the inductor current reaches at the predetermined level. This level was set at 6.0A in the evaluation of the dependence on C_{gd} and at 7.5A in the evaluation of the dependence on L_s. Then, S1 was turned off, and the gate voltage fluctuation of S1 was observed using the oscilloscope and the passive voltage probe listed in Table IV at the turn-off of S1. This test was repeated changing the value of C_{gd} or L_s to evaluate the dependence of the gate voltage fluctuation on the dimensionless number M.

It should be noted that the change in L_s slightly affected the values of L_d because the change in the common source path resulted in a slight change in the wiring path of the power circuit. However, different values of L_d result in the difference in the initial resonant energy E_{res}, which may affect the gate voltage fluctuation except for L_s and therefore should be avoided in the evaluation of the dependence of L_s. Therefore, for adjusting the value of L_d, the experimental chopper was designed to be able to elongate the drain wiring by inserting a U-shaped wire at the point marked in Fig. 10(a). The length of the drain wiring was changed by choosing either one of two U-shaped wires, shown in Fig. 11, on the wiring path from the drain of S1 to diode D1.

Consequently, the experimental conditions of the parasitic capacitors and the parasitic inductance were listed in Table V in the evaluation of the dependence on C_{gd} and Table VI in the

evaluation of the dependence on L_s. (In the evaluation of the dependence on L_s, 22pF capacitor was added between the gate and drain terminals of S1 for setting C_{gd}=31pF.) The measurement method of L_s was proposed in [20]; the measurement method of L_d and L_g was the same as in [17][18].

Figure 12 shows the evaluation results of the dependence of the gate voltage fluctuation on C_{gd}. Figure 12(a) shows the gate-source voltage waveforms at various values of C_{gd} tested under the conditions listed in Table V. Similarly as in the simulation, the result suggested the existence of the optimum value of C_{gd}, as expected by the theory. Figure 12(b) shows the dependence of the peak value of the gate voltage fluctuation on the dimensionless number M varied by changing C_{gd}. The peak voltage took the minimum value at a value of M close to zero, which is consistent with the theory.

Figure 13 shows the evaluation results of the dependence of the gate voltage fluctuation on L_s. Figure 13(a) shows the gate-source voltage waveforms at various values of L_s tested under the conditions listed in Table VI. Again similarly to the simulation, the result suggested the existence of the optimum value of L_s, as expected by the theory. Figure 13(b) shows the dependence of the peak value of the gate voltage fluctuation on the dimensionless number M varied by changing L_s. The peak voltage again took the minimum value at a value of M close to zero, which is also consistent with the theory.

Consequently, the experiment supported that the gate voltage fluctuation can be minimized by designing the balance of C_{gd} and L_s according to the proposed design instruction.

V. CONCLUSIONS

Next-generation switching devices, such as GaN-FET, are promising for reducing the switching loss and enabling the high-frequency operation owing to their high-speed switching capability. However, the high-speed switching tends to excite the parasitic LC resonance comprised of the parasitic inductance of the PCB wires and the parasitic capacitance of the switching device. This resonance generates the gate voltage fluctuation, which may cause false triggering. This paper investigated the design instruction of the parasitic inductance and the parasitic capacitance for reducing the gate voltage fluctuation of the switching device in the off-state to prevent the false turn-on. As a result, this paper elucidated a novel instruction that the optimal ratio of the gate-drain capacitance and the common source inductance can reduce the gate voltage fluctuation. The simulation and experiment, which evaluated the gate voltage fluctuation of a GaN-FET after the turn-off transition, supported minimization of the gate voltage fluctuation by optimizing the ratio between the gate-drain capacitance and the common source inductance according to the proposed design instruction.

REFERENCES

[1] M. A. Khan, G. Simin, S. G. Pytel, A. Monti, E. Santi, and J. L. Hudgin, "New developments in gallium nitride and the impact on power electronics," in Proc. IEEE Power Electron. Spec. Conf., Recife, Brazil, 2005, pp. 15–26.

[2] B. Wang, N. Tipirneni, M. Riva, A. Monti, G. Simin, and E. Santi, "An efficient high frequency drive circuit for GaN power HFETs," IEEE Trans. Ind. Appl., vol. 45, no. 2, pp. 843–853, Mar. 2009.

[3] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-frequency high-efficiency GaN-based interleaved CRM bidirectional buck/boost converter with inverse coupled inductor," IEEE Trans. Power Electron., vol. 31, no. 6, pp. 4343–4352, Jun. 2016.

[4] Z. Zhang and K. D. T. Ngo, "Multi-megahertz quasi-square-wave flyback converter using eGaN FETs," IET Power Electron., vol. 10, no. 10, pp. 1138–1146, Jun. 2017.

[5] A. Hariya et al., "Circuit design techniques for reducing the effects of magnetic flux on GaN-HEMTs in 5-MHz 100Whigh power-density LLC resonant DC-DC converters," IEEE Trans. Power Elecron., vol. 32, no. 8, pp. 5953–5963, Aug. 2017.

[6] N. Fichtenbaum, M. Giandalia, S. Sharma, and J. Zhang, "Half-bridge GaN power ICs: Performance and application," IEEE Power Electron. Mag., vol. 4, no. 3, pp. 33–40, Sep. 2017.

[7] T. Mishima and E. Morita, "High-frequency bridgeless rectifier based ZVS multiresonant converter for inductive power transfer featuring high voltage GaN-HFET," IEEE Trans. Ind. Electron., vol. 64, no. 11, pp. 9155–9164, Nov. 2017.

[8] J. Wang and H. S.-H. Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," IEEE Trans. Power Electron., vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[9] W. Zhang, Z. Zhang, F. Wang, D. Costinett, L. Tolbert, and B. Blalock, "Common source inductance introduced self-turn-on in MOSFET turn-off transient," in Proc. IEEE Appl. Power Electron. Conf. Expo., Tampa, FL, USA, 2017, pp. 837–842.

[10] A. Nishigaki, H. Umegami, F. Hattori, W. Martinez, and M. Yamamoto, "An analysis of false turn-on mechanism on power devices," in Proc. IEEE Energy Convers. Congr. Expo., Pittsburgh, PA, USA, 2014, pp. 2988–2993.

[11] H. Ishibashi, A. Nishigaki, H. Umegami, W.Martinez, and M. Yamamoto, "An analysis of false turn-on mechanism on high-frequency power devices," in Proc. IEEE Energy Convers. Congr. Expo., Montreal, QC, Canada, 2015, pp. 2247–2253.

[12] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration," IEEE Trans. Power Electron., vol. 32, no. 8, pp. 6416–6433, Aug. 2017.

[13] T. Iwaki, S. Ishiwaki, T. Sawada, and M. Yamamoto, "Mathematical analysis of GaN high electron mobility transistor false turn-on phenomenon," IET Electron. Lett., vol. 53, no. 19, pp. 1327–1329, Sep. 2017.

[14] T. Zhu, F. Zhuo, F. Zhao, F. Wang, and T. Zhao, "Quantitative model-based false turn-on evaluation and suppression for cascode GaN devices in half-bridge applications," IEEE Trans. Power Electron., vol. 34, no. 10, pp. 10166-10179, Oct. 2019.

[15] J. Chen, Q. Luo, J. Huang, Q. He, P. Sun and X. Du, "Analysis and design of an RC snubber circuit to suppress false triggering oscillation for GaN devices in half-bridge circuits," IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2690-2704, Mar. 2020.

[16] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half bridge circuits switched with wide band-gap transistors," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2380–2392, May 2014.

[17] K. Umetani, K. Yagyu, and E. Hiraki, "A design guideline of parasitic inductance for preventing oscillatory false triggering of fast switching GaN-FET," IEEJ Trans. Electr. Electron. Eng., vol. 11, no. S2, pp. S84–S90, Dec. 2016.

[18] K. Umetani, R. Matsumoto, and E. Hiraki, "Prevention of oscillatory false triggering of GaN-FETs by balancing gate-drain capacitance and common source inductance," IEEE Trans. Ind. Appl., vol. 55, no. 1, pp. 610–619, Jan./Feb. 2019.

[19] Z. Dong, X. Wu, K. Sheng, and J. Zhang, "Impact of common source inductance on switching loss of SiC MOSFET," in Proc. IEEE Int. Future Energy Electron. Conf., Taipei, Taiwan, 2015, pp. 1–5.

[20] K. Umetani, K. Aikawa, and E. Hiraki, "Straightforward measurement method of common source inductance for fast switching semiconductor devices mounted on-board," IEEE Trans. Ind. Electron., vol. 64, no. 10, pp. 8258–8267, Oct. 2017.

[21] EPC Corp., "EPC2010 datasheet," pp.3, 2013.

[22] Texas Instruments Corp., "LM5113 datasheet," pp.5, Apr. 2013.

[23] R. Matsumoto, K. Aikawa, A. Konishi, K. Umetami, and E. Hiraki, "Evaluation of impact of parasitic magnetic coupling in PCB layout on common source inductance of surface mounted package," in Proc. IEEE Intl. Conf. Power Electron. Drive Syst. (PEDS2017), Honolulu, HI, 2017, pp. 559-566.