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Origin of Common Source Inductance in Power Device Packages with Kelvin Source Terminal

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***Abstract*— The kelvin-source packages are becoming popular for high-power ultrafast switching devices to reduce the common source inductance (CSI), which induces the noise voltage in the gating circuit at the transitional change of the drain current and causes false triggering. Despite its importance, however, the actual measurement of CSI has not been reported for kelvin-source packages due to their small inductance values. This paper measured the CSI of typical kelvin-source package TO-247-4L. The result revealed that the CSI of this kelvin-source package ranged 0.2nH–0.7nH, which cannot be neglected at a switching speed greater than 1A/ns. Furthermore, this variation in CSI was found to arise from the magnetic coupling between the bonding wires of power source and gating source, implying that separating the bonding wires can further reduce the CSI.**

Keywords— common source inductance, SiC-MOSFET, power semiconductor, parasitic inductance

I. INTRODUCTION

In recent years, wide bandgap semiconductors switching devices such as SiC-MOSFETs[1] and GaN-FETs[2] based on have attracted much attention. These devices are characterized by low on-resistance and high-speed operation. Low on-resistance reduces conduction loss. fast switching also leads to lower switching losses and minimization of necessary passive components such as inductors and capacitors. For these reasons, the use of wide bandgap semiconductor switching devices can achieve minimization and high efficiency of power converters such as buck converter in Fig. 1

However, When switching devices are operated at large currents and high speeds, parasitic inductance existing such as PCB layout and bonding wire of the switching devices affects circuit operation. For Example, The self-turn-on that occurs during the turn of state of switching devices as shown in Fig. 2, Oscillatory false triggering which is a self-sustaining uncontrollable series of repetitive false triggering after a fast switching, increasing of switching losses and EMI issues. The

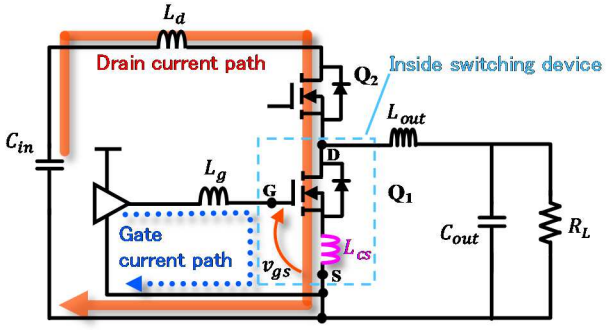


Fig. 1 Buck converter, a typical application of next-generation switching devices: common source inductance L_{cs}, power loop inductance L_d and gate driver loop inductance L_g

mechanisms of these phenomena are described in detail in references [2], [3], [4], [17]. Note that, although in all cases of phenomena caused by different mechanisms, the existence of common source inductance is pointed out as an important element that affects the occurrence of false triggering and switching losses. hereafter, the common source inductance is referred to as L_{cs}.

L_{cs} is defined as the inductance shared by the power loop and driving loop[11], as shown in Fig. 1. First when a MOSFET turns off at high di/dt, an induced voltage v_{cs} is generated at L_{cs}.

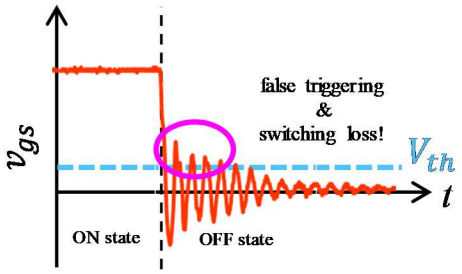


Fig. 2 False triggering of switching device at turn-off

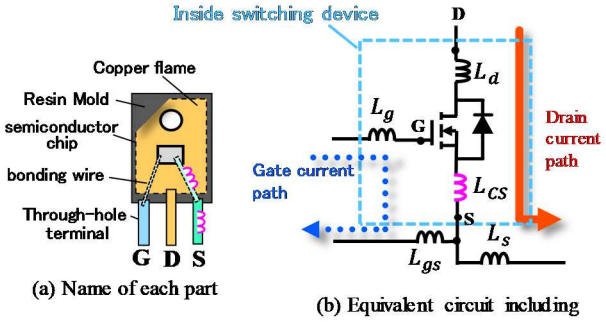


Fig. 3 Typical 3 pin packages such as TO-240

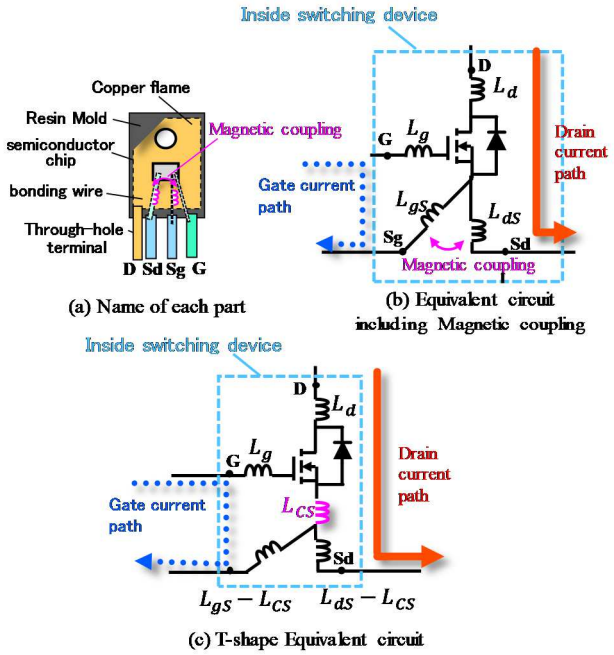


Fig. 4 4 pin packages with Kelvin source terminal such as To-240-4L

This induced voltage v_{cs} propagates to the gate drive circuit, and series resonance attributed to the gate inductance L_g and the gate-source parasitic capacitance C_{gs} generates switching noise in the gate-source voltage. When the voltage amplitude of this switching noise exceeds the MOSFET's threshold voltage V_{th}, a false triggering occurs. This can cause a shoot-through-current to flow through the MOSFET, resulting in deterioration and breakdown of the devices. Note that next-generation switching devices such as SiC-MOSFETs and GaN-FETs tend to have a low threshold voltage and are more susceptible to switching noise than conventional Si-MOSFETs. In addition, during switching transitions, the L_{CS} acts as negative feedback. It means an increase in the rise time and fall times during the turn-on and turn-off transition of switching devices. As a result, L_{CS} causes switching loss of switching devices. Therefore, to prevent false triggering and reduce switching losses in power converters, it is necessary to understand the influence of L_{CS} and design it.

Based on the above problems, various studies, and application notes have pointed out the importance of L_{CS} reduction[5][6][13][14][16]. In general, L_{CS} can be reduced by separating the current loops of the main circuit and gate drive circuit on the PCB layout. However, even with such optimal design at the PCB layout level, parasitic L_{CS} in the device package can be an issue in high-power, high-speed switching applications such as those used in power converters. Typical L_{CS} in 3 pin switching devices for high-power applications such as Fig. 3. is estimated to be several nH to several tens of nH[4]. To reduce the L_{CS} in MOSFETs, a 4 pin MOSFET based on the kelvin connection principle as shown in Fig. 4 was proposed. Hereafter, the gate terminal is denoted as G, the drain terminal as D, the power source terminal as S_d, and the Kelvin source terminal as S_g. Normally, in a 3 pin MOSFET, all the source bonding wires drawn from the semiconductor chip are connected to the same source terminal. On the other hand, the 4 pin MOSFET has a physically separated Source terminal structure in which the bonding wires are connected to the power source terminal S_d and the kelvin source terminal S_g respectively. This structure intends to eliminate the current common path of the drain current path and gate current path and it resulted in a reduction of L_{CS}. Because of this structure, 4 pin MOSFETs have been regarded as having no L_{CS} [7], but in fact, there are no references for quantitative evaluation of L_{CS} in 4 pin MOSFETs. Furthermore, recent research[8] has pointed out that L_{CS} is not the mere stray inductance of the shared path by the power loop and driving loop, but the mutual inductance between them. This previous study shows that the magnetic coupling that exists between the parasitic inductances around the MOSFET can be converted to parasitic inductances in the common source path by a T-shape equivalent transformation. This means that even in a structure such as a 4 pin MOSFET, where the drain current path and gate current path do not have a common wiring path, L_{CS} is generated due to magnetic coupling proximate path to each other, such as through-hole terminals and bonding wires inside the package. In addition, previous studies have reported that even a L_{CS} of less than 1 nH significantly increases switching losses in a buck converter working at 500 kHz[18]. This implies that L_{CS} of 4 pin MOSFET is an obstacle to improving switching speed and power efficiency. Therefore, it is important to measuring the L_{CS} of 4 pin MOSFETs to take advantage of the characteristics of next-generation switching devices in the future.

The purpose of this paper is to measure the L_{CS} on 4 pin MOSFETs and to clarify how the internal wiring structure of the device contributes to the generation of L_{CS}.

The paper is divided into four chapters. Chapter 1 described the background, issues, and objectives of this study. Chapter 2 outlines the measurement principles for measuring the common source inductance in actual measurements. Chapter 3 describes

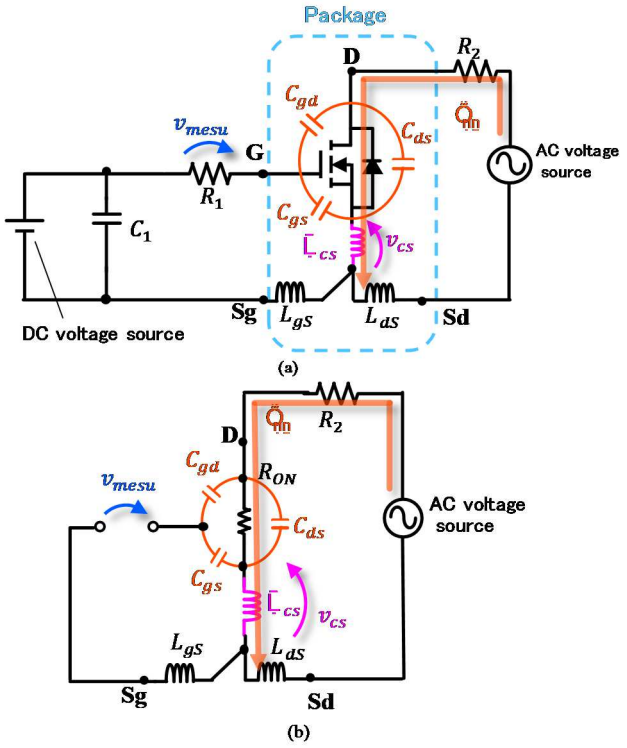


Fig. 5 Schematic diagram of the measurement method of L_{CS}.
(a) Measurement circuit applied to a switching device under test.
(b)AC equivalent circuits model

the measurement results of L_{CS} of MOSFETs in the TO-247-4L package, a typical 4 pin package offered by various manufacturers. Chapter 4 presents the validity of measured results using electromagnetic field analysis based on finite element method(FEM). The relationship between the internal package wiring structure and L_{CS} is also discussed. Based on the measurement results, whether L_{CS} of 4 pin MOSFETs can have a negative effect on switching operation is discussed. Finally, Chapter 5 presents the conclusions.

II. Measument Method

In this chapter, We presents the measurement principles for measuring the common source inductance.

Measurement of the common source inductance is difficult for several reasons[8]. One of the reasons why it is difficult to measure L_{CS} is that L_{CS} is distributed at bonding wire and through-hole terminal which are hidden inside the molded package. For this reason, it is difficult to measure L_{CS} by probing between two points using general inductance measurement devices such as impedance analyzers. However, recent research has proposed a practical measurement method for L_{CS} that solves these problems[8]. It has also been reported that L_{CS} under 1nH has been successfully measured using this method[9]. In this study, we employ this measurement method to measure the L_{CS} of a 4 pin MOSFET. The following is a brief explanation of the L_{CS} measurement principle.

Fig. 5 shows the measurement circuit for measuring L_{CS}. A resistor R_1 is a sufficiently large resistance and C_1 is a sufficiently large capacitance. R_1 and C_1 are connected in series to the gate of the switching device. A DC power supply is connected in parallel with C_1 to turn on the switching device. On the other hand, the drain and source of the switching device are connected to the AC power supply through a shunt resistor R_2. The AC power supply supplies an AC current i_{ac} to the switching device, which induces an induced voltage v_{CS} at L_{CS}. The i_{ac} is detected by the shunt resistor R_2.

Here, R_1 has a much larger impedance than the parasitic capacitance C_{gs} between the gate and source of the switching device and the parasitic inductance L_{gs} at the source terminal of the gate drive circuit. Therefore, the voltage v_{CS} induced at L_{CS} appears as v_{mesu} at R_1 without attenuation due to these parasitic components. From the above, the common source inductance L_{CS} is expressed by the equation(1), where the effective value of v_{mesu} is V_{mesu}, the effective value of the current flowing through the main circuit i_{ac} is I_{ac}, the frequency of i_{ac} is f, and the phase difference between v_{mesu} and i_{ac} is θ.

$$L_{CS} = \frac{V_{mesu}}{2\pi f I_{ac}} sin\theta \tag{1}$$

III. Experiments

This chapter presents the results of evaluating L_{CS} of a TO-247-4L package, a common 4 pin package, using the measurement principle of common source inductance L_{CS} described in Chapter 2. As pointed out in reference [9], L_{CS} is the mutual inductance between the gate drive circuit and the circuit, and its value varies depending on the physical positional relationship between the gate current path and the drain current path. Since the objective of this paper is to measure the parasitic inductance that exists inside the switching device, there must be no magnetic coupling between the main circuit wiring and the gate drive circuit on the PCB layer. Therefore, as shown in Fig. 6, the wiring paths of the main circuit current and the gate drive circuit on the test board were designed to be separated and orthogonal to each other.

Fig 7 showed test circuit board to measure common source inductance In this experiment, a frequency response analyzer (FRA) was employed to apply AC voltage for the main circuit and to measure v_{mesu} of R_1 and i_{ac} of the main circuit. Since the targets of this study are 4 pin MOSFET whose L_{CS} is considered to be very small, the value of v_{mesu} induced at L_{CS} is several tens of mV, which is very small compared to a 3-terminal MOSFET. Therefore, measurement in the high-frequency range is required to increase the voltage v_{CS} induced in L_{CS}. In a previous study (8), a measurement system using an oscilloscope and current probe was employed, but it is difficult to correct for skew between measurement devices in the high-frequency range with this measurement system. Therefore, a measurement system was constructed employing FRA, which can be calibrated accurately without using an external skew kit and has high voltage resolution.TABLE.1. shows the measurement devices used for the L_{CS} measurement. TABLE 2. shows the circuit elements used in the measurement of this experiment. TABLE 3. shows the measured L_{CS} of 21 different TO-247-4L packages. TABLE 3. shows that the L_{CS} values varied widely from 0. 24 to 0.8 nH, even though the measurements were executed on a 4 pin MOSFET in the same package.

TABLE 1. LIST OF EXPERIMENTAL INSTRUMENTS

	f :1-10MHz;　Vac : 10V
C1	Ceramic Capacitor 0.1μF(Murata)
R1	chip Resistor 1MΩ,RK73H1ETTP1004F (KOA Corp.)
R2	shunt resistor 1Ω (Vishay Foil Resistors)

TABLE 2. LIST OF EXPERIMENTAL INSTRUMENTS

Instrument	Model (Manufacturer)
frequency response analyzer	FRA51615,(NF Corp.)
DC stabilized Power Supply	PMX350-0.2A,(KIKUSUI)

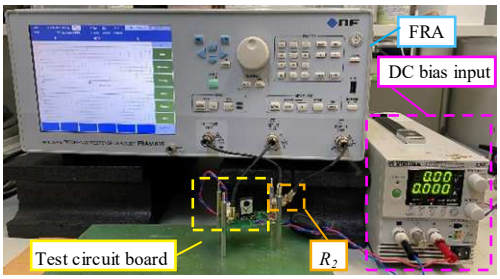


Fig. 6 Photograph of test circuit

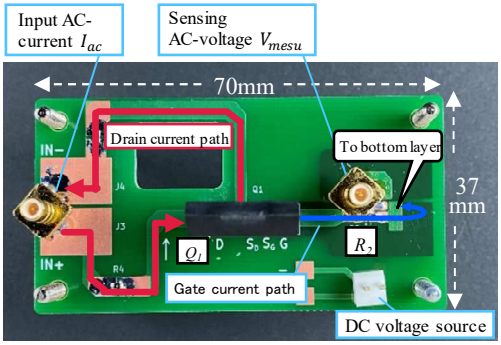


Fig. 7 Test circuit board to measure common source inductance.

IV. CONSIDERATION

A. Comparison With Simulation

In this section, the validity of the measured L_{CS} in Chapter 2 was investigated. In addition, the relationship between the differences in L_{CS} values among manufacturers and the internal wiring structure of the package is discussed. As the approach to achieve the above objectives, the resin mold of the 4 pin MOSFET of the TO-247-4L package used for the measurement was removed and the internal wiring structure was observed. Based on the internal wiring structure of the package, an electromagnetic field analysis simulation based on the finite element method (FEM) was performed.

Fig. 8 shows the internal wiring structure of a 4 pin MOSFET in three different TO-247-4L packages. In Fig.8, the differences in the number, length, and angle of bonding wires inside the package and the distance between the main circuit source and gate drive circuit bonding wires can be seen. To investigate how these differences in internal wiring structures affect L_{CS}, the bonding wire and through-hole terminal structures

TABLE 3. LIST OF MEASURED SWITHCHING DEVICES

Production ID	Manufacturer	Absolute Maximum Ratings		Measured L_{cs}[nH]
		Drain-Source Voltage V_{DS} [V]	Continuous Drain Current I_D [A]	
IPZA60R080P7XKSA1	Infineon Technologies AG	600	37	0.37
IPZA60R120P7XKSA1	Infineon Technologies AG	600	26	0.43
SCT3040KR	ROHM Co., Ltd.	1200	55	0.58
IPZ65R065C7XKSA1	Infineon Technologies AG	650	33	0.34
STW70N60DM6-4	STMicroelectronics NV	600	62	0.35
STW57N65M5-4	STMicroelectronics NV	650	42	0.56
STW38N65M5-4	STMicroelectronics NV	650	30	0.46
NTH4LN095N65S3H	ON Semiconductor	650	30	0.30
FCH023N65S3L4	ON Semiconductor	650	75	0.45
IPZ60R040C7XKSA1	Infineon Technologies AG	600	50	0.27
NVH4L040N65S3F	ON Semiconductor	650	65	0.39
NTH4LN040N65S3H	ON Semiconductor	650	62	0.44
IPZ65R019C7XKSA1	Infineon Technologies AG	700	75	0.24
IPZ60R017C7XKSA1	Infineon Technologies AG	600	109	0.35
STW75N60M6-4	STMicroelectronics NV	600	72	0.46
C3M0025065K	Wolfspeed, Inc.	650	97	0.69
G3R45MT17K	GeneSiC Semiconductor Inc.	1700	61	0.60
SCT3105KR	ROHM Co., Ltd.	1200	24	0.82
G3R20MT12K	GeneSiC Semiconductor Inc.	1200	128	0.58
NTH4L060N090SC1	ON Semiconductor	650	46	0.41
MSC015SMA070B4	Microchip Technology	700	140	0.43

of three types of MOSFETs, CT3015KR (ROHM Co., Ltd.), NTH4L060N090SC1 (ON Semiconductor), and IPX65R065C7XKSA1 (Infineon Technologies AG), were examined. Fig. 9 shows the simulation model of NTH4L060N090SC1 (ON Semiconductor). The simulation model including both bonding wire and through-hole terminals as shown in Fig. 9 is referred to as the Whole model. JMAG Ver. 21.0.02v was used as the FEM simulator. In this simulation, based on the measurement principle described in Chapter 2, the electroma10netic field generated at the drain terminal when a high-frequency current is supplied between D and S_d was analyzed and derived by detecting the voltage induced between S_g and G. The voltage applied between D and Sd was 10 V. L_{CS} was derived by averaging the L_{CS} values obtained at each frequency over the frequency range of 1-10 MHz by running simulations in 1 MHz increments. In this analysis, the magnetic coupling between the main circuit on the PCB and the gate drive circuit was regarded as negligible. The length of the through-hole terminals reproduces the length of the MOSFET when it is mounted on the PCB. In addition, in order to identify the wiring structure that determines the value of the common source inductance L_{CS} of the 4 pin MOSFET, the whole model as shown in Fig.10, was divided into (a) a bonding wire section and (b) a through-hole terminal section. The simulation model shown in Fig. 10(a),(b) is hereinafter referred to as the partial model.

First, the validity of the measured results of L_{CS} obtained in Chapter 2 was investigated. Fig. 10. shows the results of the comparison between the measured value and simulation value of L_{CS}. The relative error between the measured and simulated L_{CS} values for IPX65R065C7XKSA1 was 5.97%. The above

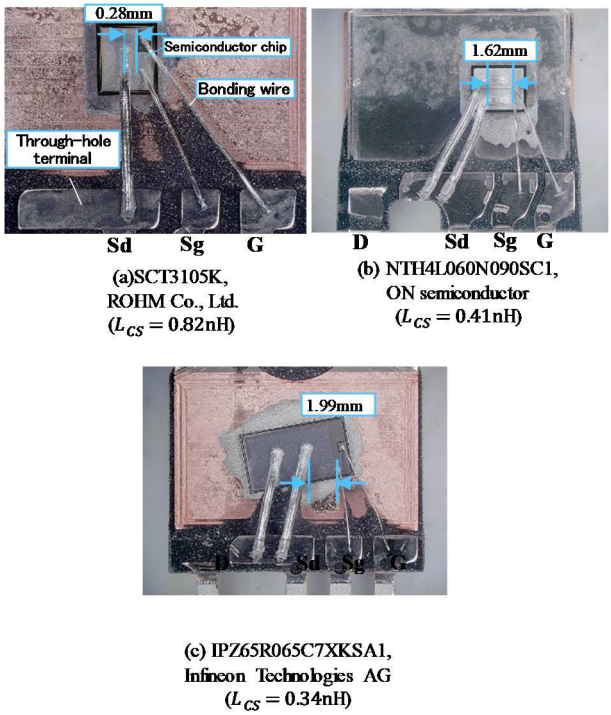


Fig.8 Internal bonding wire structures in 3 switching devices of TO-247-4L package

results confirm the validity of the L_{CS} measurement results presented in Chapter 2, and the previously unknown L_{CS} value of the 4 pin MOSFET was obtained by actual measurement. Note that the simulation model used in this electromagnetic field analysis consists of two independent components: the main circuit (copper) and the gate drive circuit (gray). therefore, this model has a structure in which there is no common part of the current path. This strongly implies that the L_{CS} in the 4 pin MOSFET is mutual inductance between the bonding wire of power source S_d and the bonding wire of kelvin source S_g

B. Clarification of parameters to determine L_{CS}

Next, we investigate the factors that determine the values of the common source inductance L_{CS} of the 4 pin MOSFET. As an approach, We employed a simple straight conductor model showed Fig. 12.

First, We focus on the relationship between the distance between the bonding wires of power source S_d and the bonding wires of the kelvin source S_g. Fig. 13 shows the relationship between L_{CS} as measured in Chapter 2 and the distance d between the bonding wires of the power source S_d and the bonding wires of the kelvin source S_g. Here, the distance d between S_d and S_g are defined as perpendicular from the starting point of the bonding wire of the kelvin source to the bonding wire of the power source as Fig. 12. As Fig.13., it was found that there is a clear correlation between the distance of these two bonding wires and L_{cs}. In a single regression analysis, the coefficient of determination(R^2) was 0.688. Note that It is generally known that the strength of magnetic coupling depends on the distance between conductors through which current flows. In other words, this result implies that the L_{CS} of the 4 pin

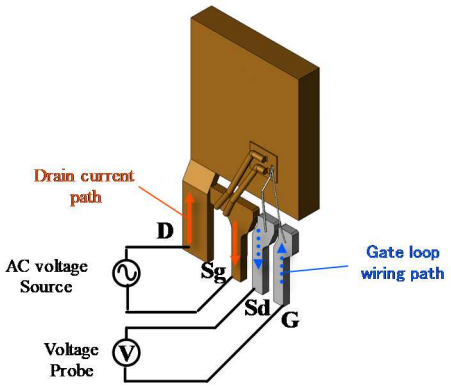


Fig. 9 Simulation model of NTH4L060N090SC1

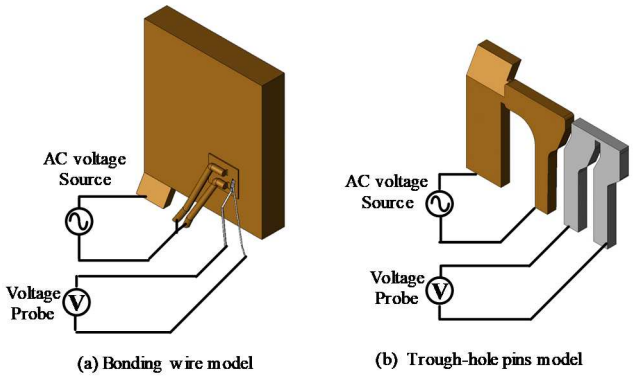


Fig.10 Partial model of simulation NTH4L060N090SC1 (ON Semiconductor)

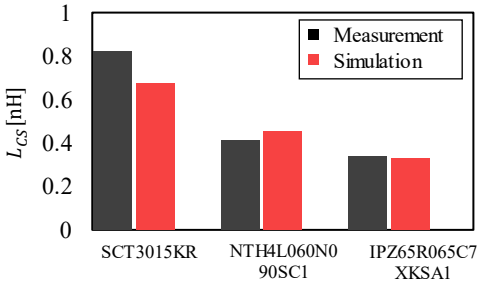


Fig.11 Comparison of measurement and simulation

MOSFET is the mutual inductance between the internal bonding wires.

second, we focused on the kelvin source length as a parameter that affects L_{CS}. In general, the magnetic coupling between conductors becomes stronger the longer the parallel conductors are. Therefore, we employed as a parameter the component of the bonding wire of the kelvin source that is parallel to the Power source, i.e., $l_{sg}\cos\theta$, as shown in Fig. 14. Fig.14. shows the relationship between $l_{sg}\cos\theta$ and L_{CS}. As a result, Fig. 14. shows that there is no significant correlation between $l_{sg}\cos\theta$ and L_{CS}.

C. Clarification of areas contributing to L_{CS}

Next, to optimize the internal wiring of the 4 pin MOSFET and reduce L_{CS}, we quantitatively evaluated which part of the internal wiring structure contributes most to the generation of L_{CS}. As an approach, we simulated the partial models of the

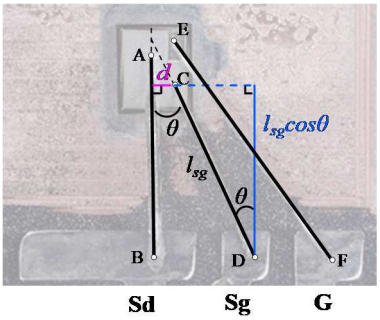


Fig.12 Straight conductor model to clear relationship between L_{CS} and inner structure of switching devices.

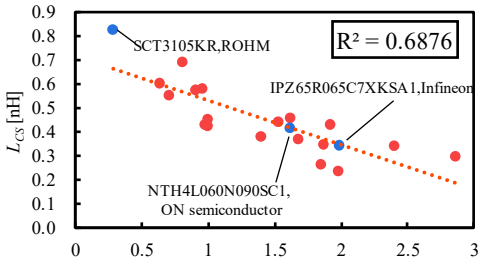


Fig.13. Relationship of measured L_{CS} on the distance between bonding wires of power source and kelvin source.

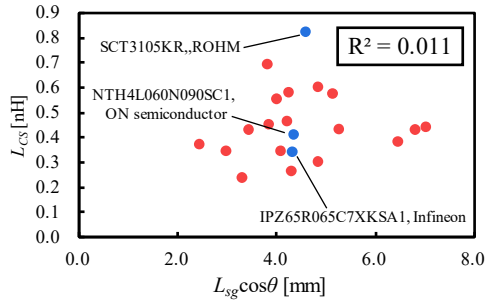


Fig.14 Relationship of measured L_{CS} on l_{sg}cosθ.

bonding wire section and the through-hole terminal section shown in Fig. 9 individually, and derive the ratio of L_{CS} in each section to the total L_{CS}. Fig. 12 shows the comparison results of the simulation of the partial models for the bonding wire part only and the through-hole terminal part only. In the SCT3015KR, the 4 pin MOSFET with the largest L_{CS} among the three types of MOSFETs measured, the L_{CS} between bonding wires accounted for 43.2% of the total partial inductance. On the other hand, for IPX65R065C7XKSA1, which has the smallest L_{CS}, the L_{CS} between bonding wires accounted for 17.1% of the total partial inductance. It was also found that the through-hole terminals resulted in an average L_{CS} of 0.272 nH at a nearly constant value. This is because the through-hole terminal structure of the TO-247-4L package is almost the same regardless of the manufacturer. The above results also show that most of the L_{CS} in the 4 pin MOSFET is caused by the mutual inductance between the bonding wire of power source and the bonding wire of the kelvin source. Furthermore, the results

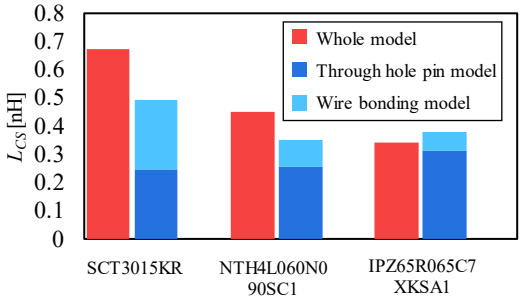


Fig.15 Ratio of L_{CS} components based on simulation.

imply that further reduction of L_{CS} can be expected by optimizing the structure of the bonding wire section. As a specific design guideline, the structure should be such that the magnetic coupling between the bonding wires of power source and the kelvin source is minimized. In other words, it is likely to be effective to widen the spacing between these wires and to make the arrangement of bonding wires closer to orthogonal. In Fig. 15, the sum of the partial inductances does not match the value of L_{CS} in the whole model. There are two main reasons for this result. First, there is a contribution of magnetic coupling between relatively distant wiring structures. The approach employed in this paper was to split the model into two partial models, one between bonding wires and the other between through-hole terminals, as shown in Fig. 10, and evaluate the ratio of magnetic coupling. However, strictly speaking, mutual inductance is expected to exist between the bonding wires of the power source and the through-hole terminals of kelvin source, as well as between the through-hole terminals of the power source and the bonding wires of the kelvin source. The second reason is that the inductance cannot be strictly expressed as the sum of the contributions of each part. As emphasized by reference [10], inductance is essentially a concept that can only be applied when the conductors form a closed loop. This indicates that magnetic coupling also exists between each of the divided partial models, and the L_{CS} of the actual measurement and the overall model is determined based on this magnetic coupling. On the other hand, the L_{CS} of the partial model does not reflect this magnetic coupling between the different partial models each other. For these two reasons, we consider that a mismatch between the sum of the partial model and the L_{CS} of the overall model is generated.

Next, we investigate whether the value of L_{CS} of the 4 pin MOSFET measured in Chapter 2 affects the actual switching operation. Based on the results of in Chapter 3, the maximum value of the measured common source inductance L_{CS} is approximately 1 nH. This indicates that a maximum voltage of 1V is induced when the drain current changes at 1A/ns during switching. However, the possibility of false triggering by L_{CS}. However, SiC-MOSFETs and GaN-FETs such as next-generation switching devices, can switch currents of 100A or more at speeds of 100ns or more, and this switching speed is being realized. Therefore, L_{CS} is likely to become an important design factor of power converters for high-power applications, and further reduction of L_{CS} may be required for MOSFETs with Kelvin connection terminals in the future.

V. CONCLUTION

In recent years, the emergence of next-generation switching devices such as SiC-MOSFETs and GaN-FETs has led to higher switching speeds and high-power capacity, and the common source inductance LCS in the switching device has increased the risk of false triggering and switching losses. Although 4-terminal MOSFETs with Kelvin source terminals have been considered to have no L_{CS}, there is no quantitative report on L_{CS} of 4 pin MOSFETs. The purpose of this paper is to measure the L_{CS} parasitic on 4 pin MOSFETs and to elucidate how the internal wiring structure of the switching device contributes to the generation of L_{CS}. As a result, it was found that most of the L_{CS} are caused by the mutual inductance between the bonding wires of the power source and the kelvin source and that the L_{CS} of the 4 pin MOSFET may affect the switching operation when the switching device is driven to take advantage of the performance of next-generation switching devices in the future. It was also implied that the arrangement of the bonding wires between the power source and kelvin source in such a way that their mutual inductance becomes small is effective in reducing the L_{CS}.

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