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Difference in Overvoltage Stress Behavior between CIS and UIS in Ohmic p-Gate GaN HEMTs

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***Abstract*— The behavior under overvoltage stress was compared between clamped inductive switching (CIS) and unclamped inductive switching (UIS) in Ohmic p-Gate GaN-HEMTs. In both cases, failure causes hole current to flow from the drain to the substrate. However, the changes in drain voltage at failure, peak voltage shift under repeated stress, and drain-source capacitance shift showed opposite trends. These differences between CIS and UIS are attributed to the distinct effects of electron and hole traps on electric field concentration at the drain electrode edge. However, regardless of the trap polarity, impact ionization at the drain electrode edge destructs the drain–substrate heterostructure, and thus current always flows between them at failure.**

Keywords*— *GaN-HEMT, overvoltage stress, avalanche breakdown

I. Introduction

GaN-HEMTs are being rapidly adopted in power electronics applications [1]. However, GaN-HEMTs have little to no avalanche-withstanding capability; their breakdown, induced by the peak electric field in GaN, usually results in catastrophic failure [2]-[3]. Therefore, commercial GaN-HEMTs are designed with a breakdown voltage much higher than the rated voltage to provide a large overvoltage margin in converter applications [4]. This, however, presents an obstacle to reducing on-resistance.

For reliable design in GaN-HEMTs, degradation behavior due to overvoltage stress have been investigated [5]-[6]. Previous experimental studies have found that holes generated by impact ionization induce catastrophic failure and time-dependent breakdown [7]-[8], and the failure location is determined by the path of the hole current.

In power electronics applications, surge voltage occurs during the turn-off switching of GaN-HEMTs, resulting in overvoltage stress. The voltage and current waveforms differ between hard and soft switching. Under hard switching, high voltage is applied before current reduction, whereas under soft switching, high voltage is applied after current turn-off. Therefore, the acceleration of channel electrons, carrier trapping, and related behavior under overvoltage are also expected to differ. However, the variation in this behavior depending on the circuit topology, as well as the processes leading to device failure, have not been studied in detail.

This paper compares the behavior of GaN-HEMTs under clamped inductive switching (CIS), which emulates surge generation in hard switching, and unclamped inductive switching (UIS), which resembles surge generation in soft switching, and reports the findings on carrier effects and failure mechanisms.

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II. Experimental Setup

The test setup is shown in Fig. 1. In the CIS, after the drain voltage rises, the drain current begins to decrease. Because the current path rapidly switches from the GaN-HEMT to the SiC-SBD, the *dI/dt* is large, and the duration of the voltage surge is short. By inserting an inductance L_d, a voltage surge is generated due to the *dI/dt* during turn-off.

In contrast, in the UIS, the current path does not change, and the output capacitance of the GaN-HEMT is charged by the drain current. Consequently, the drain voltage increases more gradually compared with the CIS, while the drain current decreases, becoming nearly zero near the drain voltage peak. A voltage surge occurs due to resonance between the load inductance and the output capacitance of the GaN-HEMT.

As described above, in CIS and UIS, similar to hard and soft switching, the magnitude of the current flowing under high voltage, the duration of the voltage surge, and the mechanism of surge generation are different. However, in both cases, increasing the test current leads to a higher surge voltage. Therefore, the test current was gradually increased to investigate the behavior leading to device failure by overvoltage stress.

For both CIS and UIS, single-pulse tests and burst tests [9], which consisted of applying the same stress repeatedly ten times, were conducted. In the burst tests of CIS and UIS, the

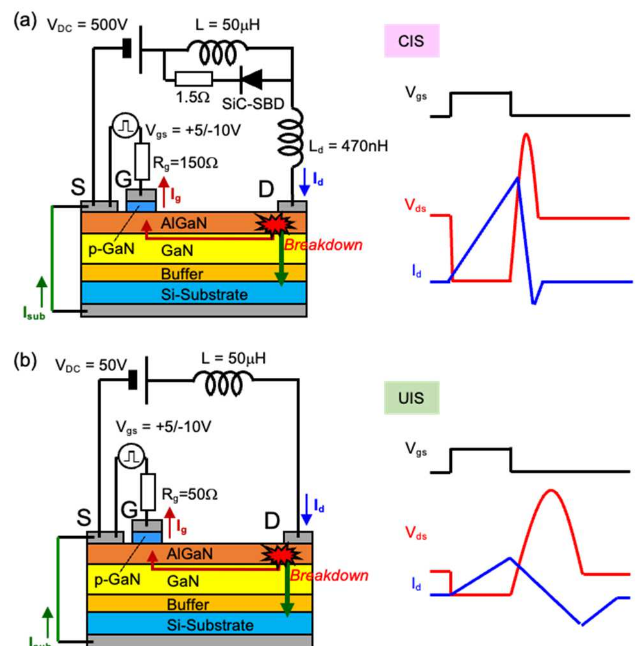

Fig.1 Test circuit of (a) clamped inductive switching (CIS) and (b) unclamped inductive switching (UIS).

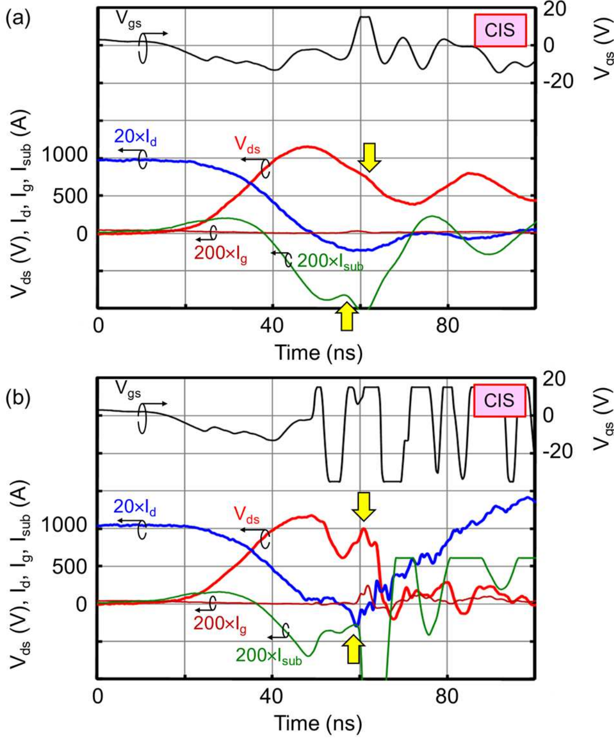

Fig. 2 Single CIS waveforms of an Ohmic p-gate GaN-HEMT (a) before failure and (b) at failure.

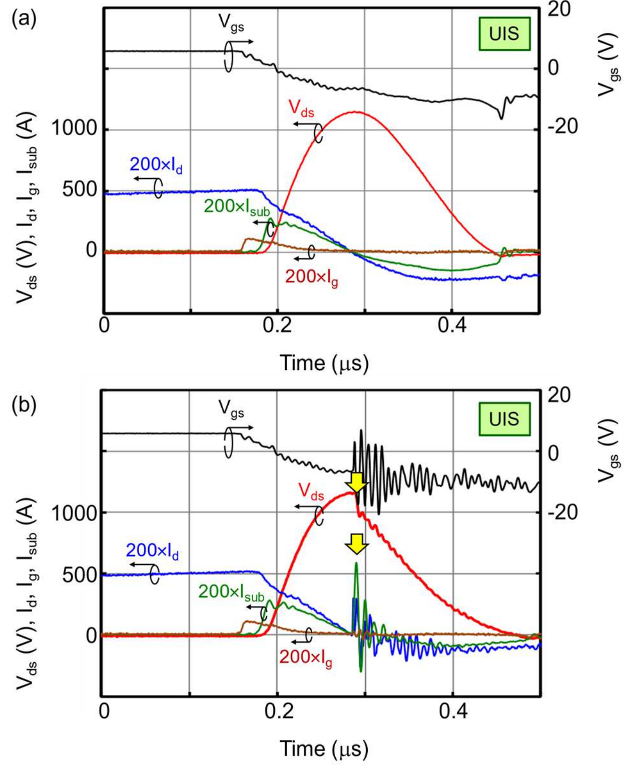

Fig. 3 Single UIS waveforms of an Ohmic p-gate GaN-HEMT (a) before failure and (b) at failure.

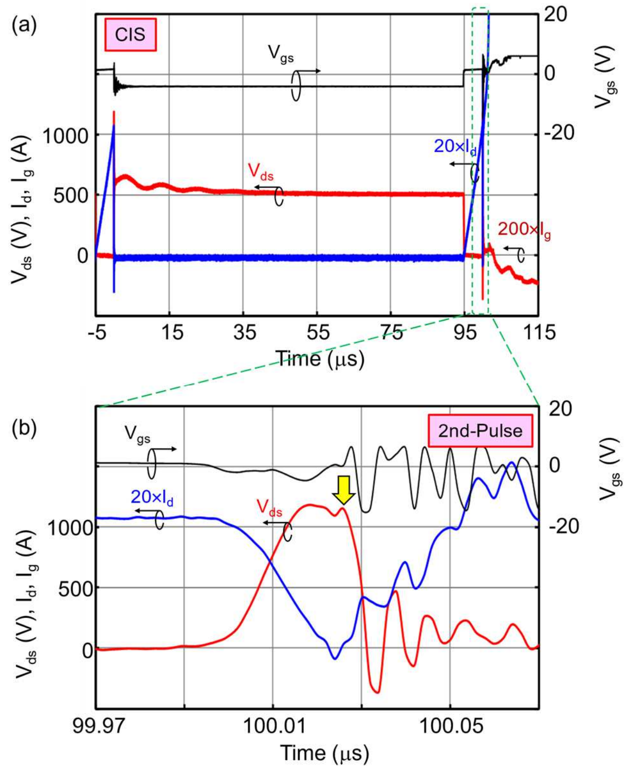

Fig. 4 (a) Burst CIS waveform of an Ohmic p-gate GaN-HEMT and (b) zoomed waveform at failure timing of second pulse.

stress cycles were set to 100 μs and 40 μs, respectively, under a constant test current. The DUT was a 600 V-class Ohmic p-gate GaN-HEMT (Infineon IGLD60R070D1) [10]. All measurements were performed at room temperature.

III. CIS and UIS Waveforms

Fig. 2 shows the waveforms before and at failure in the CIS test. After the drain voltage peak, increases in the substrate current I_{sub} and the drain voltage V_{ds} were observed. Prior to failure, these increases were small, however, at failure, distinct changes were evident. It is considered that, under high-voltage stress, impact ionization occurs, generating holes that flow into the substrate and modulate the electric field distribution through their charge, resulting in an increase in V_{ds}.

In contrast, as shown in Fig. 3, the UIS waveform exhibited a flow of I_{sub} at the time of failure, accompanied by a decrease in the drain voltage. In the UIS as well, a hole current was generated by impact ionization. However, the peak voltage decreases due to dielectric breakdown in the heterostructure between drain and substrate.

In the burst CIS waveform, a similar tendency was observed as in the single CIS test. As shown in Fig. 4, although the same stress was applied, the device did not fail during the first pulse but failed during the second pulse as shown in Fig. 4(b). In the first pulse before failure, there was no noticeable increase in the drain voltage waveform after the peak. In contrast, in the second pulse, the drain voltage increased after the peak, followed by device failure.

Also in the burst UIS, a similar tendency to that of the single UIS was observed, as shown in Fig. 5. Before failure, there was no noticeable change in the drain voltage waveform, and the drain voltage dropped suddenly at failure. From these results, it is considered that the failure mechanism is the same in both the single- and burst- stress tests. Although the behavior of the drain voltage waveform differs between CIS and UIS, in both cases, the holes generated by impact ionization affect the failure.

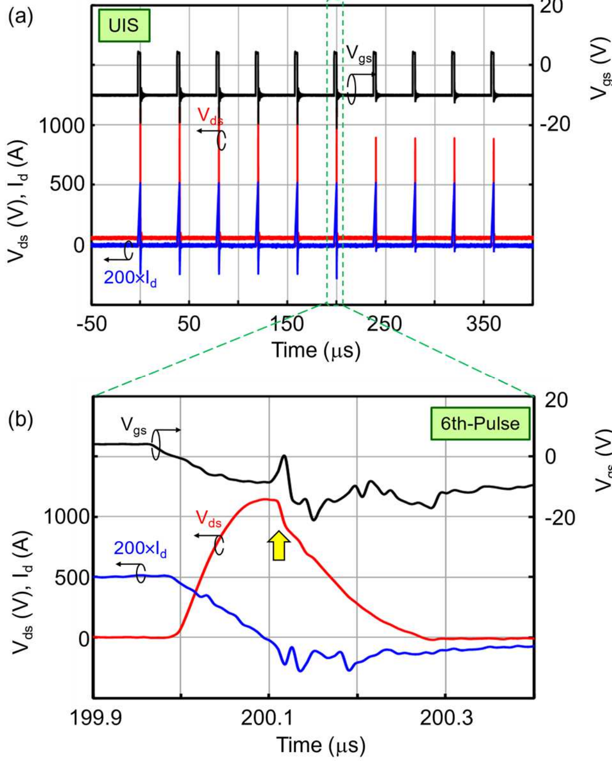

Fig. 5 (a) Burst UIS waveform of an Ohmic p-gate GaN-HEMT and (b) zoomed waveform at failure timing of sixth pulse.

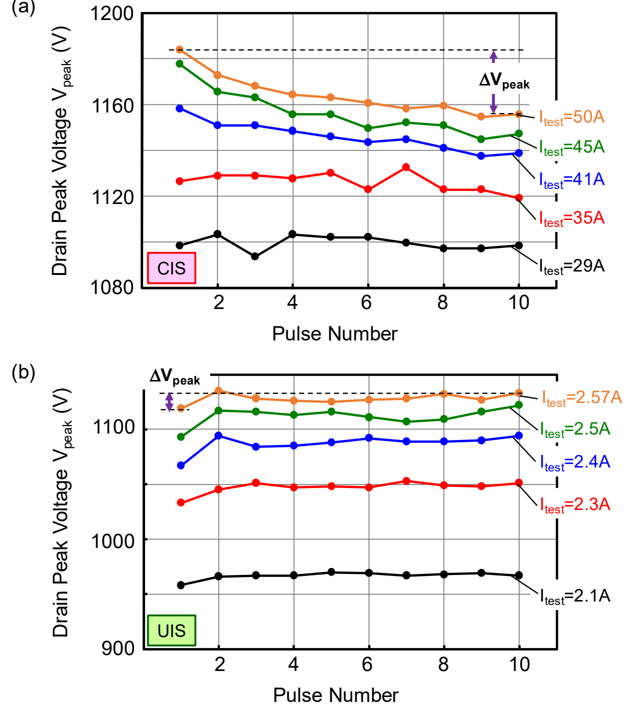

Fig. 6 Relation between peak voltage and pulse number at a function of (a) burst CIS and (b) burst UIS test currents.

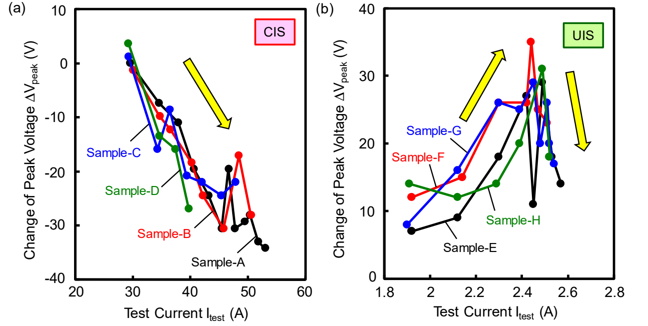

Fig. 7 Change of peak voltage by (a) burst CIS and (b) burst UIS.

IV. Discussions

The differences in drain voltage behavior between CIS and UIS are discussed as follows. Fig. 6 shows the changes in peak voltage for burst CIS and burst UIS tests. In burst CIS, repeated overvoltage stress causes the peak voltage to gradually decrease. In contrast, in burst UIS, repeated overvoltage stress tends to increase the peak voltage. The changes were enhanced with increasing test current. As shown in Fig. 7, these trends are observed across multiple devices. In burst UIS, a decrease in peak voltage is observed just before failure.

As shown in Fig. 8, the *C-V* characteristics change due to repeated overvoltage stress by burst CIS and burst CIS, suggesting that carrier trapping is the underlying cause. Fig. 9 shows the estimation of trapped carrier charge from changes in the C_{ds}–V_{ds} characteristics. The results indicate that, in burst CIS, a decrease in trapped charge suggests the presence of negative charge, corresponding to electron trapping. In contrast, in burst UIS, an increase in trapped charge suggests the presence of positive charge, corresponding to hole trapping. Furthermore, the decrease in charge observed just before failure in burst UIS is attributed to hole de-trapping.

In both burst CIS and burst UIS, the peak voltage shown in Fig. 7 and the trapped charge shown in Fig. 9 exhibit similar variations. These results suggest that carrier trapping is induced by repetitive overvoltage stress, and that the electric field distribution is modulated by the trapped carrier charge, leading to a change in the peak voltage.

Using TCAD simulations, the influence of trapped carriers on the electric field distribution under high voltage was analyzed. The device simulations were conducted using the S-Device provided by Synopsys [11]. The analysis results are shown in Fig. 10. In the simulation, carrier trapping throughout the GaN channel layer was assumed. The electric field peak at which impact ionization occurs is located at the drain electrode edge. Trapping of negative charge, corresponding to electron traps, enhances the electric field concentration at the drain electrode edge because the negative charge causes an expansion of the depletion layer. In contrast, trapping of positive charge, corresponding to hole traps, suppresses the electric field concentration at the drain electrode edge because the positive charge enhances the electric field concentration at the gate electrode edge. Consequently, the breakdown voltage decreases with negative charge and increases with positive charge, as shown in Fig. 10(b).

From these results, in burst CIS, high voltage is applied when a large current flows, leading to electron trapping and a decrease in peak voltage due to enhancement of impact ionization. In contrast, in burst UIS, the drain current near the voltage peak is small, making electron trapping less likely, while trapping of holes generated by impact ionization is pronounced, causing the peak voltage to increase. Although the peak voltage change differs between CIS and UIS, the impact ionization location remains at the drain electrode edge.

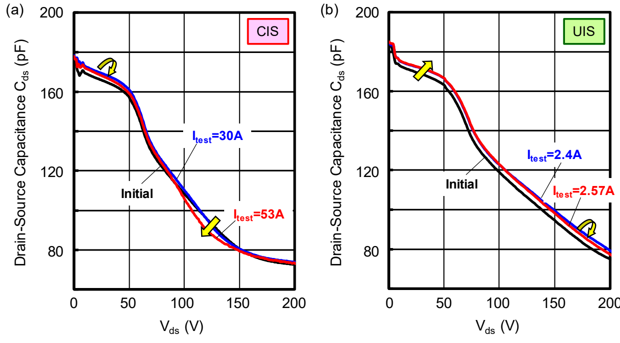

Fig. 8 Change of C_{ds}-V_{ds} curve by (a) burst CIS and (b) burst UIS.

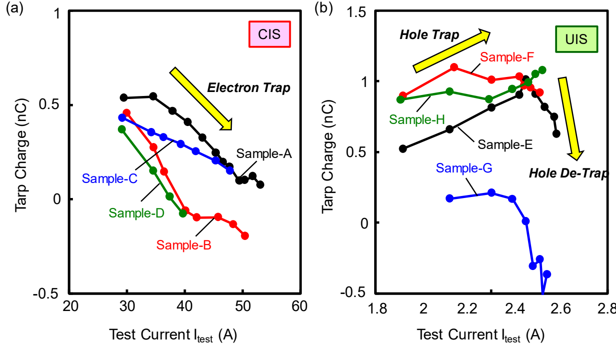

Fig. 9 Change of trapped charge by (a) burst CIS test current and (b) burst UIS test current.

Finally, a large number of holes are generated by impact ionization, leading to device failure due to dielectric breakdown of the heterostructure between the drain and the substrate. Therefore, in CIS as well, an increase in drain voltage due to the generated holes is observed at the time of failure.

V. Conclusions

The differences between CIS and UIS during overvoltage failure of Ohmic p-Gate GaN-HEMTs were investigated. Due to the difference in drain current magnitude under high-voltage application, the changes in drain voltage caused by overvoltage stress differ between CIS and UIS. In CIS, where a large current flows, electron trapping occurs, which enhances the electric field concentration at the drain electrode edge and results in a decrease in the drain peak voltage. In contrast, in UIS, where the drain current is small during high-voltage application, electron trapping does not occur; instead, hole trapping caused by impact ionization becomes dominant, leading to an increase in the peak voltage. Although the drain voltage behavior differs between CIS and UIS, in both cases, impact ionization occurs at the drain electrode edge, and the device eventually fails due to dielectric breakdown of the heterostructure between the drain and the substrate.

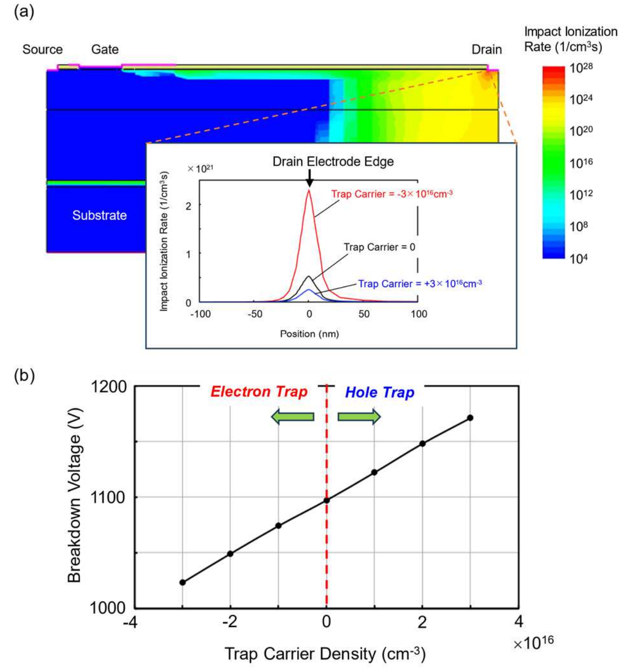

Fig. 10 Simulation results of (a) impact ionization rate distribution and (b) breakdown voltage changed by trapped charge.

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