Effect of Substrate Bias in Ohmic p-Gate GaN-HEMTs on Unclamped Inductive Switching Capability

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***Abstract*— The unclamped inductive switching (UIS) capabilities of ohmic p-gate GaN-HEMTs under various substrate bias conditions were measured. One of the critical disadvantages of GaN-HEMTs is their ultra-low UIS capability because there is no structure for the removal of holes generated by the impact ionization. Therefore, the failure position due to overvoltage stress strongly depends on the current path of the holes generated by impact ionization. This paper reports that the UIS capability of ohmic p-gate GaN-HEMTs can be improved by a floating or positive biased substrate condition due to the modulation of the hole current path. Additionally, increasing the gate resistance in the floating substrate condition slows down *dV/dt*, leading to a greater amount of energy being consumed in the semi-on state, which in turn increases the UIS capability.**

***Index Terms*—GaN-HEMTs, UIS capability, avalanche breakdown**

I. Introduction

GaN -HEMTs are being fast adopted in power electronic applications [1], [2]. However, the GaN-HEMT has no or little avalanche withstanding capability; their breakdown, induced by the peak electric field in GaN, usually results in catastrophic failure [3]-[5]. Therefore, commercial GaN-HEMTs are designed with a breakdown voltage much higher than the rated voltage to provide a large overvoltage margin in converter applications [6].

In previous works, a comprehensive methodology for achieving surge-robust GaN-FET power supplies was presented [7], and a model for calculating the switching lifetime of an application circuit by directly computing the switching stress using the waveform was proposed [8]. In power electronics applications of GaN-HEMTs, reliability is ensured by providing a large voltage margin. However, large voltage margin means designing for a higher breakdown voltage, which leads to a longer drain-gate offset distance. As a result, the drain-gate offset resistance increases, hindering the reduction of on-resistance. Therefore, by investigating the effects on dynamic breakdown voltage and degradation behavior due to overvoltage stress, not only can the mechanism of characteristic shift be clarified, but also the necessary voltage margin for power electronics applications can be discussed [9]-[11].

The failure of GaN-HEMTs due to overvoltage stress is characterized by catastrophic failure and time-dependent breakdown [12]-[17]. As a result, it appears to be similar to the breakdown of insulating layers, such as passivation films, rather than to the semiconductor layers of AlGaN/GaN heterostructures. However, in previous experimental studies, it has been found that holes are generated due to impact ionization, and the failure location is determined by the path of the hole current. In other words, time-dependent breakdown leads to catastrophic failure of heteroepitaxial layers. This occurs because the heteroepitaxial layers act as insulating films due to band discontinuity, and the hole current induces crystal defects under a high electric field through a percolation mode of time-dependent breakdown [13], [17].

A major trend observed in current ohmic p-gate GaN-HEMT products is that impact ionization occurs at the drain electrode edge. The holes generated by impact ionization flow toward the silicon substrate under the vertical electric field or toward the gate under the lateral electric field [11]. The ease of hole removal determines the location of the failure. When hole removal from the gate through the p-GaN layer is possible due to ohmic contacts, the failure occurs due to vertical hole removal, leading to the destruction of the heterostructure between the drain and the silicon substrate [13]. In contrast, when hole removal from the gate is hindered by Schottky contacts, the AlGaN barrier layer beneath the gate breaks down [17]. Based on these results, it is anticipated that improving hole

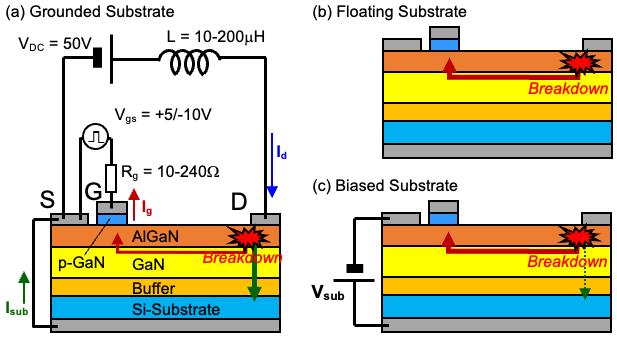

Fig.1 Test circuit of UIS and types of test sample substrate electric conditions.

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removal during avalanche breakdown will enhance unclamped inductive switching (UIS) capability.

This paper reports on the results of investigating changes in UIS capability of ohmic p-gate GaN-HEMTs by modulating hole removal flowing from the drain toward the silicon substrate by altering the electrical connection state of the silicon substrate.

II. Experiment Setup

The test circuit configuration is the same as conventional UIS test one as shown in Fig. 1(a). During the on-state of DUT, energy is stored in load inductance due to current flow. After the turn-off of the DUT, stored energy is transferred from the load inductance to the DUT by charging the output capacitance of the DUT and dissipating the energy through off-state leakage current and avalanche breakdown. With a change in the load inductance to 10–200 μH, the voltage pulse width becomes 150–500 ns. Since impact ionization occurs near the voltage peak, the duration of avalanche breakdown is approximately a few nanoseconds.

By varying the load inductance, the relationship between the UIS test current, dynamic breakdown voltage, and UIS capability was investigated. Additionally, by varying the external gate resistance from 10 to 240 Ω, the changes in dynamic breakdown voltage and UIS capability due to variations in the gate discharge current were also examined. The initial junction temperature for all UIS tests was at room temperature.

To modulate the path of the hole current generated by impact ionization, three types of substrate conditions were compared. These conditions are: 1) grounded, 2) floating, and 3) DC voltage biased. In the grounded condition, the silicon substrate is connected to the source, and by impact ionization, the substrate current I_{sub} flows from the drain to the silicon substrate due to the vertical electric field, while the gate current I_g flows to the gate due to the lateral electric field. When the substrate is floating, I_{sub} does not flow, and all the holes generated by impact ionization flow to the gate. When a positive bias is applied to the silicon substrate, the vertical electric field decreases, reducing I_{sub} and promoting the flow of I_g.

When the substrate is floating, the shielding effect of the substrate is lost, resulting in a decrease in C_{ds} and an increase in C_{gd}, as shown in Fig. 2. Since the output capacitance C_{oss}, which is the sum of C_{ds} and C_{gd}, decreases, if the UIS capability is largely determined by the energy stored in the charging of the output capacitance, floating the substrate will reduce the UIS capability.

In this experiment, the DUT was Infineon's CoolGaN™ IGLD60R070D1 [18], a 600V-class ohmic p-gate GaN-HEMT, which facilitates hole removal from the gate. The test circuit is illustrated in Fig. 1(a). The DC voltage V_{DC} was set to 50 V, and the gate input was set to 5 V in the on-state and -10 V in the off-state. The substrate bias voltage, as shown in Fig. 1(c), ranged from 100 V to 300 V. The substrate bias was applied more than 10 seconds before the UIS test. The application of a substrate bias before the UIS test raises concerns about the formation of new carrier traps and modulations in the 2DEG concentration.

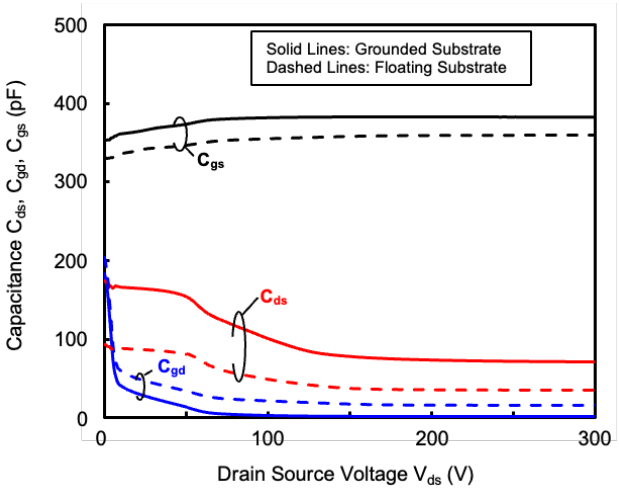

Fig. 2 C-V characteristics changed by substrate electric condition.

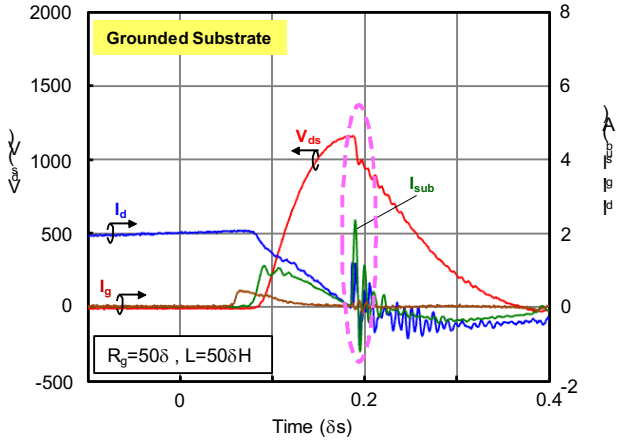

Fig. 3 Typical UIS waveform of GaN-HEMT with the substrate grounded at failure showing substrate current spike.

However, as shown later in the results of the single-pulse and burst UIS tests, no increase in dynamic on-resistance was observed. This suggests that the generation of new traps and changes in 2DEG concentration are negligibly small. The factors determining UIS capability are discussed based on changes in capability due to external gate resistance and load inductance.

The test current was adjusted by varying the pulse width used to turn on the GaN-HEMT. The pulse width was gradually increased, and the maximum current without failure was defined as the avalanche capability I_{AS}, while the peak drain voltage at that time was defined as the dynamic breakdown voltage V_{DB}. For each condition, three samples were measured. The values shown in graphs later are the averages of the three sample measurement results. Three devices were picked from the same reel.

III. UIS Waveforms

The UIS waveforms for each substrate condition are shown. Fig. 3 shows the UIS waveform at failure with the substrate grounded. Breakdown occurred at the peak drain voltage, and a rapid drop in V_{ds} was observed. At this moment, a pulse was generated in I_{sub}; however, there was no sudden increase in I_g.

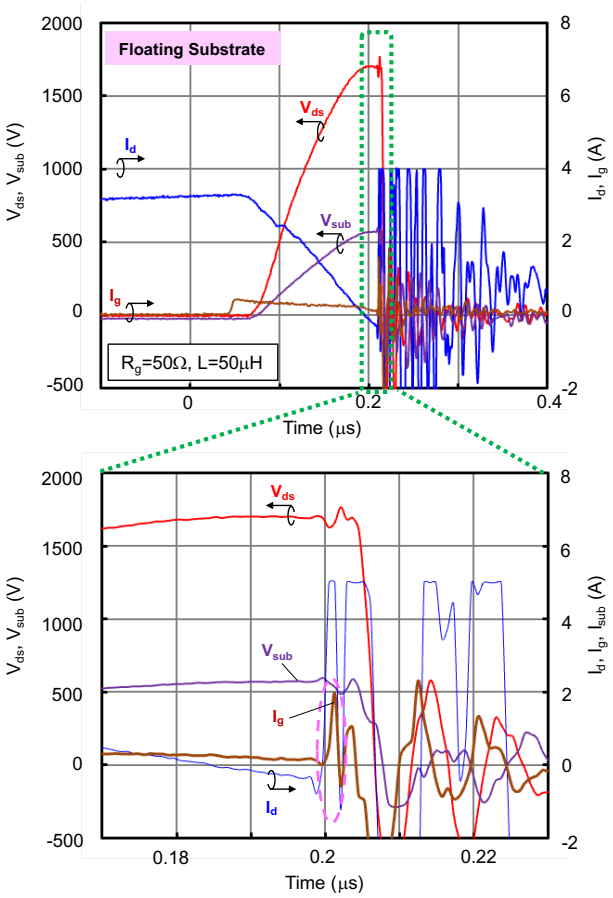

Fig. 4 Typical UIS waveform of GaN-HEMT with floating substrate at failure and its zoomed waveform showing gate current spike.

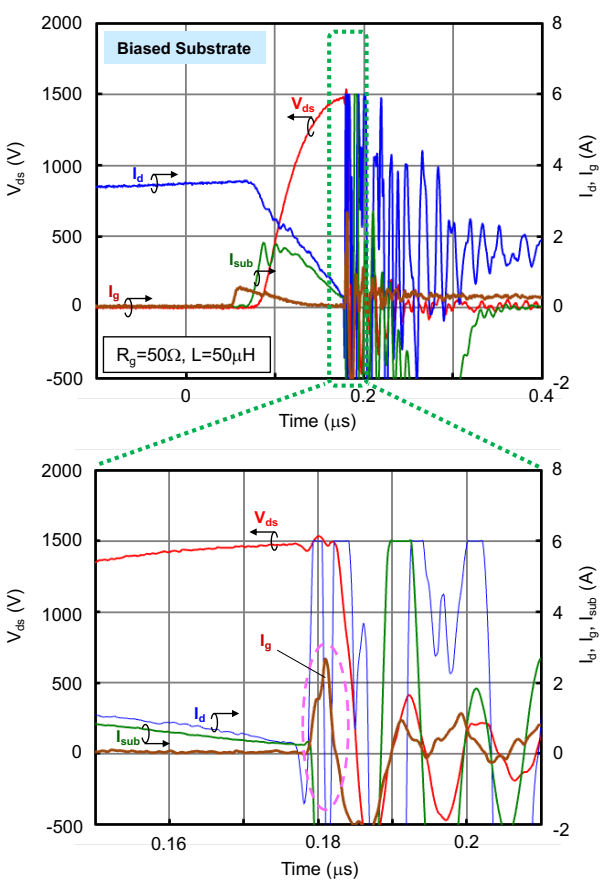

Fig. 5 Typical UIS waveform of GaN-HEMT with substrate bias of 300 V at failure and its zoomed waveform showing gate current spike.

It was confirmed that the D-S junction was damaged, while the G-S junction remained intact. From these results, it is concluded that with the substrate grounded, the heteroepitaxial layers were destroyed by the hole current flowing between the drain and the substrate, caused by the vertical electric field.

When the substrate was floating, the UIS waveform and the failure location changed. Fig. 4 shows the UIS waveform at failure with the substrate floating. Although breakdown occurred at the peak drain voltage, similar to the grounded substrate, a pulse was generated in I_g before a rapid drop in V_{ds} occurred. Both the D-S and G-S junctions were short-circuited. By floating the substrate, I_{sub} became zero, and all the hole current flowed into I_g. As a result, the AlGaN layer beneath the gate electrode was destroyed, leading to a short circuit between the G-S junction.

When a positive bias was applied to the substrate, the UIS waveform at failure became similar to that observed when the substrate was floating. Fig. 5 shows the UIS waveform at failure. Similar to the floating substrate case, a pulse was generated in I_g before the rapid drop in V_{ds} occurred due to breakdown, resulting in a short-circuit condition at the gate. The reduction of I_{sub} due to the substrate bias suppressed a damage in the heteroepitaxial layers between the drain and the substrate. However, as I_g increased, the AlGaN layer beneath the gate electrode was destroyed, leading to a short circuit at the gate.

Considering the path of the hole current, in the case of a positive biased substrate, the hole current flows through both the substrate and the gate. In contrast, under the floating substrate condition, the hole current flows only through the gate, resulting in a larger hole current in the floating substrate condition compared to the positive biased substrate condition. On the other hand, since the substrate potential is not fixed due to the floating substrate, displacement current flows in response to changes in the substrate potential. As shown in Fig. 4, when the gate current increases, the substrate potential V_{sub} decreases at the failure. Since the displacement current of gate-substrate capacitance flows in the opposite direction to the hole current, the gate current is determined by subtracting the displacement current from the hole current. In contrast, in the case of a positive biased substrate, the substrate potential is fixed, so no displacement current flows, and the gate current consists only of the hole current. Based on these considerations, when comparing the magnitude of the gate current, the positive biased substrate condition results in a larger gate current than the floating substrate condition.

IV. UIS Capabilities

To investigate the factors that determine UIS capability and the failure mechanisms, the effects of substrate electrical conditions, load inductance, and external gate resistance on UIS

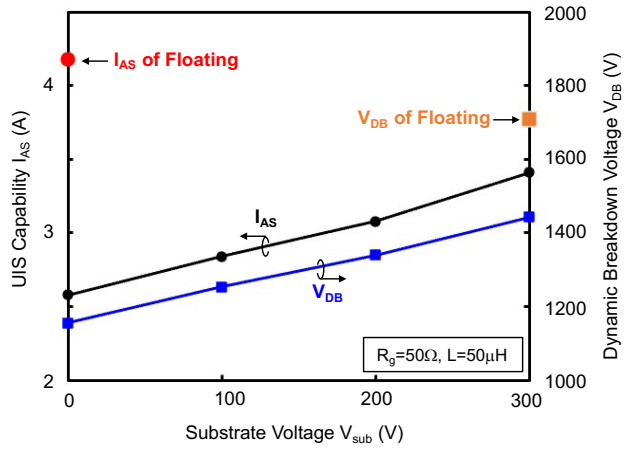

Fig. 6 Improvement of UIS capability by substrate bias due to increase of dynamic breakdown voltage.

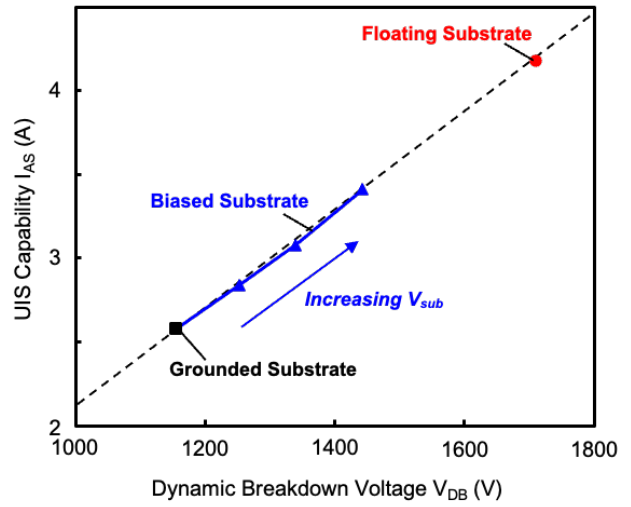

Fig. 7 Relationship between UIS capability and dynamic breakdown voltage.

capability were systematically evaluated. Based on the obtained results, potential approaches for enhancing UIS capability are discussed. Firstly, the relationship between UIS capability and the substrate electrical condition is evaluated. Fig. 6 shows the substrate voltage dependence of the UIS capability. Substrate grounding corresponds to a substrate voltage V_{sub} of 0, and the capability in the floating condition is also shown in the same figure. The UIS capability increased in proportion to the substrate voltage. Additionally, the dynamic breakdown voltage also increased proportionally with the substrate voltage. From the relationship between the UIS capability and the dynamic breakdown voltage, as shown in Fig. 7, it is evident that they align on a straight line regardless of the substrate electric condition, indicating a proportional relationship.

Based on these results, the mechanism determining the UIS capability is inferred as follows. The charging energy of the output capacitance E_{oss} is given as follows.

$$E_{oss} = \frac{1}{2} C_{oss} {V_{DB}}^2 \quad , \qquad (1)$$

where V_{DB} is the dynamic breakdown voltage. The dynamic breakdown voltage increases due to the relaxation of the

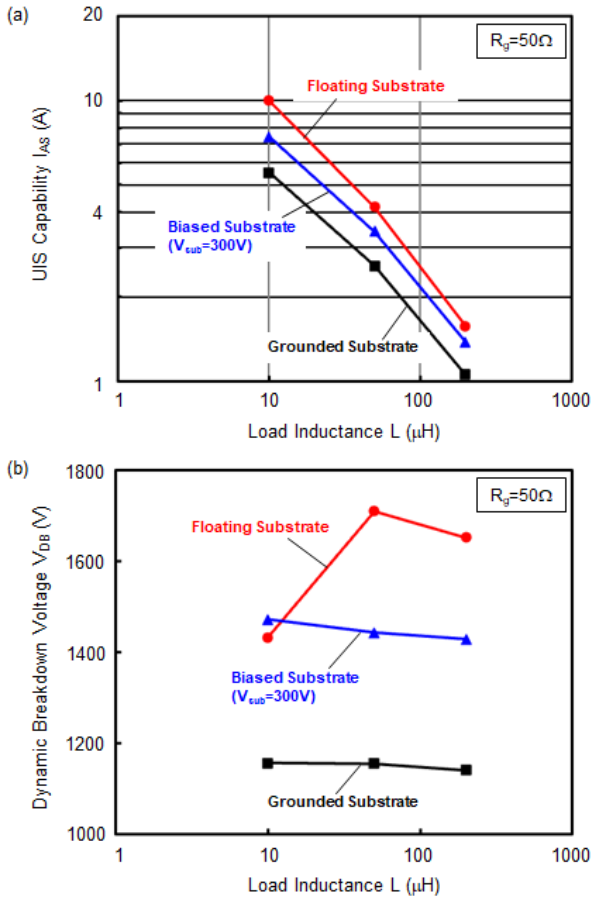

Fig. 8 (a) Relationship between UIS capability and load inductance and (b) relationship between dynamic breakdown voltage and load inductance as a function of substrate electrical condition.

vertical electric field between the drain and the substrate, which is caused by the positive bias on the substrate. The charging energy of the output capacitance C_{oss} increases with the positive bias on the substrate.

On the other hand, the energy E_{AS} stored in the load inductance L during UIS is expressed as follows.

$$E_{AS} \approx \frac{1}{2} L {I_{AS}}^2. \qquad (2)$$

As shown in Fig. 1(a), the power supply is connected during the UIS. However, since the power supply voltage V_{DC} is sufficiently small at 50 V compared to the dynamic breakdown voltage V_{DB}, the energy injected from the power supply during the UIS is negligibly small. Therefore, it can be approximated as shown in Eq. (2). From Eqs. (1) and (2), when E_{AS} equals E_{oss}, the UIS capability I_{AS} is expressed as:

$$I_{AS} \propto V_{DB}. \qquad (3)$$

Fig. 7 shows the relationship between V_{DB} and I_{AS}, when the electrical condition of the substrate is varied. As shown in Eq. (3), I_{AS} is proportional to V_{DB}. This verifies that E_{AS} is equal to E_{OSS} and the energy dissipation due to avalanche breakdown is negligibly small.

This trend was also confirmed from the dependence of UIS capability on load inductance. By varying the load inductance, the relationship between the UIS test current, dynamic breakdown voltage, and UIS capability is evaluated. The

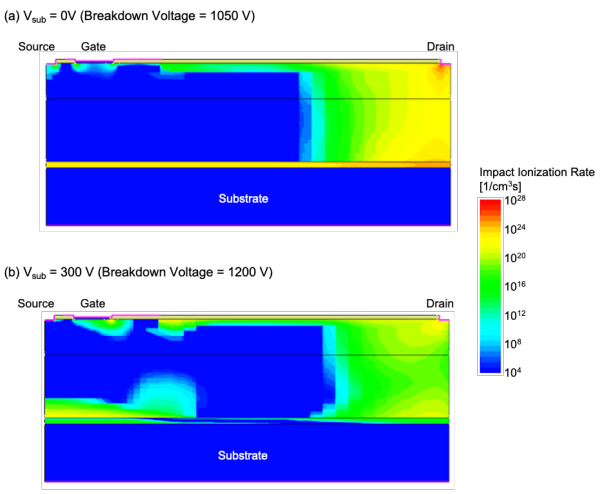

Fig. 9 Impact ionization rate distribution in a GaN-HEMT under avalanche breakdown at (a) V_{sub} = 0 V and (b) V_{sub} = 300 V.

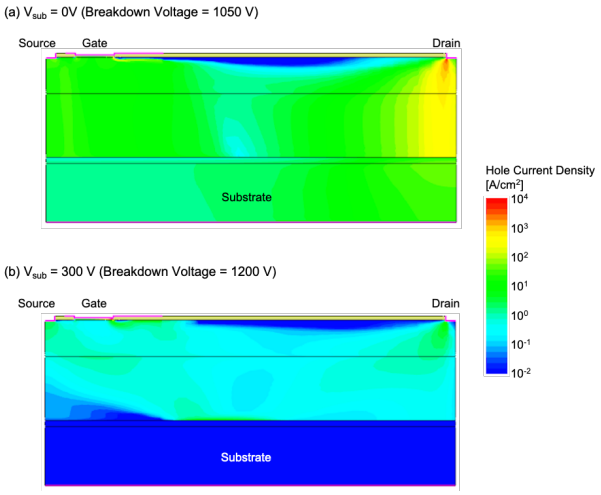

Fig.10 Hole current distribution in a GaN-HEMT under avalanche breakdown at (a) V_{sub} = 0 V and (b) V_{sub} = 300 V.

relationship between UIS capability and load inductance is shown in Fig. 8(a). If the UIS energy E_{AS} is constant, then from Eq. (2), the I_{AS} is given by

$$I_{AS} \propto L^{-\frac{1}{2}}. \quad (4)$$

Since the slope in the log-log plot of Fig. 8(a) is approximately -1/2, it is verified that E_{AS} is constant. Furthermore, as shown in Fig. 8(b), the dynamic breakdown voltage V_{DB} remains almost constant even when the load inductance L is varied. This verifies that E_{oss} remains almost constant. These results further confirm that E_{AS} is equal to E_{OSS} and the energy dissipation due to avalanche breakdown is negligibly small. Although the voltage pulse width is about 500 ns at a load inductance of 200 μH, the duration of avalanche breakdown is only a few nanoseconds, because it occurs only near the voltage peak.

In the substrate floating condition, V_{DB} decreases when the load inductance is small. This is thought to be due to the reduction in UIS energy caused by the increase in I_{AS}, which in turn increases the hole current flowing into the gate, accelerating the dielectric breakdown of the AlGaN layer.

In the case of a grounded substrate, the failure position was located between the drain and the substrate, whereas with substrate biasing or floating, the failure position shifted to the gate. The change in the failure location was investigated based on the variation in electrical characteristics before and after the UIS test. In the case of a grounded substrate, the D-S junction becomes short-circuited after failure, while the G-S junction remains unchanged. In contrast, under substrate biasing or floating conditions, the G-S junction becomes short-circuited after failure. These results also suggest a shift in the failure location. In the case of D-S junction failure, cross-sectional SEM observation revealed damage at the heterojunction between the drain and the substrate [17]. Under substrate biasing or floating conditions, the failure marks were significantly larger; therefore, cross-sectional analysis was not conducted.

In other words, the failure position changes as the hole current path varies depending on the electrical condition of the substrate. These results suggest that the UIS capability is not determined solely by E_{oss} but is also influenced by carrier generation from impact ionization.

The reduction in hole current flowing between the drain and the substrate due to changes in the substrate voltage suppresses the impact ionization of the vertical heteroepitaxial layer, causing the AlGaN layer to break down instead due to the hole current flowing into the gate. In other words, the hole current resulting from impact ionization and the dielectric breakdown of the heteroepitaxial layers ultimately determine the UIS capability.

The effect of substrate bias on impact ionization was analyzed using TCAD simulation. Sentaurus Device from Synopsys was used for the TCAD simulation [19]. Since reproducing the UIS condition involves complexities such as calibrating the time constants of traps, this simulation focused on the analysis of the static breakdown voltage. A drain voltage was applied at the gate- source voltage of 0 V. The results comparing substrate voltages of 0 V and 300 V are shown in Figs. 9 and 10. When the substrate voltage was 0 V, the static breakdown voltage was 1050 V, which matches the measured value [20]. Increasing the substrate voltage to 300 V raised the static breakdown voltage to 1200 V. As shown in Fig. 9, increasing the substrate voltage to 300 V reduced the impact ionization rate at the drain electrode edge, while increasing it at the gate electrode edge. In the simulation results, although the breakdown voltage increased with the application of substrate bias, the regions where impact ionization primarily occurred remained at the edge of the drain electrode. However, the influence of electrons generated by the increased impact ionization near the gate cannot be fully evaluated through simulation.

Accordingly, a burst UIS test was conducted to verify carrier generation induced by overvoltage stress. Fig. 11 shows the results of the burst UIS test at V_{sub} = 300 V. The test conditions were identical to those in the previous experiment [17]. As in the case where the substrate was connected to the source [17], device failure was observed during burst UIS operation when the same stress was repeatedly applied. With substrate bias, the failure location was at the gate, consistent with the results of the

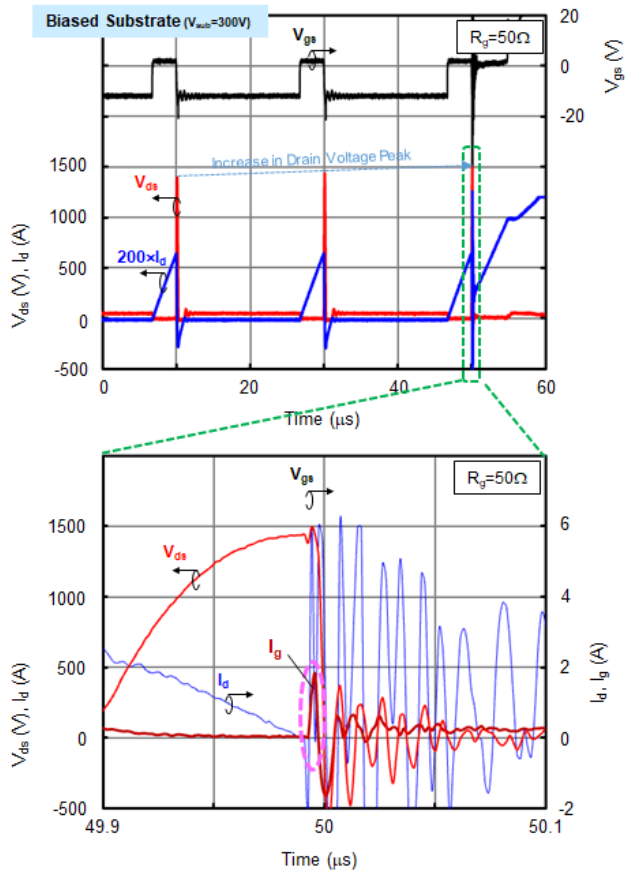

Fig. 11 Burst UIS waveform of biased substrate (V_{sub}=300V) and zoomed waveform at device failure by gate current spike generate by impact ionization.

single UIS test.

In the UIS test, the drain current is determined by the pulse width of the on-state, so the test current in the burst UIS remains unchanged. The drain voltage peak is determined by the extension of the depletion layer and the electric field in the device. If a portion of the holes generated by impact ionization are trapped near the drain, this mitigates the electric field concentration at the drain electrode edge, thereby suppressing impact ionization and increasing the dynamic breakdown voltage. This mechanism is considered responsible for the peak voltage increase observed in the burst UIS waveform. In the burst UIS test with the substrate grounded, increases in both C_{ds} and the peak voltage have been observed, and hole trapping has been verified [17]. Our measurement equipment does not support four-terminal configurations, making such measurements impossible under biased substrate conditions. Nevertheless, in the burst UIS waveform under biased substrate conditions as well, a gradual increase in the drain voltage peak was observed. This is presumed to indicate an increase in dynamic breakdown voltage due to the accumulation of positive charge caused by hole trapping near the drain.

During the off-state of the UIS test, the gate voltage is applied at -10 V, and the channel is turned off, resulting in a small channel leakage current. The main current is the displacement current caused by the extension of the depletion layer. Therefore, it is unlikely that hole accumulation reduces

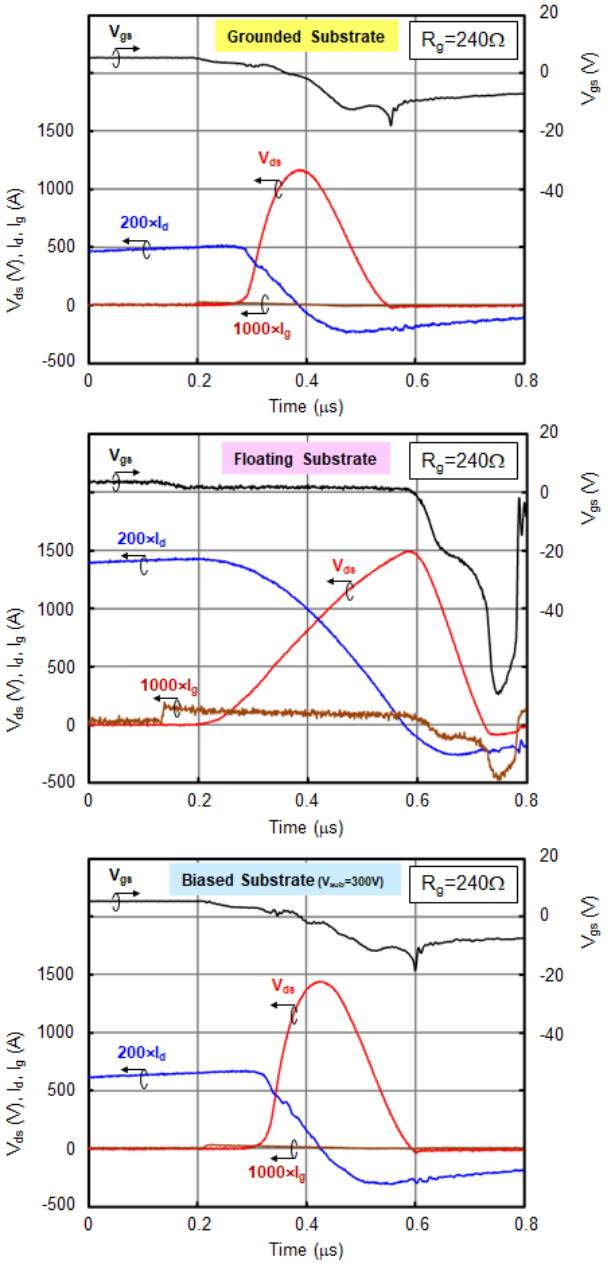

Fig. 12 UIS waveforms at R_g = 240 Ω and L = 50 μH as a function of substrate electrical condition.

the potential barrier and increases electron leakage current. If electrons generated by impact ionization significantly contributed to the failure, a reduction in dynamic breakdown voltage due to electron trapping would be expected, because the accumulation of negative charge mitigates the electric field concentration at the p-GaN gate edge and enhances electric field concentration at the drain electrode edge. However, the experimental results showed an increase in dynamic breakdown voltage. From these results, it is difficult to explain the experimental results by any mechanism other than the hole current generated by impact ionization.

By varying the external gate resistance, the changes in dynamic breakdown voltage and UIS capability due to variations in the gate discharge current are shown. When the external gate resistance is increased, a unique UIS waveform

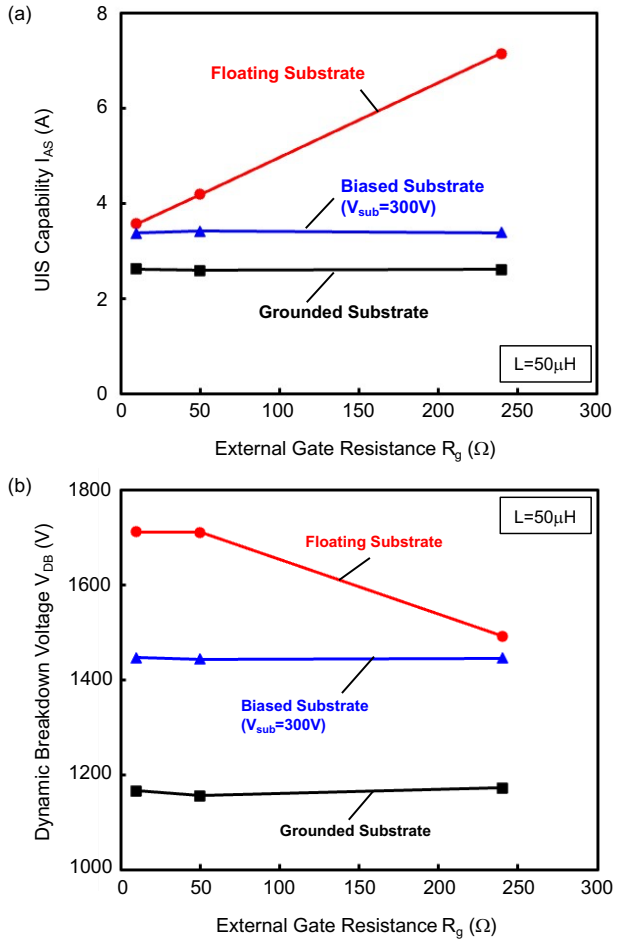

Fig. 13 (a) Relationship between UIS capability and external gate resistance and (b) relationship between dynamic breakdown voltage and external gate resistance as a function of substrate electrical condition.

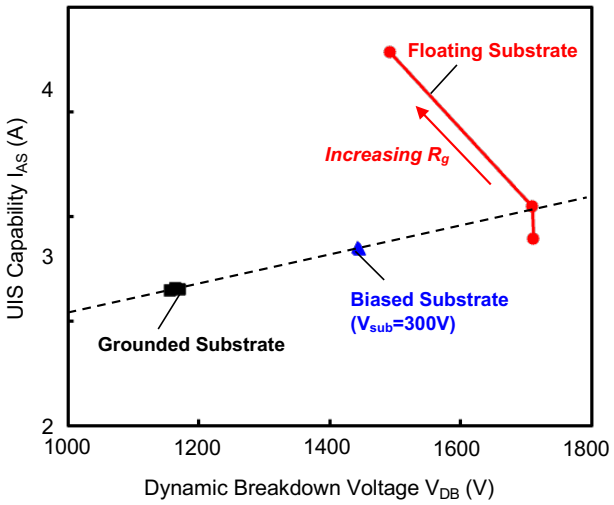

Fig. 14 Relationship between UIS capability and dynamic breakdown voltage depended on external gate resistance.

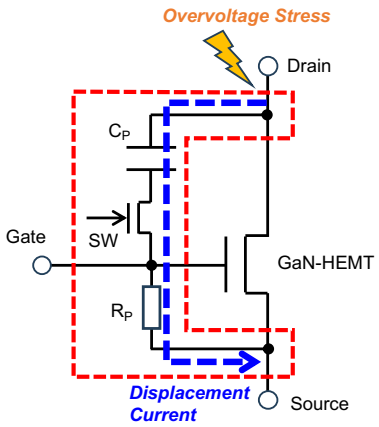

Fig. 15 An example of protect circuit for overvoltage stress.

can be observed under substrate floating conditions. Fig. 12 shows the UIS waveform before failure with a gate resistance of R_g = 240 Ω. The UIS waveform depends on the electrical condition of the substrate, with similar waveforms seen in grounded substrate and biased substrate. In contrast, under substrate floating, a large gate current flows, and the gate voltage is clamped near V_{th} due to the voltage drop caused by the gate resistance. As a result, a Miller period is observed, during which the drain voltage rises in a semi-on state. When the drain voltage passes its peak and begins to decrease, the gate current becomes negative, and the gate voltage drops significantly into the negative range.

The cause of such changes in the UIS waveform is due to differences in the feedback capacitance C_{gd}. As shown in Fig. 2, when the substrate is floating, the shielding effect of the substrate is lost, causing C_{gd} at high drain voltages to become approximately 20 times larger than when the substrate is grounded. This larger C_{gd} results in a greater displacement current flowing when the drain voltage changes, and the voltage drop across the gate resistance prevents the gate voltage from decreasing. As a result, during the rise of the drain voltage, the device enters a semi-on state, and the dV/dt slows down.

A similar waveform has been observed in the UIS waveform of SiC-JFETs [21]-[23], however, in that case, the primary cause of the gate current is the hole current generated by impact ionization. If a large hole current were also generated by impact ionization in GaN-HEMTs, the waveform of grounded or biased substrate conditions would be similar to that of a floating substrate. However, in the grounded and biased substrate conditions, neither a long Miller period nor a slowed dV/dt is observed. Therefore, the change in the UIS waveform of the floating substrate is attributed to the displacement current flowing through the large C_{gd}.

Fig. 13 shows the relationship between UIS capability and external gate resistance. In the grounded and biased substrate conditions, UIS capability is independent of the gate resistance, while in the floating substrate condition, it is highly dependent on the gate resistance. This suggests that the mechanisms determining UIS capability differ. In the grounded and biased substrate conditions, UIS capability is primarily determined by E_{oss}. Therefore, even if dV/dt changes slightly due to the gate resistance, UIS capability remains constant. In contrast, under the floating substrate condition, dV/dt is smaller compared to grounded and biased substrates, resulting in a longer time for the drain voltage to reach its peak, during which energy is consumed in the semi-on state. Increasing the gate resistance further slows down dV/dt, leading to a greater amount of energy

consumed in the semi-on state, which in turn increases UIS capability.

The mechanisms determining UIS capability are different, which causes the relationship between UIS capability and dynamic breakdown voltage to vary depending on the electrical condition of the substrate, as shown in Fig. 14. In grounded and biased substrate conditions, UIS capability is determined by E_{oss}, regardless of the gate resistance. Therefore, similar to Fig. 7, UIS capability is proportional to the dynamic breakdown voltage. However, under floating substrate conditions, as the gate resistance increases, energy consumption in the semi-on state is enhanced. Consequently, even if UIS capability increases, the dynamic breakdown voltage decreases.

Increasing gate resistance slows down switching, significantly undermining the advantages of GaN-HEMTs for high-speed switching operations. Therefore, it is not suitable for high-efficiency operation in power electronics applications. However, it can be utilized as a protective circuit when overvoltage is applied while the application circuit is not in operation. For example, as shown in Fig. 15, an additional circuit is enclosed in a red dashed line. When the application circuit is operational, the auxiliary switch *SW* can be turned off, making the additional feedback capacitance C_P negligible. However, when the application circuit is not operating, keeping *SW* in the on-state increases the feedback capacitance due to C_P. If an overvoltage is applied, a large displacement current flows through C_P, resulting in a voltage drop across the external resistor R_P, causing the circuit to enter a semi-on state. This enables energy consumption and helps prevent failure of the GaN-HEMT.

V. Conclusion

UIS capabilities of ohmic p-gate GaN-HEMTs with various substrate bias conditions were measured. UIS capability of ohmic p-gate GaN-HEMTs can be improved by floating or positive biased substrate condition due to modulation of hole current path. These results suggest that the UIS capability is not determined solely by E_{oss} but is also influenced by carrier generation from impact ionization. The hole current from impact ionization and the dielectric breakdown of the heteroepitaxial layers ultimately determine the UIS capability. Additionally, increasing the gate resistance in floating substrate condition slows down *dV/dt*, leading to a greater amount of energy consumed in the semi-on state, which in turn increases UIS capability.

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