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Dependence of UIS Capability in GaN HEMTs on Substrate Bias and p-Gate Contacts

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***Abstract*—Unclamped inductive switching (UIS) capabilities of GaN-HEMTs with various substrate bias and p-gate contact conditions were measured. One of the critical disadvantages of GaN-HEMTs is their ultra-low UIS capability, due to the lack of a structure for removing holes generated by the avalanche breakdown. Therefore, failure location by overvoltage stress strongly depends on the current path of holes generated by avalanche breakdown. This paper reports that UIS capability of ohmic p-gate GaN-HEMTs can be improved by substrate bias through modulation of hole current path. However, Schottky p-gate GaN-HEMTs show no dependence on substrate bias due to low charge-to-breakdown of the gate structure.**

Keywords—GaN-HEMT, UIS capability, avalanche breakdown

I. Introduction

GaN-HEMTs are being rapidly adopted in power electronics applications [1]. However, GaN-HEMTs have little to no avalanche-withstanding capability; their breakdown, induced by the peak electric field in GaN, usually results in catastrophic failure [2]-[3]. Therefore, commercial GaN-HEMTs are designed with a breakdown voltage much higher than the rated voltage to provide a large overvoltage margin in converter applications [4].

For reliability design in GaN-HEMTs, the effects of dynamic breakdown voltage and degradation behavior due to overvoltage stress have been investigated [5]-[6]. The failure of GaN-HEMTs due to overvoltage stress is characterized by catastrophic failure and time-dependent breakdown [7]-[8]. As a result, it seems that the breakdown occurs in the insulating layers, such as passivation films, rather than in the semiconductor layers of AlGaN/GaN heterostructures. However, previous experimental studies have found that holes are generated due to avalanche breakdown, and the failure location is determined by the path of the hole current.

The ease of hole removal determines the location of the breakdown. When hole removal from the gate through the p-GaN layer is possible due to ohmic contacts, the breakdown occurs through vertical hole removal, leading to the destruction of the heterostructure between the drain and the silicon substrate. In contrast, when hole removal from the gate through Schottky contacts, the AlGaN barrier layer beneath the gate breaks down [8]. Based on these results, it is anticipated that improving hole removal during avalanche breakdown will enhance unclamped inductive switching (UIS) capability.

This paper reports the results of investigating changes in UIS capability by modulating hole removal flowing from the drain toward the silicon substrate via substrate bias. The effect of substrate bias on UIS capability is compared between ohmic and Schottky p-gates.

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II. Experiment Setup

To modulate the path of the hole current generated by avalanche breakdown, the substrate bias V_{sub} was adjusted using a DC power supply, as shown in Fig. 1. At V_{sub} = 0 V, the silicon substrate is connected to the source, and during avalanche breakdown, the substrate current I_{sub} flows from the drain to the silicon substrate due to the vertical electric field, while the gate current I_g flows to the gate due to the lateral electric field. When the applied V_{sub} is negative, the vertical electric field decreases, reducing I_{sub} and promoting the flow of I_g.

To investigate hole removal from the gate, the p-gate contact was also focused on. 600V-class ohmic p-gate GaN-HEMTs (Infineon IGLD60R070D1) [9] and 200V-class Schottky p-gate GaN-HEMTs (EPC 2010C) [10] were tested, and a summary of devices are shown in Table I.

In this experiment, drain and gate voltages were measured using passive voltage probes, while drain, gate and substrate currents were measured using current transformers. Failure processes during the UIS were observed with an oscilloscope to clarify the stress conditions at the failure. The

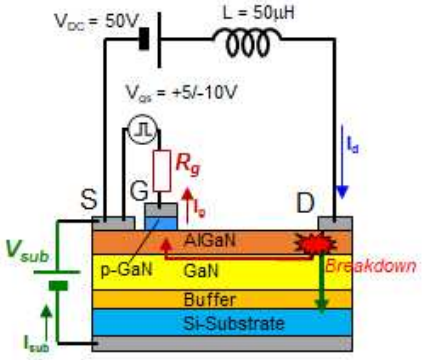

Fig.1 Test circuit of unclamped inductive switching (UIS).

Table I Summary of comparison between ohmic and Schottky p-gate GaN-HEMTs in UIS test at V_{sub} = 0V.

p-Gate Type	Ohmic	Schottky
Rating Voltage	600 V	200 V
Rating Current	15 A	22 A
Dynamic Breakdown Voltage	1150-1180 V	540-580 V
UIS Robustness	2.6 A	1.5-1.7 A
Failure Condition	Drain Failure	Gate Failure

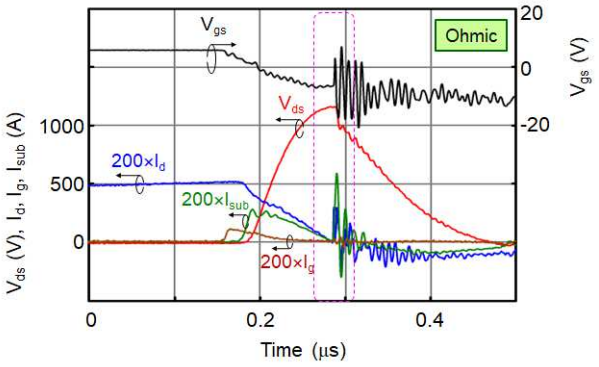

Fig. 2 Typical UIS waveform of ohmic p-gate GaN-HEMT under V_{sub} = 0 V at failure showing substrate current I_{sub} spike.

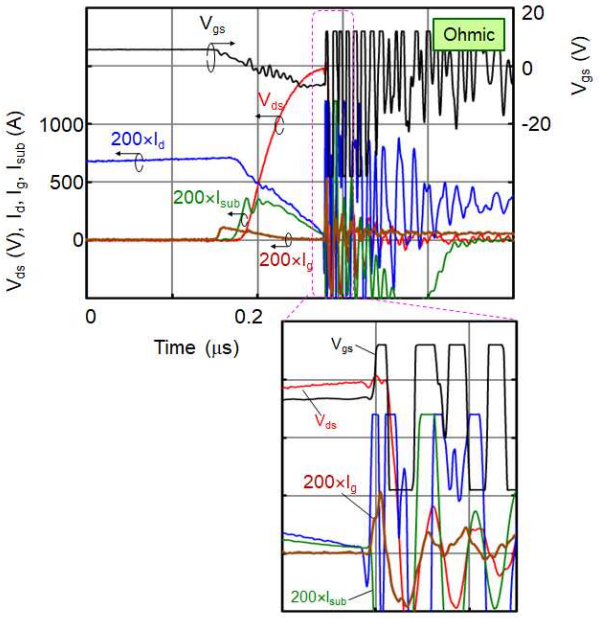

Fig. 3 Typical UIS waveform of ohmic p-gate GaN-HEMT under V_{sub} = −300 V at failure and its zoomed waveform showing gate current I_g spike.

influence of gate current stress before the UIS was also studied to discuss the effects of the crystal defects increased by hole current flow.

III. UIS Waveforms

A. Ohmic p-Gate Devices

Fig. 2 shows the UIS waveform at failure with V_{sub} = 0 V. Breakdown occurred at the peak drain voltage, and a rapid drop in V_{ds} was observed. At this moment, a pulse was generated in I_{sub}; however, there was no sudden increase in I_g. It was confirmed that the D-S junction was damaged, while the G-S junction remained intact. From these results, it is concluded that with V_{sub} = 0 V, the heteroepitaxial layers were destroyed by the hole current flowing between the drain and the substrate, caused by the vertical electric field.

The failure mode is altered by the substrate bias, which decreases I_{sub}. Fig. 3 shows the UIS waveform at failure with V_{sub} = −300 V. A pulse was generated in I_g before the rapid drop in V_{ds} occurred due to breakdown, resulting in a short-circuit condition at the gate. The reduction of I_{sub} due to the substrate bias suppressed damage in the heteroepitaxial

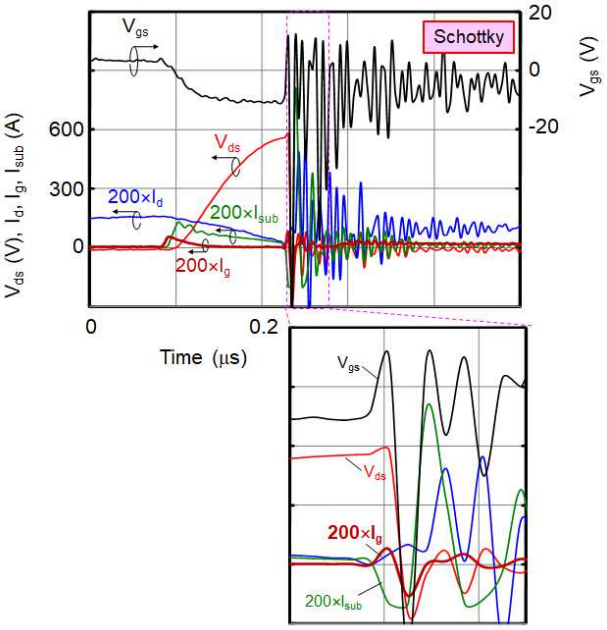

Fig. 4 Typical UIS waveform of Schottly p-gate GaN-HEMT under V_{sub} = 0 V at failure and its zoomed waveform showing gate current I_g spike.

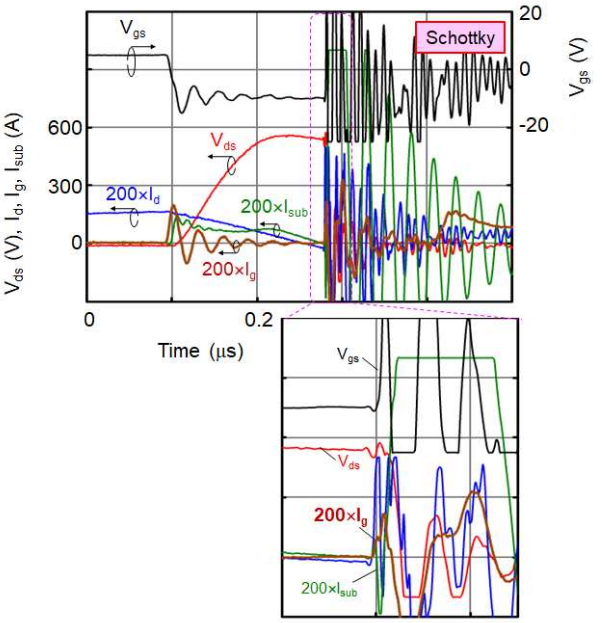

Fig. 5 Typical UIS waveform of Schottly p-gate GaN-HEMT under V_{sub} = 100 V at failure and its zoomed waveform showing gate current I_g spike.

layers between the drain and the substrate. However, as I_g increased, the AlGaN layer beneath the gate electrode was destroyed, leading to a short circuit at the gate. These results indicate that the substrate bias alters the path of the hole current generated by avalanche breakdown, leading to a change in the failure position.

B. Schottly p-Gate Devices

Fig. 4 shows the UIS waveform at failure under V_{sub} = 0 V. Similar to the ohmic p-gate device, breakdown occurs at the peak of the drain voltage. During breakdown, the gate current increases, but the substrate current does not, suggesting that the AlGaN layer beneath the gate electrode is damaged.

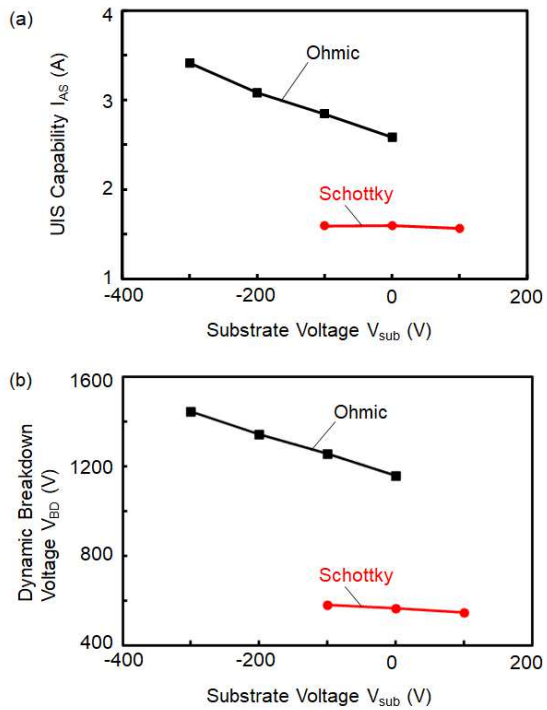

Fig.6 Substrate bias dependence of (a) UIS capability and (b) dynamic breakdown voltage.

In the Schottky p-gate device, the failure mode did not change even when the substrate bias was varied. Fig. 5 shows the UIS waveform at the failure under V_{sub} = 100 V. When a positive V_{sub} was applied, it was expected that the substrate current I_{sub} would increase, and the failure position would shift from beneath the gate electrode to the drain-substrate region. However, gate current flowed during breakdown, and the failure position did not change. It is verified that, in the Schottky p-gate device, the difficulty of hole removal from the gate is the bottleneck limiting UIS capability.

IV. Discussions

Fig. 6 shows the substrate bias dependence of UIS capability and dynamic breakdown voltage. In the ohmic p-gate device, applying a negative V_{sub} increased the UIS capability. This is because the negative V_{sub} weakened the vertical electric field between the drain and substrate, and the dynamic breakdown voltage increased, as shown in Fig. 6(b). Therefore, the energy stored in the output capacitance increased with the dynamic breakdown voltage, and the UIS capability improved. Furthermore, as the horizontal electric field between the drain and gate became stronger than the vertical electric field between the drain and substrate, the hole current generated by avalanche breakdown flowed more easily in the horizontal direction, causing the failure position to shift from the drain-substrate region to beneath the gate.

On the other hand, in the Schottky p-gate device, both UIS capability and dynamic breakdown voltage showed little dependence on the substrate bias. Even when the vertical electric field was increased through substrate bias to enhance the hole current from avalanche breakdown in the vertical direction, the difficulty of hole removal from the gate remained the bottleneck and determined the UIS capability.

To modulate hole removal from the gate, UIS capability was measured while varying external gate resistance. As

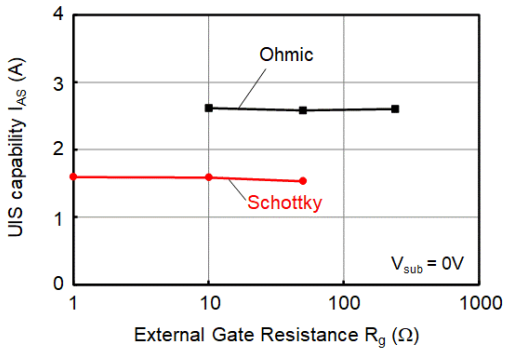

Fig.7 External gate resistance dependence of UIS capability.

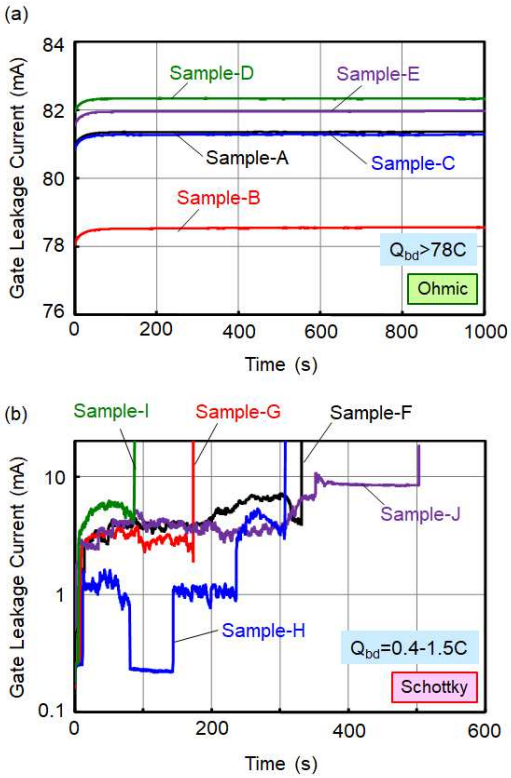

Fig.8 Time-dependent change in gate current under a forward voltage for (a) ohmic p-gate devices and (b) Schottky p-gate devices.

shown in Fig. 7, UIS capability did not change with the gate resistance. In the case of the ohmic p-gate device, it is reasonable that UIS capability does not depend on the gate resistance, considering it is determined by hole removal between the drain and substrate. However, the fact that the Schottky p-gate device also shows no dependence on gate resistance. It suggests that hole removal is restricted by factors other than the gate resistance. Specifically, it is likely that UIS capability is determined by the inhibition of hole removal due to the high resistance of the p-GaN layer or the band discontinuity in the AlGaN/GaN heterostructure.

The robustness under gate current conduction was compared between the ohmic p-gate device and the Schottky p-gate device. Fig. 8 shows the time-dependent change in gate current when a forward voltage was applied to the gate to positively inject holes. In the ohmic p-gate device, no breakdown occurred even with a sustained current of approximately 80 mA. In contrast, the Schottky p-gate device experienced breakdown when the total charge passed reached about 1 C, even though the initial leakage current was small. These results suggest that, in the Schottky p-gate

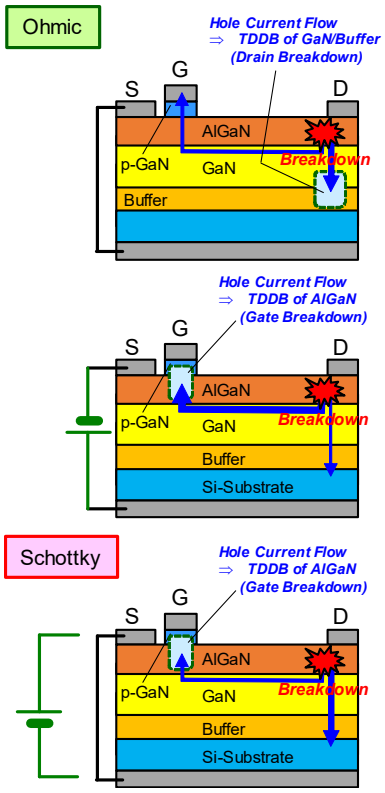

Fig.9 Failure mechanism of ohmic p-gate GaN-HEMTs and Schottky p-gate GaN-HEMTs.

device, the breakdown of the AlGaN layer was caused by the flow of hole current.

Compared to the Schottky p-gate device, the ohmic p-gate device has higher robustness against hole current. However, when UIS capability is increased through substrate bias, gate breakdown occurs. In addition, as shown in Fig. 6, the improvement in UIS capability due to substrate bias is linked to an increase in dynamic breakdown voltage. In other words, even though UIS capability improves with substrate bias, it is determined by the charging energy of the output capacitance, and the energy consumption due to avalanche current is small. These results indicate that, even in the ohmic p-gate device, hole removal from the gate is the bottleneck determining UIS capability.

Based on the above results, as illustrated in Fig. 9, the path of the hole current responsible for failure differs between the ohmic p-gate device and the Schottky p-gate device. In the ohmic p-gate device, UIS capability can be improved by suppressing hole current between the drain and substrate. However, the bottleneck limiting UIS capability, as in the Schottky p-gate device, is the difficulty of hole removal from the gate. Therefore, to enhance UIS capability, it is necessary to both relax the vertical electric field and improve hole removal from the gate.

V. Conclusions

UIS capabilities of GaN-HEMTs with various substrate biases and p-gate contact conditions were measured. The UIS capability of ohmic p-gate GaN-HEMTs can be improved by substrate bias due to the modulation of hole current path, and the failure position shifts from the drain-substrate region to beneath the gate. However, Schottky p-gate GaN-HEMTs show no dependence on substrate bias due to low charge-to-breakdown of the gate structure. Even in the ohmic p-gate device, where hole removal from the gate is the bottleneck determining UIS capability, it is necessary to both relax the vertical electric field and enhance hole removal from the gate.

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