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Paper

Thermoelectric Infrared Sensors with High Responsivity for Automotive Applications

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This paper presents the structure and fabrication process of a thermoelectric infrared sensor that provides high responsivity and a low cost potential. The processes for obtaining a precisely patterned Au-black infrared absorbing layer and reducing the internal stress of the Si_3N_4 layer deposited by LP-CVD achieve both high responsivity and an excellent time constant. A prototype sensor, having external dimensions of 160 μm x 160 μm and six pairs of thermopiles, achieved responsivity of 2100 V/W and a time constant of 25 msec at a pressure of 7.33 Pa. This performance is suitable for automotive applications.

Keywords: *infrared sensors, thermopiles, thermoelectric, vehicles, and Au -black*

1. Introduction

Reduced visibility at night drastically limits the amount of information that drivers can obtain visually. Therefore, the rate of nighttime fatal accidents is much higher than the daytime rate.

Infrared (IR) technology has been used in military applications, including night vision systems for reconnaissance and missile seeking, because of its capability for detecting hot bodies over a wide area both day and night. National security considerations and high costs have tended to prevent this technology from spreading to general applications. Examples of proposed applications to vehicles can be seen in the Advanced Safety Vehicle (ASV) Project in Japan [1].

A particularly important aspect of infrared technology in recent years has been its potential for use as a detection technique. The cooled infrared detectors that were used previously were not suitable for vehicle applications, largely because of their high price and limited lifetime of the cooling system. As a result of the advances achieved in semiconductor technology, thermal infrared detectors have been developed in recent years that make use of phase transition as in resistive or ferroelectric bolometric mode to achieve exceptionally high performance [2,3]. These thermal infrared detectors have now advanced to the point where their performance is nearly comparable to that of their cooled counterparts. However, there are various factors that make it difficult to achieve low-cost uncooled detectors. For instance, infrared detectors that make use of phase transition require precise temperature adjustment in the vicinity of the phase transition temperature, which necessitates the use of an add-on device such as a Peltier thermoelectric cooler. Another reason is that a pyroelectric sensor invariably has to be fabricated with a hybrid construction. Further cost reductions are necessary if thermal infrared sensors are to find widespread use on mass-produced vehicles. Toward that end, it is necessary to achieve a monolithic focal plane array (FPA) that would reduce the number of operations in the device fabrication process as much as possible, while still ensuring compatibility with the widely used CMOS process.

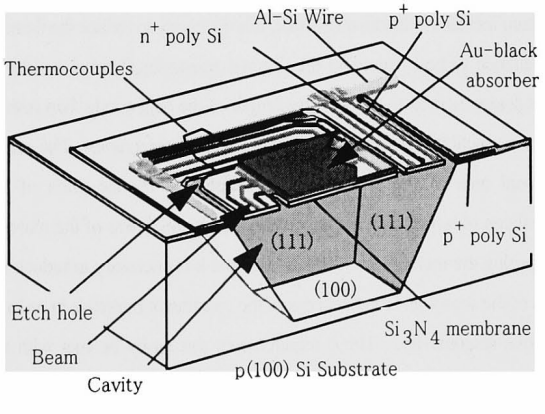

Figure 1. Cross-sectional view of a prototype sensor.

Among different types of thermal infrared sensors [4]~[10], the thermopile [8,10] is the most promising infrared FPA for automotive use because of its low cost potential and the fact that its electromotive force nature allows easy design of the latter-stage amplifier circuit. The performance of thermopiles is not necessarily sufficient for vehicle applications at present, and further improvement will require better thermal isolation of the hot and cold junctions, a higher fill factor and higher infrared absorptivity.

Long and narrow beams supporting the absorber are necessary to improve thermal isolation between hot and cold junctions. These beams tend to be influenced by the internal stress of the thin films of which they are composed. Moreover, to improve the fill factor, an asymmetric sensor layout pattern using curved beams is needed, making the beams more susceptible to the influence of internal stress. We adopted a Si^+ ion implantation technique to control the mechanical properties of the Si_3N_4 layer.

This paper first presents the structure of a prototype sensor that reconciles thermopile responsivity with the time constant. It then describes the structure, fabrication process, which features control of the mechanical properties of the Si_3N_4 layer by an ion implantation technique and a precisely patterned Au-black layer fabricated by the lift-off technique, and measured performance data of the prototype sensor.

2. Device Structure

Thermopile responsivity R and the time constant τ are given by

$$R = n \cdot \alpha \cdot R_{th} \cdot \eta \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

$$\tau \propto C_{th} \cdot R_{th} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

where n is the number of thermocouple pairs, α is the Seebeck coefficient, R_{th} is the thermal resistance between the hot and cold junctions, η is infrared radiation absorptivity and C_{th} is the thermal capacitance of the thermopiles.

Accordingly, in order to improve responsivity while holding down the resultant increase in the time constant, it is necessary to reduce the thermal capacitance without changing the thermal resistance.Thermal resistance R_{th} is determined by the ratio of the length of the heat conduction path to the cross-sectional area of the thermopiles and membrane. The cross-sectional area of the thermopiles is determined by the pitch of the polysilicon of which they are composed and the thickness of the material composing the membrane. This means that it is necessary to reduce the pitch of the sensor and the thickness of the constituent materials in order to improve responsivity. These requirements can easily be met with the CMOS process.

The cross-sectional structure of the prototype sensor is shown in Figure 1 and a Scanning Electron Microscope (SEM) micrograph of the sensor is shown in Figure 2. The prototype sensor has six pairs of thermocouples consisting of alternating areas of p-type and n-type polysilicon connected in series by the Al–Si wiring layer.

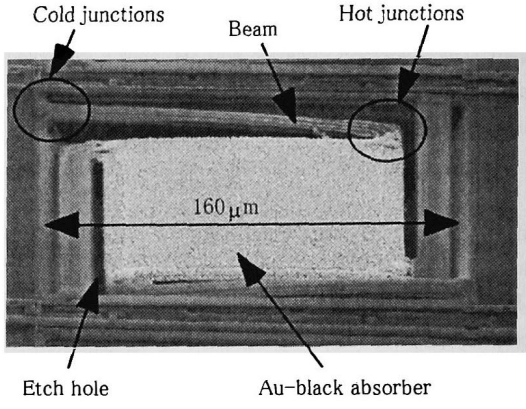

Figure 2. SEM micrograph of a prototype sensor.

The sensing area was thermally isolated from the Si substrate and supported by four beams having a length of 119 μm. The layer structure of the membrane from bottom to top consisted of a Si_3N_4 layer, thermopiles, first isolation layer, first Al - Si wiring layer, second isolation layer, amorphous Si (a-Si) layer, and the Au-black layer. The hot junctions of each thermocouple were positioned near the edge of the IR absorber and the cold junctions were located on the Si substrate. The thickness of each layer is given in Table 1.

The dimensions of the device are as follows: the total area of the device is 160 μm x 160 μm, the Au black absorber measures 116 μm x 116 μm, and the thermopiles have a length of 119 μm, a width of 0.8 μm, and a pitch of 3μm. The internal resistance of the device is 116 kΩ.

3. Fabrication Process

The prototype sensor was produced in a fabrication process consisting of the ordinary CMOS process and four special processes. The sequence of steps in the sensor fabrication process is shown in Figure 3.

3.1 Control of Internal Stress of Si_3N_4 layer The deposition temperature of the Si_3N_4 layer is 780°C. Because this temperature is higher than that of any other layer making up the prototype sensor, very large internal stress occurs in this layer. Several techniques have been reported for reducing the internal stress of the Si_3N_4 layer, such as by controlling the deposition conditions or by a phosphorus or boron ion implantation method [11]. However, there are no reports concerning

internal stress changes in the later thermal treatment process or insulation resistance of the Si_3N_4 layer. Therefore, we investigated the influence of the later thermal treatment process and the insulation resistance achieved with the ion implantation technique.

Table 1. Materials and thickness of each layer

Layers	Materials	Thickness (nm)
Sacrificial layer	Poly Si	400
Membrane	SiN by LPCVD	100
Thermopiles	Poly Si	350
1st isolation layer	BPSG	600
1st wiring layer	Al-Si	700
2nd isolation layer	P-TEOS	600
Au-black underlay	Amorphous Si	100
3rd isolation layer	PSG	300
2nd wiring layer	Al-Si	800
Passivation layer	SiN by PECVD	300
Sacrificial layer	PSG	2000

Measurement was made of the warpage of the Si substrate following deposition of the Si_3N_4 layer on one side. The internal stress σ of the Si_3N_4 layer was calculated from the measured warpage using equations (3) and (4).

$$R_m = R_b \cdot R_a / (R_b - R_a) \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (3)$$

$$\sigma = (E \cdot h^2) / [6(1-\nu) \cdot R_m \cdot t] \quad \cdots\cdots\cdots\cdots\cdots \quad (4)$$

where R_a is the radius of the Si substrate before deposition, R_b is the radius of the Si substrate after deposition, E is Young's modulus, h is the substrate thickness, ν is Poisson's ratio, and t is the thickness of the deposited layer.

Figure 4 shows that a Si_3N_4 layer without any ion implantation had very large internal stress of σ =1.32 GPa before thermal treatment, but the stress level of an ion-implanted Si_3N_4 layer was smaller than that of non implanted layer. On the other hand, the results indicate internal stress increased after thermal treatment at 950℃ for 30 min. A Si_3N_4 layer implanted with a Si^+ ion dose of 1 x 10^{16} cm^{-2} had a internal stress of σ =0.55 GPa. The dose dependence of internal stress of a Si^+ ion implanted layer is smaller than that of a B^+ ion implanted layer.

The electrical resistance of an ion-implanted Si_3N_4 layer was also measured using the Test Element Group (TEG) shown in Figure 5. Table 2 shows the measured data. The results indicate that the ion implantation technique had no effect on the resistance of the layer.

Taking into consideration these results, we fabricated a prototype sensor having a Si_3N_4 layer implanted with a Si^+ ion dose of 1 x 10^{16} cm^{-2}.

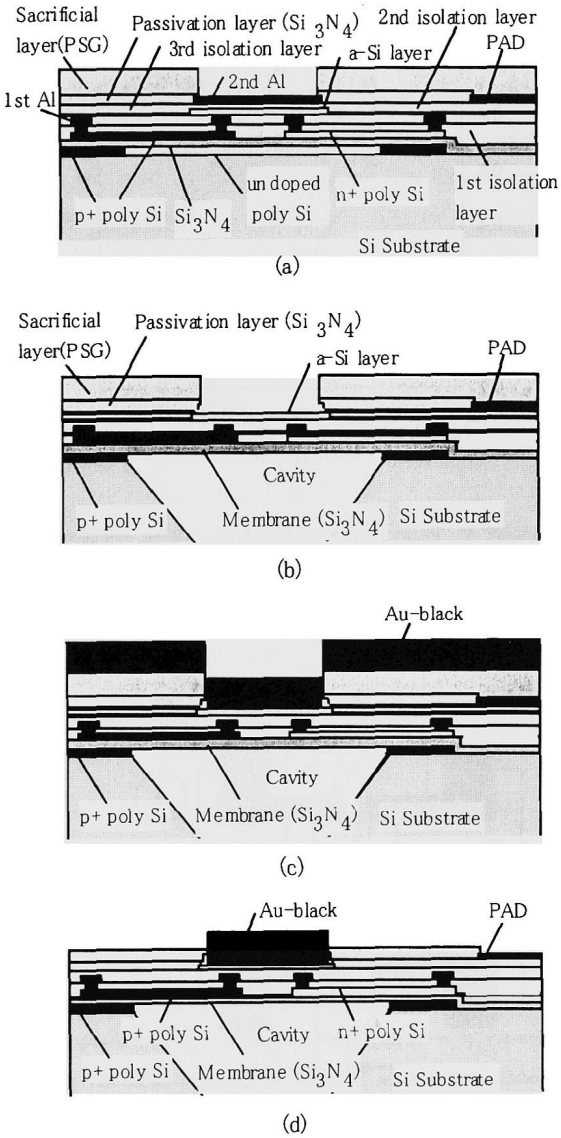

Figure 3. Sensor fabrication process ((a)PSG sacrificial layer formation, (b)Fabrication of thermal isolation structure, (c)Au-black deposition, (d)Lift-off process).

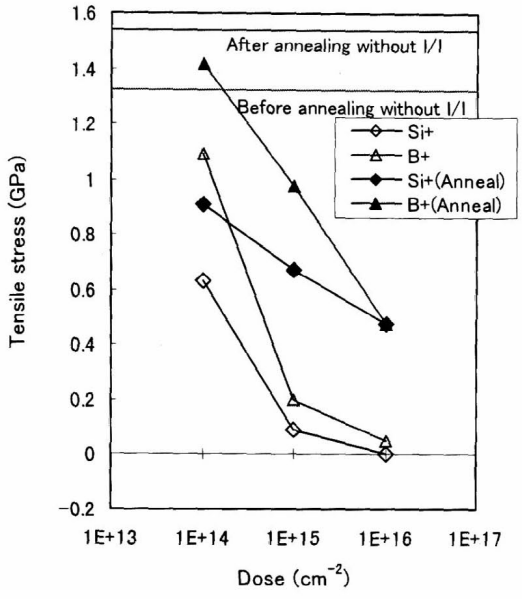

Figure 4. Internal stress of SiN layer versus implantation dose.

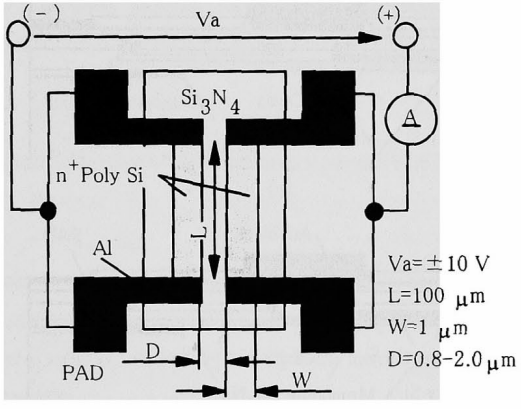

Figure 5. Insulation measurement TEG.

3.2 Fabrication of thermal isolation structure The polysilicon micromachining technique was used to fabricate the membrane structure, since good thermal isolation between the hot and cold junctions is needed to increase thermopile responsivity. Hydrazine, which has good resistivity to SiO_2, was used to etch the p-type (100) Si substrate at an etchant temperature of 80℃. In order to fabricate the membrane structure, it was necessary to under-etch the substrate below the membrane. That was accomplished by using a sacrificial layer of polysilicon [12]. Furthermore, to prevent a level difference from occurring

Table 2 Measured data for insulation test.

Ion	Dose(1/cm2)	D(μm)			
		2.0	1.5	1.0	0.8
-	Non doped	>100	>100	>100	>100
Si	1E14	>100	>100	>100	>100
Si	1E15	>100	>100	>100	>100
Si	1E16	>100	>100	>100	>100
B	1E14	>100	>100	>100	>100
B	1E15	>100	>100	>100	>100
B	1E16	>100	>100	>100	>100

(Resistance(MΩ))

in the polysilicon and Si_3N_4 substrate in the vicinity of the cold junctions, the polysilicon sacrificial layer below these junctions was doped with a high concentration of boron to inhibit the progress of etching. The layer was doped with a boron dose of 1 x 10^{16} cm^{-2} by ion implantation and annealed in a N_2 atmosphere at 950℃ for 20 min., which worked to reduce the etching rate to 1/20 of the undoped rate.

3.3 Fabrication of Au-black layer Resistance-heated vapor deposition was used to fabricate the Au-black layer. The requirements for the Au-black layer are not only good IR absorptivity, but also an excellent patterning characteristic during the lift-off process.

The chamber was first evacuated to 1 x 10^{-2} Pa and then N_2 gas was introduced to the specified pressure. The evacuation system was then disconnected from the chamber and deposition was performed in that condition. At a pressure of 53.0 Pa, gold luster was observed, but when the pressure was raised to 2.66 x 10^2 Pa, Au was deposited as fleecy particles. The Au-black layer showed high absorptivity of more than 90% when illuminated by a light source having a wavelength of 10 μm. The Au-black layer deposited under these conditions exhibited an excellent peeling characteristic in the lift-off process.

3.4 Lift-off process Patterning of the IR absorber was accomplished in the lift-off process by utilizing a PSG sacrificial layer. The process flow of are shown in Figure 3.

As shown in Figure 3 (a), a PSG sacrificial layer is first formed following completion of the ordinary CMOS process. Only the area that becomes the IR absorber is removed in advance. That area is the exposed 2nd wiring layer which is resistant to the hydrazine. Under this condition, anisotropic etching is performed with hydrazine to fabricate the thermal isolation structure.

The next step, as shown in Figure 3 (b), is to remove the second wiring layer and the third isolation layer so as to prevent interaction between the second 2nd wiring layer and the underlying amorphous Si (a-Si) layer. Their sacrificial layers are removed with etchants of H_2SO_4:H_2O_2=1:1 at

80℃ and $NH_4F:CH_3COOH:H_2O$=1:1:1, respectively, to expose the surface of the a-Si layer.

As shown in Figure 3 (c), the Au-black layer is then deposited under a pressure of 2.66 x 10^2 Pa.

Finally, as shown in Figure 3 (d), the PSG sacrificial layer is etched using an etchant of $NH_4F:CH_3COOH:H_2O$=1:1:1 to lift off the Au black from the areas other than the IR absorber. This lift-off process is completed very quickly because the low density of the Au black allows the etchant to permeate this layer.

4. Results and Discussion

The responsivity and time constant of the prototype sensor were measured using the optical and electrical setup shown in Figure 6. A cryostat was evacuated to 7.33 Pa by a rotary pump. The responsivity of the sensor was measured by illuminating it with infrared radiation emitted by a black body furnace at 500K. The time constant was measured by illuminating the sensor with a He-Ne laser beam modulated by an optical chopper. The sensor output signal was first amplified 100 times and then introduced into an oscilloscope to obtain a waveform tracing for evaluating the time constant.

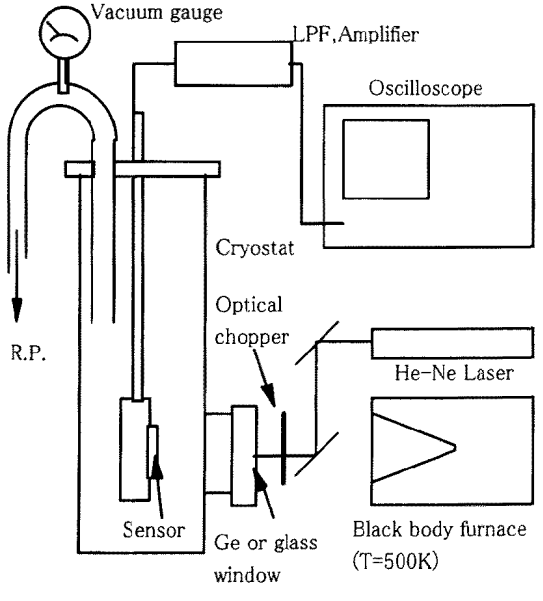

Figure 6. Measurement setup for responsivity and time constant.

The measured results shown in Figure 7 indicate that the responsivity R rose to 2100V/W as a result of reducing the pressure of the cryostat because the thermal conductance via air decreased with the pressure. The time constant τ increased to 25 msec at the same pressure. These values indicate that the sensor provides good performance equal to that of a thermopile. Moreover, the fact that the internal electrical resistance of the sensor was 116 kΩ resulted in small thermal noise and a high S/N ratio [13,14]. The measured time constant is sufficient for taking moving pictures at the standard NTSC frame rate of thirty frames per second.

The prototype sensor displayed both high responsivity and a small time constant because the precise patterning of the infrared absorbing layer provided both small thermal capacitance and large thermal resistance without increasing the time constant.

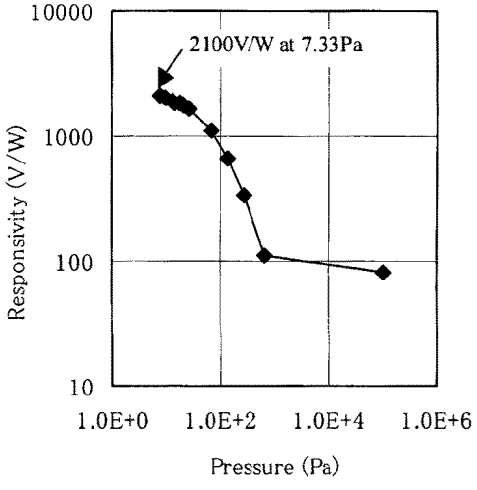

Figure 7. Measured responsivity versus pressure.

5. Summary

This paper has presented the structure of a thermoelectric infrared sensor that provides high responsivity and a small time constant and described fabrication processes for obtaining a precisely patterned Au-black infrared absorbing layer and reducing the thermal stress of the Si_3N_4 layer deposited by LP-CVD. A prototype sensor fabricated with external dimensions of 160 μm x 160 μm and six pairs of thermopiles achieved responsivity of 2100 V/W and a time constant of 25 msec at a pressure of 7.33 Pa. This performance is suitable for automotive applications.

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