Stability, Reliability, and Robustness of GaN Power Devices: A Review

Kozak, Joseph Peter

Zhang, Ruizhe

Porter, Matthew

Song, Qihao

他

出版情報：IEEE Transactions on Power Electronics. 38 (7), pp.8442-8471, 2023-07. Institute of Electrical and Electronics Engineers (IEEE)
バージョン：

Stability, Reliability, and Robustness of GaN Power Devices: A Review

Joseph Peter Kozak, *Member, IEEE*, Ruizhe Zhang, *Graduate Student Member, IEEE*, Matthew Porter, *Student Member, IEEE*, Qihao Song, *Graduate Student Member, IEEE*, Jingcun Liu, Bixuan Wang, *Graduate Student Member, IEEE*, Rudy Wang, *Senior Member, IEEE*, Wataru Saito, *Senior Member, IEEE*, and Yuhao Zhang, *Senior Member, IEEE*

***Abstract*—Gallium nitride (GaN) devices are revolutionarily advancing the efficiency, frequency, and form factor of power electronics. However, the material composition, architecture, and physics of many GaN devices are significantly different from silicon and silicon carbide devices. These distinctions result in many unique stability, reliability, and robustness issues facing GaN power devices. This article reviews the current understanding of these issues, particularly those related to dynamic switching, and their impacts on system performance. Instead of delving into reliability physics, this article intends to provide power electronics' engineers the necessary information for deploying GaN devices in the existing and emerging applications, as well as provide references for the qualification evaluations of GaN power devices. The issues covered in this article include the dynamic instability of device parameters (e.g., ON-resistance, threshold voltage, and output capacitance), the device robustness in avalanche, overvoltage and short-circuit conditions, the device's switching reliability and lifetime, as well as the device's ruggedness under radiation and extreme (cryogenic and elevated) temperatures. Knowledge gaps and immediate research opportunities in the relevant fields are also discussed.**

***Index Terms*—Cryogenic temperature, failure analysis, gallium nitride (GaN), high-electron mobility transistors (HEMTs), JFETs, MOSFETs, power electronics, power semiconductor devices, radiation, reliability, robustness, stability.**

I. Introduction

POWER semiconductor devices are utilized as solid-state switches in power electronics' systems. To date, three power semiconductors have been commercialized, i.e., silicon (Si), silicon carbide (SiC), and gallium nitride (GaN) [1]. As compared with Si and SiC, GaN has superior properties, including the larger bandgap and higher critical electric field. Additionally, the AlGaN/GaN heterostructure forms two-dimensional electron gas (2DEG) with very high mobility, which can be further used to construct the high-electron mobility transistor (HEMT). GaN power HEMTs have been recently commercialized with the voltage classes from 15 to 900 V, and they are seeing rapid adoption in power supplies, data centers, Lidar systems, and fast chargers in consumer electronics [2], [3], [4], [5]. Benefitted from the smaller capacitances and charges, GaN power devices have enabled the lighter, smaller, and more efficient power electronics' systems. The market size of GaN power devices is projected to exceed $1.26 billion by 2027 [5].

While GaN devices are currently being deployed in a variety of applications, there are still open questions to be answered regarding their stability, reliability, and robustness. This is largely because the architecture and physics of GaN HEMTs are very different from Si and SiC devices, such as MOSFETs, JFETs, and insultated gate bipolar transistors (IGBTs). GaN HEMT is a lateral device without p-n junction connected between source and drain, and its current is confined in a two-dimensional channel with a thickness of merely a few nanometers. Additionally, many GaN HEMTs are fabricated on foreign substrates, e.g., Si and sapphire, leading to a higher density of defects and traps as compared with Si and SiC devices built on native substrates.

Extensive efforts in academia and industry are ramping up to address the stability, reliability, and robustness issues facing GaN devices. For example, over 300 and 200 articles have been published on the topics of "GaN reliability" and "GaN power reliability" in the year 2021 according to the Web of Science database. In addition, while there has maintained a steady trend of publishing reliability studies on the R&D GaN devices demonstrated in research laboratories, an increase in publication on commercially available devices is observed. This trend converges with the industry's efforts on developing the standards for GaN qualification. For example, the "JEDEC" JC-70 committee has been providing insights into new test methodologies for GaN power devices [6].

In the previous literature, various aspects of GaN power HEMT reliability have been periodically surveyed [7], [8], [9], [10], [11], but most of these articles are from the device physics

Manuscript received 18 October 2022; revised 26 January 2023; accepted 25 March 2023. Date of publication 11 April 2023; date of current version 19 May 2023. This work was supported by the Center for Power Electronics Systems Industry Consortium. Recommended for publication by Associate Editor S. Tian. *(Corresponding author: Yuhao Zhang.)*

Joseph Peter Kozak is with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA, and also with Johns Hopkins University Applied Physics Laboratory, Laurel, MD 20723 USA (e-mail: jpkozak@vt.edu).

Ruizhe Zhang, Matthew Porter, Qihao Song, Jingcun Liu, Bixuan Wang, and Yuhao Zhang are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: rzzhang@vt.edu; maporter@vt.edu; qihao95@vt.edu; liujingcun0523@gmail.com; bixuanwang@vt.edu; yhzhang@vt.edu).

Rudy Wang is with the Milan Power Electronics Laboratory, Delta Electronics (Americas), Ltd., Durham, NC 27709 USA (e-mail: rudy.wang@deltaww.com).

Wataru Saito is with the Research Institute for Applied Mechanics, Kyushu University, Fukuoka 816-8580, Japan (e-mail: wataru3.saito@riam.kyushu-u.ac.jp).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3266365.

Digital Object Identifier 10.1109/TPEL.2023.3266365

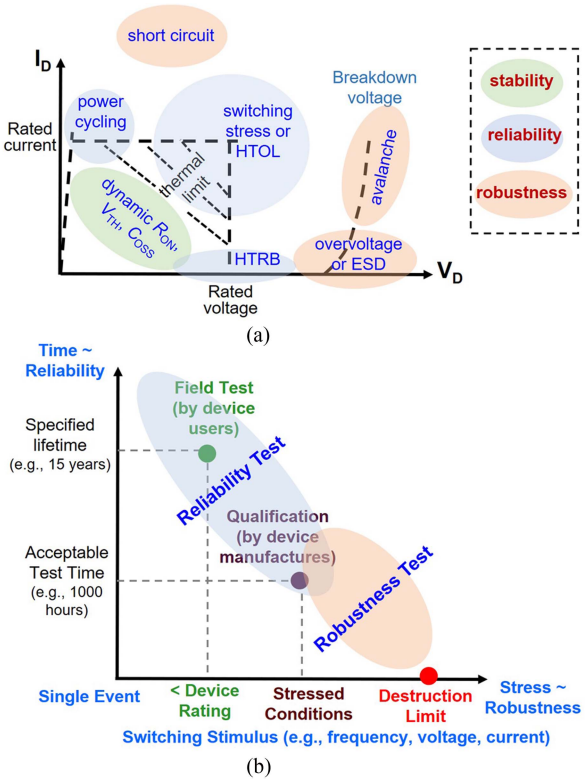


Fig. 1. (a) Device electrical stressors in common stability, reliability, and robustness studies in comparison with the device's SOA. (b) Relationship between the stimulus stress and evaluation timescale for reliability and robustness tests. The scope of reliability tests, robustness tests, field test, and qualification test is illustrated.

perspective and are centric on R&D devices. The processing technology, material, and structure of R&D devices are usually immature compared with commercial devices, and some test conditions for reliability physics' studies are different from the device operations in practical converters. These situations make it difficult for power electronics' engineers to correlate the reliability physics and the nonideal behaviors of commercial GaN devices in converters. This challenge also hinders the further development of the health monitoring, prognosis, and protection systems.

This article attempts to address this gap by summarizing the current understanding on the stability, robustness, and reliability of GaN power devices, with an emphasis on reports of industrial devices. This article also tries to separate stability, robustness, and reliability issues, although in practice they often come interdependently with relatively ambiguous boundaries.

Fig. 1(a) illustrates the device electrical stressors in common stability, reliability, and robustness studies in comparison to the device's rating and safe-operating area (SOA). Stability usually refers to recoverable changes in device electrical characteristics as a result of the transient or sustained switching operation within the SOA [10]. Due to carrier trapping and detrapping within the device structure, the device characteristics can deviate from the static ones without leading to device failure.

Reliability and robustness often refer to nonrecoverable device degradation and failure. The stimulus (e.g., current or voltage) stress in reliability and robustness tests is usually near the SOA boundary and outside the SOA, respectively. Fig. 1(b) shows the other angle to differentiate reliability and robustness. Robustness tests often approach the destruction limits of device stimuli with a timescale much shorter than reliability tests. The timescale of robustness tests can be even down to a single cycle of switching, while that of reliability tests is usually at least hours up to weeks, months, and years.

The stability, reliability, and robustness overview for GaN power devices is motivated by three overarching questions.

1) What are additional power losses induced by the device parametric instability in conduction and switching?
2) What information do various device- and circuit-level reliability tests provide for practical applications?
3) What is the device's circuit-level resilience against surge energy, overvoltage, overcurrent, and their concurrence?

The answers of these questions ultimately help power electronics' engineers to achieve the desired efficiency in GaN converters and reserve proper margin during the design for desired lifetime of the GaN-based power product.

In addition to the conventional applications, GaN power devices are regarded as promising candidates for space, aeronautical, and defense applications. The devices for these applications are usually required to be rugged against radiation and at extremely high or low temperatures. Hence, the radiation and extreme temperature robustness have become increasingly important for power devices.

The rest of this article is organized as follows. Section II overviews the current commercial GaN power devices and common failure locations. Section III overviews the traditional qualification and reliability test results reported for GaN HEMTs, and Section IV surveys the extended reliability data from major GaN device vendors. Section V presents the stability issues of GaN HEMTs, including the dynamic ON-resistance, dynamic threshold voltage, and output capacitance losses, which are all critical to power applications particularly at high frequencies. Section VI details the robustness of GaN HEMTs in out-of-SOA conditions, such as overvoltage, short circuit (SC), and surge energy. Section VII discusses the research exploring the switching reliability and lifetime of GaN devices in converters and under mission profiles. While GaN HEMTs are discussed in prior sections, Section VIII introduces the robustness of the emerging vertical GaN devices that are being commercialized in the industry. Sections IX and X discuss the radiation and extreme temperature ruggedness of GaN devices, respectively. Section XI lists some immediate research needs. Finally, Section XII concludes this article.

Note that the reliability studies of nonindustrial emerging GaN devices are not covered in this article. Some multidimensional GaN devices [1], such as FinFETs [12], [13] and multichannel HEMTs [14], have demonstrated breakthrough performance in ultralow voltage classes down to a few volts [15], [16] and in higher voltage up to 10 kV [17], [18]. While reliability studies of these devices are ramping up [19], [20], [21], they are still at a relatively early stage of development.

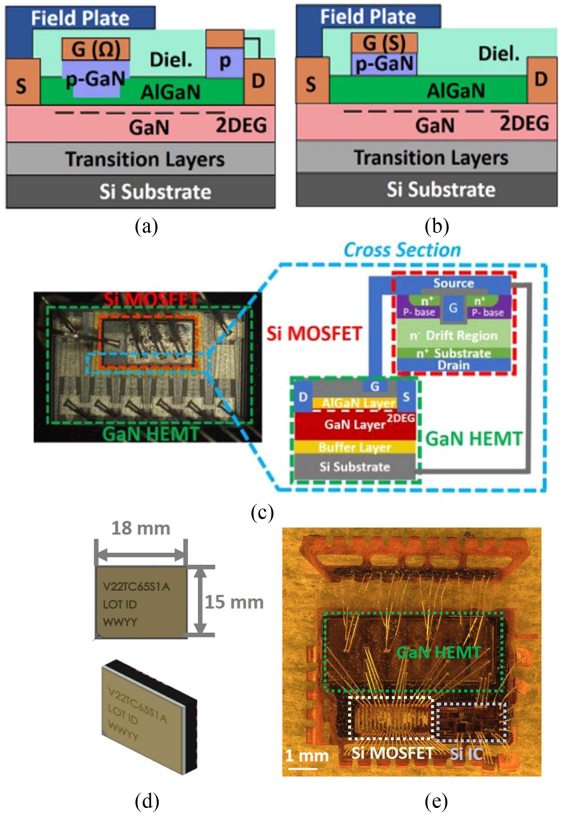


Fig. 2. Schematic of (a) GaN SP-HEMT and (b) GaN HD-GIT. (c) Photograph and schematic of a decapsulated cascode GaN HEMT. (d) Photograph of a packaged direct-drive GaN HEMT. (e) Photograph of a decapsulated direct-drive GaN HEMT from another vendor.

II. Current GaN Devices and Usual Failure Locations

A. Current GaN Power Devices

Four types of device architectures are primarily employed in commercially available GaN products. Two of these include the hybrid-drain gate injection transistor (HD-GIT) and the Schottky p-gate HEMT (SP-HEMT). These technologies are discrete devices and utilize a p-GaN layer in the gate stack to realize the enhancement-mode (E-mode) operation. Their schematics are shown in Fig. 2(a) and (b).

The other two architectures can be considered composite devices where the cascode structure and direct-drive modules utilize multiple semiconductor dies of which the GaN HEMT is usually the depletion mode (D-mode). Fig. 2(c) shows a photograph of a decapsulated cascode HEMT and its schematics [22], [23]. Fig. 2(d) and (e) show the photographs of direct-drive GaN device/module from two different vendors [24].

Fig. 3 depicts the current and voltage ratings of available commercial GaN devices from various vendors. The precommercial vertical GaN field effect transistor (FET) is also included and will be elaborated in Section VIII.

To be cost competitive, the majority of commercial GaN HEMTs are fabricated on Si substrates. Above this substrate includes a transition layer and then the primary GaN buffer layer. An AlGaN layer is deposited above the GaN buffer layer,

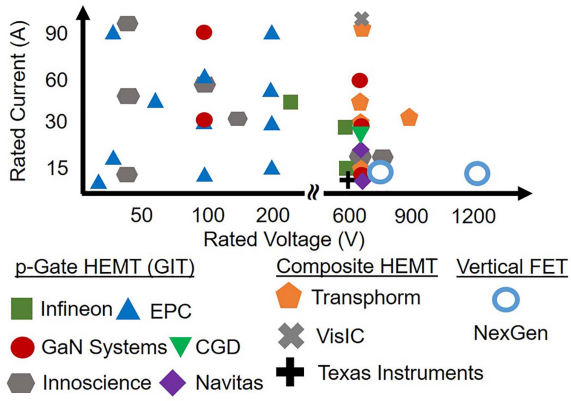


Fig. 3. Current and voltage ratings of commercial and precommercial GaN devices from various vendors.

and it is the interface between the AlGaN and GaN layers that creates the primary channel to conduct current. The lattice mismatch of these two layers creates a piezoelectric effect, which creates a 2DEG channel. The drain, gate, and source terminals are oriented laterally above the AlGaN layer. The p-GaN in the gate stack is key to realization of E-mode operation. This E-mode operation is the preferred choice for power electronics' applications.

The distinction between HD-GIT [see Fig. 2(a)] and SP-HEMT [see Fig. 2(b)] is mainly located in the gate and drain region. The gate metal forms an Ohmic contact to p-GaN in the HD-GIT and a Schottky contact in the SP-HEMT. The AlGaN layer in the HD-GIT is usually recessed, enabling a closer proximity of p-GaN to the 2DEG. The Ohmic contact and AlGaN recess in the HD-GIT favors hole injection into the 2DEG channel, enabling the conductivity modulation. In addition, the HD-GIT includes a p-GaN region connected to the drain, which enables the hole injection into the channel and buffer to alleviate the electron trapping. By contrast, the current conduction in the SP-HEMT only relies on electrons, and minimal holes are injected into the device channel and buffer regions.

In the cascode and direct-drive devices, the traditional high-voltage D-mode GaN devices are oriented with a lower voltage E-mode Si power MOSFET. Through the connection of the two devices [23], [25], a high-voltage E-mode device is created for the cascode device.

The direct-drive devices advance this principle further by incorporating integrated circuit (IC). In this way, a gate driver can be implemented with the power semiconductor to optimize the gate-loop performance and ease the requirements of additional components. Some devices also include sensing and protection ICs for added capabilities.

Overall, these two topologies allow for the use of D-mode HEMT, which usually has a simpler gate stack in comparison to the HD-GIT and SP-HEMT [26]. However, the inclusion of multiple chips in the package brings additional driving challenges as well as the introduction of new failure and instability mechanisms that could be triggered and coupled between the multiple chips [22]. These challenges will be elaborated in the later sections.

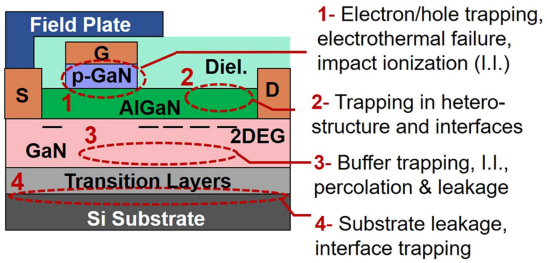


Fig. 4. Illustration of typical trapping locations and other physical processes that can lead to stability, reliability, and robustness issues.

B. Usual Failure Locations

Here, we list some common failure modes and locations in GaN HEMTs to provide an abstract, physical reference for understanding results in the following sections. In Si and SiC MOSFETs, there are known issues within the gate-oxide layer due to various stresses from the gate and drain biases [27], [28]. Additionally, the p-n junction of the MOSFET structure has shown various bipolar stability issues [29].

Differently, many reliability issues of GaN HEMTs are predominantly imposed by carrier trapping effects at various interfaces and layers within the device, as illustrated in Fig. 4. Severe trapping can greatly affect the local electric field and current density, thereby impacting the device ON-resistance, breakdown voltage, and capacitances. In addition to trapping, some other physical processes, such as impact ionization, electrothermal failure, and percolation path creation, can also lead to device failure under different stresses. For example, the carriers generated in impact ionization, if not removed efficiently, can induce the destructive device breakdown [30]. In the GaN HEMT, these processes usually occur at the gate region, AlGaN/dielectric interface, GaN buffer region, transitional layers, and Si substrates. In composite-type GaN devices, the failure locations can be more diverse, e.g., in the multichip interconnect or in Si chips.

III. Traditional Qualification and Reliability Test

As illustrated in Fig. 1(b), traditional accelerated lifetime and reliability tests are designed to help in the qualification of packaged devices for industrial applications by evaluating two primary focuses stressing either the semiconductor-oriented or the packaging-oriented failure mechanisms. While there are international entities that have produced standards for testing semiconductors (e.g., JEDEC, IEC, AEC-Q, MIL-STD, etc.), many qualifications have a foundation from Si technologies. It is now largely an industrial consensus that these standard qualifications (e.g., JEDEC qualification) for GaN devices are necessary but not sufficient and must be followed up by other comprehensive tests. A few industry groups, such as the JEDEC JC-70 Committee [6] and the joint ZVEI European Center for Power Electronics (ECPE) group [31], are actively working to evaluate and update these standards, and provide guidelines for future device evaluations focused on the stresses that GaN devices would experience over the traditional Si transistors.

TABLE I
Exemplar List of the AEC Q101 Qualification Tests for a 650 V, 50 mΩ GaN Cascode HEMT

Test	Symbol	Conditions
High-temperature reverse bias	HTRB	T_J = 150°C, V_{DS} = 650 V, 1000 hrs
Highly accelerated temp and humidity	HAST	130 °C, 85% RH, 33.3 PSI, Bias = 100 V, 96 hrs
Temperature cycle	TC	–66/150 °C, 2 Cycles/hr, 1000 Cycles
Temperature cycling hot tests	TCHT	125 °C Test after TC
Wire-bond integrity	WBG	150 °C, 500 hrs
Power cycle	PC	25/125 °C, ΔT=100 °C, 15,000 Cycles
High-temperature storage life	HTSL	150 °C, 1000 hrs
High-temperature gate bias (Cascode)	HTGB	150 °C, 1000 hrs, V_{GSS} = 18 V
High-temperature gate bias (HEMT only)	HTGB #2	150° C, 1000 hrs, V_{GSS} = –35 V
High-humidity high-temp reverse bias	H3TRB	85 °C, 85% RH, 1000 hrs, 100 V
Unbiased accelerated stress test	UHAST	130 °C, 85% RH, 96 hrs
Destructive physical analysis	DPA	Post TC and HAST

Automotive qualification for GaN devices has attracted great traction recently. Traditional automotive qualification routines are usually based on the AEC-Q100/Q101/Q200 family for Si devices. Table I illustrates one of the first reported automotive qualifications for a 650 V, 50 mΩ cascode GaN HEMT based on the AEC-Q101 standard [32]. The AEC-Q101 qualification for other GaN devices (e.g., SP-HEMT) comprises similar tests except for using a positive gate bias (e.g., 6 V) in the relevant gate tests.

The ECPE recently released a comprehensive automotive qualification standard, namely LV324, expanded upon the AEC standard [31]. The standard comprises a large number of tests categorized into three groups, the qualification characterization tests (QC), qualification environment tests (QE), and qualification lifetime tests (QL). The QC consists of tests on the device's parasitic stray inductance, thermal resistance, and SC robustness. The QE tests involve thermal shock, vibration, and mechanical shock. The composition of the QL tests is similar to that shown in Table I.

While good qualification data have been released by many GaN device vendors, it would be still very useful for power electronics' engineers to know possible GaN device degradation under these qualification tests, particularly for the evaluation of future devices. Hence, we briefly summarize the reported GaN device degradation under several representative qualification and reliability tests, including the static dc-bias tests, such as high-temperature reverse bias (HTRB) and high-temperature gate bias (HTGB), as well as switching tests, such as power cycling.

A. High-Temperature Reverse Bias

HTRB experiments used for device qualification usually apply a stress at 80% of the device rating (for some applications, such as the automotive, up to 100% of the rating) [33]. These qualifying experiments can take thousands of hours [34], [35], [36]. Under HTRB stress, a positive shift has been reported in the ON-resistance ($R_{\mathrm{DS,ON}}$) and threshold voltage (V_{TH}), but the changes do not reach a failed state [37], [38], [39]. In more accelerated HTRB experiments (where the drain voltage is higher than the rated voltage), the V_{TH} instability in some early GaN HEMTs has shown up to a 50% increase, which is above the notional 20% shift failure boundary but recoverable [40].

Determining the voltage stresses in the accelerated HTRB experiments is a challenge for GaN HEMTs because of their dynamic breakdown voltage [41]; this is in comparison with MOSFETs that have an inherently constant avalanche breakdown voltage [27], [42]. Additionally, when MOSFETs are stressed in HTRB experiments, they show an increase in gate-leakage current (I_{GSS}) but some GaN HEMTs show a decrease in I_{GSS} and drain-leakage currents (I_{DSS}) [40], [43]. These shifts in electrical parameters are all related to electron trapping and detrapping [34], [35], [40].

B. High-Temperature Gate Bias

HTGB experiments apply a high static bias onto the gate terminal of the GaN device. Similar tests with a static bias and step-stress processes have been used to determine the gate voltage rating of GaN HEMTs [37], [44], [45], [46], [47], which will be further discussed in Section VII.

HTGB experiments have also shown to cause shifting in V_{TH} and $R_{\mathrm{DS,ON}}$ [37], [43], [44] due to trapped charges in the gate stack. The type of contact formed on p-GaN, either Schottky or Ohmic, would impact these drifts [48]. The Ohmic contact is capable of more efficient hole injection in comparison with the Schottky contact, which would minimize the V_{TH} shift [37].

C. Power Cycling

Power cycling experiments are primarily used to stress the packaging of a commercial device and the interface between the device and package. The stress is created through the repeated, (self) heating of the device with ON-state current causing strain in the mechanical layers due to the differences in the coefficient of thermal expansion mismatch [49], [50], [51].

The p-gate GaN HEMTs have been reported to show V_{TH} and $R_{\mathrm{DS,ON}}$ increase in power cycling [49], [51]. Depending on the magnitude of the temperature swing, I_{DSS} has also shown to increase as well [49], [52]. While solder fatigue has been reported and does impact the increase in $R_{\mathrm{DS,ON}}$, the changes in V_{TH} and I_{DSS} provide evidence that trapping effects cause further degradation in device [49].

Composite-type devices have a greater susceptibility to degradation and failure within the mechanical interconnections from power cycling stresses. Both Xu et al. [49] and Franke et al. [50] have reported that the cascode devices show an increase in $R_{\mathrm{DS,ON}}$. The V_{TH}, however, was not identified as a sensitive precursor parameter for cascode devices under power cycling experiments [49]. The final failure mechanism was attributed to bond-wire lift-off between the Si MOSFET and GaN HEMT [50].

IV. Extended Reliability Data by Device Vendors

While all GaN power devices from major vendors have passed the JEDEC and AEC-Q standards, additional reports have been published by these vendors to provide data regarding the device stability, reliability, and robustness beyond the Si qualification standards. Table II summarizes these extended test data from major GaN device vendors, including EPC, Infineon, GaN Systems, and Transphorm [53], [54], [55], [56].

As illustrated in the table, the common extended reliability data from various vendors mainly address several aspects:

1) dynamic $R_{\mathrm{DS,ON}}$ issue, which is related to device parametric stability and conduction loss in applications;
2) the accelerated lifetime extraction under various stimuli, including the drain-to-source bias (V_{DS}), gate-to-source bias (V_{GS}), and temperature;
3) the accelerated lifetime testing under various mission profiles mimicking the device operations in some representative applications.

Examples of such switching stress include the hard-switched boost converter, double-pulse-based setup, and soft-switched converters. In some context, such test is named the high-temperature operating life (HTOL) test, and the test circuit topologies include a boost converter [32] and the half-bridge converters with *RC* load or *RL* load [57].

The extensive test data manifest the insufficient qualification of GaN HEMTs using the conventional Si standards. However, one can find that the data presented by different vendors are often obtained from different methods, and most of the derived reliability models are vendor specific. For example, the V_{DS} overvoltage robustness is characterized by both dc stress and pulsed voltage by Infineon and only by dc stress by other vendors. Another example is the large variety of circuit topologies used to extract the switching stress lifetime by various vendors. Finally, critical device robustness, such as the SC capability, is only reported by one vendor, and some other parameters, such as avalanche (surge-energy) capability, are not reported by any vendor.

To address these gaps, many studies have been performed by researchers and engineers in the academia and industry to do the following:

1) explore and compare various methods to characterize the stability, reliability, and robustness of GaN HEMTs;
2) identify the common or distinct behaviors that are correlated to characteristic device structures instead of being vendor specific;
3) generalize unified models for device dynamic parameters and lifetimes for various GaN HEMTs.

While not all of these gaps have been fully addressed, the summary of current understandings provides useful information for device users. The high-level explanation of the relevant physical mechanisms could help device users understand the potential problems of GaN devices and how they differ from

TABLE II
SUMMARY OF EXTENDED RELIABILITY TEST METHODS AND RESULTS FROM MAJOR GaN DEVICE VENDORS

Test	Vendor	Test method	Behavior	Mechanism	Major Results Reported
Dynamic $R_{DS,ON}$ Test	EPC	Hard switch	dynamic $R_{DS,ON}$ higher than static $R_{DS,ON}$	Hot-electron trapping	Charge trapping and $R_{DS,ON}$ model established with factors of V_{DS}, I_D, f_{sw}, and T_J
	Infineon				Minimal dynamic $R_{DS,ON}$ up to 600 V at 10 MHz
	GaN Systems				Dynamic $R_{DS,ON}$ impacted more by T_J than by the trapping
Drain Acceleration Lifetime	EPC	DC stress	serious $R_{DS,ON}$ shift	Hot-electron trapping	Nonmonotonic relationship with T_J. 1 ppm over 10 Years at rated V_{DS} at 150 °C
	Infineon	DC stress	catastrophic breakdown	TDDB-like failure behavior	100 ppm for 15 Years at 480 V V_{DS} at 125 °C
		Pulsed voltage		Electrical breakdown	Transient voltage ratings identified to include in the datasheet
	Transphorm	DC stress	catastrophic breakdown	Dielectric breakdown	>>20 Years lifetime at 650 V V_{DS}, 175 °C T_J.
Gate Acceleration Lifetime	EPC	DC stress	catastrophic failure	Failure in Schottky contact	Failure insensitive to T_J, 1 ppm in 10 Years at recommended V_{GS}
	GaN Systems				100 ppm in > 10^{10} hrs at recommended V_{GS}
Switching Stress Lifetime	Infineon	Hard-switch boost	N/A	N/A	Lifetime model with the factors of I_D, V_{DS} and f_{sw}
	GaN Systems	LLC/PFC converter	catastrophic failure	N/A	lifetime > 3 million Years for data center LLC and PFC applications
	Transphorm	Double-pulse based setup		N/A	Lifetime model with the acceleration factor V_{DS}
SC	EPC	Hard-switch fault and fault under load	catastrophic failure	Thermal runaway	Over 10 µs SC withstanding time at 60 V V_{DS} in both conditions
HTOL	Transphorm	Hard-switch boost	N/A	N/A	No degradation after 3000 HRs running at T_J of 175 °C and frequency of 300 kHz

Si and SiC devices. These summaries and explanations will be provided in the next few sections.

V. STABILITY IN SWITCHING

Parametric instability in GaN HEMTs is usually associated with the trapping behavior (trapping and detrapping). The accurate measurement of parametric shifts, particularly in high-frequency switching, is very challenging. This is because the occupation probability of traps depends on its electrical history and the trapping behavior usually spans the time constants over many orders of magnitude [10]. Here, we first scrutinize various measurement methods [58], [59] and clarify the time constant range associated with each method. This allows us to understand how the results from these measurements correlate to device switching operation in practical converters.

Generally, three types of stability and reliability tests have been widely used for power devices, i.e., the dc stress test, pulse *I–V* test, and circuit test. Table III summarizes the key features of these tests. The dc stress test usually characterizes the relatively long-term parametric shifts after an OFF-state dc stress. It cannot capture the parametric shifts that recover within the poststress measurement time (usually at least ∼10 s). Therefore, the measured shifts are not representative of those present in transient switching. The pulse *I–V* test can probe the dynamic parametric shifts in a short time (down to 1 μs) right after the switching stress. However, the pulse *I–V* condition is still different from converters, as it is based on the square wave with a resistive load and has a limited *dv/dt*.

TABLE III
COMPARISON OF THREE TEST APPROACHES THAT ARE COMMONLY USED FOR EVALUATING THE STABILITY AND RELIABILITY OF POWER DEVICES

Method	DC stress test	Pulse I–V test	Circuit test
Stress Time	seconds to hours	1 µs–100 ms [PW(1–D)/D]*	10 ns–10 µs
Stress Type	DC; OFF-state	Square-wave switching (resistive load); OFF-state	Inductive switching; ON- and OFF- state
Measured Parameter	R_{ON}, V_{TH}, I_{GSS}, I_{DSS}, C	R_{ON}, V_{TH}, I_{GSS}, I_{DSS}, C	R_{ON}, C (V_{TH})
Time of Measurement	> 10 s	1 µs–100 ms (PW)	10 ns–1 µs
Key information for applications	parametric shifts that cannot recover within seconds	dynamic parametric shifts in square-wave pulses	parametric shifts under application-use conditions
Note and limitations	used to monitor long term and permanent parametric shifts	usually resistive loads; pulse rise time > 100 ns for high bias, limited *dv/dt*	distinction may exist in single pulse and steady state; in situ measurement challenging

*PW: pulsewidth; D: duty cycle.

Circuit tests allow for characterization of device's parametric shifts under the application-use conditions. Additionally, benefitted from the small time constant of the stress that can be implemented in circuits, the switching stress of interest is no longer limited to the OFF-state stress but can also

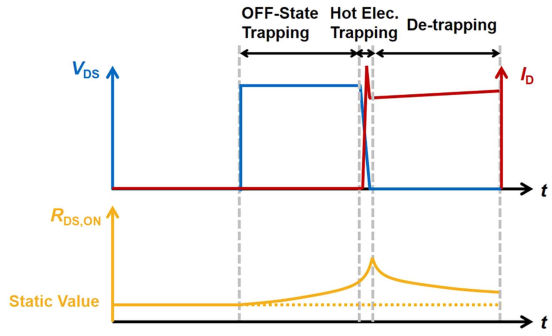


Fig. 5. Schematic of $R_{\mathrm{DS,ON}}$ variation during a switching event of GaN HEMTs due to trapping and detrapping effects.

accommodate the ON-state stresses (e.g., SC and gate overvoltage). The challenges in circuit tests are on the in situ measurement of the parametric shift of interest with a minimal disturbance on the converter operation. Finally, one should be careful about the parametric shifts evaluated in the single-event and steady-state switching, which could be different due to the distinction in trapping states. This will be further explained in the evaluation of D-$R_{\mathrm{DS,ON}}$ and dynamic breakdown voltage.

In the remaining part of this section, we will present three major parametric stability issues in GaN HEMTs during their normal switching operations (i.e., within the SOA).

A. Dynamic ON-Resistance

Dynamic $R_{\mathrm{DS,ON}}$ (D-$R_{\mathrm{DS,ON}}$) is a well-known issue in various types of GaN HEMTs, where the $R_{\mathrm{DS,ON}}$ is higher than its measured dc value after high blocking voltage stress. D-$R_{\mathrm{DS,ON}}$ leads to undesirable increases in the device conduction loss and junction temperature, yet it is not commonly specified in datasheets. This D-$R_{\mathrm{DS,ON}}$ poses serious challenges in designing GaN-based power converters, especially for high-frequency applications. Over the past decade, extensive studies have been devoted toward understanding and addressing different aspects of the D-$R_{\mathrm{DS,ON}}$ phenomenon, including its physical origin, dependency factors, characterization method, etc.

1) Physical Origin: D-$R_{\mathrm{DS,ON}}$ roots from the trapping effect in various possible regions of the GaN HEMT structure, as shown in Fig. 4. Leakage current electrons injected under high drain bias [60] and hot electrons generated during switching transitions due to the overlap of high voltage and high current [61] could cause charge trapping in the buffer layer, GaN channel and gate region, as well as near the surface and/or in the dielectric. Each of these can decrease the 2DEG conductivity and increases $R_{\mathrm{DS,ON}}$. The physical mechanisms have been thoroughly reviewed in [62] and will not be elaborated in this article. At the device level, various technologies, such as surface passivation optimization [63], elaborately designed GaN buffer [64], and optimal field-plate structure [65], have been proposed to reduce the trapping effects and eliminate the D-$R_{\mathrm{DS,ON}}$ issue.

Fig. 5 illustrates the typical $R_{\mathrm{DS,ON}}$ variation during a switching event of GaN HEMTs. The increase in D-$R_{\mathrm{DS,ON}}$ (electron-trapping effect) mainly exists in two stages: the first one is induced in the OFF-state, and the second is related to the hard turn-ON process. In the ON-state, detrapping of these electrons allows the $R_{\mathrm{DS,ON}}$ to gradually settle back to its static value. Note that the soft turn-ON process is not expected to induce significant D-$R_{\mathrm{DS,ON}}$ in most GaN HEMTs.

As the review [62] published in 2019, many recent studies on SP-HEMTs and HD-GITs have reported consistently new understandings on the D-$R_{\mathrm{DS,ON}}$ issue. First, the D-$R_{\mathrm{DS,ON}}$ is more strongly affected by the hard turn-ON process than the OFF-state [66], [67], [68], [69]; Second, the OFF-state stress primarily induces electron trapping in the buffer, while the hard turn-ON stress induces electron trapping in both the buffer and the interface between AlGaN and passivation layer [67], [70]. Some studies report the interface/surface trapping to dominate in the hard turn-ON process while observing the impact of buffer region design [66], [67] and drain field-plate design [71] on surface trapping. Studies have also shown that the traps relevant to the hard turn-ON process possess a broadly distributed but relatively shallow energy level [72], [73].

2) Dependency Factors: As D-$R_{\mathrm{DS,ON}}$ is caused by the device switching transition, numerous research articles have reported the influence of varying operating conditions in power converters on the D-$R_{\mathrm{DS,ON}}$.

The number of trapped electrons depends very much on the blocking voltage, and a nonmonotonic relation between D-$R_{\mathrm{DS,ON}}$ and OFF-state and drain-to-source voltage ($V_{\mathrm{DS,OFF}}$) has been identified in [74], [75], and [76]. It has been shown that D-$R_{\mathrm{DS,ON}}$ increases with $V_{\mathrm{DS,OFF}}$ until it reaches a maximum at typically 100–300 V (for a ~600-V rated device). However, the D-$R_{\mathrm{DS,ON}}$ recovers to smaller values at higher $V_{\mathrm{DS,OFF}}$ due to partial neutralization of buffer traps [74]. Additionally, the load current (I_L) affects the hot-electron acceleration, and thus trapping efficacy, particularly in the hard turn-ON process. Therefore, a higher D-$R_{\mathrm{DS,ON}}$ is observed as I_L increases [77], [78]. Switching speed (and duration) determines the quantity of trapped hot electrons, so a larger gate resistance could induce the more serious D-$R_{\mathrm{DS,ON}}$ issue [79]. Higher gate current/gate voltage [80] can facilitate a faster detrapping process during the ON-state and contributes to a smaller D-$R_{\mathrm{DS,ON}}$.

As the time constant of trapping behavior can span from nanoseconds to seconds [81], [82], D-$R_{\mathrm{DS,ON}}$ is dependent on the switching frequency and duty cycle [83]. The probability of electron trapping and detrapping is also related to junction temperature (T_J). Inconsistent reports are present for various devices that the D-$R_{\mathrm{DS,ON}}$ either increase [84] or decrease [85] at higher T_J or show more complex dependences [86]. For example, the D-$R_{\mathrm{DS,ON}}$ of HD-GITs is found to increase with T_J at low $V_{\mathrm{DS,OFF}}$ but decrease with T_J at high $V_{\mathrm{DS,OFF}}$, which is related to the effectiveness of hole injection in HD-GITs [86]. The dependence between D-$R_{\mathrm{DS,ON}}$ on T_J may be device specific and impacted by $V_{\mathrm{DS,OFF}}$ and switching schemes.

Finally, the D-$R_{\mathrm{DS,ON}}$ differs in hard switching (HSW) and soft switching [87], [88], [89], but its dependency could be device specific [90]. Soft switching leads to a lower D-$R_{\mathrm{DS,ON}}$ in SP-HEMTs [91] by eliminating the impact by hot-electron effects; in HD-GITs, injected holes from the drain p-GaN layer

TABLE IV
COMPARISON OF CHARACTERIZATION METHODS COMMONLY USED FOR EVALUATING D-$R_{DS,ON}$ OF GaN POWER HEMTS

Method	Type of device	Circuit topology	Type of load	Note and limitations	Reference
Pulsed I-V	On-wafer	/	Resistive	Nonrealistic switching locus and slew rate; limited frequency; pulse overlap is changed to accommodate HSW/soft switching	[60], [82]
DPT	Packaged	Half-bridge	Inductive	Usually does not specify the stress time before the first pulse; may underestimate the actual D-$R_{DS,ON}$ in repetitive switching	[79], [86], [87], [95]
		Full-bridge			[85]
Continuous Switching	Packaged	Half-bridge	Inductive	Working on packaged devices; may add cycle (packaging) time for R&D devices	[78], [90], [96]
		Buck			[83], [97]
		Resonant converter			[85]
		Resonant inverter	Resistive		[98]
	On-wafer	Boost	Inductive	Need careful parasitic control; very hard to reach high switching speed and high voltage/current at wafer level	[66], [99]

during HSW effectively release the trapped electrons, so soft switching may even result in a higher D-$R_{DS,ON}$ [90].

3) Characterization Method and Results: Despite extensive efforts in D-$R_{DS,ON}$ characterizations, large discrepancies have been reported in the literature from a minimal increase to a ten times higher gain over static R_{ON} [92], even for commercial devices. It was recently pointed out that this inconsistency largely originates from the characterization methods [92]. Table IV summarizes the key aspects of three most commonly used D-$R_{DS,ON}$ characterization methods, including pulsed *I–V* test, double-pulse test (DPT), and steady-state continuous-switching test. By employing source measure units to modulate the voltage bias at multiple device terminals, the pulse *I–V* test is usually performed at wafer level with resistive load and used in many trapping physics' studies [82], [93], [94]. The overlap of current and voltage could be changed to simulate HSW/soft switching, but it cannot mimic the switching locus and slew rate (e.g., *dv/dt*) in real applications.

The classic DPT method, as recommended by the JEDEC standard [95], has been used in various circuit topologies with inductive load [79], [85], [86], [87], [95]. However, DPT could miscalculate the device D-$R_{DS,ON}$ in continuous-switching power converters [96] because it ignores the accumulation effects in repetitive switching cycles. In addition, DPT usually does not specify the OFF-state stress time before the first pulse, which could lead to uncertainties in D-$R_{DS,ON}$.

More recently, state-of-the-art D-$R_{DS,ON}$ test design has been focusing on the continuous-switching method where the GaN devices are switched to the steady state in power converters, including half-bridge topology [78], [90], [96], buck converter [83], [97], resonant converter [85], [98], etc. With the realistic application profile, steady-state continuous-switching test is the best practice to perform a D-$R_{DS,ON}$ characterization. It is noteworthy that D-$R_{DS,ON}$ in continuous-switching converter (boost converter circuit [99]) has been performed at the wafer level, which could significantly shorten the R&D process of GaN HEMTs. The key to achieve this ON-wafer dynamic characterization is the accurate control of parasitics in the whole system, e.g., probe tip, connectors, and cables, which allows for reaching high switching speed and switching voltage/current.

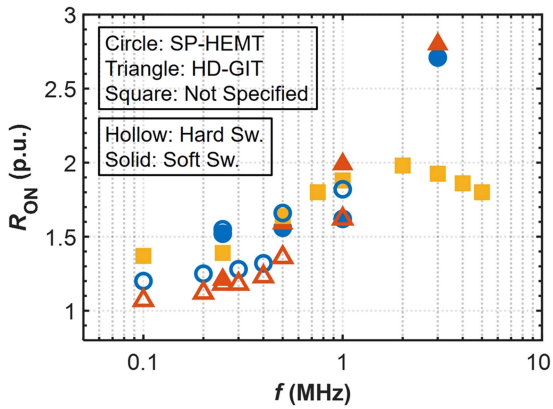


Fig. 6. Literature values of normalized D-$R_{DS,ON}$ to the static value of commercial GaN HEMTs under steady-state switching conditions.

Fig. 6 and Table V show the normalized D-$R_{DS,ON}$ measurement results of commercial GaN HEMTs under the steady-state switching conditions, characterized from hundreds of kilohertz up to several megahertz [80], [90], [97], [100]. Target devices include both SP-HEMTs and HD-GITs, whereas measurements of composite devices are still lacking. These devices were tested at nominal voltage levels (~67% voltage rating, e.g., 400 V for 600/650-V devices) and nominal current level (~50% current rating, e.g., 8 A for 15-A devices). With a steady-state switching measurement protocol, the worst-case D-$R_{DS,ON}$ of commercial GaN HEMTs was found to be less than three times higher than the static value. For the same device, D-$R_{DS,ON}$ generally increases as the switching frequency goes up. Below 1 MHz, the D-$R_{DS,ON}$ among all tested devices was within twice the static value, regardless of switching mode (hard or soft). In multi-MHz switching, D-$R_{DS,ON}$ of certain devices presented a saturation with frequency (e.g., 2 MHz in Fig. 6). This could be a result that the time constant of the combination of trapping and detrapping effects is exceeded [97].

From the application viewpoint, the D-$R_{DS,ON}$ characterized in application-use conditions provide valuable references for converter design and performance evaluation. The efficiency of GaN-based converters is directly affected by D-$R_{DS,ON}$ due to the increased conduction loss. Thermal management needs

TABLE V
SUMMARY OF THE NORMALIZED D-$R_{DS,ON}$ TEST RESULTS OF COMMERCIAL GAN HEMTS UNDER STEADY-STATE SWITCHING CONDITIONS

Device Technology	Device Rating	Test Condition			Normalized D-$R_{DS,ON}$ Result
		Voltage/ Current	Type of Sw.	Freq. (kHz)	
SP-HEMT	650 V/ 30 A [90]	400 V/ 15 A	Hard	250	1.55
				500	1.66
				1000	1.82
		400 V/ 10 A	Soft	250	1.52
				500	1.56
				1000	1.62
	650 V/ 15 A [80]	400 V/ 8 A	Hard	100	1.2
				200	1.25
				300	1.28
				400	1.32
	650 V/ 15 A [100]	400 V*	Soft	3000	2.71
GIT	600 V/ 13 A [90]	400 V/ 7.5 A	Hard	250	1.18
				500	1.36
				1000	1.62
		400 V/ 5 A	Soft	250	1.21
				500	1.59
				1000	1.99
	600 V/ 13 A [80]	400 V/ 8 A	Hard	100	1.07
				200	1.12
				300	1.18
				400	1.23
	600 V/ 15 A [100]	400 V*	Soft	3000	2.8
Not specified	<200 V, current rating hidden [97]	<135 V/ 1 A	Soft	100	1.37
				250	1.39
				500	1.64
				750	1.8
				1000	1.88
				2000	1.98
				3000	1.93
				4000	1.86
				5000	1.8

*Current stress not specified

careful consideration, and the device SOA may be shrunk (where the upper left boundary is limited by $R_{DS,ON}$). The possibly higher T_J and reduced SOA of GaN HEMTs could further affect the lifetime projection of GaN-based power converter.

B. Output Capacitance Loss

In addition to $R_{DS,ON}$, GaN HEMTs produce the losses generated from the output capacitance (C_{OSS}). The C_{OSS} loss is generated when the equivalent output capacitance of the OFF-state power device is subsequently charged and discharged; this loss is equal to zero in an ideal capacitor. In GaN HEMTs, output charge versus V_{DS} characteristics show hysteresis in large signal, dynamic double sweep, producing power loss in a cycle of charging and discharging. This C_{OSS} loss issue first gained attention in Si superjunction devices [101], [102] and recently in GaN HEMTs.

Fig. 7 shows a comprehensive comparison of C_{OSS} losses reported in various types of GaN HEMTs as compared with some Si and SiC devices [103], [104], [105], [106], [107]. GaN HEMTs are experiencing considerable C_{OSS} losses, e.g.,

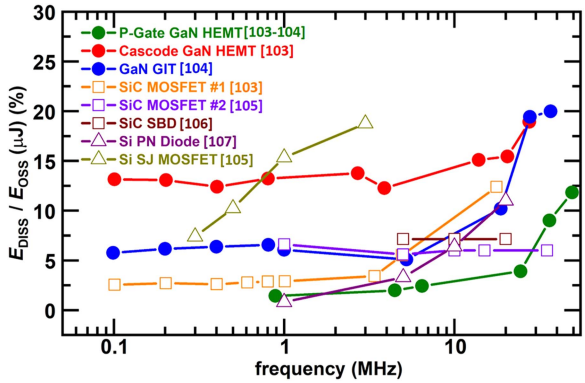


Fig. 7. Comparison of the ratios of the reported C_{OSS} loss over the total C_{OSS} stored energy in various GaN HEMTs, SiC MOSFETs, SiC diodes, Si diodes, and Si superjunction (SJ) MOSFETs.

larger than 20% of the total C_{OSS} stored energy (E_{OSS}) at the frequencies above 20 MHz, which is rarely observed in other types of power devices. From the system viewpoints, this loss starts to become a significant portion of the device total loss in high-frequency (>MHz) soft-switching applications [103]. In HSW or low-frequency applications, this loss is typically much lower than the other device losses (e.g., *I–V* overlap loss). It can induce an unexpected junction temperature climb-up [104], [108] and significantly impair the system efficiency [98], [109].

Several approaches have been utilized to characterize the C_{OSS} loss, which are summarized in Table VI. In general, researchers attempted to quantify this loss by using either the calorimetric (thermal) method [108] or the electrical methods, including the Sawyer–Tower method, nonlinear resonance method, and unclamped inductive switching (UIS) method [104], [110], [111].

All these methodologies have advantages and limitations. For example, in the calorimetric approach, the device under test (DUT) is placed in parallel with an active switch; the DUT is turned OFF all the time with the V_{DS} set by the active switch, and the DUTs C_{OSS} loss is derived from its T_J change. This method allows for measuring the device C_{OSS} loss in working soft-switched converters without frequency limitation. In this method, however, the system calibration could be laborious and the separation of device C_{OSS} losses from other losses could be challenging and time-consuming. Also, the accuracy of the calorimetric measurement can be lesser at low power levels.

By contrast, the implementation of an electrical method and the relevant data processing is usually simpler. The Sawyer–Tower method relies on a network consisting of the DUT, a reference capacitor, and a power amplifier that generates the sinusoidal excitation. The DUT is always OFF; its large-signal charge–voltage waveforms can be obtained from the network's input voltage (v_{IN}) and the capacitor voltage (v_{REF}), followed by the C_{OSS} loss extraction from the hysteresis of charge-voltage waveforms. In the nonlinear resonance and UIS methods, the DUT operates in both ON and OFF states. In its OFF-state, a resonance is produced between the load inductor and the DUTs C_{OSS}; the C_{OSS} loss is extracted by analyzing the loss in this resonance process based on the DUTs V_{DS} or I_{DS} waveforms.

TABLE VI
SUMMARY OF THE PROPOSED C_{OSS} LOSS MEASUREMENT APPROACHES AS WELL AS THEIR FEATURES, ADVANTAGES, AND LIMITATIONS

Methodology	Features				Advantages	Limitations
	DUT State	Number of Required Components	Key Device Parameter Monitored	C_{OSS} Loss Extraction		
Calorimetric [108]	*OFF*	Many	T_J	Maybe complex	• Application-use condition: soft-switch, high-frequency converters. • Immune to limitations of electrical approaches, e.g., distorted waveforms at high frequency.	• DUT constant OFF; System setup and calibration could be complicated and time-consuming. • The separation of C_{OSS} loss from other losses can be challenging.
Sawyer-Tower [104]	*OFF*	Medium	v_{REF}, v_{IN}	Relatively Convenient	• Small number of components required. • Can generate Q–V and C–V curves of the DUT in large-signal switch.	• DUT constant OFF. • Selection and implementation of the key components may affect the loss extraction accuracy.
Nonlinear Resonance [110]	*ON and OFF*	Few	DUT's V_{DS}	Convenient	• Very small number of components involved. • Can evaluate the impact of ON-state current on C_{OSS} loss	• Accuracy sensitive to waveform distortion and data processing. • Does not account for C_{OSS} loss due to the conduction of leakage current.
UIS [111], [112]	*ON and OFF*	Few	DUT's I_{DS}	Convenient	• Very few components involved. • Can evaluate the impact of ON-state current on C_{OSS} loss • Account for conductive and capacitive C_{OSS} losses	• Need to carefully calculate the ESR losses of inductors, capacitors, and parasitics

Despite the simpler setup, the accuracy of these electrical approaches may be compromised due to the variability and noise of waveforms and equipment, e.g., limited probe bandwidth, probe delays, and waveform distortion at high frequencies [113], [114]. In addition to the tradeoff between thermal and electrical approaches, the Calorimetric and Sawyer–Tower methods only involve the device OFF-state, which disallows for the study of the impact of ON-state current on C_{OSS} loss. All these tradeoffs need to be considered when interpreting the C_{OSS} loss data from various methods.

Finally, the origin of C_{OSS} loss in GaN HEMTs is still contentious [108], [112], [115], [116], while a consensus is reached that the carrier trapping/detrapping induced C_{OSS} hysteresis is a key root cause. However, the location, time constant, energy level, and physical origins of the relevant traps remain unclear [112]. The leakage current in the epitaxial structure [108] and the resonance on the Si substrate [116] have been reported to contribute to the C_{OSS} loss. With the origin of C_{OSS} loss remaining not fully clear, there have been relatively few reports on its reduction strategies. An experimental work has shown that the C_{OSS} losses can be reduced by re-engineering the GaN HEMT architecture and epitaxial stack [108].

From the application viewpoint, the C_{OSS} loss significantly impacts the device selection for high- and very high frequency power converters [105]. In parallel to understanding its origin and mitigation from device perspectives, an immediate need for applications is to provide such information in the device datasheet and the relevant models in the device application note. To facilitate this to happen soon, a widely accepted characterization method is preferable, which should ideally involve the device ON- and OFF-states and best represents the device's steady-state switching in converters [111], [112].

C. Dynamic Threshold Voltage in SP-HEMT

Bias-temperature V_{TH} instability has been a crucial research topic of Si and SiC MOSFETs for decades. It was also studied for GaN HEMTs with various gate architectures. Early studies focused on GaN metal–insulator–semiconductor (MIS) HEMTs. The V_{TH} instability in MIS-HEMTs is due to the trapping at the insulator/GaN interface or in the bulk dielectric, which are similar to Si and SiC MOSFETs. A thorough review of the V_{TH} instability in GaN MIS-HEMTs is provided in [117].

In recent years, as p-gate gradually becomes the prevailing E-mode GaN technology, the research focus shifts to commercial p-gate HEMTs [87], [118], [119], [120], [121], [122], [123]. Unlike the V_{TH} instability in MOSFETs and MIS-HEMTs, the dynamic V_{TH} is an intrinsic property related to the floating p-GaN layer in SP-HEMT. As shown in Fig. 4, the SP-HEMT gate stack consists of a p-GaN Schottky junction back-to-back series connected with a p-GaN/AlGaN/GaN p-n junction. As the bias condition (forward or reverse) of these two junctions is opposite, the charges in the p-GaN layer cannot be effectively supplied or extracted in fast switching, making a "floating" p-GaN layer.

Latest progress in the V_{TH} instability studies for SP-HEMTs is reviewed in [124]. The charge storage process in p-GaN usually leads to a positive dynamic V_{TH} shift [120]. This V_{TH} shift increases with the OFF-state blocking voltage and the switching frequency [122]. It is worth mentioning that the GIT features an Ohmic contact on p-GaN, allowing for effective charge supply/extraction and thereby a stable V_{TH}.

In addition to the floating p-GaN, trapping may also contribute to the dynamic V_{TH}. Under a forward V_{GS}, a V_{TH} shift can be impacted by two trapping mechanisms [125], [126], [127]. The

first mechanism is hole trapping and recoverable, which creates a negative V_{TH} shift. The second mechanism is electron trapping and slow in recovery, causing a positive V_{TH} shift [125], [127].

The dynamic V_{TH} shift could considerably impact the device switching operations [124]. With a positive shift, the reverse conduction voltage of SP-HEMT increases, leading to higher power loss. The dynamic V_{TH} will primarily impact the turn-ON loss of SP-HEMTs [43]. It also demands a sufficiently high gate-drive voltage to fully turn-ON the device, which reduces the safety margin for the gate reliability. Hence, circuit simulations should consider the dynamic V_{TH} to depict the practical circuit characteristics. Recently, a SPICE model with dynamic V_{TH} is developed [121] and used to analyze the switching transients in a phase-leg circuit [128].

D. Other Issues Associated With Composite Devices

Since composite devices are combinations of multiple chips, they may face instability issues not only on GaN HEMTs but also associated with the interconnection between Si devices and GaN HEMTs. For example, some instability issues have been reported in cascode GaN HEMTs. During high-current, turn-OFF conditions, a divergent oscillation can occur because of the capacitance mismatch between the GaN and Si switches [129]. Additionally, the added inductance to the bond wires between the switches and the Si avalanche can also cause an increase in the internal switching losses [130]. To minimize the interconnection induced loss, the latest generation of commercial cascode GaN HEMTs eliminates the internal bond wires between the two chips by directly stacking the Si chip onto the source pad of GaN HEMT [22]. However, in some extreme instances, false turn-ON events can occur [131], and SC oscillations can cause catastrophic failures [132]. On the other hand, the gate instability is usually not an issue in the cascode GaN HEMT or direct-drive device because an Si MOSFET is primarily driving the device or additional protection circuits are copackaged with the GaN HEMT.

VI. Robustness

A critical robustness requirement of power devices in many applications, such as motor drives, automotive powertrains, and electric grids, is the capability of withstanding overvoltage, overcurrent, and surge-energy events before the protection circuitry intervenes. The robustness is usually characterized by UIS (i.e., avalanche) and SC tests for Si and SiC power transistors. GaN HEMTs are known to possess limited SC robustness and no avalanche capabilities. Moreover, under some out-of-SOA conditions, GaN HEMTs withstand the stress or degrade/fail very differently as compared with Si and SiC devices. This section will present the SC, surge energy, and overvoltage robustness of GaN HEMTs. Note that the gate robustness is also very relevant to p-gate GaN HEMTs. Due to its close correlation with the gate lifetime, we will discuss it in Section VII.

A. SC Robustness

SC fault events occur when a conduction path with minimum impedance is present between the switching transistor and the power supply. The SC events usually drive devices into the saturation mode of operation, with both a high voltage and a high conduction current stressing the device [133]. A typical SC robustness requirement is the 10 μs SC withstanding time (t_{SC}) under the bus voltage (V_{BUS}) and driving conditions identical to the application-use operation [134]. If the 10 μs t_{SC} is unattainable, according to the U.S. Department of Energy 2025 Vehicle Drive Roadmap [135], a 2 μs t_{SC} of the power device together with the ultrafast protection circuit is needed.

There are generally four types of SC conditions that can happen in a power electronics system: the arm SC, which is also called the hard-switching fault (HSF) or SC type I, the series arm SC, the output SC, and the ground SC [136], [137]. Among these conditions, HSF is usually employed for the evaluation of the power device SC robustness [134]. This section summarizes the single-event t_{SC}, failure mechanisms, and repetitive SC test results recently reported for GaN HEMTs.

From the application viewpoint, it is critical to measure the SC capability under the application-use driving conditions (e.g., the same driving circuitry and voltage). Table VII summarizes the reported t_{SC} of various GaN HEMTs under the driving condition similar to their normal operation [138], [139], [140], [141], [142], [143], [144], [145], [146], [147], [148]. Note that the t_{SC} variation seen in some articles is believed to be due to distinct driver conditions. For example, a large gate resistor (R_G) is used in [149] and [150], leading to long t_{SC}. The large R_G slows down the device turn-ON, resulting in a smaller peak SC current. Additionally, the device gate-leakage current increases in the SC withstanding process due to the temperature elevation.

TABLE VII
Summary of SC Robustness Reported for Commercial and R&D GaN Power Transistors

Status	Type	Rated voltage (V)	R_G (Ω)	V_{GS} (V)	L_{para} (nH)	V_{BUS} (V)	t_{SC} (μs)
Comm.	SP-HEMT	650	10	5	~10	300	308 [138]
						350	0.7 [138]
						360	0.66 [138]
						360	0.5-0.9 [139]
				6		320	0.5-0.9 [139]
			N/A			350	0.7 [140]
						400	0.6 [140]
		80			N/A	60	12.1 [53]
	GIT	600	RC driver		N/A	350	>10 [141]
						360	0.2 [141]
	Cascode	650	1	8	50	100	12 [142]
						200	5 [142]
						300	4.4 [142]
			8	12	48	300	1.80 [143]
			16	6.5	7.5	250	7.60 [144]
R&D	D-mode	650	50	8	N/A	400	0.50 [147]
	SP-HEMT	600	6.3	5	48	200	2.00 [143]
		N/A	15	6	<10	400	>10 [148]
	Cascode	650	45	9	N/A	400	>3 [145]
Vertical GaN		650	RC driver		48	400	30.5 [146]

R_G and L_{para} are the resistance and parasitic inductance in the gate driver.
V_{BUS} is the bus voltage.

The leakage current across the large R_G could make the device $V_{\rm GS}$ significantly lower than the usual operation [151], leading to even lower SC current and a thermal stress much lower than practical SC scenarios.

The reported $t_{\rm SC}$ for 650 V SP-HEMTs is generally below 1 μs at $V_{\rm BUS}$ higher than 350 V [133], [139], [140], [150], [151], [152]. For HD-GITs, an *RC* driving circuit is employed with a large R_G (100+ Ω) to minimize the quiescent gate current [141]. This suppresses the device $V_{\rm GS}$ under the SC stress, leading to a fast I_D drop and a $t_{\rm SC}$ >10 μs at $V_{\rm BUS}$ below 350 V [141], [153], [154]. However, similar to SP-HEMTs, the $t_{\rm SC}$ drops drastically to < 1 μs at $V_{\rm BUS}$ > 350 V [141], [151], [153]. Cascode devices also show limited SC robustness. As the cascode gate is the Si MOS, the $t_{\rm SC}$ is not sensitive to R_G [143], [151]. Very few SC reports are available on direct-drive device. Song et al. [24] report the SC tests of a 650 V, 100 A direct-drive GaN HEMT, which is intentionally stopped in 100 ns. The device can withstand an SC current up to 358 A within this SC duration.

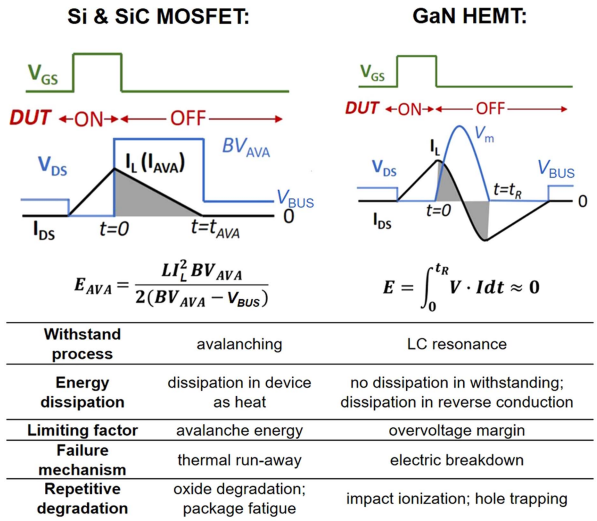
Extensive efforts have been made to understand the limiting mechanism of the SC capability in GaN HEMTs, particularly at high $V_{\rm BUS}$. In long SC duration tests with a low $V_{\rm BUS}$ [141], [150], devices fail thermally. At high $V_{\rm BUS}$, many reports converge on the electrical failure. In [147], it is proposed that the SC failure could be caused by the high electric field induced by the hole accumulation underneath the gate in which the holes are generated from impact ionization. Castellazzi et al. [141] also report the correlation between the SC-induced high carrier density and electric field crowding at the drain-side gate edge. A gate–drain region failure in the SC condition is also reported in [143]. In [148], a wafer-level transient voltage measurement is used to monitor the potential profile in the gate–drain region under the SC stress. The failure is revealed to depend on the electric field propagation speed; when high electric field reaches the drain edge, impact ionization induces the failure.

Within the single-event SC SOA, the insufficient robustness of GaN HEMTs in repetitive SC stresses has been reported. In [133], the SP-HEMT fails after seven 1.2 μs SC pulses at 300 V. At lower $V_{\rm BUS}$, the repetitive SC stresses lead to an increase in $R_{\rm DS,ON}$ and decrease in $I_{\rm DSS}$ [133], [140], [149]. These parametric shifts are all evidences toward electron trapping in the buffer and gate regions during the repetitive SC operation. The repetitive SC tests on HD-GITs are reported in [141] and [155]. Under this stress, the evolution of crack formation and aluminum extrusion has been observed [155].

For the cascode HEMT, two additional mechanisms have been revealed to limit its SC robustness. First, the parasitics of the Si-GaN chip interconnection can excite the self-sustained gate oscillation in the SC condition, leading to the GaN HEMT false turn-ON and failure [132], [144]; second, the cascode HEMT has a lower thermal self-regulation capability on the gate control as compared with HD-GITs and SP-HEMTs [151].

From the application viewpoint, the short $t_{\rm SC}$ of current GaN HEMTs requires the incorporation of protection circuits for applications where the SC fault could occur. The protection circuit should detect the fault and clear it within 100–200 ns. This is difficult to achieve by conventional desaturation circuits due to their long response time [156] and the false protection drawn by the high *dv/dt* [157]. Recently, ultrafast SC protection circuits for GaN HEMTs have been demonstrated by multiple groups [157], [158], [159], [160], [161]. The fault detection and clearance time demonstrated by these circuits are generally below 100 ns. Additional desirable features have also been presented, such as strong *dv/dt* noise immunity [157], applicability to the parallel-connected GaN HEMTs [159], and monolithic integration with the GaN device [161]. In addition to fast protection, other circuit approaches are also proposed, such as connecting the GaN HEMT with an Si MOSFET [162], to enhance the SC capability.

Finally, besides circuit approaches, device-level innovations have been reported to improve the $t_{\rm SC}$ of GaN devices. A straightforward approach is to reduce the saturation current (and the associated electric field crowding under the SC condition) by removing segments of the 2DEG channel along the width of GaN HEMT [145], [163]. This approach enables a $t_{\rm SC}$ over 3 μs in industrial cascode GaN HEMTs. A more significant improvement is demonstrated in 600–700 V vertical GaN FETs, with a $t_{\rm SC}$ over 30 μs at 400 V [146], [164], [165]. This vertical GaN FET will be elaborated in Section VIII.



Withstand process	avalanching	LC resonance
Energy dissipation	dissipation in device as heat	no dissipation in withstanding; dissipation in reverse conduction
Limiting factor	avalanche energy	overvoltage margin
Failure mechanism	thermal run-away	electric breakdown
Repetitive degradation	oxide degradation; package fatigue	impact ionization; hole trapping

Fig. 8. Surge-energy withstand process, dissipation path, failure mechanism, and repetitive degradation of the avalanche transistor (Si&SiC MOSFET) and the nonavalanche transistor (GaN HEMT). Figure adapted from the article presented in [169].

B. Surge Energy and Overvoltage Robustness

In addition to SC robustness, the ruggedness against surge energy is highly desirable for power devices [166], [167], [168]. Historically, the surge-energy robustness of Si/SiC MOSFETs and IGBTs relies on their avalanche capability, an impact ionization and multiplication phenomenon that allows the device to accommodate high current at high $V_{\rm DS}$ (i.e., avalanche breakdown voltage, $BV_{\rm AVA}$). As shown in Fig. 8, when devices are subject to surge energy, $V_{\rm DS}$ rapidly ramps to and clamps at $BV_{\rm AVA}$. The drain current (I_D) drops to zero, accompanied by resistive dissipation of the surge energy via avalanching in device. This energy dissipation prevents the further energy circulation in converters. Hence, the surge-energy ruggedness is often referred

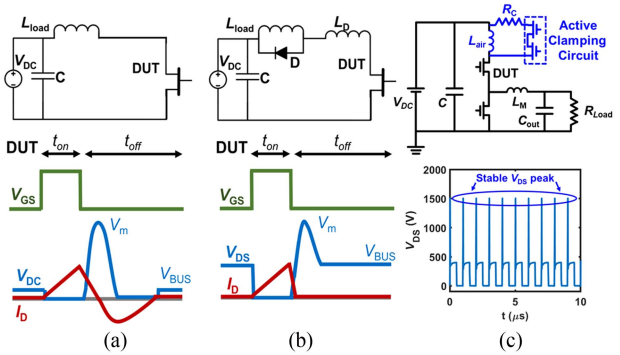


Fig. 9. Schematic of three overvoltage ruggedness evaluation circuits: the UIS circuit (left), the CIS circuit (middle), and the soft-switch buck converter with an ACC (right), as well as the typical waveforms in these tests.

to as avalanche ruggedness. The avalanche energy (E_{AVA}), the maximum energy that a power device can dissipate without triggering thermal runway, has become an important metrics for device robustness [169].

GaN HEMTs, however, do not have the intrinsic avalanche capability [30]. The JEDEC JC 70 committee has recently identified their surge-energy robustness to be a critical issue for evaluation [6]. When GaN HEMTs are subject to surge energy, they show a swift increase in V_{DS} (see Fig. 8) as the result of the resonance between their C_{OSS} and the parasitic inductance of the circuit [169], [170]. This withstanding process cannot dissipate energy until the resonance voltage becomes negative, leading to the reverse turn-ON of GaN HEMTs. In the withstand process, the primary electrical failure is related to the overvoltage margin of the device, i.e., the dynamic breakdown voltage [41]. This *BV* in the transient switching could be different from the static *BV* measured through the quasi-static *I–V* sweep on the curve tracer [22], [41], [171], [172].

The above discussion manifests the convergence of surge-energy robustness and overvoltage robustness for GaN HEMTs. In general, GaN HEMTs designed with a higher dynamic *BV* and larger C_{OSS} can withstand a larger surge energy at the price of the compromised switching speed [169]. This tradeoff can be considered when designing and selecting any nonavalanche power device for various applications. In the remaining part of this session, we will discuss the characterization methods of dynamic *BV* and overvoltage ruggedness, the characterization results, and implications for GaN applications.

1) Characterization Methods: To date, three methods have been developed to characterize the overvoltage ruggedness and dynamic *BV* for GaN HEMTs, i.e., the UIS circuit, the clamped inductive switching (CIS) circuit [169], and the active clamping circuit (ACC) [172], [173]. The schematic and typical waveforms of these three circuits are illustrated in Fig. 9.

The UIS test is a widely used method to characterize the power device surge-energy robustness. It is a JEDEC standard [174] and has been routinely used to measure the E_{AVA} and BV_{AVA} [175], [176], [177]. The UIS tests of GaN HEMTs have been reported since 2016 [178], [179], [180], [181], [182], [183]. Zhang et al. [169] reveal the detailed withstanding physics,

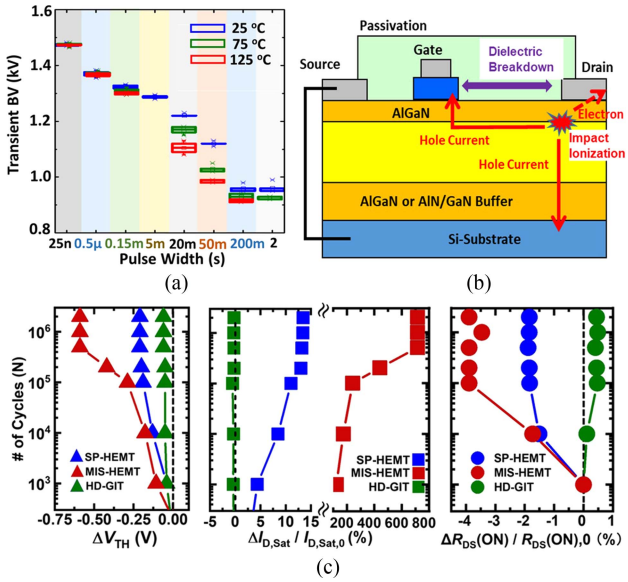


Fig. 10. (a) Dynamic *BV* of a 650 V SP-HEMT at various pulsewidths and temperatures [41]. (b) Illustration of breakdown mechanism of GaN HEMTs and the associated physical processes. (c) Shifts in threshold voltage, saturation current, and ON-resistance in three GaN HEMTs as the increased cycles of overvoltage HSW near *BV* [26].

failure boundary, and failure mechanisms for GaN HEMTs in UIS tests. Later, UIS tests for different types of GaN HEMTs [22], [25], [170], [184], [185] in single-pulse and repetitive stresses [23], [186] as well as at different temperatures [187] have been reported.

The UIS test is also an effective method to characterize the dynamic *BV* of a nonavalanche power device, such as GaN HEMT [41]. By tuning the load inductance, the dynamic *BV* of a 650 V rated GaN HEMT under various pulsewidth (and *dv/dt*) and temperatures is shown in Fig. 10(a). The dynamic *BV* (up to 1400 V) is significantly higher than the static *BV* (950 V) [41]. This suggests a higher overvoltage margin of GaN HEMTs in switching. These dependences of the dynamic *BV* can be explained by the trapping dynamics and the resulted change of the peak electric field magnitude in GaN HEMTs [41].

Differently, the cascode device shows a dynamic *BV* lower than the static *BV* in the UIS test [22], suggesting an inferior overvoltage ruggedness in switching. The 650 V rated cascode devices exhibit a dynamic *BV* (1.4–1.7 kV) lower than the static *BV* (1.8–2.2 kV); the dynamic *BV* also shows a strong frequency dependence, dropping from >1.4 kV at 1 kHz to 1.25 kV at 100 kHz [22]. These phenomena are explained by the GaN trapping affected by the Si MOSFET avalanche [22].

Despite the simplicity, the UIS test differs from many converter operations due to a relatively low V_{BUS} and the absence of the overlap between high current and high voltage. To address these limitations, the CIS circuit is proposed with a high V_{BUS} and a controlled "parasitic" inductance to create voltage overshoot in the HSW turn-OFF process [169], as illustrated in Fig. 9(b). This CIS test has been applied to SP-HEMTs [169], [171], [188] and HD-GITs [169], [188], [189]. The CIS tests with varying stressors (*dv/dt*, ambient temperature) show a failure

overvoltage boundary consistent with the UIS tests under the same conditions.

A limitation of UIS and CIS circuits is the difficulty of evaluating the device's overvoltage ruggedness in very high frequency switching. To address this limitation, a soft-switching buck converter with an ACC is developed in [172] and [173], as shown in Fig. 9(c), which allows for the continuous kilovolt overvoltage switching at a frequency up to 1 MHz. This test is applied to SP-HEMTs and HD-GITs from different vendors to study the failure boundary and ruggedness. Most devices show a consistent overvoltage failure boundary (i.e., dynamic *BV*) with the UIS/CIS measurements up to MHz [173].

2) Overvoltage/Surge Robustness and Application Insights: The studies on the overvoltage ruggedness of GaN HEMTs in continuous switching started from the repetitive UIS tests, as reported by multiple groups. For HD-GITs, the earlier generation devices showed some level of parametric shifts in I_{DSS} and output characteristics [178], [183], while these shifts were not reported in newer generation devices [41]. SP-HEMTs have been reported to show a negative, recoverable shift in I_{DSS} due to buffer trapping [41], [178], [181], [182], [186]. Cascode devices show recoverable shifts in $R_{\mathrm{DS,ON}}$, I_{DSS}, and junction capacitances after repetitive UIS tests [22], [23].

More recently, CIS circuits have been used as an advanced tool to study the GaN HEMTs ruggedness in overvoltage HSW. SP-HEMTs, HD-GITs, and MIS-HEMTs (used in direct-drive devices) have been reported to survive the repetitive overvoltage HSW with an overvoltage up to 90% of the dynamic *BV* [171], [189], [190]. However, different devices exhibit significant distinction in the magnitude of parametric shifts and their recovery speed.

Despite the distinction, a common cause of these shifts is the trapping of the holes generated in the impact ionization during the overvoltage switching, as shown in Fig. 10(b). This process is related to the breakdown mechanism of GaN HEMTs [30], [191]. When V_{DS} approaches the dynamic *BV*, peak electric field is usually present near the drain or below the edge of source field plate, initiating the impact ionization. While the generated electrons are removed through the drain, the generated holes flow toward the gate and substrate [171]. The hole trapping or hole accumulation can produce parametric shifts, electric field crowding, and destructive breakdown.

A comprehensive study of overvoltage HSW up to the 90% dynamic *BV* for various GaN HEMTs is presented in [26]. Fig. 10(c) shows the evolution of parametric shifts with the increased CIS switching cycle, revealing a saturation and stabilization in all devices. These parametric shifts are all recoverable but require different techniques for various devices, as the device's poststress recovery is dominated by the hole detrapping and removal. The HD-GIT shows a fast natural recovery. The through-gate hole removal in SP-HEMT can be accelerated by negative gate bias and high temperatures. The MIS-HEMT can be recovered by applying positive gate and substrate biases, which make holes recombine in the 2DEG channel. These results suggest, despite the lack of avalanche in GaN HEMTs, the impact ionization places an important role in determining their ruggedness in overvoltage switching [26].

When the frequency of overvoltage switching is higher (e.g., $>$100 kHz), two premature failures have been reported for some SP-HEMTs, leading to failures at the voltage level much lower than the dynamic *BV* [173]. One failure features a drastic, nearly unrecoverable $R_{\mathrm{DS,ON}}$ increase, leading to conduction loss ramp-up and thermal failure. The other failure exhibits an increase in I_{DSS} and a catastrophic breakdown at lower voltage. These two premature failure mechanisms are both due to the severe trapping occurred in the GaN HEMT at very high frequency. To screen the devices suffering from these extrinsic failures, high-frequency continuous UIS tests can be used as an effective method [173].

The above results provide several implications for GaN applications. First, for applications that require the device to withstand single-event or repetitive surge energy, selection of GaN devices with high overvoltage margin (dynamic *BV*) and large C_{OSS} is essential. With sufficient overvoltage margin and C_{OSS}, the surge energy that GaN HEMTs can withstand could be similar to the avalanche energy rating of Si and SiC devices. Second, for normal operations, GaN HEMTs are quite robust against the transient overvoltage and oscillation beyond their voltage rating. However, for some devices, continuous voltage overshoot at high frequency could be detrimental. In this case, overvoltage suppression circuits that do not sacrifice the device fast switching capability could be needed, similar to those developed for SiC devices [192], [193]. For example, an ultrafast self-powered voltage overshoot suppression circuit is recently demonstrated for GaN HEMTs in solid-state circuit breaker applications [194]. One factor to consider when designing such circuit is the dependence of GaN overvoltage ruggedness on frequency, as the trap accumulation is affected more by frequency than the switching speed or slew rate.

Another need relevant to applications is on providing the transient voltage rating for GaN HEMTs. As shown in Table II, the transient voltage rating and the relevant acceleration model are only available from one GaN device vendor. On the other hand, a large variation in overvoltage margin is seen from GaN devices (e.g., a dynamic *BV* ranging from $\sim$1 to $\sim$2 kV for 650 V GaN devices from various vendors). Since such transient voltage rating could be frequency and temperature dependent, a unified test method and standard as well as the associated lifetime model are highly desirable.

VII. Switching Lifetime

For Si devices, some well-known standards, such as JEDEC JESD47, have been utilized for decades to provide guidelines for lifetime extraction. This approach is based on understanding of the failure modes of Si devices, as well as statistical calculations to assure the accuracy with limited samples. These traditional qualification tests, however, do not consider the switching conditions of power devices. Most of the test specified in JEDEC only utilizes static, high-voltage biases, and high temperatures. For GaN devices, due to the diverse failure modes, it is an open question on the viability of using static stress tests to evaluate the device lifetime. Many recent works are exploring the evaluation

of GaN device lifetime under the application-use switching condition. This section presents such efforts in probing the gate lifetime, drain switching lifetime, and the device switching lifetime under mission profiles.

A. Gate Lifetime

Conventional Si and SiC power transistors (e.g., IGBTs and MOSFETs) usually comprise a MOS gate, and the gate lifetime is limited by the oxide reliability. The MOS reliability and lifetime are usually characterized by the HTGB test or the time-dependent dielectric breakdown (TDDB) test, which can follow the JEDEC JESD92 standard [195]. The gate oxides in Si and SiC devices have been conformed to show sufficient intrinsic lifetime at high temperatures [196]. Recent efforts on SiC gate lifetime study center on the lifetime testing and modeling for extrinsic failures [196], [197], [198], [199].

For commercial D-mode GaN MIS-HEMTs used in direct-drive and cascode devices, very few gate lifetime studies have been reported except for the good HTGB qualification data from vendors. Most publications of MIS-HEMTs are based on research devices with nitride dielectrics [200], [201], [202], [203] or Al_2O_3 [204] as the gate insulator [205]. The gate failure in most of these MIS-HEMTs shows the TDDB behavior [206], [207], [208]. A 20 years lifetime (100 pm, 130 °C) extrapolation is reported for a 0.2 mm^2 gate area at positive gate voltage of 9.4 V [200].

Recently, gate lifetime studies gradually centered around the SP-HEMT, as it has become a common device platform in many foundries. A critical issue in the SP-HEMT driver design is to suppress the V_{GS} overshoot induced by the parasitic gate-loop inductance or commutation crosstalk, as the margin between the typical drive voltage and the maximum allowable voltage of SP-HEMT can be as low as 1 V [209]. Moreover, as explained in Section IV-C, the Schottky-type p-gate is not fully insulating but comprises a floating p-GaN layer.

Several methods similar to those presented in Table III have been used to study the gate lifetime of SP-HEMTs. The dc tests with a constant-voltage stress or step-voltage stress have been widely employed [210], [211], [212], [213], [214], [215], [216], [217]. Fig. 11(a) and (b) shows the evolution of I_{GSS} of a commercial SP-HEMT in a step-stress test until failure, revealing a TDDB behavior [45]. As shown in Fig. 11(c), the time to fail (t_{BD}) data at a certain V_{GS} could be fitted by Weibull distribution (F is the cumulative probability function), and the shape parameter (β) higher than 1 indicates the wear-out failure. As shown in Fig. 11(d), the Weibull distributions can extract t_{BD} at each V_{GS} for a given failure rate, and the t_{BD}–V_{GS} relation is further fitted by a power law from which the maximum allowable V_{GS} for a ten-year lifetime can be extrapolated for the failure rate of 63% and 0.1%. Another recent work found that the time-to-fail data from dc tests show an exponential dependency on $1/I_G$ and follow a LogNormal rather than a Weibull distribution [218].

Recently, the square-wave pulse *I–V* test was used to study the gate breakdown and reliability [45], [219], [220], [221]. The I_G evolution data similar to those in dc tests can be obtained from

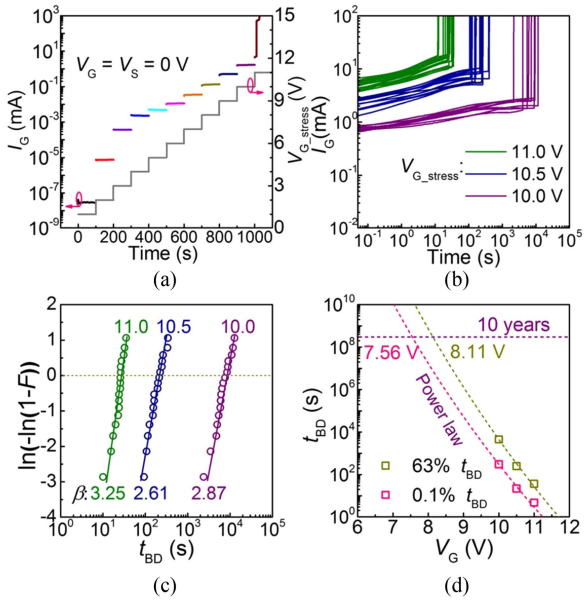


Fig. 11. Gate current evolution of SP-HEMTs in a dc step-stress test is shown in (a) and (b). (c) Weibull distribution of the time-to-failure (t_{BD}) data taken at V_{GS} of 10 V, 10.5 V, and 11 V. (d) Projection of maximum V_{GS} for a ten-year lifetime at a failure rate of 0.1% and 63%. Figures reproduced from the article presented in [45].

pulse *I–V* tests for lifetime extraction. Diverse dependencies of the gate lifetime in pulse *I–V* tests have been reported in the literature. The effective gate lifetime (i.e., the product of duty cycle and total lifetime) is reported to increase at higher temperatures and be weakly dependent on frequency from dc to 100 kHz [45]. In comparison, Millesimo et al. [220], [222] report that the effective gate lifetime decreases at increased frequency and duty cycle, when the frequency reaches 1 MHz. This is explained by the difficulties for the electrostatics in p-GaN to keep up with the V_{GS} switching at high frequency.

These diverse dependencies suggest the strong impact of switching schemes on the SP-HEMT gate lifetime. This may lead to the inapplicability of the gate lifetime obtained from dc tests to device operations in power converters. Recently, a circuit method is proposed to evaluate the gate lifetime under the inductive load switching [223], the condition of which is not accessible by dc or pulse *I–V* methods. As the parasitic-induced gate overshoot has a resonance nature, this method features a resonance-like gate ringing with the pulsewidth down to 20 ns and an inductive switching concurrently in the drain–source loop. Fig. 12(a) shows the circuit schematic, and Fig. 12(b) shows the produced V_{GS} overshoot in the HSW. As shown in Fig. 12(c), the single-pulse failure boundary, i.e., the dynamic gate breakdown voltage, is found to be strongly affected by the drain–source switching locus, e.g., HSW and drain–source grounded (DSG), pulsewidth, and temperature. These dependences are not observed in the MOS-type gates in the Si IGBT and SiC MOSFET. In addition to failure boundary, the application of this method to characterize the gate's switching lifetime is desirable.

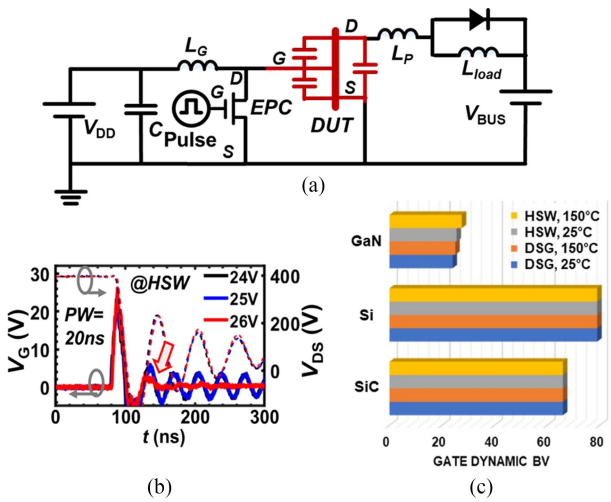


Fig. 12. (a) Schematic of the inductive load circuit to measure the gate overvoltage reliability. (b) Produced V_G and V_{DS} waveforms for gate voltage overshoot with a peak magnitude of 24, 25, and 26 V under 400 V HSW. (c) Measured dynamic gate breakdown voltage of GaN SP-HEMT, Si IGBT, and SiC MOSFET under HSW and DSG conditions at 25 °C and 150 °C. Figures reproduced from the article presented in [223].

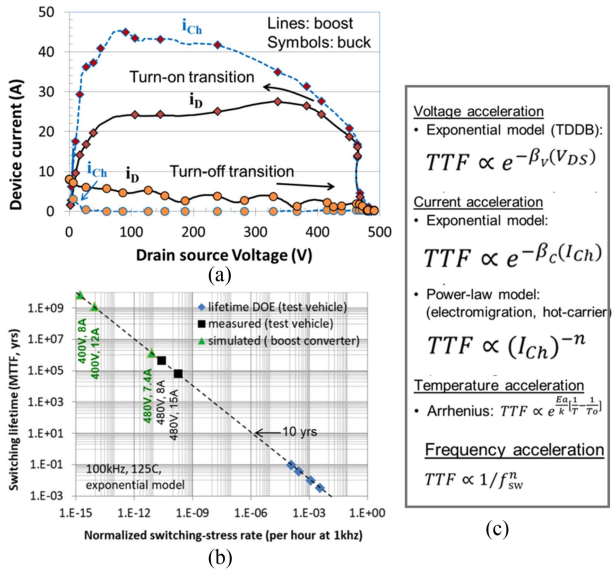


Fig. 13. (a) Switching locus plots for hard-switched buck and boost topologies, showing both drain and channel currents. (b) Switching lifetime extrapolation for boost converter applications. (c) Model functions used for various accelerators. Figures reproduced from the article presented in [232].

Finally, from the various reports on the time-dependent breakdown of SP-HEMT [39], [125], [211], [212], [213], [215], [216], [224], [225], [226], [227], [228], the failure mechanism remains contentious [228]. While all reports show the failure of devices with an increase in gate-leakage current, some reports claim that the failure is caused by the high electric field in the metal/p-GaN Schottky junction or AlGaN barrier layer [126], [210], [224], [227], while others have credited the failure to the generation of a percolation pathway [211], [212], [213], [215], [226], [229]. The positive temperature coefficient of the failure boundary in a commercial SP-HEMT [45] disagrees with the classic percolation-induced TDDB theory; instead, it is explained by the impact ionization in p-GaN and the resulted degradation of the Schottky contact on p-GaN [45].

Overall, the SP-HEMT gate stack architecture appears to have lifetime concerns, particularly in fast switching. Further investigations are ongoing to provide new gate architectures at the device level [216], [224], and driver techniques at the circuit level [46], [230], [231].

B. Switching-Oriented Lifetime Extraction

The importance of employing switching circuits to extract the GaN HEMT lifetime holds not only for the gate but also for the drain–source loop. For the conventional Si transistors, HTRB tests at multiple drain biases between the rated voltage and BV_{AVA} are widely used for lifetime extraction, as voltage is a major lifetime accelerator. However, due to the distinct and complex breakdown mechanisms in GaN HEMTs, the viability of the HTRB-based lifetime extraction is questionable.

Recent efforts have explored the lifetime evaluation of GaN HEMTs based on the application-use switching conditions that involve both HSW and soft-switching stresses throughout the converter operation [168], [232]. Some of these efforts reported by device vendors are summarized in Table II. In addition, a generalized approach to determine the switching lifetime of a GaN HEMT is presented in [232]. Similar to the overvoltage stress tests, some of these experiments utilize the CIS circuit with the HSW turn-ON stresses instead of turn-OFF stresses. The *I–V* switching locus, as shown in Fig. 13(a) [232], utilizes the HSW turn-ON event in a CIS circuit to match that seen in a boost converter application. Through repetitive cycling under these switching events until failure, a lifetime plot is created. These results are then compared with application lifetime tests as well as the simulated lifetime metrics, which are extracted through calculations utilizing the switching energy as the primary parameter. Fig. 13(b) shows how this generalized testbed and switching energy focused method have been used to baseline the lifetime of GaN devices in varying applications [232]. The acceleration models for four representative stressors, i.e., V_{DS}, channel current (I_{Ch}), temperature, and frequency, are illustrated in Fig. 13(c).

C. Mission-Profile Lifetime Considerations

The mission-profile-based model for electronic system lifetime extraction has seen evolutions recently. For example, the hybrid electric vehicle (HEV)/electric vehicle (EV) onboard chargers require more than 30 000 h lifetime, which is 3–4 times higher than the traditional internal combustion engines. Some other pulsed power application, such as medical equipment, will charge and discharge the load with power cycle in the range of millisecond [233]. Once the failure mechanism is identified, system-level solution to extract the lifetime can be deployed [234].

The mission-profile-based lifetime extraction usually suggests the need for considering more system-level variables,

which could be more complex than the device-level reliability and robustness. From industry standpoint, such system-level variables typically include the packaging, system integration, harmonics, and electromagnetic interference (EMI).

The reliability issues associated with the package of GaN devices are strengthened by the diverse packages required to accommodate various chip footprints [235]. Si devices manufactured by different vendors now have standard footprint for the user to pick up from. However, for GaN devices, the footprint still varies between different vendors, which creates inconvenience for the end user and also not secure supply from procurement standpoint. Because of this packaging variety, reliability for each new packaging needs extra evaluation from vendors.

To accelerate the adoption of advanced GaN devices, the integrated function of gate driver built-in protection can be essential. The desirable system-level protection includes the overcurrent, overtemperature, and undervoltage lockout. Low-inductance design is also essential through system-level integration, which will minimize the nonideal symptoms, such as ringing and voltage overshoot [236]. Finally, the gate charge of GaN devices is much lower than Si devices. The enhanced *dv/dt* and *di/dt* in GaN device operations will inevitably create more system-level harmonics and EMI issues and, thus, desire novel and practical EMI solutions. The impact of EMI and harmonics on GaN device reliability and lifetime is still unclear.

VIII. Emerging Vertical GaN Device

Vertical GaN devices are regarded as candidates to expand GaNs application space into the medium-voltage range [5], [13], [20], [21], [237]. In this section, we introduce the latest reliability and robustness results of industrial vertical GaN devices, as they demonstrated breakthrough avalanche and SC capabilities. Additionally, vertical devices are less prone to surface traps, as the peak electric field is usually located inside the GaN layers. Until now, several multikilovolt vertical GaN diodes and 1.2–2 kV vertical GaN transistors have been reported, with architectures including p-n diode [238], Schottky barrier diode (SBD) [239], junction barrier Schottky diode [240], current-aperture vertical electron transistor [241], trench MOSFET [242], fin-channel MOSFET [243], and fin-channel JFET [244]. The fin-shaped vertical channel can enable a high channel density and, thus, a low channel resistance, at the same time enabling the E-mode operation [12], [13].

Despite still under active development, vertical GaN devices have shown to pass multiple traditional reliability qualification experiments, such as HTRB, HTOL, temperature humidity bias, and temperature cycling [245]. In these experiments, the fundamental failure mechanisms can usually trace back to the quality of the substrate and epitaxy material. Substrate orientation, surface preparation, and epi growth initiation are found to be critical in the device performance and reliability [21], [245]. As the bulk GaN substrates to date remains a higher dislocation density than Si or SiC, it can be expected that the device reliability will be further improved as the substrate and epitaxial growth technologies mature. Gate stability studies of vertical GaN transistors have also been reported, e.g., the evaluation of GaN fin MOSFET under positive gate step stress [246] and GaN trench MOSFETs under drain step stress [247].

Recent studies have also demonstrated superior switching stability of vertical GaN devices. With less surface-trapping effect as well as good crystalline quality, vertical GaN devices are less susceptible (or even free) to D-$R_{\mathrm{DS,ON}}$ issues; this has been experimentally verified in a 600-V rated SBD by the DPT method [239]. Minimal $R_{\mathrm{DS,ON}}$ change has been observed under various switching conditions, including OFF-state stress bias up to 500 V, OFF-state stress time within 10^{-6} to10^{2} s, high temperature up to 150 °C, and different load current levels.

The GaN p-n junction is a critical building block for many vertical GaN power diodes and transistors. The overcurrent and overvoltage ruggedness of industrial vertical GaN p-n diodes are comprehensively reported in [248] and [249]. GaN p-n diodes show a critical surge current of 54 A (over tenfold higher than the rated current) and a critical surge-energy density of 180 J/cm^2 in 10-ms surge current tests, with the surge-energy density being comparable with SiC devices [248]. Note that the associated device physics is different in GaN and Si p-n junctions. With little conductivity modulation in GaN p-n junctions, the good surge current capability is attributed to the increased acceptor ionization in p-GaN at high temperatures [248]. This suggests a high overcurrent robustness of GaN p-n junctions with small bipolar current and fast switching capabilities.

In addition to surge robustness, the industrial GaN p-n diodes also demonstrate strong avalanche capabilities with BV_{AVA} up to 2 kV, maximum avalanche current (I_{AVA}) up to 61 A, and a critical avalanche energy density of 7.6 J/cm^2 (comparable with SiC p-n junctions) [248], [249]. Note that the main-junction avalanche may be shielded in the static *I*–*V* sweep by a trap filling process at the edge termination; therefore, it is necessary to characterize the avalanche capability in GaN devices in the UIS circuit tests [249].

For transistors, the industrial vertical GaN Fin-JFETs [see Fig. 14(a)] recently demonstrated a specific R_{ON} of 0.82 m$\Omega \cdot$ cm^2, a V_{TH} of 2 V, a BV_{AVA} with positive temperature coefficient [see Fig. 14(b)], a $\sim$10 ns switching time in 600-V/4-A DPT, and good thermal stability up to 200 °C [244], [250]. Moreover, vertical GaN FinFET shows textbook-like avalanche waveforms in the UIS tests, being the first avalanche-capable GaN power transistor [244], [250]. The critical energy density is up to 10 J/cm^2, which is comparable with SiC devices and much higher than Si devices [251].

The natural I_{AVA} path in vertical GaN Fin-JFETs is through the gate p-n junction, which may require extra protection circuitry in the gate driver. It is recently shown that I_{AVA} in GaN Fin-JFETs can be tuned to flow through the source, by using an *RC*-interface driver, which turns ON the fin channel during the avalanche [see Fig. 14(c)] [252]. Under this condition, the major avalanche current path migrates from the gate p-n junction to the n-GaN fin channel, producing an interesting "avalanche through fin" process [252].

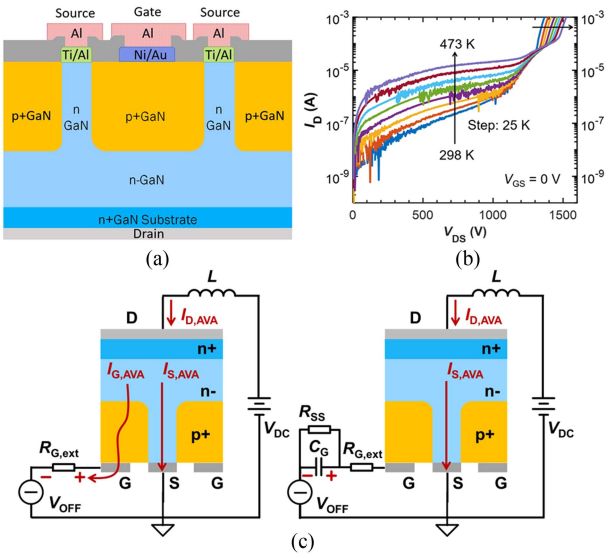


Fig. 14. (a) Schematic of vertical GaN Fin-JFET. (b) Temperature-dependent OFF-state *I–V* characteristics. (c) Illustration of the distinct avalanche paths under a MOSFET gate driver and an *RC*-interface gate driver. Figures adapted from the articles presented in [250] and [252].

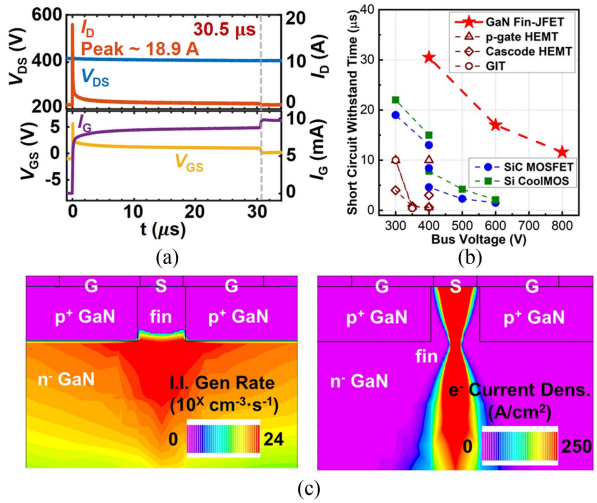


Fig. 15. (a) SC withstanding waveforms of a 650 V vertical GaN Fin JFET at $V_{\mathrm{BUS}} = 400$ V. (b) Comparison of SC withstanding time versus bus voltage for 600–700 V unipolar E-mode transistors. (c) Contours of impact ionization generation rate and electron current density in a Fin JFET unit cell under the SC condition when V_{BUS} approaches BV_{AVA}. Figures reproduced from the article presented in [146].

In addition to avalanche capabilities, GaN fin JFETs also exhibited the significantly enhanced SC robustness. Zhang et al. [146] present the SC characterization of a 650 V GaN fin JFET, revealing a t_{SC} of 30.5 μs at 400 V V_{BUS} [see Fig. 15(a)], 17.0 μs at 600 V, and 11.6 μs at 800 V (i.e., the BV_{AVA}). To date, these t_{SC} are the longest reported in 600–700 V E-mode unipolar power transistors [see Fig. 15(b)]. Additionally, GaN fin JFETs fail with an open-circuit signature in SC tests, exhibiting a retained BV_{AVA}. This failure signature is highly desirable for system applications. In contrast, most of the other transistors are reported to fail short under the SC stress. GaN fin JFETs are also reported to be robust in repetitive 10 μs, 400 V SC tests [146] and even up to V_{BUS} of 600 V [164], the V_{BUS} close to its rated voltage.

The underlying device physics that enables an SC capability at BV_{AVA} is also found to be the "avalanche through fin," as illustrated in Fig. 15(c) [165]. In this condition, the thermal (I_{AVA}) stress is mainly located at the fin channel, which is separated from the main blocking junction below the p-GaN gate that supports BV_{AVA}. Hence, when device fails thermally, the BV_{AVA} usually retains, enabling the open-circuit failure signature. This reflects the overall robustness of GaN fin JFETs under the concurrence of overvoltage and overcurrent.

IX. Radiation Robustness

The use of GaN devices is attractive in space, aeronautical, and defense applications, where system weight is at a premium. Devices for these applications must demonstrate tolerance to high doses of radiation exposure. While GaN as a material is inherently radiation hardened due to a high displacement threshold energy (the energy required to create a displacement in the lattice of the material) and ionization threshold energy (the mean energy required by a high energy particle to create an electron-hole pair), radiation hardness of GaN devices depends upon the device design and material quality [253]. The physics and outcomes of radiation damage in lateral GaN HEMTs differ from those in traditional vertical Si and SiC FETs.

Device-level radiation effects can be grouped into three categories: total ionizing dose (TID), displacement damage, and single-event effects (SEEs). These effects, and their relation to local physical processes in GaN HEMTs, are outlined in Fig. 16(a). TID effects are induced by the deposition of energy by ionizing radiation due to either photons (X-rays) or ions, while displacement damage effects are due to the displacement of atoms in the irradiated device due to energy transfer. SEEs are due to the transient response of the device to the ionization induced during an instantaneous strike by a radiation particle. Both TID and displacement damage induce changes in the device, which are a function of the total dose of radiation absorbed, while SEE are transient events that may induce instantaneous device degradation or failure. SEEs, in particular, are of primary concern in power devices due to the potential for failed devices to induce unrecoverable HSFs in converter circuits [254]. The state of research into these effects in E-mode GaN HEMTs is discussed in the following text.

A. Total Ionizing Dose

Due to the lack of gate oxide, p-gate GaN HEMTs are expected to be generally tolerant to TID effects. Recent work reveals that the TID effects in GaN HEMTs are bias dependent [255], which is also reported in SP-HEMTs and HD-GITs. SP-HEMTs show negligible V_{TH} shift when all terminals are grounded up to a dose of 1 MRad(Si); a negative V_{TH} shift is observed over a 1 MRad(Si) test under V_{DS} of 80% of the rated voltage [256]. Comparison between 80 and 200 V rated devices demonstrates a larger V_{TH} shift in the higher voltage device [257]. Little work has been found on radiation studies of composite GaN devices, but such devices are expected to be

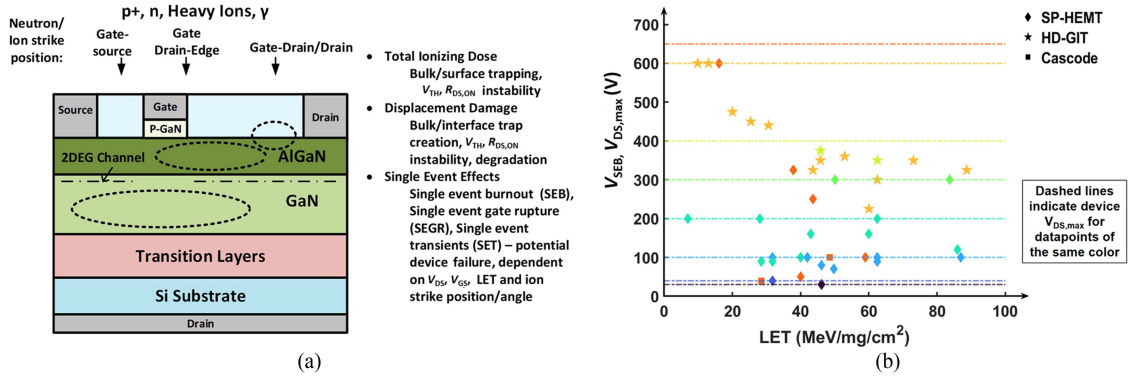


Fig. 16. (a) Radiation types and strike location in relation to the structure and damage induced in an HEMT. (b) Compilation of V_{SEB} values found for E-mode HEMTs in the literature as a function of $V_{\mathrm{DS,MAX}}$ and LET.

more susceptible to TID effects due to the use of an Si MOSFET with the gate oxide. As annealing is shown to reverse some of the effects of TID exposure in GaN HEMTs [255], further investigation is needed of TID effects on GaN devices under the switching conditions where self-heating may be significant.

Fewer studies have been performed on the effect of TID on the dynamic characteristics of GaN HEMTs. HD-GITs show minimal D-$R_{\mathrm{DS,ON}}$ shift after exposure to 300 kRad of Co-60 exposure (1 MeV X-rays) [258]. SP-HEMTs also show minimal change after 300 kRad of 10 keV X-ray TID exposure [259].

B. Displacement Damage

Displacement damage effects in GaN HEMTs are primarily a function of the energy, mass, and charge of the irradiating particle. These effects can be quantified by the nonionizing energy loss deposited by the interaction of the radiation particle with the material of the device, which can be related to the displacement damage dose [253].

Various HD-GITs and SP-HEMTs are tested both under bias in [260] under proton and neutron irradiation to a maximum total fluence of 6×10^{15} cm^{-2}. The devices, if unbiased, can survive up to maximum fluence, while failures are observed in devices biased at high OFF-state biases. Similar results are found in [257], where SP-HEMTs are exposed to total fast neutron fluence of 1×10^{12} to 1×10^{15} cm^{-2}. A reduction in I_{GSS} is observed a function of fluence, while V_{TH} and $R_{\mathrm{DS,ON}}$ do not change as a function of exposure. In contrast, a study of a research grade SP-HEMT at high proton fluence in [261] shows a negative V_{TH} shift and a fivefold increase in $R_{\mathrm{DS,ON}}$ after irradiation with a 5 MeV proton dose of 2×10^{15} cm^{-2}. These results are attributed to the creation of defects in the p-GaN gate. Interestingly, irradiation of HD-GITs with high energy protons up to a fluence of 6×10^{14} cm^{-2} in [262] demonstrates a small positive V_{TH} shift. More work is needed to understand the susceptibility mechanisms between the SP-HEMT and HD-GIT designs to radiation displacement damage effects.

C. Single-Event Effects

SEEs are transient events due to the strike of a high energy radiation particle into a device structure under bias. The creation of a large track of electron-hole pairs in devices under bias can lead to device degradation or instantaneous failure. While SEE can be important in strikes by high energy neutrons and protons, the primary cause of SEE in operational devices is due to heavy ion strikes originating from high energy cosmic rays. Primary metrics for quantifying the potential for damage from a heavy ion strike is the linear energy transfer (LET) of the ion, and the range of the ion in the structure. LET is related to the magnitude of charge generation and transfer, while the range of the ion (as a function of the device structure) will determine the susceptible areas of the device to SEE events [254]. Both device structure and bias condition influence the susceptibility of a device to SEE.

Three SEE types are important in power devices: single-event burnout (SEB), single-event gate rupture (SEGR), and single-event transients (SETs). Due to the lack of a gate oxide in most GaN HEMT structures, SEGR is not expected to be important. Most work reviewed here follows the MIL-STD-750 Method 1080 for testing the device robustness against SEE effects: devices are biased in the OFF-state to a fraction of the rated V_{DS}, and drain current is observed during irradiation until a failure transient is observed [263]. The V_{DS} at which SEB is observed is denoted as V_{SEB} and can be used to give a baseline for the SOA of the HEMT under heavy ion irradiation of a given LET. Additional device damage can occur from the effects of SETs during heavy ion exposure of HEMTs for V_{DS} bias less than V_{SEB}, such as increased OFF-state drain and gate leakage [264].

When a heavy ion strikes the high-field gate–drain region of an HEMT, a short can be induced between the gate and drain, which can be due to the initiation of impact ionization in the access region or dielectric passivation failure. Other SEEs include drain-to-substrate shorting and potential charge amplification effects in the GaN buffer layer. Several SP-HEMTs rated at 40 V, 100 V, and 200 V are tested in [264] under ^{127}I irradiation at 276 MeV at rated voltage. SEB is observed in the higher voltage rated devices with cumulative damage due to strikes leading SEB. In SEB, drain current is shown to spike to a short condition, while the gate current shows a transient than a recovery, potentially indicating failure between the drain and source rather than the gate and the drain.

In [265], HD-GIT and SP-HEMT devices are tested under variable LET, dc bias, and incident angle. As in [264], devices show increased SEE susceptibility at higher blocking bias.

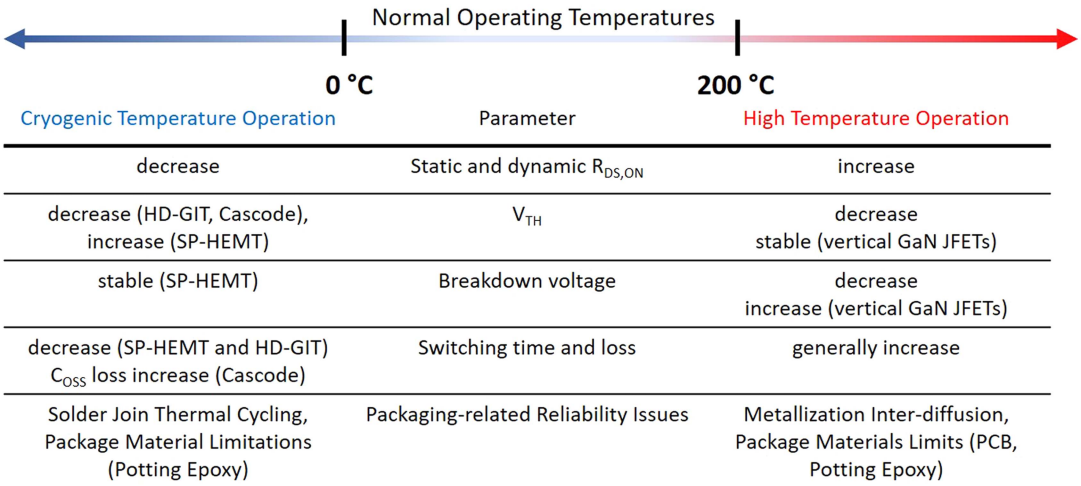


Fig. 17. Summary of the reported device parametric shifts and packaging-related issues of GaN power devices at extreme temperatures.

Interestingly, V_{SEB} is shown to decrease for both HD-GITs and SP-HEMTs as incident ion angle is increased to 60°. Postfailure analysis shows failure points at the drain edge of the gate; and a failure mechanism is proposed [266]. Further testing of HD-GITs in [267] confirmed the angular dependence of SEE. Postfailure analysis of these tests shows failures in devices tested at perpendicular ion incidence that induced direct damage from the drain contact to the substrate. Parallel incidence ions are shown to result in failures in which thermal failure destroyed and bridged the gate to the drain contact. A dielectric failure mode in the intermetallic region between source and drain is found in [268] for SP-HEMTs.

In comparison with SP-HEMTs and HD-GITs, testing of 650 V cascode devices showed significantly reduced V_{SEB}, at 100 V under 48.5 MeVcm^2/mg in [268] and 40 V under 28.5 MeVcm^2/mg in [269]. A range of experimentally determined V_{SEB} values found in the literature as a function of device voltage and LET of the irradiation is shown in Fig. 16(b).

Due to the dependence of V_{SEB} on V_{DS} (and V_{GS}) bias, SOAs can be established for derating of GaN HEMTs to consider SEE dependence. Several companies now offer SEE-rated components, including EPC-Space and Renesas. EPC-Space SP-HEMTs are offered with SEE SOAs up to 300 V at LET values up to 83.7 MeVcm^2/mg [270]. However, significant questions remain unanswered about the dependence of SEE in GaN devices on device architecture, bias, and temperature, especially under switched conditions. As the susceptibility of GaN devices is a strong function of operation condition, interplay between the failure modes must be examined to determine the overall reliability of a GaN HEMT for a radiation critical application.

X. Extreme Temperature Robustness

Here, we define the extreme temperature range as device operation at temperatures below 0 °C or above 200 °C (as demarcated in Fig. 17). From an application perspective, the ability of power electronics to operate at cryogenic temperatures is desirable for weight-sensitive transport applications, such as shipping [271] and aircraft [272]. The emergence of reliable power devices that can operate at cryogenic temperature is especially important for aeronautics and space power systems where temperature extremes to below −200 °C [273] can be expected over the operating life of deep space missions. For these applications, the reliability and performance studies of the integrated device-package system, rather than the device alone, are necessary. Packaging-based effects can be important at cryogenic temperatures due to thermal cycling issues and changing material properties of solder joints and die bonds [274]. This section will focus on the extrapolated intrinsic performance and reliability issues of E-mode GaN HEMTs at extreme temperatures but will examine temperature-related packaging reliability issues that have been shown to occur in the experimental literature when pertinent.

A. Cryogenic Temperature Performance and Reliability

Due to the nature of the 2DEG channel, the performance of GaN HEMTs at cryogenic and high-temperature extremes differs from that found in the traditional vertical devices in Si or SiC. Studies on the dc characteristics of E-mode GaN HEMTs demonstrate a general decrease in $R_{\mathrm{DS,ON}}$ as temperature decreases [275], [276], [277]. This effect is attributed to the increase in channel mobility with decreasing temperature under both the gate and the access region. Due to the 2DEG channel making up the majority of the ON-state resistance of GaN HEMT, no carrier freeze-out effects on $R_{\mathrm{DS,ON}}$ occur as temperature decreases. HD-GITs were found in [275] to have a smaller decrease in $R_{\mathrm{DS,ON}}$ with temperature, which is attributed to increased trap state density and, hence, decreased channel mobility due to the recessed etch gate.

The V_{TH} behavior as a function of temperature has been shown to differ among HD-GIT, SP-HEMT, and cascode GaN HEMT. Tests in [275] demonstrated a negative temperature coefficient for V_{TH} down to 4.2 K for both HD-GIT and cascode devices, with a larger temperature variation found in the Cascode device due to the driving Si MOSFET. In contrast, V_{TH} in SP-HEMTs tested in that work and, in [276] and [277], was found to have a positive temperature coefficient due to the

dominance of Schottky barrier height variation with temperature on V_{TH} level in the SP-HEMT. GaN SP-HEMT static *BV* was found to be relatively stable as a function of temperature down to 100 K [277]. Several studies in D-mode GaN HEMTs have shown that dynamic $R_{DS,ON}$ sees a strong temperature dependence upon a variety of device processing, buffer design, and surface state-related issues. Similar issues are, thus, expected in E-mode GaN HEMT designs [278], [279], [280]. A study in [281] examined the effect of cryogenic temperatures in a commercial SP-HEMT device, finding that dynamic $R_{DS,ON}$ measured at 400 V decreased with temperature with a similar temperature dependence as the static $R_{DS,ON}$.

Dynamic switching performance of commercial SP-HEMT and HD-GIT at cryogenic temperatures was investigated in [275], [277], and [281]. Tests of the HSW performance of SP-HEMTs were examined in [277] and [281] using a DPT. The turn-ON and turn-OFF energy loss was found to decrease by 30% as temperature decreased from 298 to 133 K, with the majority of switching loss due to the turn-ON transient. Work to measure the effective soft-switching loss for SP-HEMT, HD-GIT, and cascode devices as a function of temperature was performed in [275] down to 4.2 K using the Sawyer–Tower method to measure the C_{OSS} loss. Small temperature variations were found for one SP-HEMT and the HD-GIT device, while the tested cascode device showed a large loss increase as the temperature fell below 200 K. The distinct temperature dependence is found to be manufacturer dependent and not a function of device structure.

To the best of our knowledge, long-term reliability of GaN HEMTs at cryogenic temperatures has not yet been studied in depth. The work performed in [277] found several failure modes related to the increase in *di/dt* as temperature decreased, resulting in premature gating of the upper transistor in the phase leg due to the intrinsic parasitic inductance in the device packaging.

B. Elevated Temperature Performance and Reliability

High-temperature performance and reliability of GaN HEMTs, particularly industrial devices, have only recently been investigated due to the challenges in developing high-temperature packages [235]. An initial study of experimental nonrecessed GaN GITs was performed in [282] up to 420 °C for four different buffer designs. V_{TH} in all four device designs was found to have a similar negative temperature coefficient, which resulted in a normally ON behavior for a specific buffer at 420 °C. $R_{DS,ON}$ was found to increase with temperature due to the high-temperature degradation of 2DEG mobility and contact resistance. Similar work in [283] examined the dc characteristics of bare-die R&D and packaged commercial SP-HEMTs up to 500 °C and 250 °C, respectively, and found a similar increase in $R_{DS,ON}$ and small negative temperature coefficient for V_{TH} with increasing temperature. High-temperature static characterization of industrial 1.2 kV vertical GaN Fin-JFETs was reported in [250], revealing a V_{TH} shift below 0.15 V and $R_{DS,ON}$ increase by two times at 200 °C as compared with those at 25 °C; the *BV* at 200 °C is considerably higher than that at 25 °C due to the avalanche capability.

In general, the switching time and loss of GaN HEMTs are expected to increase with temperature. The switching loss of commercial SP-HEMTs was reported in [284] to show a larger temperature coefficient than SiC MOSFETs, particularly at high currents. In comparison, dynamic switching characteristics at high temperature of an early commercial cascode device were investigated in [285] up to 200 °C, with no significant variation in switching speed or loss observed as temperature increased.

As for device reliability, V_{DS} step-stress testing of the R&D GaN HEMTs in [282] up to breakdown showed a decrease in the observed V_{DS} failure voltage from 380 V at room temperature to 160 V at 420 °C, which was attributed to vertical leakage through the epitaxial stack. A high-temperature robustness test in nitrogen gas of SP-HEMTs in [283] found that V_{TH} remained stable over 20 days of exposure, while $R_{DS,ON}$ and saturation current were found to degrade depending upon the presence of bonding pads, indicating the determining role of packaging in device reliability at high-temperature extremes. A recent review article has discussed in detail the power device packaging for high-temperature applications [235].

XI. Immediate Research Needs

While there has been much advance in the understanding of GaN device stability, reliability, and robustness, there are still a number of immediate research needs. These gaps are important for the increased adoption of GaN devices in power electronics' applications. Some of these research needs include the following.

1) Full understanding of trapping locations (e.g., surface, channel, and buffer) and energetics (e.g., shallow, deep, and acceptor- or donor-type) that correlate to each stability, reliability, and robustness issue, which allows for addressing these issues through the improvements in material, processing, and device designs.
2) New circuit methods for the in situ measurement and monitoring of device parametric stability in high-frequency switching with minimal disturbance on converter operations.
3) Accurate models that describe the device failure rate as a function of operating stimuli (i.e., voltage, current, and their concurrence under various switching schemes) for both the device's drain–source loop and gate loop.
4) Reliability, robustness, and qualification of GaN devices for application-specific mission profiles, e.g., electric vehicle powertrains, solar and wind power conversion, power supplies, etc.
5) Improved compact and TCAD models accounting for the device dynamic characteristics (e.g., D-$R_{DS,ON}$, V_{TH} shift, and C_{OSS} loss) that are ideally applicable to multiple types of GaN devices.
6) Protection methodologies for the necessary fast turn-OFF of GaN HEMTs under SC, overvoltage, and surge-energy events.
7) Full understanding of gate reliability and robustness under application-use conditions, as well as lifetime models accounting for intrinsic and extrinsic failures.

8) Further radiation qualifications and investigations on the TID and SSE breakdowns of the different GaN device structures for integration into the aeronautical and aerospace industries.
9) Further qualification and evaluation of GaN power devices under extreme temperature conditions for aerospace applications and the emerging quantum computing applications.
10) Stability, reliability, and robustness of high-current GaN devices and modules, accounting for the packaging-device interplays.
11) Device innovations, e.g., D-$R_{\mathrm{DS,ON}}$ free GaN HEMTs, avalanche and SC capable GaN HEMTs, vertical GaN devices, higher voltage and higher current GaN devices.
12) Stability, reliability, and robustness of GaN power technologies that do not possess good counterparts in Si and SiC, e.g., the full-GaN-integrated power device and IC, the single-chip bidirectional GaN switch.

XII. Summary

GaN devices, both discrete and composite, offer a plurality of benefits to power electronics' applications. Since these devices have only recently entered the commercial markets and they possess significantly different device structures and physics as compared with Si and SiC power devices, many stability, reliability, and robustness questions remain to be addressed before their full integration into various applications.

This article presents a comprehensive discussion on the stability, reliability, and robustness issues of GaN devices, with the particular emphasis on their presence under dynamic switching conditions and their impact on power electronics' systems. Some key takeaways include the following.

1) Traditional Si-based qualification standards are not sufficient for GaN HEMTs; GaN device vendors have published many extended reliability/stability/robustness data, but many evaluation methods have not been standardized.
2) GaN HEMTs suffer from parametric instability in high-frequency switching; the D-$R_{\mathrm{DS,ON}}$ and C_{OSS} loss issues can induce additional conduction and switching losses, respectively; the characterization of these parametric shifts is preferable to be performed under or best similar to the application-use conditions.
3) GaN HEMTs possess limited SC capabilities and minimal avalanche capabilities; the SC capabilities can be significantly impacted by bus voltage; the dynamic BV differs from the static BV and is the key determining factor for the surge energy and overvoltage robustness; GaN HEMTs can be designed to withstand higher surge energy with a larger overvoltage margin and higher C_{OSS}; the GaN HEMT overvoltage robustness could become inferior at high frequencies.
4) GaN HEMTs' lifetime is preferable to be characterized based on the application-use switching conditions; the gate lifetime in p-gate HEMT can become a limiting factor of the overall device lifetime.
5) Vertical GaN devices show good promise for realizing a reduced parametric instability as well as good avalanche and SC robustness, which is comparable or even superior to SiC and Si devices.
6) The radiation ruggedness is strongly dependent on the OFF-state blocking bias; significant voltage derating must be considered for radiation critical applications.
7) GaN HEMTs show particular promise for cryogenic temperature applications due to the unique properties of the 2DEG channel; preliminary promising results have also been reported for high-temperature applications.

Acknowledgment

The authors would like to thank Prof. F. Udrea at the University of Cambridge and S. Bahl at Texas Instrument for long collaborations and discussions, the discussion with Prof. J. Kolar in the 2022 CPES Annual Conference and the discussions with E. Persson from Infineon, L. Balogh from Texas Instrument, as well as V. Blasko and T. Byrd from Lockheed Martin during the 2022 CPES Research Conference, and other industrial GaN collaborators, such as Innoscience, Visic Technologies, NexGen Power Systems, Cambridge GaN Devices, etc.

References

[1] Y. Zhang, F. Udrea, and H. Wang, "Multidimensional device architectures for efficient power electronics," *Nature Electron.*, vol. 5, no. 11, pp. 723–734, Nov. 2022, doi: 10.1038/s41928-022-00860-5.
[2] H. Amano et al., "The 2018 GaN power electronics roadmap," *J. Phys. D, Appl. Phys.*, vol. 51, no. 16, Mar. 2018, Art. no. 163001, doi: 10.1088/1361-6463/aaaf9d.
[3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.
[4] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.
[5] K. H. Teo et al., "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *J. Appl. Phys.*, vol. 130, no. 16, Oct. 2021, Art. no. 160902, doi: 10.1063/5.0061555.
[6] T. McDonald and S. W. Butler, "Progress and current topics of JEDEC JC-70.1 power GaN device quality and reliability standards activity: Or: What is the avalanche capability of your GaN transistor?," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2021, pp. 1–6, doi: 10.1109/IRPS46558.2021.9405225.
[7] G. Meneghesso et al., "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008, doi: 10.1109/TDMR.2008.923743.
[8] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Rel.*, vol. 49, no. 9/11, pp. 1200–1206, Sep. 2009, doi: 10.1016/j.microrel.2009.07.003.
[9] G. Meneghesso et al., "Reliability and parasitic issues in GaN-based power HEMTs: A review," *Semicond. Sci. Technol.*, vol. 31, no. 9, Aug. 2016, Art. no. 093004, doi: 10.1088/0268-1242/31/9/093004.
[10] J. A. del Alamo and E. S. Lee, "Stability and reliability of lateral GaN power field-effect transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4578–4590, Nov. 2019, doi: 10.1109/TED.2019.2931718.
[11] M. Meneghini et al., "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, Nov. 2021, Art. no. 181101, doi: 10.1063/5.0061354.
[12] Y. Zhang et al., "GaN FinFETs and trigate devices for power and RF applications: Review and perspective," *Semicond. Sci. Technol.*, vol. 36, no. 5, Mar. 2021, Art. no. 054001, doi: 10.1088/1361-6641/abde17.

[13] Y. Zhang and T. Palacios, "(Ultra)wide-bandgap vertical power FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.

[14] L. Nela, M. Xiao, Y. Zhang, and E. Matioli, "A perspective on multi-channel technology for the next-generation of GaN power devices," *Appl. Phys. Lett.*, vol. 120, no. 19, May 2022, Art. no. 190501, doi: 10.1063/5.0086978.

[15] H. W. Then et al., "Advanced scaling of enhancement mode high-K gallium nitride-on-300mm-Si(111) transistor and 3D layer transfer GaN-silicon finfet CMOS integration," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 11.1.1–11.1.4, doi: 10.1109/IEDM19574.2021.9720710.

[16] H. W. Then et al., "High-K gate dielectric depletion-mode and enhancement-mode GaN MOS-HEMTs for improved OFF-state leakage and DIBL for power electronics and RF applications," in *Proc. IEEE Int. Electron Devices Meeting*, 2015, pp. 16.3.1–16.3.4, doi: 10.1109/IEDM.2015.7409710.

[17] M. Xiao, Y. Ma, K. Liu, K. Cheng, and Y. Zhang, "10 kV, 39 mΩ·cm2 multi-channel AlGaN/GaN Schottky barrier diodes," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 808–811, Jun. 2021, doi: 10.1109/LED.2021.3076802.

[18] M. Xiao et al., "Multi-channel monolithic-cascode HEMT (MC2-HEMT): A new GaN power switch up to 10 kV," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 5.5.1–5.5.4, doi: 10.1109/IEDM19574.2021.9720714.

[19] M. Meneghini et al., "Degradation mechanisms of GaN-based vertical devices: A review," *Physica Status Solidi A*, vol. 217, no. 7, 2020, Art. no. 1900750, doi: 10.1002/pssa.201900750.

[20] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: A review and outlook," *J. Phys. D, Appl. Phys.*, vol. 51, no. 27, 2018, Art. no. 273001, doi: 10.1088/1361-6463/aac8aa.

[21] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, "Materials and processing issues in vertical GaN power electronics," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 75–84, May 2018, doi: 10.1016/j.mssp.2017.09.033.

[22] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of cascode GaN HEMTs in unclamped inductive switching," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4148–4160, Apr. 2022, doi: 10.1109/TPEL.2021.3122740.

[23] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of cascode GaN HEMTs under repetitive overvoltage and surge energy stresses," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 363–369, doi: 10.1109/APEC42165.2021.9487252.

[24] Q. Song et al., "Evaluation of 650V, 100A direct-drive GaN power switch for electric vehicle powertrain applications," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, 2021, pp. 28–33, doi: 10.1109/WiPDA49284.2021.9645143.

[25] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Failure mechanisms of cascode GaN HEMTs under overvoltage and surge energy events," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2021, pp. 1–7, doi: 10.1109/IRPS46558.2021.9405208.

[26] J. P. Kozak et al., "Degradation and recovery of GaN HEMTs in overvoltage hard switching near breakdown voltage," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 435–446, Jan. 2023, doi: 10.1109/TPEL.2022.3198838.

[27] J. P. Kozak, R. Zhang, J. Liu, K. D. T. Ngo, and Y. Zhang, "Degradation of SiC MOSFETs under high-bias switching events," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5027–5038, Oct. 2022, doi: 10.1109/JESTPE.2021.3064288.

[28] S. Pu, F. Yang, B. T. Vankayalapati, and B. Akin, "Aging mechanisms and accelerated lifetime tests for SiC MOSFETs: An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 1232–1254, Feb. 2022, doi: 10.1109/JESTPE.2021.3110476.

[29] R. Zhang, X. Lin, J. Liu, S. Mocevic, D. Dong, and Y. Zhang, "Third quadrant conduction loss of 1.2–10 kV SiC MOSFETs: Impact of gate bias control," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2033–2043, Feb. 2021, doi: 10.1109/TPEL.2020.3006075.

[30] R. Zhang and Y. Zhang, "Power device breakdown mechanism and characterization: Review and perspective," *Jpn. J. Appl. Phys.*, vol. 62, Feb. 2023, Art. no. SC0806, doi: 10.35848/1347-4065/acb365.

[31] M. Rittner, M. Thoben, and K. Kriegel, "Automotive qualification routines for power electronics components in electrified powertrains," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, 2018, pp. 1–6.

[32] P. Parikh et al., "(Invited) 650 volt GaN commercialization reaches automotive standards," *ECS Trans.*, vol. 80, no. 7, Aug. 2017, Art. no. 17, doi: 10.1149/08007.0017ecst.

[33] "Temperature, bias, and operating life | JEDEC," Accessed on: Jan. 7, 2022. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-22-a108c

[34] S. Khalil et al., "Trap-related parametric shifts under DC bias and switched operation life stress in power AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014, pp. CD.4.1–CD.4.9, doi: 10.1109/IRPS.2014.6861127.

[35] J. Lin, H. Liu, S. Wang, C. Liu, M. Li, and L. Wu, "Effect of the high-temperature off-state stresses on the degradation of AlGaN/GaN HEMTs," *Electronics*, vol. 8, no. 11, Nov. 2019, Art. no. 1339, doi: 10.3390/electronics8111339.

[36] T. Kikkawa et al., "600 V JEDEC-qualified highly reliable GaN HEMTs on Si substrates," in *Proc. IEEE Int. Electron Devices Meeting*, 2014, pp. 2.6.1–2.6.4, doi: 10.1109/IEDM.2014.7046968.

[37] O. Chihani et al., "Temperature and voltage effects on HTRB and HTGB stresses for AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. P–RT.2–1–P–RT.2–6, doi: 10.1109/IRPS.2018.8353685.

[38] L. Brunel et al., "Analysis of Schottky gate degradation evolution in AlGaN/GaN HEMTs during HTRB stress," *Microelectron. Rel.*, vol. 53, no. 9/11, pp. 1450–1455, Sep. 2013, doi: 10.1016/j.microrel.2013.07.095.

[39] M. Meneghini et al., "Power GaN HEMT degradation: From time-dependent breakdown to hot-electron effects," in *Proc. IEEE Int. Electron Devices Meeting*, 2018, pp. 30.5.1–30.5.4, doi: 10.1109/IEDM.2018.8614605.

[40] L. RuGuan, W. YuanSheng, Z. Chang, L. XueYang, L. Ping, and H. Yun, "Impact of high temperature reverse bias (HTRB) stress on the degradation of AlGaN/GaN HEMTs," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, 2014, pp. 1–2, doi: 10.1109/EDSSC.2014.7061108.

[41] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic breakdown voltage of GaN power HEMTs," in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 23.3.1–23.3.4, doi: 10.1109/IEDM13553.2020.9371904.

[42] C. DiMarino and B. Hull, "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 263–267, doi: 10.1109/WiPDA.2015.7369294.

[43] F. Yang, C. Xu, and B. Akin, "Characterization of threshold voltage instability under off-state drain stress and its impact on p-GaN HEMT performance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4026–4035, Aug. 2021, doi: 10.1109/JESTPE.2020.2970335.

[44] R. L. Kini et al., "An investigation of frequency dependent reliability and failure mechanism of pGaN gated GaN HEMTs," *IEEE Access*, vol. 8, pp. 137312–137321, 2020, doi: 10.1109/ACCESS.2020.3011453.

[45] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong, and K. J. Chen, "Frequency- and temperature-dependent gate reliability of Schottky-type p-GaN gate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3453–3458, Aug. 2019, doi: 10.1109/TED.2019.2924675.

[46] J. P. Kozak et al., "An analytical model for predicting turn-on overshoot in normally-off GaN HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 99–110, Mar. 2020, doi: 10.1109/JESTPE.2019.2947152.

[47] A. Barchowsky et al., "Analytical and experimental optimization of external gate resistance for safe rapid turn on of normally off GaN HFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1958–1963, doi: 10.1109/APEC.2017.7930966.

[48] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, "An overview of normally-off GaN-based high electron mobility transistors," *Materials*, vol. 12, no. 10, Jan. 2019, Art. no. 1599, doi: 10.3390/ma12101599.

[49] C. Xu, F. Yang, E. Ugur, S. Pu, and B. Akin, "Performance degradation of GaN HEMTs under accelerated power cycling tests," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 4, pp. 269–277, Dec. 2018, doi: 10.24295/CPSSTPEA.2018.00027.

[50] J. Franke, G. Zeng, T. Winkler, and J. Lutz, "Power cycling reliability results of GaN HEMT devices," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 467–470, doi: 10.1109/ISPSD.2018.8393704.

[51] M. A. González-Sentís, P. Tounsi, A. Bensoussan, and A. Dufour, "Degradation indicators of power-GaN-HEMT under switching power-cycling," *Microelectron. Rel.*, vol. 100–101, Sep. 2019, Art. no. 113412, doi: 10.1016/j.microrel.2019.113412.

[52] M. A. González-Sentís, P. Tounsi, A. Bensoussan, and A. Dufour, "Drift effects and trap analysis of power-GaN-HEMT under switching power cycling," in *Proc. 8th Int. Conf. Sci. Electron., Technol. Inf. Telecommun.*, 2020, vol. 2, pp. 185–193, doi: 10.1007/978-3-030-21009-0_17.

[53] "Reliability report phase 14," Accessed on: Jan. 23, 2023. [Online]. Available: https://epc-co.com/epc/design-support/gan-fet-reliability/reliabilityreportphase14

[54] "Gallium nitride–reliability and qualification of CoolGaN^{TM} GIT HEMTs–infineon technologies," Accessed on: Jan. 23, 2023. [Online]. Available: https://www.infineon.com/cms/en/product/gated-document/gallium-nitride-reliability-and-qualification-of-coolgan-git-hemts-2-of-5-5546d46266a498f50166c9bebef322aa/

[55] "GaN semiconductors qualification and reliability," *GaN Systems*, Accessed on: Jan. 23, 2023. [Online]. Available: https://gansystems.com/reliability/

[56] "Quality & reliability," *Transphorm*, Accessed on: Jan. 23, 2023. [Online]. Available: https://www.transphormusa.com/quality-reliability/

[57] M.-C. Lin et al., "New circuit topology for system-level reliability of GaN," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 299–302, doi: 10.1109/ISPSD.2019.8757683.

[58] G. Zu et al., "Review of pulse test setup for the switching characterization of GaN power devices," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3003–3013, Jun. 2022, doi: 10.1109/TED.2022.3168238.

[59] J. Gareau, R. Hou, and A. Emadi, "Review of loss distribution, analysis, and measurement techniques for GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7405–7418, Jul. 2020, doi: 10.1109/TPEL.2019.2954819.

[60] M. Meneghini et al., "Temperature-dependent dynamic R_{ON} in GaN-based MIS-HEMTs: Role of surface traps and buffer leakage," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 782–787, Mar. 2015, doi: 10.1109/TED.2014.2386391.

[61] M. Meneghini et al., "Trapping in GaN-based metal-insulator-semiconductor transistors: Role of high drain bias and hot electrons," *Appl. Phys. Lett.*, vol. 104, no. 14, Apr. 2014, Art. no. 143505, doi: 10.1063/1.4869680.

[62] S. Yang, S. Han, K. Sheng, and K. J. Chen, "Dynamic on-resistance in GaN power devices: Mechanisms, characterizations, and modeling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1425–1439, Sep. 2019, doi: 10.1109/JESTPE.2019.2925117.

[63] X. Li et al., "Investigating the current collapse mechanisms of p-GaN gate HEMTs by different passivation dielectrics," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 4927–4930, May 2021, doi: 10.1109/TPEL.2020.3031680.

[64] S. Stoffels et al., "The physical mechanism of dispersion caused by AlGaN/GaN buffers on Si and optimization for low dispersion," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2015, pp. 35.4.1–35.4.4, doi: 10.1109/IEDM.2015.7409833.

[65] R. Chu et al., "1200-V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, May 2011, doi: 10.1109/LED.2011.2118190.

[66] N. Modolo et al., "Cumulative hot-electron trapping in GaN-based power HEMTs observed by an ultrafast (10 V/ns) on-wafer methodology," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5019–5026, Oct. 2022, doi: 10.1109/JESTPE.2021.3077127.

[67] A. Minetto et al., "Hot-electron effects in AlGaN/GaN HEMTs under semi-ON DC stress," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4602–4605, Nov. 2020, doi: 10.1109/TED.2020.3025983.

[68] N. Modolo et al., "A physics-based approach to model hot-electron trapping kinetics in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 673–676, May 2021, doi: 10.1109/LED.2021.3067796.

[69] E. Fabris et al., "Hot-electron trapping and hole-induced detrapping in GaN-based GITs and HD-GITs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 337–342, Jan. 2019, doi: 10.1109/TED.2018.2877905.

[70] B. Butej, V. Padovan, D. Pogany, G. Pobegen, C. Ostermaier, and C. Koller, "Method to distinguish between buffer and surface trapping in stressed normally-on GaN GITs using the gate-voltage dependence of recovery time constants," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3087–3093, Jun. 2022, doi: 10.1109/TED.2022.3170293.

[71] A. Minetto et al., "Drain field plate impact on the hard-switching performance of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5003–5008, Oct. 2021, doi: 10.1109/TED.2021.3101182.

[72] N. Modolo et al., "Trap-state mapping to model GaN transistors dynamic performance," *Sci. Rep.*, vol. 12, no. 1, Dec. 2022, Art. no. 1755, doi: 10.1038/s41598-022-05830-7.

[73] Y. Yao et al., "Identification of semi-on-state current collapse in AlGaN/GaN HEMTs by drain current deep level transient spectroscopy," *IEEE Electron Device Lett.*, vol. 43, no. 2, pp. 200–203, Feb. 2022, doi: 10.1109/LED.2021.3135900.

[74] M. Cioni, N. Zagni, F. Iucolano, M. Moschetti, G. Verzellesi, and A. Chini, "Partial recovery of dynamic RON versus off-state stress voltage in p-GaN gate AlGaN/GaN power HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4862–4868, Oct. 2021, doi: 10.1109/TED.2021.3105075.

[75] S. Karboyan, M. J. Uren, Manikant, J. W. Pomeroy, and M. Kuball, "On the origin of dynamic RON in commercial GaN-on-Si HEMTs," *Microelectron. Rel.*, vol. 81, pp. 306–311, Feb. 2018, doi: 10.1016/j.microrel.2017.10.006.

[76] P. Moens et al., "Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs," in *Proc. IEEE Int. Electron Devices Meeting*, 2015, pp. 35.2.1–35.2.4, doi: 10.1109/IEDM.2015.7409831.

[77] Y. Cai, A. J. Forsyth, and R. Todd, "Impact of GaN HEMT dynamic on-state resistance on converter performance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1689–1694, doi: 10.1109/APEC.2017.7930926.

[78] P. J. Martínez, P. F. Miaja, E. Maset, and J. Rodríguez, "A test circuit for GaN HEMTs dynamic R_{ON} characterization in power electronics applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1456–1464, Sep. 2019, doi: 10.1109/JESTPE.2019.2912130.

[79] F. Yang, C. Xu, and B. Akin, "Experimental evaluation and analysis of switching transient's effect on dynamic on-resistance in GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10121–10135, Oct. 2019, doi: 10.1109/TPEL.2019.2890874.

[80] K. Zhong et al., "I_G- and V_{GS}-dependent dynamic R_{ON} characterization of commercial high-voltage p-GaN gate power HEMTs," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8387–8395, Aug. 2022, doi: 10.1109/TIE.2021.3104592.

[81] J. Joh and J. A. del Alamo, "A current-transient methodology for trap analysis for GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, Jan. 2011, doi: 10.1109/TED.2010.2087339.

[82] D. Jin and J. A. del Alamo, "Methodology for the study of dynamic ON-resistance in high-voltage GaN field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3190–3196, Oct. 2013, doi: 10.1109/TED.2013.2274477.

[83] B. Kohlhepp, D. Kübrich, M. Tannhäuser, A. Hoffmann, and T. Dürbaum, "Test setup for dynamic ON-state resistance measurement of high- and low-voltage GaN-HEMTs under hard and soft switching operations," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7740–7751, Oct. 2020, doi: 10.1109/TIM.2020.2985186.

[84] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Quantifying dynamic on-state resistance of GaN HEMTs for power converter design via a survey of low and high voltage devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4036–4049, Aug. 2021, doi: 10.1109/JESTPE.2020.3024930.

[85] T. Zhao, R. Burgos, and J. Xu, "Dynamic ON-resistance characterization of GaN HEMT under soft-switching condition," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, 2021, pp. 246–249, doi: 10.1109/WiPDA49284.2021.9645123.

[86] S. Li, S. Yang, S. Han, and K. Sheng, "Investigation of temperature-dependent dynamic RON of GaN HEMT with hybrid-drain under hard and soft switching," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 306–309, doi: 10.1109/ISPSD46842.2020.9170048.

[87] H. Wang, R. Xie, C. Liu, J. Wei, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic R_{ON} characterization and gate-drive design considerations," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6, doi: 10.1109/ECCE.2016.7855231.

[88] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of dynamic on-resistance in GaN transistors: Under soft- and hard-switching conditions," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2011, pp. 1–4, doi: 10.1109/CSICS.2011.6062461.

[89] T. Yao and R. Ayyanar, "A multifunctional double pulse tester for cascode GaN devices," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9023–9031, Nov. 2017, doi: 10.1109/TIE.2017.2694381.

[90] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-state resistance test and evaluation of GaN power devices under hard- and soft-switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019, doi: 10.1109/TPEL.2018.2844302.

[91] K. Li, P. L. Evans, and C. M. Johnson, "Characterisation and modeling of gallium nitride power semiconductor devices dynamic on-state resistance," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5262–5273, Jun. 2018, doi: 10.1109/TPEL.2017.2730260.

[92] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic on-resistance in GaN-on-Si HEMTs: Origins, dependencies, and future characterization frameworks," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5581–5588, Jun. 2020, doi: 10.1109/TPEL.2019.2955656.

[93] D. Jin and J. A. del Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 333–336, doi: 10.1109/ISPSD.2012.6229089.

[94] P. Moens et al., "On the impact of carbon-doping on the dynamic RON and off-state leakage current of 650V GaN power devices," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 37–40, doi: 10.1109/ISPSD.2015.7123383.

[95] "Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices," Accessed on: Aug. 20, 2021. [Online]. Available: https://www.jedec.org/standards-documents/docs/jep173

[96] X. Geng, C. Kuring, M. Tannhaeuser, and S. Dieckerhoff, "Experimental evaluation and analysis of dynamic on-resistance in hard- and soft-switching operation of a GaN GIT," in *Proc. PCIM Eur. Digit. Days; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–8.

[97] G. Zulauf, M. Guacci, J. M. Rivas-Davila, and J. W. Kolar, "The impact of multi-MHz switching frequencies on dynamic on-resistance in GaN-on-Si HEMTs," *IEEE Open J. Power Electron.*, vol. 1, pp. 210–215, Jul. 2020, doi: 10.1109/OJPEL.2020.3005879.

[98] K. Surakitbovorn and J. R. Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in *Proc. IEEE 18th Workshop Control Model. Power Electron.*, 2017, pp. 1–6, doi: 10.1109/COMPEL.2017.8013330.

[99] A. Barbato et al., "Fast system to measure the dynamic on-resistance of on-wafer 600 V normally off GaN HEMTs in hard-switching application conditions," *IET Power Electron.*, vol. 13, no. 11, pp. 2390–2397, 2020, doi: 10.1049/iet-pel.2019.1455.

[100] B. J. Galapon, A. J. Hanson, and D. J. Perreault, "Measuring dynamic on resistance in GaN transistors at MHz frequencies," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, 2018, pp. 1–8, doi: 10.1109/COMPEL.2018.8460051.

[101] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015, doi: 10.1109/TED.2015.2455072.

[102] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, "C_{OSS} measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 578–584, Jan. 2019, doi: 10.1109/TED.2018.2880952.

[103] A. Jafari et al., "Comparison of wide-band-gap technologies for soft-switching losses at high frequencies," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12595–12600, Dec. 2020, doi: 10.1109/TPEL.2020.2990628.

[104] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "C_{OSS} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.

[105] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019, doi: 10.1109/TPEL.2018.2874420.

[106] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. Rivas-Davila, "Output capacitance loss characterization of silicon carbide Schottky diodes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 865–878, Jun. 2019, doi: 10.1109/JESTPE.2019.2904290.

[107] Z. Tong, J. Roig-Guitart, T. Neyer, J. D. Plummer, and J. M. Rivas-Davila, "Origins of soft-switching C_{oss} losses in SiC power MOSFETs and diodes for resonant converter applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4082–4095, Aug. 2021, doi: 10.1109/JESTPE.2020.3034345.

[108] M. Guacci et al., "On the origin of the C_{oss}-losses in soft-switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019, doi: 10.1109/JESTPE.2018.2885442.

[109] S. Park and J. Rivas-Davila, "Power loss of GaN transistor reverse diodes in a high frequency high voltage resonant rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1942–1945, doi: 10.1109/APEC.2017.7930963.

[110] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal C_{OSS} and C_{OSS} losses of transistors based on nonlinear resonance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2242–2246, Mar. 2020, doi: 10.1109/TPEL.2019.2938922.

[111] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "A simple and accurate method to characterize output capacitance losses of GaN HEMTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6, doi: 10.1109/ECCE50734.2022.9948018.

[112] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "Output capacitance loss of GaN HEMTs in steady-state switching," *IEEE Trans. Power Electron.*, Mar. 2023, to be published.

[113] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10-kV SiC MOSFETs and diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, Jun. 2018, doi: 10.1109/TPEL.2017.2729892.

[114] N. Perera et al., "Analysis of large-signal output capacitance of transistors using Sawyer–Tower circuit," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3647–3656, Jun. 2021, doi: 10.1109/JESTPE.2020.2992946.

[115] J. Zhuang, G. Zulauf, J. Roig-Guitart, J. Plummer, and J. Rivas, "Small- and large-signal dynamic output capacitance and energy loss in GaN-on-Si power HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1819–1826, Apr. 2021, doi: 10.1109/TED.2021.3063062.

[116] M. Samizadeh Nikoo, R. Abdul Khadar, A. Jafari, M. Zhu, and E. Matioli, "Resonances on GaN-on-Si epitaxies: A source of output capacitance losses in power HEMTs," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 735–738, May 2021, doi: 10.1109/LED.2021.3064021.

[117] G. Meneghesso, M. Meneghini, C. De Santi, M. Ruzzarin, and E. Zanoni, "Positive and negative threshold voltage instabilities in GaN-based transistors," *Microelectron. Rel.*, vol. 80, pp. 257–265, Jan. 2018, doi: 10.1016/j.microrel.2017.11.004.

[118] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of threshold voltage shift in p-GaN gate AlGaN/GaN transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, Aug. 2018, doi: 10.1109/LED.2018.2847669.

[119] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017, doi: 10.1109/TPEL.2016.2610460.

[120] J. Wei et al., "Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019, doi: 10.1109/LED.2019.2900154.

[121] H. Xu, J. Wei, R. Xie, Z. Zheng, J. He, and K. J. Chen, "Incorporating the dynamic threshold voltage into the SPICE model of Schottky-type p-GaN gate power HEMTs," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5904–5914, May 2021, doi: 10.1109/TPEL.2020.3030708.

[122] K. Zhong, H. Xu, Z. Zheng, J. Chen, and K. J. Chen, "Characterization of dynamic threshold voltage in Schottky-type p-GaN gate HEMT under high-frequency switching," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 501–504, Apr. 2021, doi: 10.1109/LED.2021.3062656.

[123] J. Chen et al., "OFF-state drain-voltage-stress-induced VTH instability in Schottky-type p-GaN gate HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3686–3694, Jun. 2021, doi: 10.1109/JESTPE.2020.3010408.

[124] J. Wei, H. Xu, R. Xie, and K. J. Chen, "Principles and impacts of dynamic threshold voltage in a p-GaN gate high-electron-mobility transistor," *Semicond. Sci. Technol.*, vol. 36, no. 2, Jan. 2021, Art. no. 024006, doi: 10.1088/1361-6641/abd008.

[125] S. Stoffels et al., "Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2019, pp. 1–10, doi: 10.1109/IRPS.2019.8720411.

[126] W. Vandendaele et al., "A novel insight of pBTI degradation in GaN-on-Si E-mode MOSc-HEMT," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. 4B.2–4B.1–4B.2–6, doi: 10.1109/IRPS.2018.8353580.

[127] A. N. Tallarico et al., "PBTI in GaN-HEMTs with p-type gate: Role of the aluminum content on Delta_VTH and underlying degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 38–44, Jan. 2018, doi: 10.1109/TED.2017.2769167.

[128] R. Xie et al., "Switching transient analysis for normally-off GaN transistor with p-GaN gate in a phase-leg circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3711–3728, Apr. 2019, doi: 10.1109/TPEL.2018.2852142.

[129] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding divergent oscillation of a cascode GaN device under high-current turn-off condition," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 593–601, Jan. 2017, doi: 10.1109/TPEL.2016.2532799.

[130] X. Huang, W. Du, F. C. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET avalanche and achieving zero-voltage switching for cascode GaN devices," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 593–600, Jan. 2016, doi: 10.1109/TPEL.2015.2398856.

[131] T. Zhu, F. Zhuo, F. Zhao, F. Wang, and T. Zhao, "Quantitative model-based false turn-on evaluation and suppression for cascode GaN devices in half-bridge applications," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10166–10179, Oct. 2019, doi: 10.1109/TPEL.2018.2890680.

[132] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Investigation on the short-circuit oscillation of cascode GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6292–6300, Jun. 2020, doi: 10.1109/TPEL.2019.2947274.

[133] H. Li et al., "E-mode GaN HEMT short circuit robustness and degradation," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1995–2002, doi: 10.1109/ECCE.2017.8096401.

[134] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 256–263, Mar./Apr. 1995, doi: 10.1109/28.370271.

[135] "Electrical and electronics technical team roadmap," Energy Efficiency and Renewable Energy (EERE), Washington, DC, USA, Jun. 2013, doi: 10.2172/1220125.

[136] Z. Xu and F. Wang, "Experimental investigation of Si IGBT short circuit capability at 200°C," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 162–168, doi: 10.1109/APEC.2012.6165814.

[137] Fuji Electric, "REH984c.pdf," Tokyo, Japan, Accessed on: Jan. 7, 2022. [Online]. Available: https://www.fujielectric.com/products/semiconductor/model/igbt/application/box/doc/pdf/REH984c/REH984c.pdf

[138] C. Abbate, G. Busatto, A. Sanseverino, D. Tedesco, and F. Velardi, "Experimental study of the instabilities observed in 650V enhancement mode GaN HEMT during short circuit," *Microelectron. Rel.*, vol. 76–77, pp. 314–320, Sep. 2017, doi: 10.1016/j.microrel.2017.07.020.

[139] C. Abbate, G. Busatto, A. Sanseverino, D. Tedesco, and F. Velardi, "Failure mechanisms of enhancement mode GaN power HEMTs operated in short circuit," *Microelectron. Rel.*, vol. 100–101, Sep. 2019, Art. no. 113454, doi: 10.1016/j.microrel.2019.113454.

[140] H. Li et al., "Robustness of 650-V enhancement-mode GaN HEMTs under various short-circuit conditions," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1807–1816, Mar./Apr. 2019, doi: 10.1109/TIA.2018.2879289.

[141] A. Castellazzi, A. Fayyaz, S. Zhu, T. Oeder, and M. Pfost, "Single pulse short-circuit robustness and repetitive stress aging of GaN GITs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. 1–10, doi: 10.1109/IRPS.2018.8353593.

[142] D. Pappis, K. Goebel, and P. Zacharias, "Short circuit capability of 650 V normally off GaN E-HEMT and MOSFET-HEMT cascode," in *Proc. PCIM Europe; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2017, pp. 1–8.

[143] N. Badawi, A. E. Awwad, and S. Dieckerhoff, "Robustness in short-circuit mode: Benchmarking of 600V GaN HEMTs with power Si and SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7, doi: 10.1109/ECCE.2016.7855410.

[144] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Experimental study on the short-circuit instability of cascode GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1686–1692, Apr. 2020, doi: 10.1109/TED.2020.2974518.

[145] D. Bisi et al., "Short-circuit capability demonstrated for GaN power switches," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 370–375, doi: 10.1109/APEC42165.2021.9486987.

[146] R. Zhang et al., "Breakthrough short circuit robustness demonstrated in vertical GaN fin JFET," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6253–6258, Jun. 2022, doi: 10.1109/TPEL.2021.3138451.

[147] X. Huang et al., "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SCSOA)," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's*, 2014, pp. 273–276, doi: 10.1109/ISPSD.2014.6856029.

[148] I. Hwang et al., "Estimation of short circuit capability of GaN HEMTs using transient measurement," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1208–1211, Aug. 2021, doi: 10.1109/LED.2021.3090341.

[149] J. Sun, J. Wei, Z. Zheng, and K. J. Chen, "Short circuit capability characterization and analysis of p-GaN gate high-electron-mobility transistors under single and repetitive tests," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8798–8807, Sep. 2021, doi: 10.1109/TIE.2020.3009603.

[150] P. J. Martínez et al., "Unstable behaviour of normally-off GaN E-HEMT under short-circuit," *Semicond. Sci. Technol.*, vol. 33, no. 4, Mar. 2018, Art. no. 045006, doi: 10.1088/1361-6641/aab078.

[151] M. Fernández et al., "Short-circuit study in medium-voltage GaN cascodes, p-GaN HEMTs, and GaN MISHEMTs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9012–9022, Nov. 2017, doi: 10.1109/TIE.2017.2719599.

[152] M. Fernández et al., "Short-circuit capability in p-GaN HEMTs and GaN MISHEMTs," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 455–458, doi: 10.23919/ISPSD.2017.7988916.

[153] M. Fernández et al., "P-GaN HEMTs drain and gate current analysis under short-circuit," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 505–508, Apr. 2017, doi: 10.1109/LED.2017.2665163.

[154] T. Oeder, A. Castellazzi, and M. Pfost, "Experimental study of the short-circuit performance for a 600V normally-off p-gate GaN HEMT," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 211–214, doi: 10.23919/ISPSD.2017.7988925.

[155] F. D'Aniello, A. Fayyaz, A. Castellazzi, T. Oeder, and M. Pfost, "Damage accumulation in GaN GITs exposed to repetitive short-circuit," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 451–454, doi: 10.1109/ISPSD.2019.8757692.

[156] H. Li et al., "An ultra-fast short circuit protection solution for E-mode GaN HEMTs," in *Proc. 1st Workshop Wide Bandgap Power Devices Appl. Asia*, 2018, pp. 187–192, doi: 10.1109/WiPDAAsia.2018.8734686.

[157] J. Wu, W. Meng, F. Zhang, G. Dong, and J. Shu, "A short-circuit protection circuit with strong noise immunity for GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2432–2442, Feb. 2021, doi: 10.1109/TPEL.2020.3013984.

[158] X. Lyu et al., "A reliable ultrafast short-circuit protection method for E-mode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8926–8933, Sep. 2020, doi: 10.1109/TPEL.2020.2968865.

[159] F. Karakaya, O. S. Alemdar, and O. Keysan, "Layout-based ultrafast short-circuit protection technique for parallel-connected GaN HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6385–6395, Oct. 2021, doi: 10.1109/JESTPE.2021.3052611.

[160] R. Hou, J. Lu, Z. Quan, and Y. W. Li, "A simple desaturation-based protection circuit for GaN HEMT with ultrafast response," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6978–6987, Jun. 2021, doi: 10.1109/TPEL.2020.3040727.

[161] W. L. Jiang et al., "An integrated GaN overcurrent protection circuit for power HEMTs using SenseHEMT," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9314–9324, Aug. 2022, doi: 10.1109/TPEL.2022.3158655.

[162] A. Kanale and B. J. Baliga, "Achieving short circuit capability for 600 V GaN FETs using a gate-source-shorted Si depletion-mode MOSFET in series with the source," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2020, pp. 1–6, doi: 10.1109/WiPDAAsia49671.2020.9360275.

[163] D. Bisi et al., "Short-circuit protection for GaN power devices with integrated current limiter and commercial gate driver," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 181–185, doi: 10.1109/APEC43599.2022.9773446.

[164] R. Zhang et al., "Exceptional repetitive-short-circuit robustness of vertical GaN fin-JFET at high voltage," in *Proc. IEEE 34th Int. Symp. Power Semicond. Devices ICs*, 2022, pp. 205–208, doi: 10.1109/ISPSD49238.2022.9813618.

[165] R. Zhang et al., "Vertical GaN Fin JFET: A power device with short circuit robustness at avalanche breakdown voltage," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2022, pp. 1–8, doi: 10.1109/IRPS48227.2022.9764569.

[166] S. R. Bahl and P. Brohlin, "A new approach to validate GaN FET reliability to power-line surges under use-conditions," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2019, pp. 1–4, doi: 10.1109/IRPS.2019.8720479.

[167] A. Castellazzi et al., "Transient out-of-SOA robustness of SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2017, pp. 2A–3.1–2A–3.8, doi: 10.1109/IRPS.2017.7936255.

[168] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level reliability of GaN devices," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, pp. 4A–3–1–4A–3–6, doi: 10.1109/IRPS.2016.7574528.

[169] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-energy and overvoltage ruggedness of p-gate GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13409–13419, Dec. 2020, doi: 10.1109/TPEL.2020.2993982.

[170] R. Zhang, J. P. Kozak, J. Liu, M. Xiao, and Y. Zhang, "Surge energy robustness of GaN gate injection transistors," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–7, doi: 10.1109/IRPS45951.2020.9129324.

[171] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True breakdown voltage and overvoltage margin of GaN power HEMTs in hard switching," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 505–508, Apr. 2021, doi: 10.1109/LED.2021.3063360.

[172] R. Zhang, Q. Song, Q. Li, and Y. Zhang, "Overvoltage ruggedness and dynamic breakdown voltage of p-gate GaN HEMTs in high-frequency switching up to megahertz," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 175–180, doi: 10.1109/APEC43599.2022.9773713.

[173] R. Zhang, Q. Song, Q. Li, and Y. Zhang, "Overvoltage robustness of p-gate GaN HEMTs in high frequency switching up to megahertz," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6063–6072, May 2023, doi: 10.1109/TPEL.2023.3237985.

[174] "Addendum No. 5 to JESD24—Single pulse unclamped inductive switching (UIS) avalanche test method: | JEDEC," Accessed on: Nov. 27, 2019. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-24-5

[175] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectron. Rel.*, vol. 58, pp. 164–176, Mar. 2016, doi: 10.1016/j.microrel.2015.12.034.

[176] A. Fayyaz et al., "A comprehensive study on the avalanche breakdown robustness of silicon carbide power MOSFETs," *Energies*, vol. 10, no. 4, Apr. 2017, Art. no. 452, doi: 10.3390/en10040452.

[177] J. O. Gonzalez, R. Wu, S. N. Agbo, and O. Alatise, "Robustness and reliability review of Si and SiC FET devices for more-electric-aircraft applications," *Microelectron. Rel.*, vol. 100–101, Sep. 2019, Art. no. 113324, doi: 10.1016/j.microrel.2019.06.016.

[178] W. Saito and T. Naka, "UIS test of high-voltage GaN-HEMTs with p-type gate structure," *Microelectron. Rel.*, vol. 64, pp. 552–555, Sep. 2016, doi: 10.1016/j.microrel.2016.07.066.

[179] T. Naka and W. Saito, "UIS withstanding capability and mechanism of high voltage GaN-HEMTs," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 259–262, doi: 10.1109/ISPSD.2016.7520827.

[180] W. Saito and T. Naka, "Relation between UIS withstanding capability and I-V characteristics in high-voltage GaN-HEMTs," *Microelectron. Rel.*, vol. 76–77, pp. 309–313, Sep. 2017, doi: 10.1016/j.microrel.2017.07.009.

[181] J. Marek et al., "Impact of repetitive UIS on modern GaN power devices," in *Proc. 11th Int. Conf. Adv. Semicond. Devices Microsyst.*, 2016, pp. 173–176, doi: 10.1109/ASDAM.2016.7805923.

[182] J. Kozárik, J. Marek, M. Jagelka, L. Černaj, A. Chvala, and D. Donoval, "Power p-GaN HEMT under single and multi-pulse UIS conditions," in *Proc. 12th Int. Conf. Adv. Semicond. Devices Microsyst.*, 2018, pp. 1–4, doi: 10.1109/ASDAM.2018.8544555.

[183] P. J. Martinez, S. Letz, E. Maset, and D. Zhao, "Failure analysis of normally-off GaN HEMTs under avalanche conditions," *Semicond. Sci. Technol.*, vol. 35, 2020, Art. no. 035007, doi: 10.1088/1361-6641/ab6bad.

[184] S. Li et al., "Comparison investigations on unclamped-inductive-switching behaviors of power GaN switching devices," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 5041–5049, May 2022, doi: 10.1109/TIE.2021.3076705.

[185] S. Liu et al., "Single pulse unclamped-inductive-switching induced failure and analysis for 650 V p-GaN HEMT," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11328–11331, Nov. 2020, doi: 10.1109/TPEL.2020.2988976.

[186] S. Li et al., "Investigations on electrical parameters degradations of p-GaN HEMTs under repetitive UIS stresses," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 2227–2234, Apr. 2021, doi: 10.1109/JESTPE.2020.2970786.

[187] C. Zhang et al., "Unclamped-inductive-switching behaviors of p-GaN HEMTs at cryogenic temperature," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11507–11510, Oct. 2022, doi: 10.1109/TPEL.2022.3173725.

[188] J. P. Kozak, R. Zhang, J. Liu, Q. Song, M. Xiao, and Y. Zhang, "Hard-switched overvoltage robustness of p-gate GaN HEMTs at increasing temperatures," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 677–682, doi: 10.1109/ECCE44975.2020.9235461.

[189] J. P. Kozak, Q. Song, R. Zhang, J. Liu, and Y. Zhang, "Robustness of GaN gate injection transistors under repetitive surge energy and overvoltage," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2021, pp. 1–5, doi: 10.1109/IRPS46558.2021.9405173.

[190] Q. Song et al., "GaN MIS-HEMTs in repetitive overvoltage switching: Parametric shift and recovery," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2022, pp. 10B.4–1–10B.4–7, doi: 10.1109/IRPS48227.2022.9764548.

[191] W. Saito, T. Suwa, T. Uchihara, T. Naka, and T. Kobayashi, "Breakdown behaviour of high-voltage GaN-HEMTs," *Microelectron. Rel.*, vol. 55, no. 9/10, pp. 1682–1686, Aug./Sep. 2015, doi: 10.1016/j.microrel.2015.06.126.

[192] X. Liao, H. Li, R. Yao, Z. Huang, and K. Wang, "Voltage overshoot suppression for SiC MOSFET-based DC solid-state circuit breaker," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 4, pp. 649–660, Apr. 2019, doi: 10.1109/TCPMT.2019.2899340.

[193] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A review of switching oscillations of wide bandgap semiconductor devices," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13182–13199, Dec. 2020, doi: 10.1109/TPEL.2020.2995778.

[194] G. E. Mejia-Ruiz, M. R. A. Paternina, A. Zamora-Mendez, J. C. Rosas-Caro, and G. Bolivar-Ortiz, "A novel GaN-based solid-state circuit breaker with voltage overshoot suppression," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 8949–8960, Sep. 2022, doi: 10.1109/TIE.2021.3116557.

[195] "Procedure for characterizing time-dependent dielectric breakdown of ultra-thin gate dielectrics: | JEDEC," Accessed on: Sep. 27, 2022. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-92

[196] C.-T. Yen et al., "Oxide breakdown reliability of SiC MOSFET," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2019, pp. 1–3, doi: 10.1109/WiPDAAsia.2019.8760324.

[197] K. P. Cheung, "SiC power MOSFET gate oxide breakdown reliability—Current status," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. 2B.3–1–2B.3–5, doi: 10.1109/IRPS.2018.8353545.

[198] T. Aichinger and M. Schmidt, "Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–6, doi: 10.1109/IRPS45951.2020.9128223.

[199] T. Liu et al., "Gate oxide reliability studies of commercial 1.2 kV 4H-SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–5, doi: 10.1109/IRPS45951.2020.9129486.

[200] S. A. Jauss, K. Hallaceli, S. Mansfeld, S. Schwaiger, W. Daves, and O. Ambacher, "Reliability analysis of LPCVD SiN gate dielectric for AlGaN/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2298–2305, May 2017, doi: 10.1109/TED.2017.2682931.

[201] Y. Qi et al., "Evaluation of LPCVD SiN_x gate dielectric reliability by TDDB measurement in Si-substrate-based AlGaN/GaN MIS-HEMT," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 1759–1764, May 2018, doi: 10.1109/TED.2018.2813985.

[202] T.-L. Wu et al., "Time dependent dielectric breakdown (TDDB) evaluation of PE-ALD SiN gate dielectrics on AlGaN/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2015, pp. 6C.4.1–6C.4.6, doi: 10.1109/IRPS.2015.7112769.

[203] M. Hua et al., "Characterization of leakage and reliability of SiNx gate dielectric by low-pressure chemical vapor deposition for GaN-based MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3215–3222, Oct. 2015, doi: 10.1109/TED.2015.2469716.

[204] S.-W. Tang, S. B. Kutub, and T.-L. Wu, "Robust forward gate bias TDDB stability in enhancement-mode fully recessed gate GaN MIS-FETs with ALD Al2O3Gate dielectric," in *Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits*, 2020, pp. 1–4, doi: 10.1109/IPFA49335.2020.9260907.

[205] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmik, and Z. Yatabe, "State of the art on gate insulation and surface passivation for GaN-based power HEMTs," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 85–95, May 2018, doi: 10.1016/j.mssp.2017.09.028.

[206] S. Warnock and J. A. del Alamo, "OFF-state TDDB in high-voltage GaN MIS-HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2017, pp. 4B–3.1–4B–3.6, doi: 10.1109/IRPS.2017.7936309.

[207] S. Warnock and J. A. del Alamo, "Progressive breakdown in high-voltage GaN MIS-HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, pp. 4A–6–1–4A–6–6, doi: 10.1109/IRPS.2016.7574531.

[208] S. Warnock, A. Lemus, J. Joh, S. Krishnan, S. Pendharkar, and J. A. del Alamo, "Time-dependent dielectric breakdown in high-voltage GaN MIS-HEMTs: The role of temperature," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3132–3138, Aug. 2017, doi: 10.1109/TED.2017.2717924.

[209] S. K. Murray et al., "Transient overvoltage detection technique for GaN HEMTs integrated in a 200-V GaN-on-SOI process," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 1400–1405, doi: 10.1109/APEC43599.2022.9773399.

[210] T.-L. Wu et al., "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Oct. 2015, doi: 10.1109/LED.2015.2465137.

[211] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmík, "Gate reliability investigation in normally-off p-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 385–388, Apr. 2016, doi: 10.1109/LED.2016.2535133.

[212] I. Rossetto et al., "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.

[213] S. Stoffels et al., "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2017, pp. 4B–4.1–4B–4.9, doi: 10.1109/IRPS.2017.7936310.

[214] A. Stockman et al., "Gate conduction mechanisms and lifetime modeling of p-gate AlGaN/GaN high-electron-mobility transistors," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5365–5372, Dec. 2018, doi: 10.1109/TED.2018.2877262.

[215] A. N. Tallarico et al., "Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 99–102, Jan. 2017, doi: 10.1109/LED.2016.2631640.

[216] L. Zhang, Z. Zheng, S. Yang, W. Song, J. He, and K. J. Chen, "p-GaN gate HEMT with surface reinforcement for enhanced gate reliability," *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 22–25, Jan. 2021, doi: 10.1109/LED.2020.3037186.

[217] M. Millesimo et al., "High-temperature time-dependent gate breakdown of p-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5701–5706, Nov. 2021, doi: 10.1109/TED.2021.3111144.

[218] P. Moens and A. Stockman, "A physical-statistical approach to AlGaN/GaN HEMT reliability," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2019, pp. 1–6, doi: 10.1109/IRPS.2019.8720521.

[219] J. He et al., "Characterization and analysis of low-temperature time-to-failure behavior in forward-biased Schottky-type *p*-GaN gate HEMTs," *Appl. Phys. Lett.*, vol. 116, no. 22, Jun. 2020, Art. no. 223502, doi: 10.1063/5.0007763.

[220] M. Millesimo et al., "Gate reliability of p-GaN power HEMTs under pulsed stress condition," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2022, pp. 10B.2–1–10B.2–6, doi: 10.1109/IRPS48227.2022.9764592.

[221] Y. Cheng et al., "Gate reliability of Schottky-type p-GaN gate HEMTs under AC positive gate bias stress with a switching drain bias," *IEEE Electron Device Lett.*, vol. 43, no. 9, pp. 1404–1407, Sep. 2022, doi: 10.1109/LED.2022.3188555.

[222] M. Millesimo et al., "The role of frequency and duty cycle on the gate reliability of p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 43, no. 11, pp. 1846–1849, Nov. 2022, doi: 10.1109/LED.2022.3206610.

[223] B. Wang et al., "Dynamic gate breakdown of p-gate GaN HEMTs in inductive power switching," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 217–220, Feb. 2023, doi: 10.1109/LED.2022.3227091.

[224] C. Wang, M. Hua, S. Yang, L. Zhang, and K. J. Chen, "E-mode p-n junction/AlGaN/GaN HEMTs with enhanced gate reliability," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 14–17, doi: 10.1109/ISPSD46842.2020.9170039.

[225] M. Hua et al., "Gate current transport in enhancement-mode p-n junction/AlGaN/GaN (PNJ) HEMT," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 669–672, May 2021, doi: 10.1109/LED.2021.3068296.

[226] G. Meneghesso, M. Meneghini, C. De Santi, and E. Zanoni, "GaN-based lateral and vertical devices: Physical mechanisms limiting stability and reliability," in *Proc. Electron Devices Technol. Manuf. Conf.*, 2019, pp. 68–70, doi: 10.1109/EDTM.2019.8731064.

[227] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, "High-voltage p-GaN HEMTs with OFF-state blocking capability after gate breakdown," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 530–533, Apr. 2019, doi: 10.1109/LED.2019.2897694.

[228] G. Zhou et al., "Determination of the gate breakdown mechanisms in p-GaN gate HEMTs by multiple-gate-sweep measurements," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1518–1523, Apr. 2021, doi: 10.1109/TED.2021.3057007.

[229] F. Li et al., "Temperature-dependent hot electron effects and degradation mechanisms in 650-V GaN-based MIS-HEMT power devices under hard switching operations," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6424–6431, Oct. 2021, doi: 10.1109/JESTPE.2021.3061570.

[230] W.-R. Lin, C. Suarez, K. Umetani, and W. Martinez, "Gate drivers techniques and solutions for GaN HEMTs in high frequency applications," in *Proc. IEEE 29th Int. Symp. Ind. Electron.*, 2020, pp. 712–716, doi: 10.1109/ISIE45063.2020.9152415.

[231] W.-R. Lin, U. Chatterjee, and W. Martinez, "Characterization of enhancement-mode asymmetrical GaN transistor half bridge in high frequency operation," in *Proc. 23rd Eur. Conf. Power Electron. Appl.*, 2021, pp. 1–7.

[232] S. R. Bahl, F. Baltazar, and Y. Xie, "A generalized approach to determine the switching lifetime of a GaN FET," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2020, pp. 1–6, doi: 10.1109/IRPS45951.2020.9129631.

[233] R. Wang, J. Sabate, K. Mainali, T. Sadilek, P. Losee, and Y. Singh, "SiC device junction temperature online monitoring," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 387–392, doi: 10.1109/ECCE.2018.8558298.

[234] F. Xu et al., "Reliability odometer of power semiconductor device used for high performance high power amplifiers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–5, doi: 10.1109/ECCE.2016.7855389.

[235] Y. Qin et al., "Thermal management and packaging of wide and ultra-wide bandgap power devices: A review and perspective," *J. Phys. D, Appl. Phys.*, vol. 56, no. 9, Jan. 2023, Art. no. 093001, doi: 10.1088/1361-6463/acb4ff.

[236] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2681–2688, doi: 10.1109/ECCE.2011.6064128.

[237] Y. Zhang et al., "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.

[238] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical power p-n diodes based on bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015, doi: 10.1109/TED.2014.2360861.

[239] S. Han, S. Yang, R. Li, X. Wu, and K. Sheng, "Current-collapse-free and fast reverse recovery performance in vertical GaN-on-GaN Schottky barrier diode," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5012–5018, Jun. 2019, doi: 10.1109/TPEL.2018.2876444.

[240] F. Zhou et al., "Demonstration of avalanche and surge current robustness in GaN junction barrier Schottky diode with 600-V/10-A switching capability," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12163–12167, Nov. 2021, doi: 10.1109/TPEL.2021.3076694.

[241] H. Nie et al., "1.5-kV and 2.2-mΩ-cm^2 vertical GaN transistors on bulk-GaN substrates," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 939–941, Sep. 2014, doi: 10.1109/LED.2014.2339197.

[242] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "Over 10 a operation with switching characteristics of 1.2 kV-class vertical GaN trench MOSFETs on a bulk GaN substrate," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 459–462, doi: 10.1109/ISPSD.2016.7520877.

[243] Y. Zhang et al., "Large-area 1.2-kV GaN vertical power FinFETs with a record switching figure of merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.

[244] J. Liu et al., "1.2 kV vertical GaN fin JFETs with robust avalanche and fast switching capabilities," in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 23.2.1–23.2.4, doi: 10.1109/IEDM13553.2020.9372048.

[245] I. C. Kizilyalli, P. Bui-Quang, D. Disney, H. Bhatia, and O. Aktas, "Reliability studies of vertical GaN devices based on bulk GaN substrates," *Microelectron. Rel.*, vol. 55, no. 9/10, pp. 1654–1661, Aug./Sep. 2015, doi: 10.1016/j.microrel.2015.07.012.

[246] M. Ruzzarin et al., "Degradation of vertical GaN FETs under gate and drain stress," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, pp. 4B.1–1–4B.1–5, doi: 10.1109/IRPS.2018.8353579.

[247] S. You et al., "Vertical GaN devices: Process and reliability," *Microelectron. Rel.*, vol. 126, Nov. 2021, Art. no. 114218, doi: 10.1016/j.microrel.2021.114218.

[248] J. Liu et al., "Surge current and avalanche ruggedness of 1.2-kV vertical GaN p-n diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.

[249] J. Liu et al., "Trap-mediated avalanche in large-area 1.2 kV vertical GaN p-n diodes," *IEEE Electron Device Lett.*, vol. 41, no. 9, pp. 1328–1331, Sep. 2020, doi: 10.1109/LED.2020.3010784.

[250] J. Liu et al., "1.2-kV vertical GaN fin-JFETs: High-temperature characteristics and avalanche capability," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2025–2032, Apr. 2021, doi: 10.1109/TED.2021.3059192.

[251] R. Zhang et al., "Robust through-fin avalanche in vertical GaN fin-JFET with soft failure mode," *IEEE Electron Device Lett.*, vol. 43, no. 3, pp. 366–369, Mar. 2022, doi: 10.1109/LED.2022.3144698.

[252] J. Liu et al., "Tuning avalanche path in vertical GaN JFETs by gate driver design," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5433–5443, May 2022, doi: 10.1109/TPEL.2021.3132906.

[253] B. D. Weaver et al., "Editors' choice—On the radiation tolerance of AlGaN/GaN HEMTs," *ECS J. Solid State Sci. Technol.*, vol. 5, no. 7, pp. Q208–Q212, 2016, doi: 10.1149/2.0281607jss.

[254] P. C. Adell and L. Z. Scheick, "Radiation effects in power systems: A review," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1929–1952, Jun. 2013, doi: 10.1109/TNS.2013.2262235.
[255] R. Jiang et al., "Total ionizing dose effects in passivated and unpassivated AlGaN/GaN HEMTs," in *Proc. 16th Eur. Conf. Radiat. Its Effects Compon. Syst.*, 2016, pp. 1–4, doi: 10.1109/RADECS.2016.8093099.
[256] A. Lidow and K. Smalley, "Radiation tolerant enhancement mode gallium nitride (eGaN) FET characteristics," presented at GOMAC Tech Conf., Las Vegas, NV, USA, Mar. 2012.
[257] A. Lidow, A. Nakata, M. Rearwin, J. Strydom, and A. M. Zafrani, "Single-event and radiation effect on enhancement mode gallium nitride FETs," in *Proc. IEEE Radiat. Effects Data Workshop*, 2014, pp. 1–7, doi: 10.1109/REDW.2014.7004594.
[258] P. J. Martínez, E. Maset, D. Gilabert, E. Sanchis-Kilders, and J. B. Ejea, "Evidence of dynamic-R_{on} degradation on low-dose ^{60}Co gamma radiation AlGaN/GaN HEMTs," *Semicond. Sci. Technol.*, vol. 33, no. 11, Nov. 2018, Art. no. 115017, doi: 10.1088/1361-6641/aae616.
[259] A. C. V. Bôas et al., "Radiation hardness of GaN HEMTs to TID effects: COTS for harsh environments," in *Proc. 19th Eur. Conf. Radiat. Its Effects Compon. Syst.*, 2019, pp. 1–4, doi: 10.1109/RADECS47380.2019.9745697.
[260] D. Lynn, G. Villani, B. Hommels, and M. Ullan, "High-voltage multiplexing for the ATLAS strip tracker," presented at IEEE Symposium on Nuclear Science, Atlanta, GA, USA, Oct. 2017.
[261] D. M. Keum, H.-K. Sung, and H. Kim, "Degradation characteristics of normally-off p-AlGaN gate AlGaN/GaN HEMTs with 5 MeV proton irradiation," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 258–262, Jan. 2017, doi: 10.1109/TNS.2016.2612227.
[262] A. Floriduz and J. D. Devine, "High-energy proton irradiation effects on GaN hybrid-drain-embedded gate injection transistors," *Microelectron. Rel.*, vol. 110, Jul. 2020, Art. no. 113656, doi: 10.1016/j.microrel.2020.113656.
[263] "Environmental test methods for semiconductor devices," MIL-SPEC-750, 2016. Accessed: Jan. 23, 2023. [Online]. Available: https://www.atecorp.com/ATECorp/media/PDFs/750-1.pdf
[264] C. Abbate et al., "Experimental study of single event effects induced by heavy ion irradiation in enhancement mode GaN power HEMT," *Microelectron. Rel.*, vol. 55, no. 9/10, pp. 1496–1500, Aug./Sep. 2015, doi: 10.1016/j.microrel.2015.06.139.
[265] L. Z. Scheick, "Recent gallium nitride power HEMT single-event testing results," in *Proc. IEEE Radiat. Effects Data Workshop*, 2016, pp. 1–6, doi: 10.1109/NSREC.2016.7891731.
[266] L. Scheick, "A mechanism for destructive single-event effect in gallium nitride power HEMTs," in *Proc. 17th Eur. Conf. Radiat. Its Effects Compon. Syst.*, 2017, pp. 1–7, doi: 10.1109/RADECS.2017.8696100.
[267] E. Mizuta et al., "Single-event damage observed in GaN-on-Si HEMTs for power control applications," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1956–1963, Aug. 2018, doi: 10.1109/TNS.2018.2819990.
[268] M. Zerarka et al., "Cosmic ray immunity of COTS normally-off power GaN FETs for space, aeronautic and automotive applications," in *Proc. 20th Eur. Conf. Radiat. Its Effects Compon. Syst.*, 2020, pp. 1–5, doi: 10.1109/RADECS50773.2020.9857695.
[269] M. Zerarka and O. Crepel, "Radiation robustness of normally-off GaN/HEMT power transistors (COTS)," *Microelectron. Rel.*, vol. 88–90, pp. 984–991, Sep. 2018, doi: 10.1016/j.microrel.2018.07.148.
[270] "FBG30N04C," *EPC Space*, Accessed on: Oct. 12, 2022. [Online]. Available: https://epc.space/products/gan-discretes/fbg30n04c/
[271] K. Rajashekara and B. Akin, "A review of cryogenic power electronics—Status and applications," in *Proc. Int. Electr. Mach. Drives Conf.*, 2013, pp. 899–904, doi: 10.1109/IEMDC.2013.6556204.
[272] H. Mhiesan, M. M. Hossain, A. U. Rashid, Y. Wei, and A. Mantooth, "Survey of cryogenic power electronics for hybrid electric aircraft applications," in *Proc. IEEE Aerosp. Conf.*, 2020, pp. 1–7, doi: 10.1109/AERO47225.2020.9172807.
[273] M. Elbuluk, A. Hammoud, and R. Patterson, "Power electronic components, circuits and systems for deep space missions," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, 2005, pp. 1156–1162, doi: 10.1109/PESC.2005.1581775.
[274] H. Gui et al., "Review of power electronics components at cryogenic temperatures," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5144–5156, May 2020, doi: 10.1109/TPEL.2019.2944781.
[275] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2021, doi: 10.1109/TPEL.2020.3047466.
[276] J. Colmenares, T. Foulkes, C. Barth, T. Modeert, and R. C. N. Pilawa-Podgurski, "Experimental characterization of enhancement mode gallium-nitride power field-effect transistors at cryogenic temperatures," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 129–134, doi: 10.1109/WiPDA.2016.7799923.
[277] R. Ren et al., "Characterization and failure analysis of 650-V enhancement-mode GaN HEMT for cryogenically cooled power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 66–76, Mar. 2020, doi: 10.1109/JESTPE.2019.2949953.
[278] R. Cuerdo et al., "The kink effect at cryogenic temperatures in deep submicron AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 209–212, Mar. 2009, doi: 10.1109/LED.2008.2011289.
[279] S. Nuttinck, S. Pinel, E. Gebara, J. Laskar, and M. Harris, "Cryogenic investigation of current collapse in AlGaN/GaN HFETS," presented at Gallium Arsenide Applications Symposium, Munich, Germany, Oct. 2003.
[280] C.-H. Lin, W.-K. Wang, P.-C. Lin, C.-K. Lin, Y.-J. Chang, and Y.-J. Chan, "Transient pulsed analysis on GaN HEMTs at cryogenic temperatures," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 710–712, Oct. 2005, doi: 10.1109/LED.2005.856709.
[281] Y. Wei, M. M. Hossain, and A. Mantooth, "Comprehensive cryogenic characterizations of a commercial 650 V GaN HEMT," in *Proc. IEEE Int. Future Energy Electron. Conf.*, 2021, pp. 1–6, doi: 10.1109/IFEEC53238.2021.9661762.
[282] C. Fleury et al., "High temperature performances of normally-off p-GaN gate AlGaN/GaN HEMTs on SiC and Si substrates for power applications," *Microelectron. Rel.*, vol. 55, no. 9/10, pp. 1687–1691, Aug. 2015, doi: 10.1016/j.microrel.2015.06.010.
[283] M. Yuan et al., "High temperature robustness of enhancement-mode p-GaN-gated AlGaN/GaN HEMT technology," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices Appl.*, 2022, pp. 40–44, doi: 10.1109/WiPDA56483.2022.9955304.
[284] J. Oliveira, A. Alhoussen, F. Loiselay, H. Morel, and D. Planson, "Switching behavior and comparison of wide bandgap devices for automotive applications," in *Proc. 23rd Eur. Conf. Power Electron. Appl.*, 2021, pp. 1–10, doi: 10.23919/EPE21ECCEEurope50061.2021.9570434.
[285] Z. Xu, W. Zhang, F. Xu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Investigation of 600 V GaN HEMTs for high efficiency and high temperature applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 131–136, doi: 10.1109/APEC.2014.6803299.

Joseph Peter Kozak (Member, IEEE) received the B.S. degree in engineering physics and the M.S. degree in electrical engineering from the University of Pittsburgh, Pittsburgh, PA, USA, in 2014 and 2016, respectively, and the Ph.D. degree in electrical engineering from the Center for Power Electronic Systems, Virginia Tech, Blacksburg, VA, USA, in 2021.

Since then, he has been a Senior Electrical Engineer with Johns Hopkins Applied Physics Laboratory in the spacecraft power engineering group. His current research interests include robustness, reliability, and physics of failure of new wide bandgap semiconductors, and their implementation into power electronics systems.

Ruizhe Zhang (Graduate Student Member, IEEE) received the B.S. degree in material physics from Fudan University, Shanghai, China, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA.

He joined Virginia Polytechnic Institute and State University in 2019. His current research interests include design, characterization, reliability, and ruggedness of wide-bandgap power devices.

Matthew Porter (Student Member, IEEE) received the B.S. degree in electrical and computer engineering from United States Naval Academy, Annapolis, MD, USA, in 2010, and the M.S. degree in electrical and computer engineering from Naval Postgraduate School, Monterey, CA, USA, in 2011. He is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His current research interests include wide bandgap power device fabrication and design, radiation effects in wide bandgap semiconductor devices, and power device reliability.

Qihao Song (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering in 2019 from Virginia Tech, Blacksburg, VA, USA, where he is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems.

His current research interests include characterization, robustness, reliability, and physics of failure of wide-bandgap power semiconductor devices, as well as the impact and integration of these devices into power electronics' converters.

Jingcun Liu received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2021.

From 2019 to 2020, he was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His research interests include design, characterization, robustness, and reliability of power semiconductor devices.

Bixuan Wang (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2018 and 2021, respectively. She is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA.

Her current research interests include characterization, robustness, and reliability of wide-bandgap power devices.

Rudy Wang (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree in electrical engineering from the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in 2004, 2007, and 2012, respectively.

After graduation, he joined the General Electric company first with GE Global Research and then with GE Aviation. He was a Senior Staff Engineer and Project Leader. In 2020, he joined Milan M. Jovanovic Power Electronics Lab, Delta Electronics (Americas) Ltd. He has authored or coauthored more than 50 papers in refereed journals and international conference proceedings and more than 25 awarded U.S. patents. His research and development interests include electric circuit and topologies, wide-band gap device-based converter design, high power density and harsh environment power electronics, electromagnetic interference technology, etc. His current focus in Delta is in medium-voltage fast EV charging and other relevant applications.

Dr. Wang was a recipient of the third and second place William M. Portnoy Award for the Best Paper published in the IEEE Energy Conversion Congress and Exposition in 2012 and 2018, and the GE Gold Medal Inventor award in 2019. Since 2015, he has been an Associate Editor for the IEEE TRANSACTION ON INDUSTRIAL APPLICATIONS and IEEE TRANSACTION ON POWER ELECTRONICS. From 2015 to 2019, he was the Chair of the Power Electronics Devices and Components Committee in IEEE Industry Applications Society.

Wataru Saito (Senior Member, IEEE) received the B.Eng., M.Eng., and Dr. Eng. degrees in electrical and electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1994, 1996, and 1999, respectively.

In 1999, he joined Toshiba Corporation, Kawasaki, Japan. Since 2019, he has been with Kyushu University, Fukuoka, Japan. His current research interests include basic research on power semiconductor devices and related application technologies.

Dr. Saito was a recipient of the Conference Prize Paper Award in 2008 IEEE Power Electronics' Specialists Conference. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES. He formerly served on the committee member of Power Devices and ICs Committee in IEEE Electron Device Society from 2015 to 2020.

Yuhao Zhang (Senior Member, IEEE) received the B.S. degree in physics from Peking University, Beijing, China, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2013 and 2017, respectively.

From 2017 to 2018, he was a Postdoctoral Associate with MIT. Since 2018, he has been an Assistant Professor with the Center for Power Electronics Systems, Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA. His research interests include power semiconductor devices, (ultra-)wide-bandgap semiconductor materials, power electronics' applications, and machine learning assisted codesign. He has authored or coauthored more than 130 journal articles and conference proceedings and is an inventor of five granted U.S. patents.

Dr. Zhang was the recipient of the 2017 MIT Microsystems Technologies Laboratory Doctoral Dissertation Seminar Award, 2019 IEEE George Smith Award, 2021 National Science Foundation CAREER Award, as well as 2021 Outstanding Assistant Professor Award and 2022 Faculty Fellow Award of Virginia Tech Engineering.