Development of Self-Impedance Matching Rectifiers for Beamforming-Based Wireless Power Transfer Systems

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Development of Self-Impedance Matching Rectifiers for Beamforming-Based Wireless Power Transfer Systems

By

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ABSTRACT

Recently, 5G systems are deployed and are in use almost every country in the world. Ever since Nikola Tesla invented and demonstrated the concept of the wireless power transfer (WPT), people are trying to employ wireless power transfer to power the devices that are powered with wired. From last few decades, researchers are investigating for wireless energy harvesting (EH) and wireless power transfer (WPT) technologies to deliver energy for various applications. After the recent development beamforming-based WPT system is gathering important attention to deliver power to devices ranging from lower power smaller IoTs, personal gadgets, biomedical implants, etc., to high power appliances like personal computers refrigerators, etc. A critical component within these technologies is the rectifier circuit, responsible for converting alternating current (AC) harvested from wireless signals into usable direct current (DC) power. In most of these rectifiers, the performance parameters like efficiency and circuit size are limited by the matching networks that are required at the input side of the rectifier circuit. In this thesis, we developed efficient rectification circuits that will be applicable for beamforming-based WPT system application that range operation from low power to high power within single circuit, self-impedance matching circuit without input matching and with compact circuit size using CMOS technology which are discussed below.

Firstly, a single rectifier that can operate efficiently at both low power and high-power conditions is developed which is truly applicable for both beamforming-based WPT whose power level varies in wide range from very low (few micro watts) to very high (few watts). A frequency-switching technique is proposed for developing dual power band rectifier to accommodate both low-power and high-power applications within a single circuit. Two distinct operating frequencies: f_1 = 900 MHz for low-power and f_2 = 2.4 GHz for high-power scenarios were chosen. The rectifier ensures stable operation across varying input power levels by dynamically switching between these frequencies. To optimize performance, Schottky diodes HSMS 2850 and HSMS 2860 are chosen for f_1 and f_2, respectively, based on their performance characteristics relative to input power. Instead of conventional lumped inductors, defected ground structure (DGS)-based inductors are utilized in matching circuits to enhance efficiency and stability. To achieve maximum RF-to-DC conversion efficiency in both low and high-power conditions, two different optimal loads are required. This is accomplished using the load-modulation technique with Bipolar Junction Transistors (BJTs), enabling efficient power conversion across a range of power levels. Measurement results demonstrate that more than 50% conversion efficiency is achieved across the wide power range of 18 dBm to 2 dBm and 8 dBm to 20 dBm. Furthermore, the compact circuit size of 35 mm × 30 mm underscores its suitability for various applications.

Secondly, the impedance matching circuit in a rectifier is a crucial factor in determining overall performance and circuit size. Traditional matching networks at the input have many limitations, such as bulky circuits, higher losses, and narrow bandwidth. The self-impedance

matching technique addresses many of these limitations by eliminating the need for additional matching networks at the input. A novel concept of self-impedance matching in rectifier design is proposed by incorporating a driving rectifier in parallel with a conventional voltage doubler circuit. The input impedance of the wideband rectifier is matched using the driving rectifier, which includes a half-wave rectifier, a series stub line, and a grounding capacitor. The series stub adjusts the operating frequency and the efficiency bandwidth (EBW) of the rectifier. This method simplifies rectifier design by removing the need for additional input impedance matching networks and allows simultaneous control of EBW and operating bandwidth. A Defected Ground Structure (DGS) is used instead of a conventional lossy microstrip line to design a high-impedance series stub line, making the circuit more compact and improving the quality factor. Measurement results show more than 50% power conversion efficiency (PCE) across the frequency range of 3 GHz to 5.8 GHz, covering the entire sub-6 GHz band of the 5G network with minimal variation. The fabricated prototype on a Printed Circuit Board (PCB) has a circuit size of 0.756 cm^2.

Thirdly, to design more compact rectifier circuit that is more feature in miniaturization applications like wireless power transfer in biomedical implants a compact size high efficiency Complementary Metal-Oxide-Semiconductor (CMOS) rectifier was proposed and designed with the resonance control technique employing the concept of parallel rectifier. This topology is advantageous to develop a rectifier in the desired frequency by optimizing it for the target resonance. The methodology involves the integration of two rectifiers, where one is main rectifier, specifically designated for rectification purposes and the other is auxiliary, serves for impedance matching, resulting in no matching at input. Furthermore, the auxiliary rectifier offers control over resonance of the proposed rectifier. The proposed design achieves more than 40% conversion efficiency at 22 dBm of input power for the broadband range from 2.4 GHz to 3.5 GHz, with an active circuit size of 0.21 mm^2.

Finally, an ultra-wideband CMOS rectifier was proposed employing a novel parasitic cancellation technique using single inductor (L_p) at the gate side (G) of the transistor (M) along with the L-matching at the input. The proposed technique significantly improves the efficiency in between the resonances due to L-matching and parasitic cancellation, resulting maximum flat efficiency is obtained throughout the ultra-wideband range. The proposed design achieves more than 48% conversion efficiency at 18 dBm of input power for the broadband range from 1.9 GHz to 4.1 GHz, with an active circuit size of 0.51 mm^2.

All these compact and high-performance rectifiers that are proposed and developed in this thesis are advantageous for the application in the beamforming based WPT for products ranging from the small gadgets and the high-power application and covers all the operating frequency bands. Moreover, the operation of these rectifiers in sub-6 GHz band are suitable for current 5G bands applications.

ACKNOWLEDGEMENT

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Abbreviations

ADS	:	Advanced Design System
CMOS	:	Complementary Metal-Oxide Semiconductor
DC	:	Direct Current
DGS	:	Defected Ground Structure
EH	:	Energy Harvesting
EM	:	Electromagnetic
HFSS	:	High Frequency Simulation Software
IoT	:	Internet of Things
PCB	:	Printed Circuit Board
PCE	:	Power Conversion Efficiency
RF	:	Radio Frequency
VNA	:	Vector Network Analyzer
WEH	:	Wireless Energy Harvesting
WPT	:	Wireless Power Transfer
WSN	:	Wireless Sensor Network

Chapter 1: Introduction

1.1 Overview

1.1.1 Electromagnetic Waves and Wireless Power Transfer

Electromagnetic waves are oscillations of electric and magnetic fields that travel through space. They encompass a wide range of frequencies, from low-frequency radio waves to high-frequency gamma rays. These waves, which include radio waves, microwaves, and light, carry energy through the air from a transmitter to a receiver without needing physical connections like wires. These waves are fundamental to various forms of wireless communication and energy transfer. Electromagnetic waves are essential for wireless power transfer.

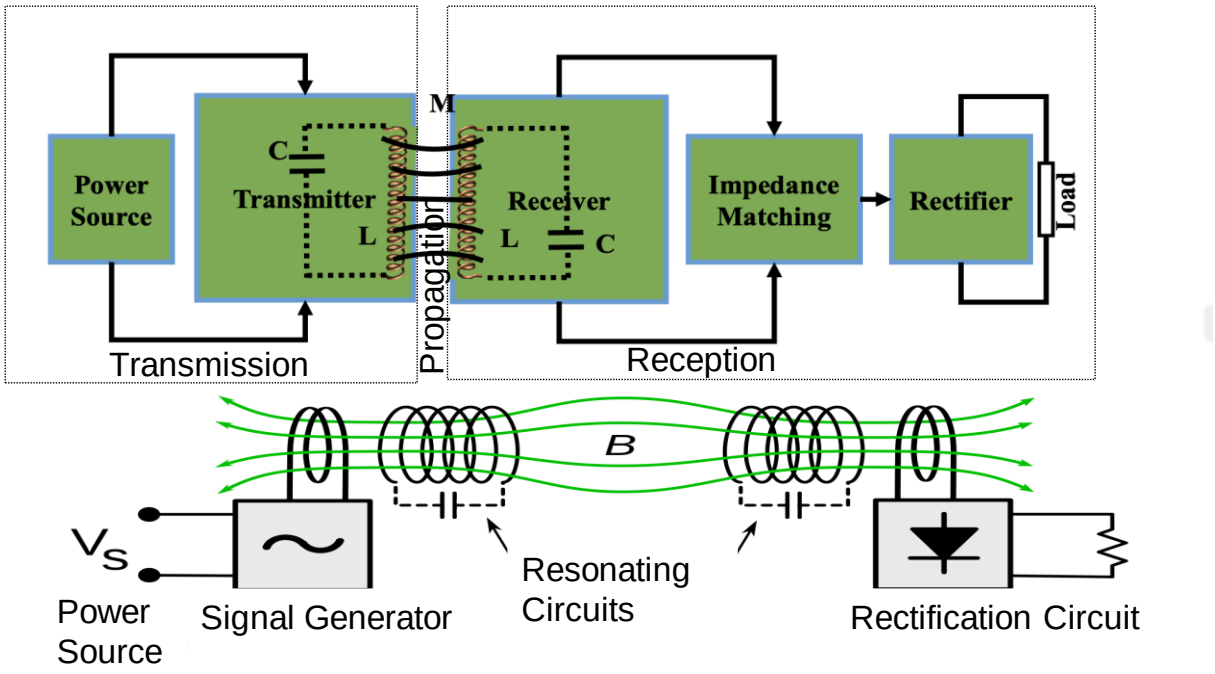

Fig. 1. 1: Basic wireless power transfer technology.

In the late 19th and early 20th centuries, Nikola Tesla was one of the first to experiment with the concept of wireless power transfer (WPT). He demonstrated the transmission of electrical energy without wires using his Tesla coil, an invention that could wirelessly transmit electricity over short distances. Advancing upon the tesla experiment, in recent decades, scientists and companies are developing more efficient and practical methods of wireless power transfer technologies such as inductive coupling (used in wireless charging pads) and resonant

inductive coupling have become common for charging small devices like smartphones and electric toothbrushes. In advanced and long-haul power transfer, researchers are working for microwave power transfer for space satellites to power wirelessly. However, in all the overall WPT process involves transmission, propagation, and reception all through electromagnetic waves (EM) as shown in Fig. 1.1, which is:

1. **Transmission**: A power transmitter generates electromagnetic waves using an antenna or array of antennas. The transmitter converts electrical energy into electromagnetic waves, which are then emitted into the surrounding space.
2. **Propagation**: These waves travel through the air or vacuum, carrying energy with them. The propagation of electromagnetic waves can be influenced by various factors such as frequency, distance, and obstacles in the environment.
3. **Reception**: A power receiver, equipped with an antenna, captures the electromagnetic waves and converts them back into electrical energy. This energy can then be used to power devices or stored for later use.

1.1.2 Beamforming in Wireless Power Transfer

Conventional wireless power transfer has lower transmission efficiency due to the spread of the EM waves around the resonating coils. Several techniques have been proposed to increase the transmission efficiency like using metamaterial-based antennas, reflectors behind the transmitter, etc. Also, in high frequencies the power available from the wireless system in distance is lower than conventional system. Beamforming is a technique used to focus electromagnetic waves in a specific direction, enhancing the efficiency, power level, and effectiveness of wireless power transfer. It involves an array of antennas that work together to direct the waves towards a target. Multiple antennas emit electromagnetic waves that are carefully synchronized in phase and timing. This synchronization ensures that the waves combine constructively at the desired location. By adjusting the phase and timing of the signals from each antenna, the direction of the beam can be controlled. This allows for the energy to be focused on a specific point, rather than spreading out in all directions. When these waves meet at the target location, they interfere constructively, amplifying the energy at that point. This focused energy transfer is much more efficient than traditional omnidirectional methods like WPT ensuring proper availability of the EM waves at target application.

If we listed out the importance and target that we want to achieve from the beamforming based WPT as shown in Fig. 1.2, we have:

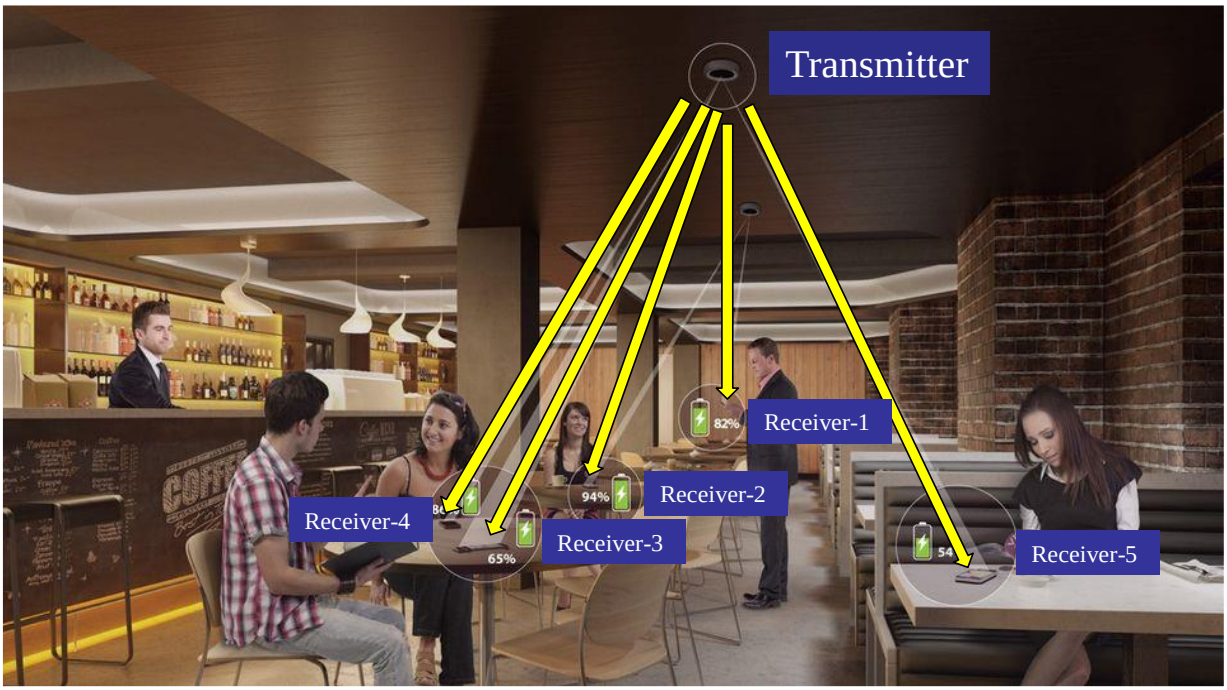

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Fig. 1. 2: Concept of beamforming based WPT.

1. **Enhanced Efficiency**: Beamforming concentrates energy towards the target device, minimizing energy loss and maximizing the amount of power received. This is especially important for high-power applications.
2. **Extended Range**: By focusing the energy, beamforming allows for effective power transfer over greater distances, making it practical for various applications, from small gadgets to large appliances.
3. **Dynamic Tracking**: Beamforming systems can dynamically track moving devices, ensuring continuous power delivery even as the devices change positions. This is achieved by adjusting the phase and timing of the signals in real-time.
4. **Versatility**: Beamforming can be applied to a wide range of scenarios, from personal gadgets to industrial machinery, drones, and even remote or disaster-stricken areas where traditional power infrastructure is unavailable.

1.2 Problem Definition and Conventional Studies

In any WPT system, to convert the maximum EM waves to electrical energy, a good rectification circuit is necessary [1]-[8]. Beamforming based-WPT also requires a highly efficient compact rectifier that can work at wide power and the frequency range is crucial to get rid of the multiple rectification circuit for each power level and frequency bands. In conventional rectification circuits, after the diode losses most of the losses are contributed by the matching circuit required for input matching. Due to which, the power conversion efficiency (PCE) of the overall beamforming based WPT becomes lower which is undesirable.

There are many rectification circuits reported in the literature based on the application areas [9]-[37], [38]-[45]. Usually, rectification circuits consist of rectifying units, usually diodes/switches like semiconductor diodes, silicon-controlled rectifiers, silicon-based semiconductor switches, etc. Also, the topologies like half wave rectifier, full wave rectifier, bridge rectifier, Dickson Voltage Multiplier, Voltage doubler etc., used as rectifier is different for different applications [9]-[21]. So, RF/Microwave designers choose the topologies of rectifier which tend to present high rectification efficiency for their WPT systems design.

In last few decades, researchers targeted to design a rectifier circuit that can provide higher rectification efficiency for both low-power and high-power conditions, so that the hybrid system of energy harvesting (EH) and WPT can be achieved. In hybrid system, the freely available energy can be harvested first and then for the insufficient energy, we can use WPT system that helps to achieve energy optimization. Also, the field of wireless power transfer and energy harvesting targets the system for multiple frequencies so that the single system can be utilized for multiple transmitters and multiple receivers. But usually, a rectifier circuit design with matching network at input limited the bandwidth and provides a narrow band with higher losses. Using narrow band rectifiers, it is very difficult to cover the wide range of frequency because the system becomes complex and bulky. To achieve good efficiency for multiple frequencies of rectifier, rectifier with multiband like triple-band rectifier, quad-band rectifier and six-band rectifier are reported. However, such multiband rectifiers support only specific frequency bands making the overall system bulky. Also, while designing a rectifier the use of impedance matching network at input makes the circuit very lossy because the all-input power is directly affected by the inductor losses and the very less amount of power will be reached at

the output. Therefore, to achieve higher efficiency in a wide range of working frequency of rectifier, the concept of self-impedance matching wideband rectifier is proposed.

1.3 Research Motivation and Objective

After successful application for one-to-one WPT system, now researchers are dreaming to develop a system that offers sustainable energy system on the beamforming-based WPT to power inhouse appliances and even supporting ambitious space energy transmission. For such driving research there is an urgent need for a robust rectifier solution that would be effective for highly efficient system to beamforming-based WPT applications. Generally, the impedance matching circuits are designed with big capacitors and inductors and in a traditional way, such matching networks are used at input side of the rectifier. While using the big inductor at input, there is higher power losses due to the inductor, resulting in poor efficiency. Another significant drawback of the traditional matching circuit is the limited operating bandwidth. Therefore, to achieve wideband operation usually multiple matching networks are utilized which makes the overall circuity too bulky and lossy.

We developed a highly efficient ultrawide band rectifier without matching circuit in the printed circuit board (PCB) [40]. The concept of self-impedance matching addresses many of traditional limitations that occur due to the use of matching at input. Self-impedance matching technique involves designing the rectifier without additional matching networks at the input side, enhancing efficiency by reducing losses associated with inductor and parasitic components as well as provide the wide operational bandwidth. The rectifiers designed in PCB technology have the drawback of bulky circuits making them questionable for their application in compact system design. The availability of newer advanced semiconductor technology like low profile complementary metal oxide semiconductor (CMOS) that has good performance even at very high frequencies pushed me to utilize it to design compact footprint on-chip rectifier circuit working for high frequency and high-power application. This potentially helps to easy integration with the system-on-chip development to design a compact and low loss beamforming-based WPT system.

The key objectives and motivations of this research work are listed below:

- Designing and optimizing high-power rectifiers capable of efficient RF to DC conversion under varying operational conditions of load, power, frequencies that are primary variables in the beamforming-based WPT system.
- Investigating novel approaches such as self-impedance matching to enhance rectifier efficiency, bandwidth, and circuit footprint.
- Evaluating the performance of rectifiers developed in various technologies like PCB and CMOS.
- Design of high-quality factor defected ground structured (DGS) inductors to replace the low-quality factor lumped inductor to minimize the losses.
- Validating theoretical design equations findings through practical implementation and experimental validation.

1.4 Thesis Outline

The thesis is structured to achieve the above objectives and the major achievements which are organized as follows in Chapters 2-5:

Chapter 2 presents the design of frequency switching dual power band rectifier with load-modulation technique. This chapter describes the DGS inductor design, load modulation technique using BJT and handling of dual-power band by switching the frequency at input.

Chapter 3 presents the design of miniaturized sub-6 GHz rectification circuit utilizing self-impedance matching technique. This chapter describes the self-impedance matching technique to achieve wideband rectification specifically targeting 5G network as well as discussing the technique of resonance control just by changing the inductance value.

Chapter 4 presents the design of a new rectification technique employing auxiliary rectifier for resonance control achieving compact size and high efficiency in CMOS. This chapter describes the role of auxiliary rectifier for impedance matching as well as discussing the advantages of CMOS design compared to PCBs one.

Chapter 5 presents the design of a new rectification technique employing parasitic cancellation technique for achieving compact size and high parasitic cancellation and the L matching for impedance matching to achieve the ultrawideband over 2.2 GHz bandwidth.

Chapter 6 summarizes the conclusions of the overall thesis work, highlighting the major contributions. It also includes a discussion on future research ideas.

Chapter 2: Frequency Switching Dual Power Band Rectifier with Load-Modulation Technique

2.1 Introduction

In beamforming-based WPT, the available power level can range from much lower 1μW to much higher few Watts. Therefore, for such systems rectification circuits should typically need to perform well under both low and high-power conditions, respectively. Consequently, individual rectifiers are usually designed for such system for each power levels like in energy harvesting (EH) and WPT system [46]-[49]. Some rectifier designs have been developed to achieve both low-power and high-power rectification from a single circuit [20], [42]. However, these designs generally exhibit low RF-to-DC conversion efficiency. Although rectifiers capable of covering a wide range of input power with good conversion efficiency have been reported [41], [50], they employ complex impedance matching with long transmission lines, resulting in bulky and lossy circuits. Therefore, a dual power-band rectifier circuit that utilizes frequency switching at the input is proposed which provides maximum conversion efficiency over a wide input power range with a compact design.

2.2 Working Principle

The working principle of frequency switching dual power band rectifier with load-modulation technique is described as:

- The proposed rectifier utilizes two separate operating frequencies at input i.e., f_1 and f_2 aiming low-power and high-power rectifications, respectively.
- Individual rectifiers with individual matching networks for f_1 and f_2 are first designed and then connected them parallelly sharing the same input source, depicted in Fig. 2.1.
- When selected frequency at input is f_1, Rectifier-I is activated for low-power rectification whereas the selected frequency at input is f_2, Rectifier-II is activated for high-power rectification, respectively. Therefore, by switching the input frequency, desired operating power can be achieved.
- To enhance the efficiency of the proposed rectifier, low quality factor (Q-factor) lumped inductors are replaced by high Q-factor defected ground structure (DGS) inductors.

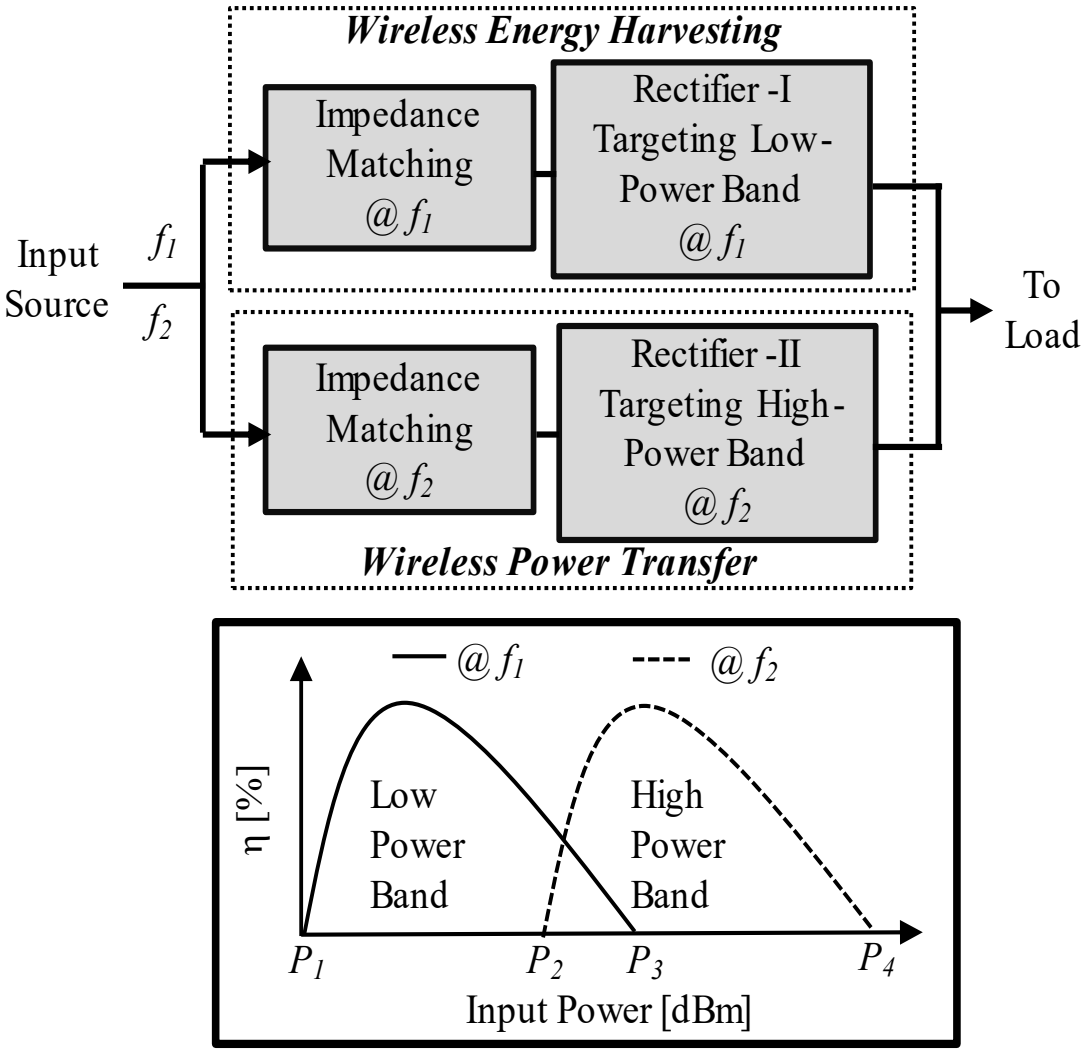


Fig. 2. 1: Block diagram to illustrate the working principle of frequency switching dual power band rectification circuit.

2.3 Design of Frequency Switching Dual-power band Rectifier

The rectifier circuit designed for low-power applications operates at f_1 = 900 MHz and utilizes rectifying diode D_1 (Schottky diode HSMS 2850), referred to as Rectifier-I. Conversely, the rectifier circuit aims for high-power applications operates at f_2 = 2.4 GHz and employs rectifying diode D_2 (Schottky diode HSMS 2860), named Rectifier-II, as illustrated in Fig. 2.2. The conjugate matching for Rectifier-I at f_1, denoted as $Z_{in1}{}^*$ is achieved employing a series capacitor (C_1) with value of 0.4 pF and a grounding inductor (L_1) with value of 34 nH. Similarly, for Rectifier-II at f_2, denoted as $Z_{in2}{}^*$ is obtained utilizing a series capacitor (C_2) with value of 0.4 pF and a grounding inductor (L_2) with value of 5 nH. The input source for both Rectifier-I and Rectifier-II is the same but they operate at different frequencies.

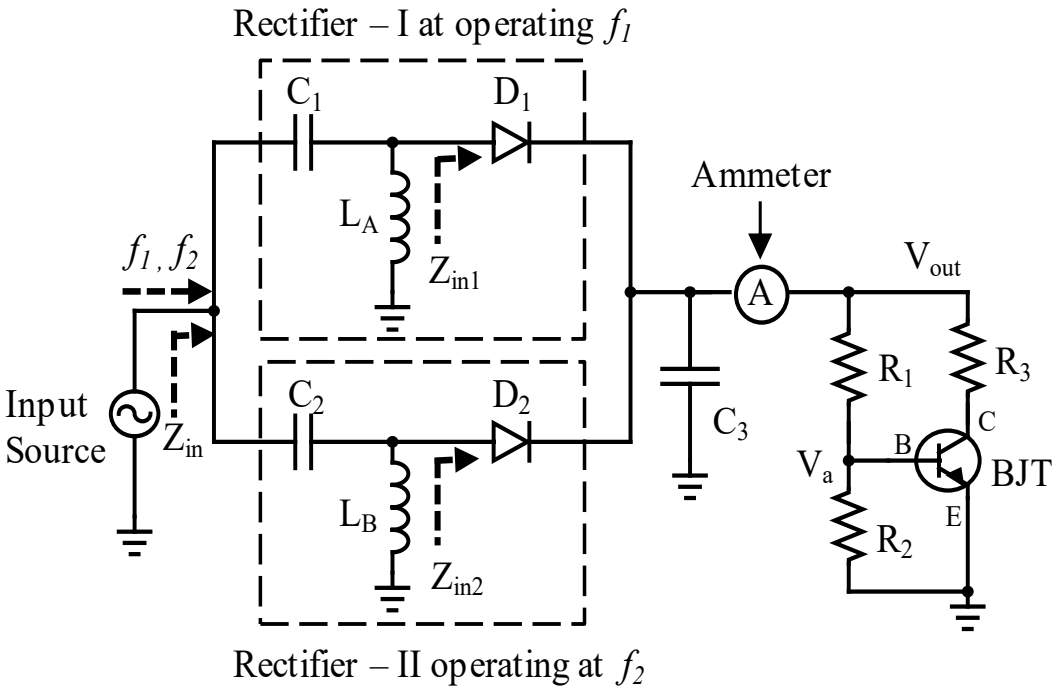
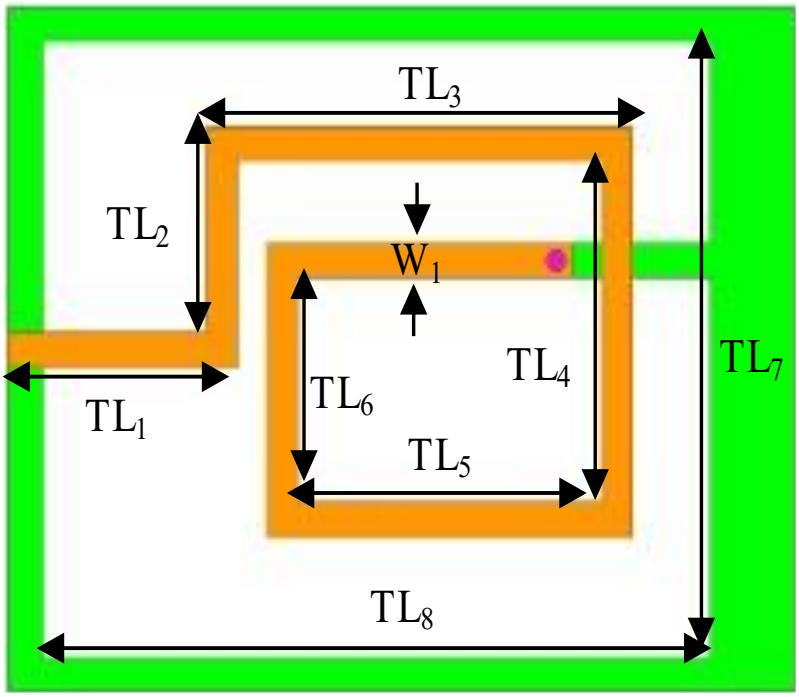


Fig. 2. 2: Schematic diagram of frequency switching dual power band rectification circuit.

2.3.1 Defected Ground Structure (DGS) Inductors Design

The required inductance values for input impedance matching of Rectifier-I and Rectifier-II are 34 nH and 5 nH, respectively, which are relatively high. However, commercially available lumped inductors often have lower Q-factors. Rectifiers designed with higher inductance values, but low *Q*-factors tend to exhibit lower RF-to-dc conversion efficiency. To overcome this challenge and achieve higher inductance with a high *Q*-factor for efficient rectification, defected ground structure (DGS) inductors can be employed. These inductors are designed to disrupt the current grounding path. In this study, the required inductance is achieved with a good *Q*-factor using the DGS topology, achieved by introducing cuts in the ground plate, as depicted in Fig. 2.3 and Fig. 2.5.

The inductance (*L*) and quality factor (*Q*-factor) obtained from the DGS layout and their equivalent circuit are compared in Fig. 2.4 and Fig. 2.6, respectively. The designed DGS inductors achieve an inductance of 33.98 nH with a *Q*-factor of 110.67 at 900 MHz and an inductance of 4.85 nH with a *Q*-factor of 239.43 at 2.4 GHz, respectively. This demonstrates that the simulated *Q*-factors from the DGS designs for both 34 nH and 5 nH are significantly higher than those provided by commercially available lumped inductors with the same inductance values.



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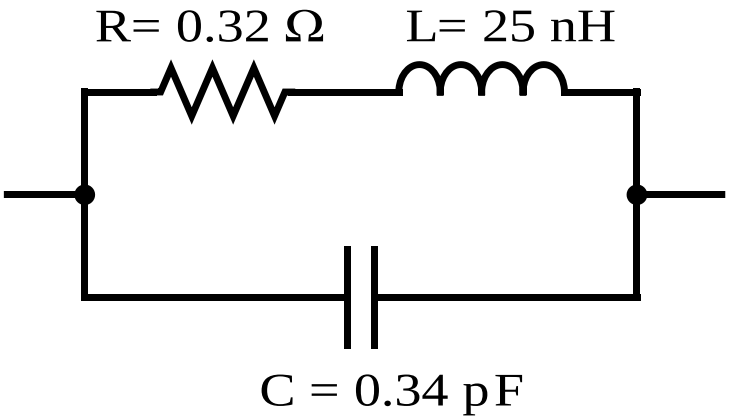


(b)

Fig. 2. 3: Design of DGS inductor for 34 nH of inductance. (a) Layout of DGS inductor (b) Equivalent circuit diagram. Dimensions are in mm: TL_1 = 3.8, TL_2 = 3, TL_3 = 7, TL_4 = 6, TL_5 = 5, TL_6 = 3.3, TL_7 = 9, TL_8 = 11, W_1 = 0.5.

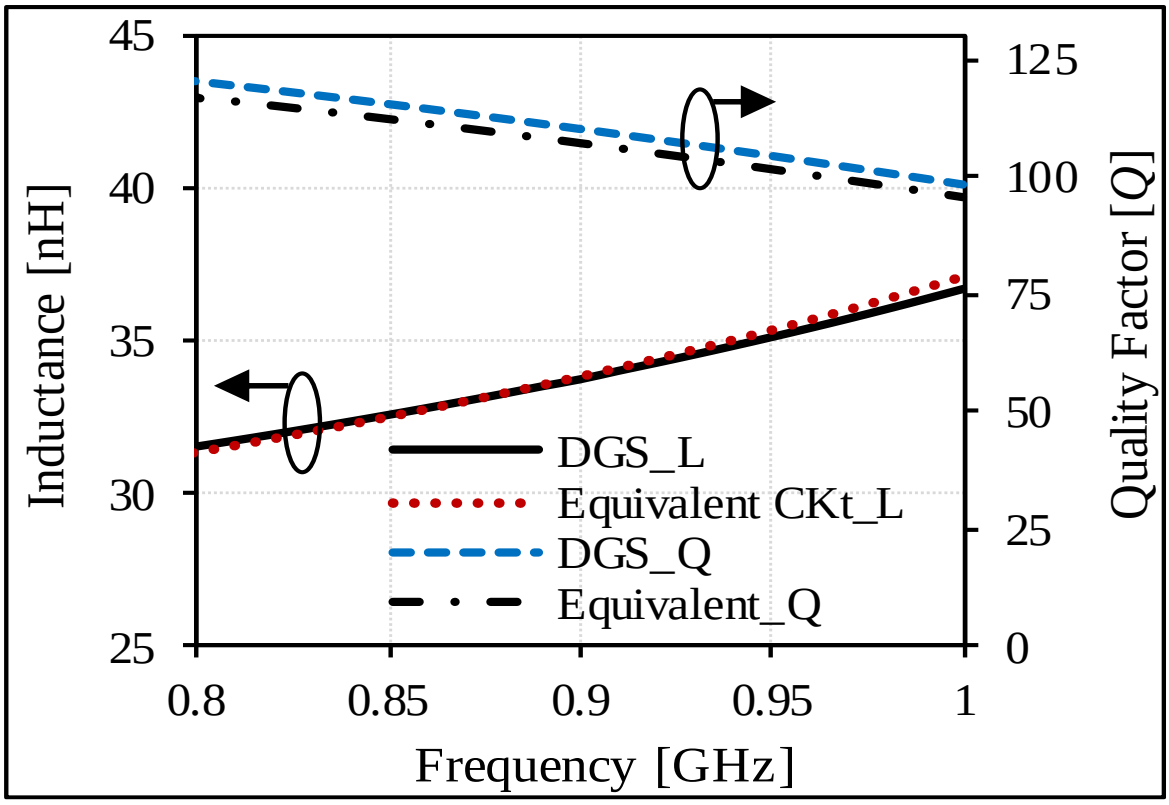
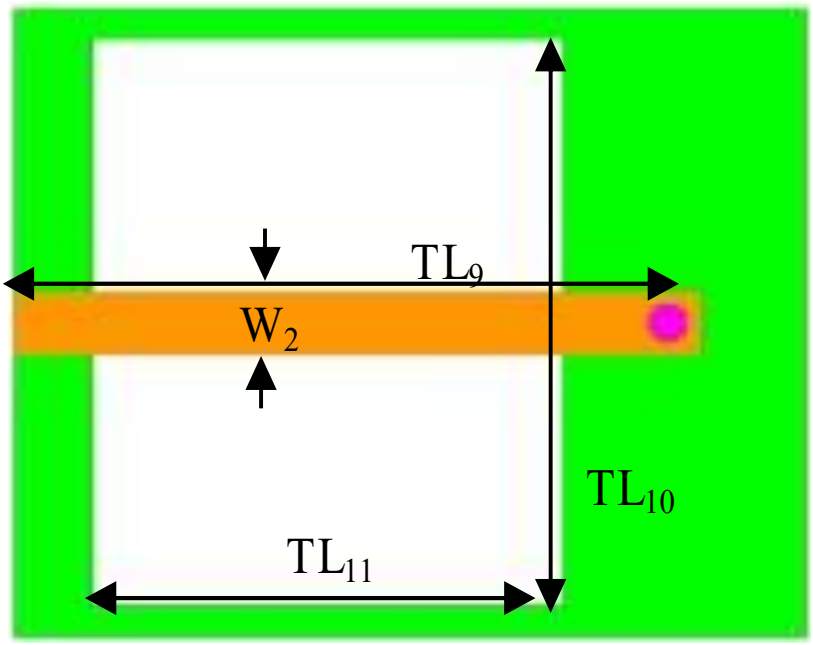


Fig. 2. 4: Comparison of inductance and quality factor of inductor in Fig. 2.3. At target 900 MHz it achieved inductance of 33.98 nH with a Q-factor of 110.67.



(a)

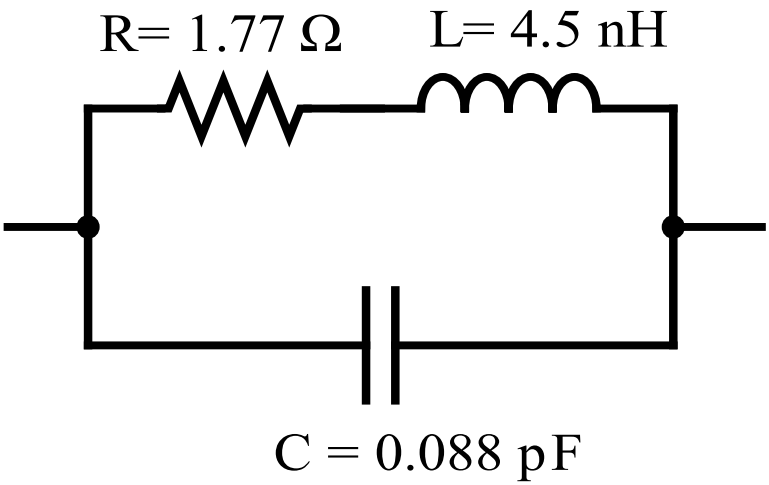


Fig. 2. 5: Design of DGS inductor to obtain 5 nH of inductance. (a) Layout of DGS inductor (b) Equivalent circuit diagram. Dimensions are in mm: TL_9 = 5.2, TL_{10} = 4.5, TL_{11} = 3.5, W_2 = 0.5.

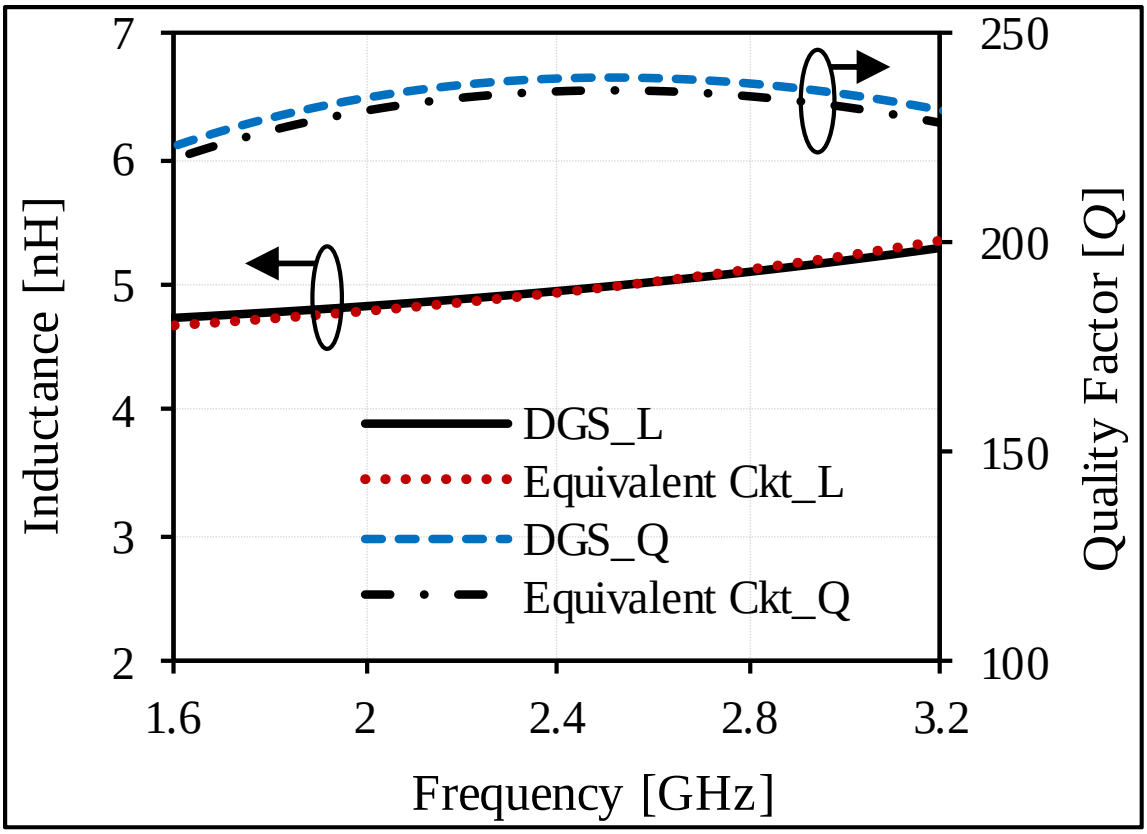


Fig. 2. 6: Comparison of inductance and quality factor of inductor in Fig. 2.5. At target 2.4 GHz frequency it achieved inductance of 4.85 nH with a Q-factor of 239.43,

2.3.2 Load Modulation Technique

From simulation, the optimal efficiency load required for Rectifier-I operating at f_1 is 5.6 KΩ, while the load required for Rectifier-II operating at f_2 is 550 Ω. To achieve these different loads from a single circuit, a load modulation technique is used with an NPN BJT, as shown in Fig. 2.7. The NPN transistor turns off when the voltage at point 'a' is below 0.75 V (i.e., the transistor is OFF for $V_a < 0.75V$), and it turns ON when the voltage at point 'a' exceeds 0.75 V (i.e., the transistor is ON for $V_a > 0.75$ V).

When the input power is below 0 dBm, the transistor remains OFF, meaning only two resistive loads, R_1 and R_2, are active. The equivalent resistance (R_{eq}) in this state is the sum of R_1 and R_2 i.e., $R_{eq} = R_1 + R_2$. During the simulation, R_1 is set to 3.2 KΩ and R_2 to 2.4 KΩ, resulting in an equivalent resistance of 5.6 KΩ. When the input power exceeds 8 dBm, the transistor turns ON, activating all three resistive loads: R_1, R_2, and R_3. In this state, the equivalent resistance (R_{eq}) is calculated as the parallel combination of ($R_1 + R_2$) with ($R_3 + R_{BJT}$), i.e., $R_{eq} = (R_1 + R_2)// (R_3 + R_{BJT})$ where R_{BJT} is the resistance of the BJT, and R_1 and R_2 remain fixed. Consequently, to achieve an equivalent resistance of 550 Ω, R_3 is selected to be 590 Ω during the simulation, with the remaining resistance coming from the NPN BJT.

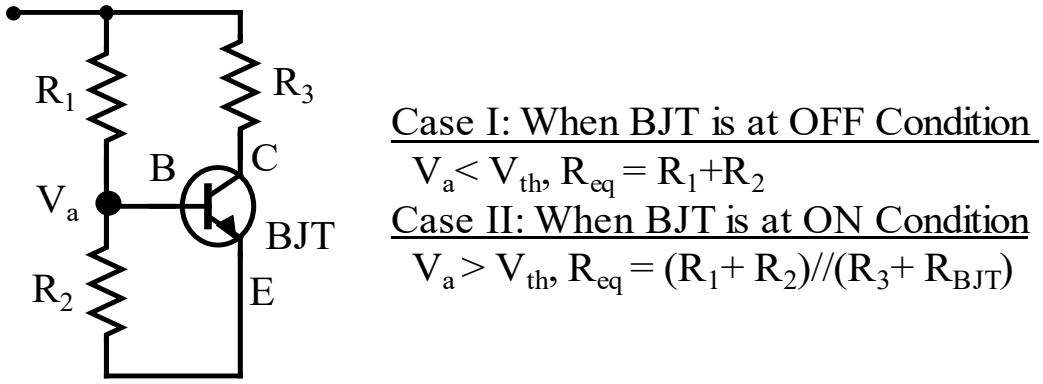


Fig. 2. 7: Load modulation for simultaneous low-power and high-power operating using BJT.

2.4 Fabrication of Frequency Switching Dual-power band Rectifier

For validation purposes, the proposed idea of frequency-switching dual power band rectification circuit is being fabricated on a Rogers3003TM substrate, which has a height of 0.762 mm and a dielectric constant of 3. The circuit simulation of this rectifier is conducted

using Keysight Advanced Design System (ADS), and the layout is designed using Ansys High-Frequency Structure Simulator (HFSS) software. In this proposed circuit, capacitor C_3 is employed to filter unwanted AC signals at point 'a', ensuring a pure DC at output. The final layout with all the dimensions and the fabricated prototype of the proposed rectifier are shown in Fig. Fig. 2.8 and Fig. 2.9, respectively.

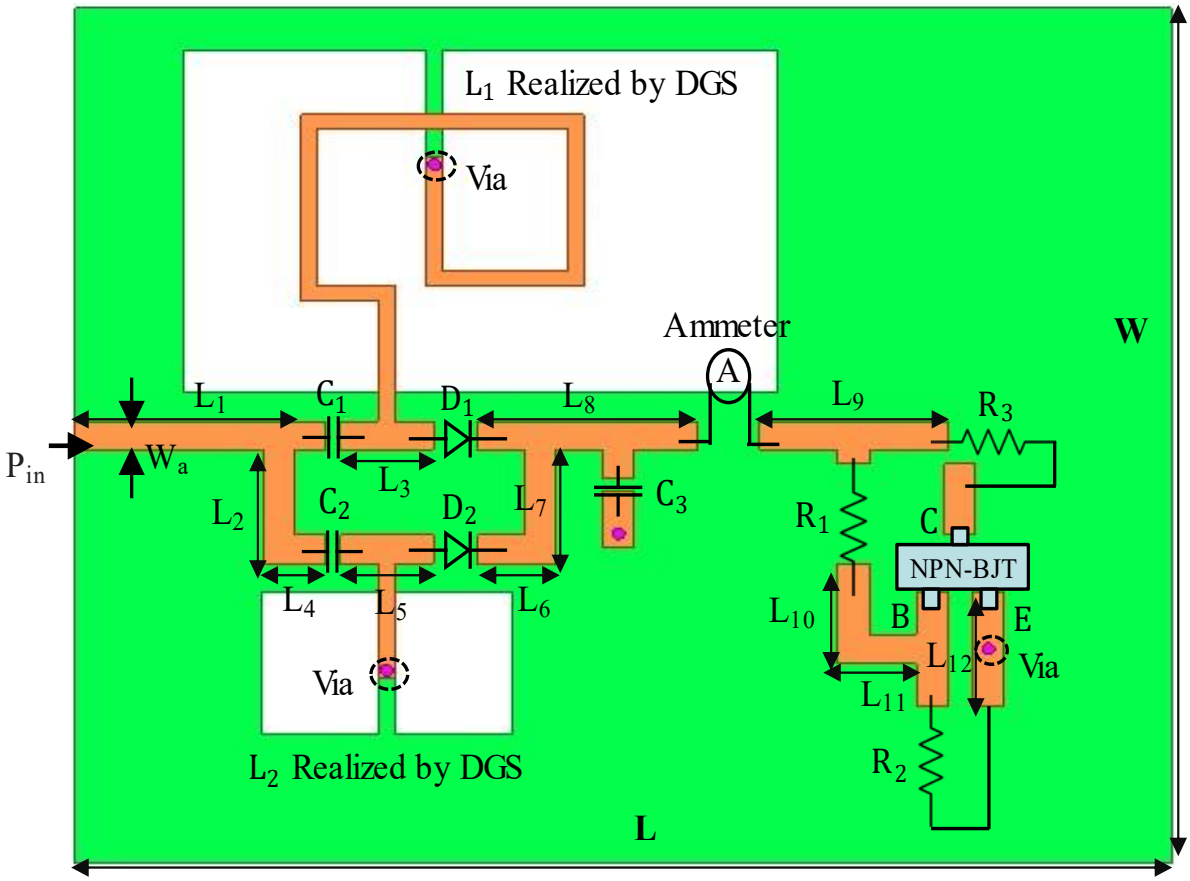


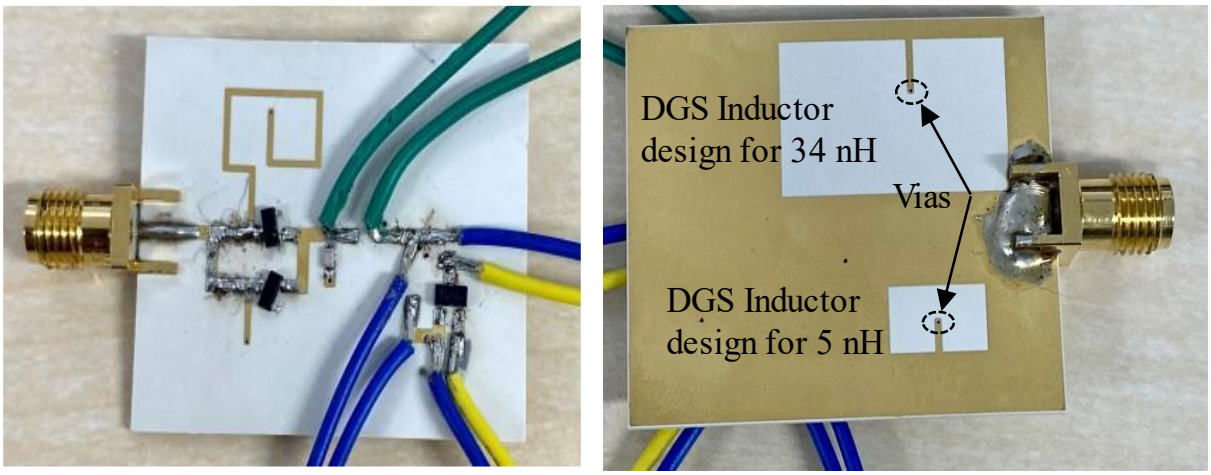
Fig. 2. 8: Layout of the proposed rectifier with all dimensions (in mm): L1 = 6.5, L2 = 4, L3 = 3, L4 = 2, L5 = 3, L6 = 2.5, L7 = 4, L8 = 7, L9 = 6, L10 = 3.5, L11 = 2.5, L12 = 4, Wa = 1, L = 35, W = 30.

2.5 Measurement of Frequency Switching Dual-power band Rectifier

2.5.1 Measurement of Reflection Coefficient (|S_{11}|)

The measurement was performed using the Keysight PNA series vector network analyzer (Part #N5222A), radiofrequency cables, resistors, and breadboard. The input signals for different power levels and the frequencies were laid open from PNA using the coaxial cable to

the proposed dual power band rectifier prototype, and the reflection coefficient were recorded for dual power band conditions.

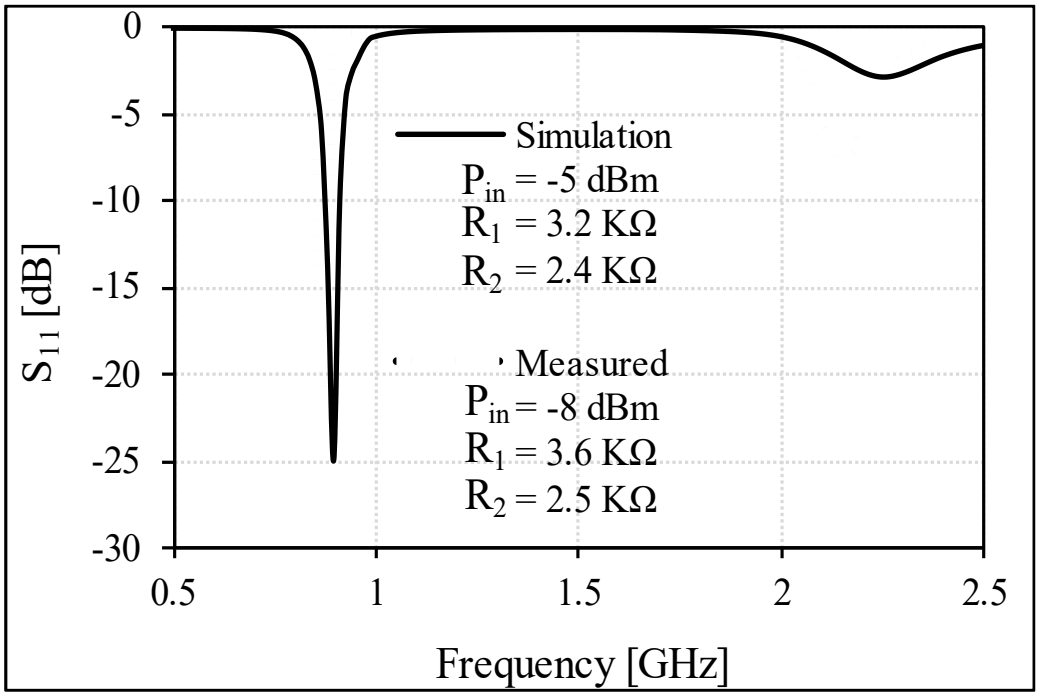


(a) (b)

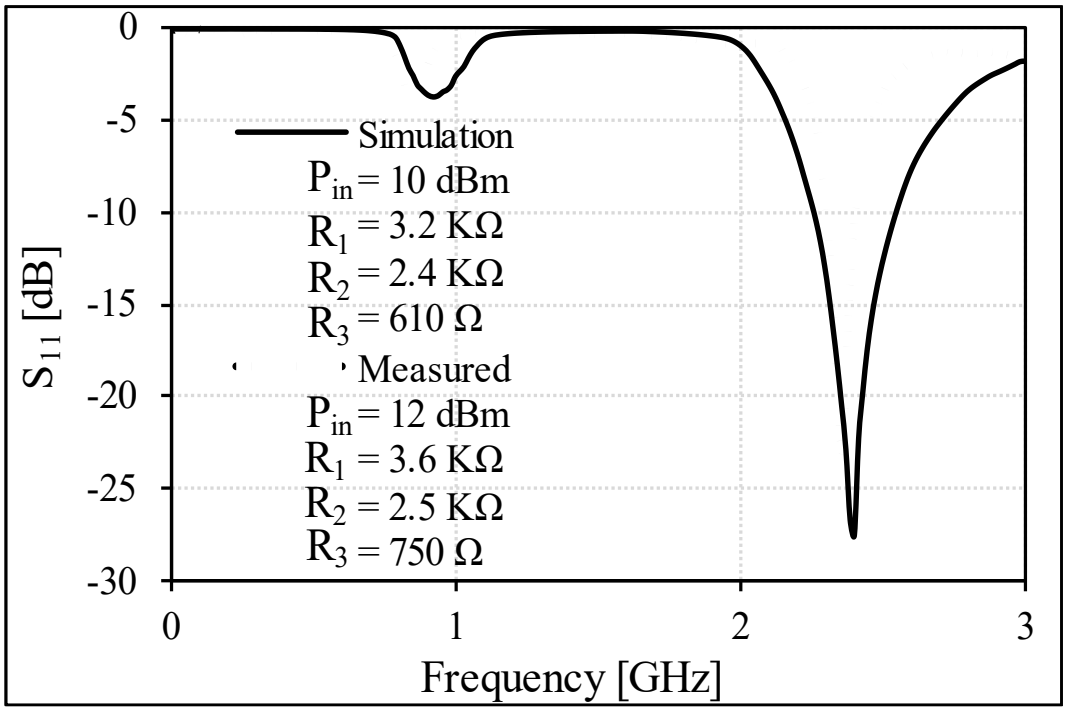
Fig. 2. 9: Fabricated device of the frequency switching dual-power band rectifier (a) Front side (b) Back side.

The comparison between simulated and measured $|S_{11}|$ values for frequency band f_1, intended for low-power applications, is depicted in Fig. 2.10(a) under their optimal input power and optimal load conditions (i.e., P_{in} = -5 dBm, R_1 = 3.2 KΩ and R_2 = 2.4 KΩ for simulation and P_{in} = -8 dBm, R_1 = 3.6 KΩ and R_2 = 2.5 KΩ for measurement, respectively). Similarly, Fig. 2.10(b) illustrates the comparison of simulated and measured $|S_{11}|$ for frequency band f_2, aimed at high-power applications, also under its optimal input power and optimal load conditions (i.e., P_{in} = 10 dBm, R_1 = 3.2 KΩ, R_2 = 2.4 KΩ, and R_3 = 610 Ω for simulation and P_{in} = 12 dBm, R_1 = 3.26 KΩ, R_2 = 2.5 KΩ, and R_3 =750 Ω for measurement, respectively).

During the measurements, frequency f_1 deviates from 900 MHz to 880 MHz where the frequency f_2 deviates from 2.4 GHz to 2.35 GHz, respectively. The input source for both Rectifier-I and Rectifier-II is same, therefore, for frequency f_1, there is a contribution of some losses due to the Rectifier-II circuit and similarly for frequency f_2, there is a contribution of some losses appeared due to the Rectifier-I circuit, respectively. These losses may be mainly appeared from the actual value of the capacitor and the soldering effect that we were not able to include during both the circuit and the electromagnetic simulation. Nevertheless, the measurement result shows that reflection coefficient $|S_{11}|$ stays well below -10 dB for both frequencies f_1 and f_2 our proposed dual power band rectifier.

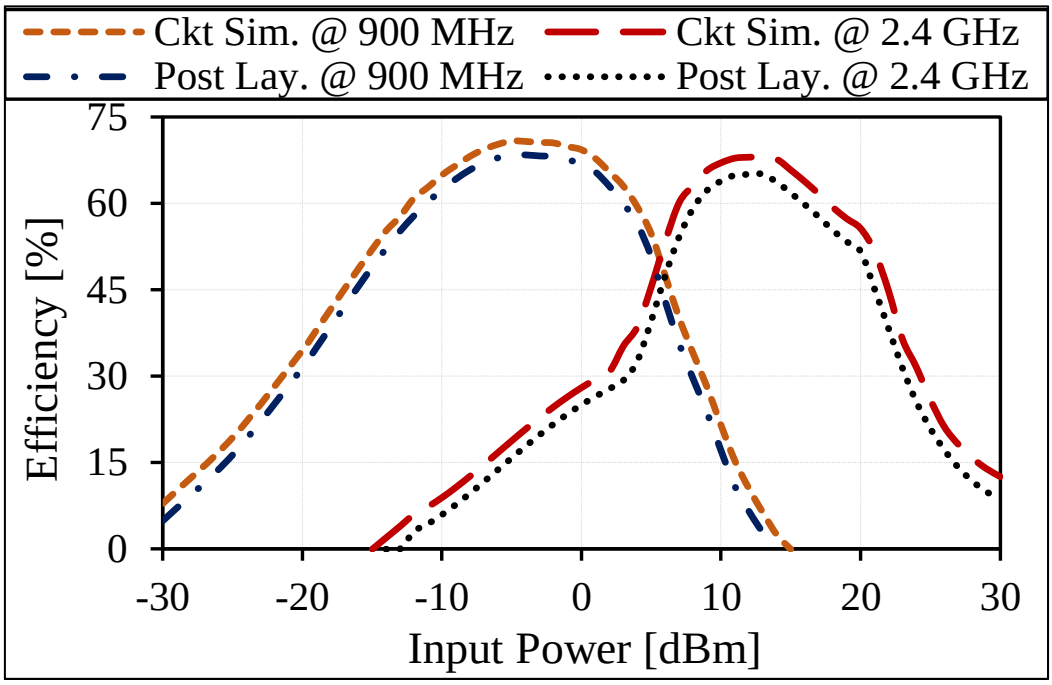


(a)

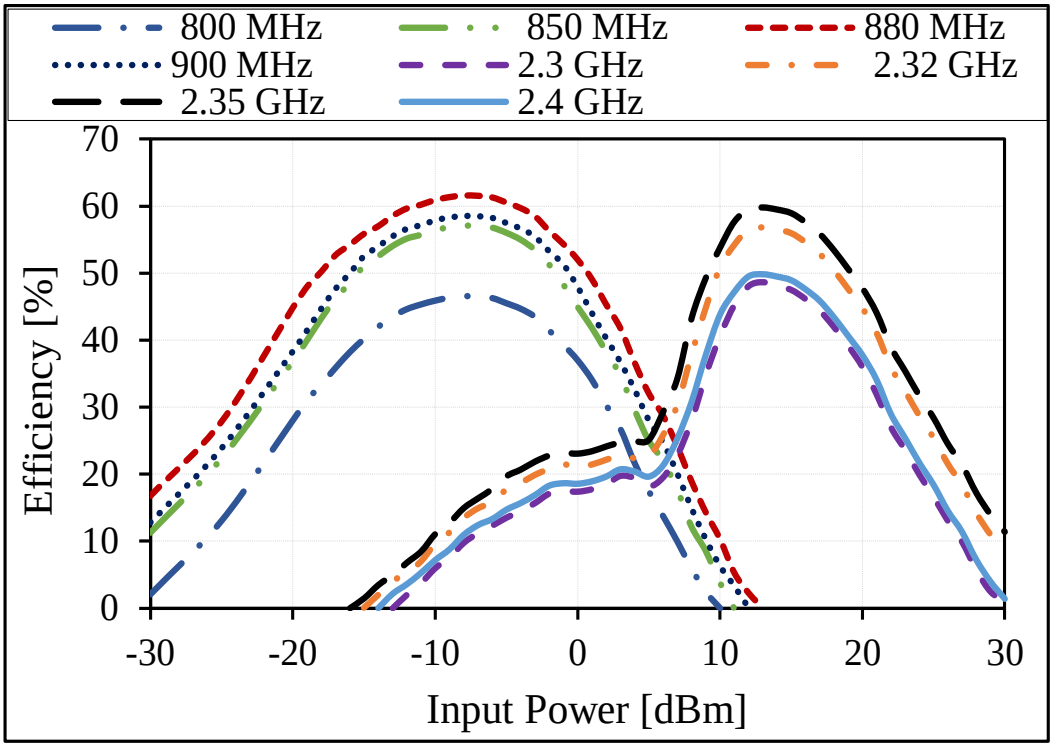


(b)

Fig. 2. 10: Comparison of simulated and measured reflection coefficient $|S_{11}|$ (a) For operating frequency f_1, targeting low-power application (b) For operating frequency f_2, targeting high-power application.



(a)



(b)

Fig. 2. 11: RF-to-dc conversion efficiency versus input power for different frequencies. (a) Simulated (b) Measured.

2.5.2 Measurement of RF-to-dc Conversion Efficiency (η)

The RF-to-DC conversion efficiency obtained from circuit simulation and post-layout simulation of the proposed rectifier, with respect to input power levels for operating frequencies of 900 MHz and 2.4 GHz targeting low and high-power rectification, respectively, is depicted in Fig. 2.11(a).

For 900 MHz, the simulated maximum conversion efficiency exceeds 50% across an input power range of -15 dBm to 5 dBm with an optimal efficiency load of R_1 = 3.2 KΩ and R_2 = 2.4 KΩ, peaking at 68.545% efficiency at an input power of -5 dBm. Similarly, for 2.4 GHz, the simulated maximum conversion efficiency is above 50% within an input power range of 5 dBm to 17 dBm, with an optimal efficiency load of R_1 = 3.2 KΩ, R_2 = 2.4 KΩ, and R_3 = 610 Ω, reaching a peak efficiency of 65.081% at an input power of 10 dBm.

From the measurement of proposed rectifier, the obtained RF-to-dc conversion efficiency with respect to input power levels for different operating frequencies is shown in Fig. 2.11(b). For low-power band, the measured maximum conversion efficiency remains more than 50 % for the input power range of -18 dBm to 2 dBm at 880 MHz operating frequency with optimal efficiency load of R1 = 3.6 KΩ and R2 = 2.5 KΩ, with peak efficiency of 61.547% at Pin = -8 dBm. Similarly, for high-power band, the measured maximum conversion efficiency remains more than 50 % for the input power range of 8 dBm to 20 dBm at 2.35 GHz operating frequency with the optimal efficiency load of R1 = 3.6 KΩ, R2 =2.5 KΩ and R3 = 750 Ω, with peak efficiency of 59.521% at Pin = 12 dBm.

2.6 Summary

In this chapter, by tuning operating frequency at input, dual power bands are obtained from a single rectifier circuit with higher efficiency. In this rectifier development, frequency f_1 = 900 MHz is selected for low-power applications whereas f_2 = 2.4 GHz is selected for high-power applications. For impedance matching of the Rectifier-I and Rectifier-II, the required inductance values of 34 nH and 5 nH respectively are realized using DGS topology, resulting in reduced inductor loss and improved efficiency. This rectifier covered the input power range from -18 dB to 2 dBm and 8 dBm to 20 dBm maintaining more than 50 % of RF-to-dc conversion efficiency with overall circuit size of 35mm × 30mm. This dual power band rectifier

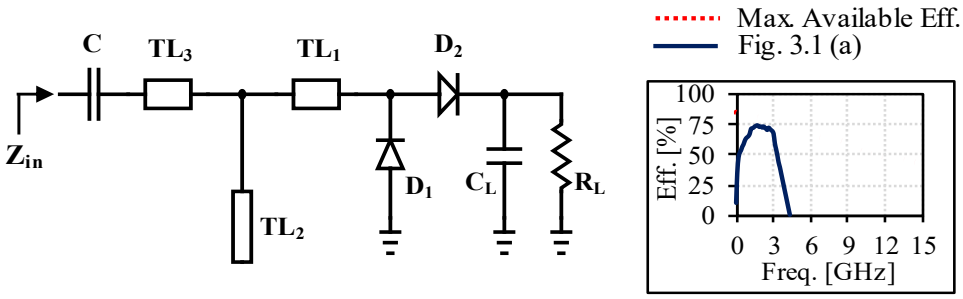
using a single rectifier circuit is the first development. The features of this single rectifier capable of working from as low as 15 μW to 0.1 W shows the bright sight that it a potential candidate for beamforming-based WPT that would require to work at the wide input power range for powering the target application.

Chapter 3: Miniaturized sub-6 GHz Rectification Circuit Utilizing Self-Impedance Matching Technique

3.1 Introduction

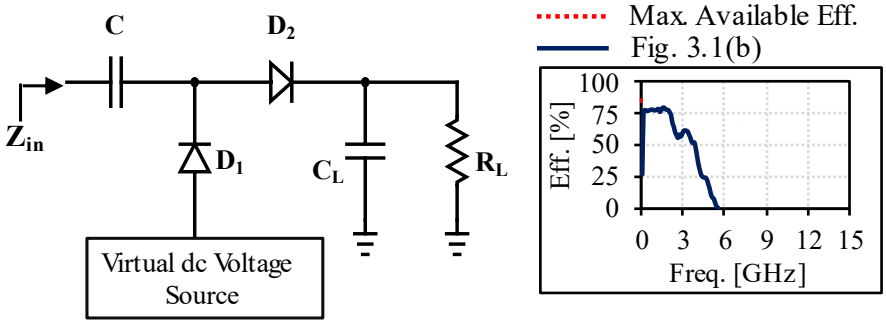
The recent introduction of 5G communication systems has brought about a significant transformation in the global telecommunications landscape. The rapid commercial deployment of 5G has been witnessed in various regions, including Japan. The 5G network encompasses different frequency ranges according to regions, such as 3.4-3.8 GHz in Europe, 3.6-4.2 GHz and 4.4-4.9 GHz in Japan, and 3.7-4.2 GHz in the USA. An intriguing characteristic of 5G communication signals is their substantial electromagnetic (EM) energy content. This presents an opportunity to harness free energy from the surroundings through 5G beamforming systems. The harvested energy can be used to power wireless sensor networks (WSNs) and Internet of Things (IoT) devices [51]-[54], which offers sustainability, cost efficiency, extended battery life, increased flexibility and scalability, and enhanced reliability, making 5G EH a recent popular trend. In future to power the high-power devices like laptops and mobiles wirelessly, a 5G beamforming-based WPT would be a potential area. But to cover the available frequency bandwidth, an efficient and compact ultra-wideband EH system is required. The performance of such an EH system is highly determined by the rectification circuit, which is essential for converting received EM signals into direct current (dc) [55].

Conventionally, in 2G/3G EH, low-power rectifiers are designed to convert the energy received from the base station located at a longer distance. However, in the case of 5G beamforming networks, transmitters are located closer to homes, offices, and workplaces. As a result, the available 5G signals exhibit high power density, the high-power rectifiers are therefore required to harvest these signals [56], [57]. Previous research has explored various rectifier designs for wideband rectifications, but many of them either used multi-band matching techniques with multiple long transmission lines [58]-[63] or employed complex matching topologies [64]-[68] resulting in bulky circuitry. Additionally, the rectifiers designed for higher frequencies exhibit higher losses due to impedance mismatch, parasitic effects, and circuit bulkiness, ultimately leading to lower power conversion efficiency (PCE) [69]. Therefore, achieving a wideband rectifier covering higher frequency bands with the highest power conversion efficiency and compact circuit size is a challenging task.



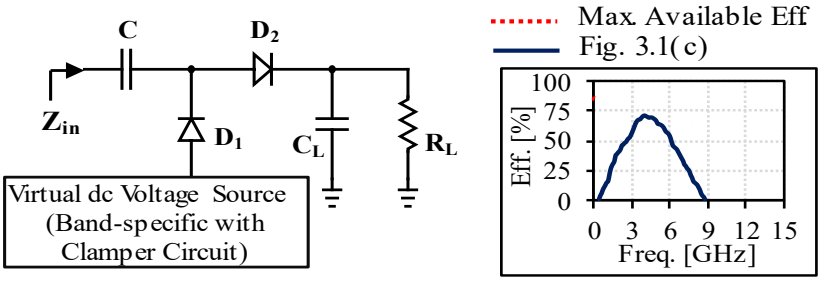
Disadvantage:
i) Bulky Circuit Size
ii) Uncontrolled on Peak EBW

(a)



Disadvantage:
i) Uncontrolled on Peak EBW

(b)



Result Obtained:
i) Compact Circuit Size
ii) Controlled on Peak EBW

(c)

Fig. 3.1: Comparison of maximum available EBW from voltage doubler circuit with the obtained EBW from different rectifier topologies. (a) Ref. [70]. (b) Ref. [40]. (c) Proposed rectifier. ** Conditions for Maximum Available Efficiency of Voltage Doubler are, port(z) = 100 Ohm, Pin = 20 dBm, f = 4 GHz, RL = 800 ohm.

The rectifier reported in [70] achieved over 50% of PCE for an ultra-wideband of 200 MHz to 3.2 GHz by employing a T-matching network at the input as shown in Fig. 3.1(a). However, this design topology used long-transmission lines TL_1, TL_2, and TL_3 to realize the T-matching network, resulting in a bulky circuit size of 5.7 cm^2. Also, the rectifier reported in [40] utilized the concept of a virtual dc voltage source, as shown in Fig. 3.1(b), that helped to eliminate the necessity of additional matching at input. This approach resulted in a compact circuit size of 1.48 cm2 with higher efficiency bandwidth (EBW) of 60 MHz to 3.32 GHz, along with more than 50% PCE. Nonetheless, this rectifier lacked the active elements to control the operating bandwidth maintaining maximum PCE. To the best of the author's knowledge, no rectifiers have been reported that can simultaneously control both the operating bandwidth and the peak PCE while maintaining a compact circuit size. In this work, our approach employs a novel idea of self-impedance matching using a driving rectifier as a virtual dc voltage source, as shown in Fig. 3.1(c). The driving rectifier has a half-wave rectifier with a series stub as an active element responsible for the rectifier's bandwidth and efficiency.

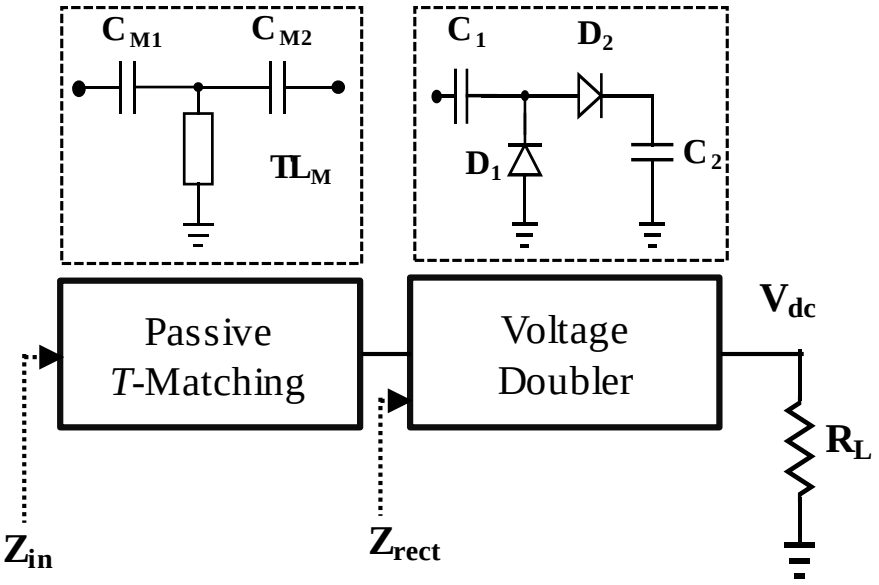
3.2 Design of Miniaturized sub-6 GHz Rectification Circuit Utilizing Self-Impedance Matching

3.2.1 Design Topologies for Wideband Rectification

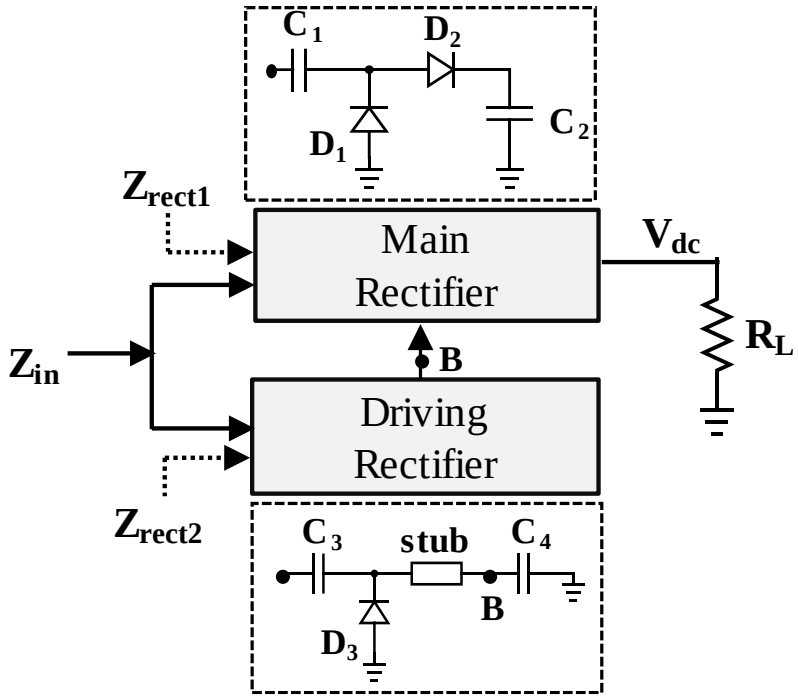
Rectifiers designed with passive matching networks, such as T-matching at the input, as depicted in Fig. 3.2(a), can provide ultra-wideband performance within a specific range. However, using such matching networks results in increased circuit bulkiness and poses a challenge in simultaneous optimization of operating bandwidth and PCE of the rectifier. This necessitates a trade-off between bandwidth and efficiency. To address this challenge, the innovative concept of self-impedance matching is introduced. This approach involves incorporating a voltage doubler circuit, referred to as the main rectifier for the actual rectification process, and replacing traditional input matching networks by a parallel driving rectifier, as shown in Fig. 3.2(b).

Fig. 3.2(c) shows the EBWs of the rectifier designed with two different approaches: i) passive *T*-matching using two matching capacitors C_{M1} and C_{M2} and one grounding short-stub line T_{LM} at the input (as shown in Fig. 3.2(a)), and ii) proposed self-impedance matching (as shown in Fig. 3.2(b)). In Fig. 3.2 (a), the values of C_{M1}, C_{M2}, and T_{LM} used to get the EBW of 25% and 67% are 0.26 pF, 0.33 pF, 5.5 mm and 0.81 pF, 0.88 pF, 3.5 mm, respectively. From

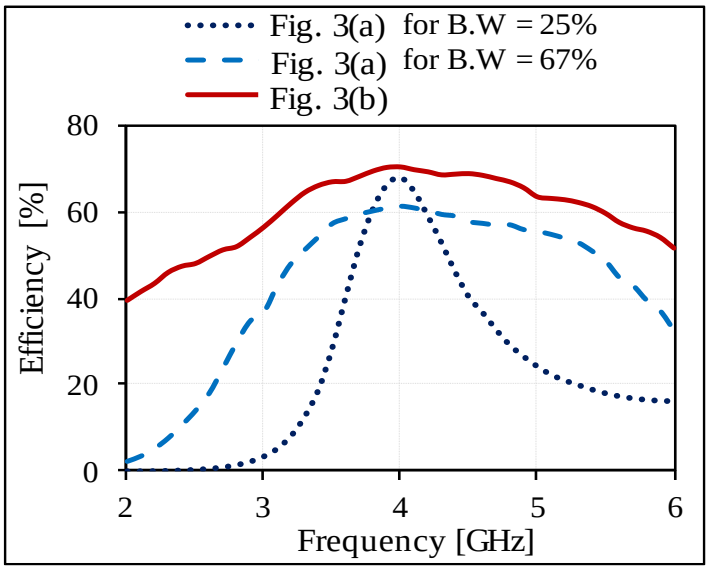
the simulation results, it is evident that the rectifier designed with *T*-matching at the input achieves higher efficiency but only within a narrow bandwidth and, to attain a wideband response, must have to compromises in terms of efficiency as shown in Fig. 3.2(c). In contrast, the proposed rectifier covers a wide frequency range while consistently maintaining high efficiency throughout the wide bandwidth.



(a)



(b)



(c)

Fig. 3. 2: Wideband rectifier design using (a) Passive T-matching network at input. (b) Proposed self-impedance matching technique. (c) Comparison of simulated efficiency bandwidths (EBWs) of Fig. 3.2(a) and Fig. 3.2(b).

3.2.2 Self-Impedance Matching Technique for Wideband Rectification

The schematic circuit diagram of the proposed rectifier is shown in Fig. 3.3. The proposed rectifier consists of two branches, the upper branch is a voltage doubler named the main rectifier, and the lower branch is a driving rectifier which is designed with a single diode and a stub line. Both the main rectifier and the driving rectifier are connected to the same input power. The key motivation of this method is to remove the input matching requirement at the input side. The equivalent model of the proposed rectifier including the diode parameters are shown in Fig. 3.4(a) and 3.4(b), respectively. The stub line is represented by the transmission line parameters in terms of the impedance (Zo) and the electrical length (θ).

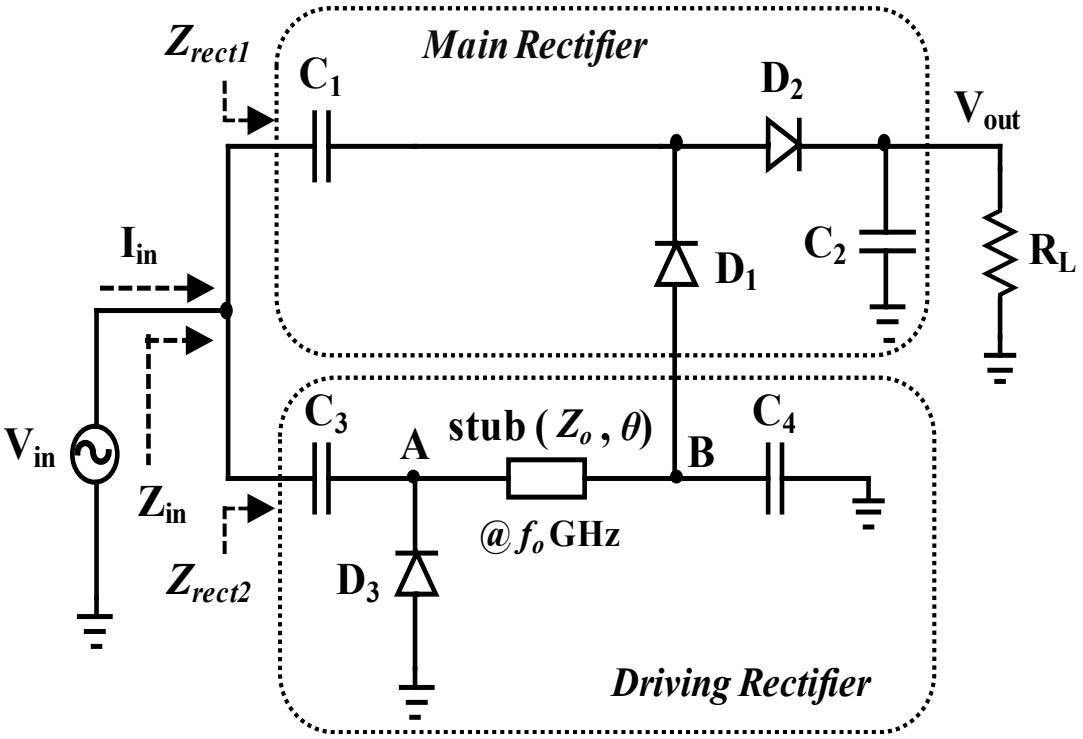
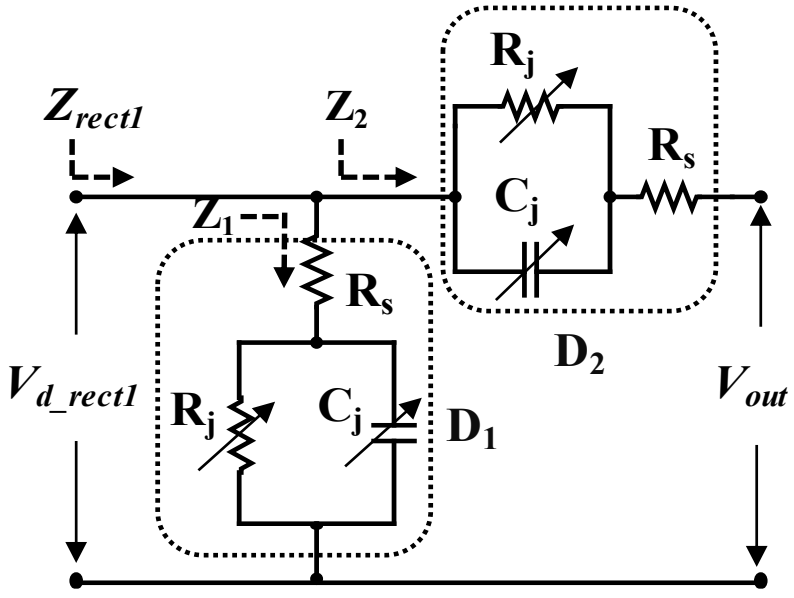
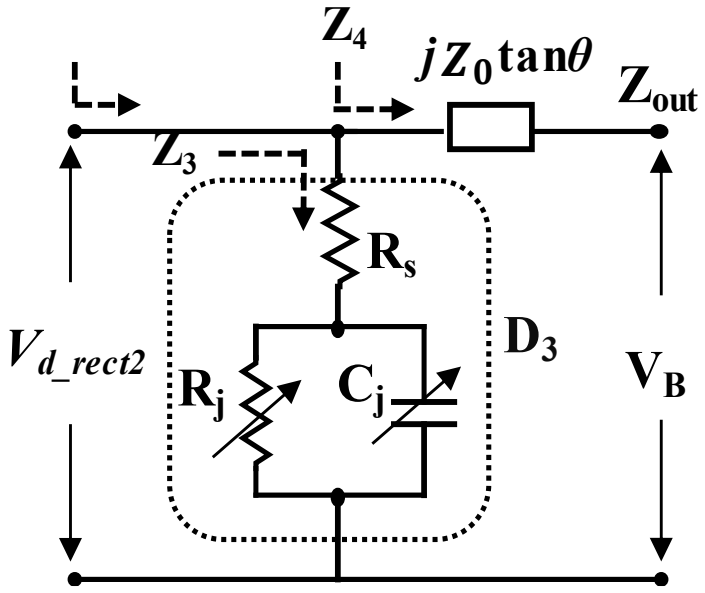


Fig. 3. 3: Schematic diagram of the proposed rectifier with self-impedance matching technique.



(a)



(b)

Fig. 3. 4: Equivalent circuit model of (a) Main rectifier circuit. (b) Driving rectifier circuit.

Diodes D_1, D_2, and D_3 are Schottky diode HSMS 2860 model, which consists of a series resistance (R_s), junction resistance (R_j), and junction capacitance (C_j). The incident voltage across the diodes D_1 and D_3 are represented as V_{d_rect1} and V_{d_rect2}, respectively, and the diode's junction voltage is V_j expressed as:

$$V_{d\_rect1} = -V_{out} + V_{d1\_rect1} \cos \omega t \tag{3.1}$$

$$V_{d\_rect2} = -V_B + V_{d1\_rect2} \cos \omega t \tag{3.2}$$

$$V_j = \begin{cases} -V_{j0} + V_{j1} \cos(\omega t - \phi), & Diode\ is\ OFF \\ V_f, & Diode\ is\ ON \end{cases} \tag{3.3}$$

where, V_{out} is output dc voltage, and V_B is dc voltage generated at point B. Similarly, V_{d1_rect1} and V_{d1_rect2} are peak incident voltages over the diodes D_1 and D_3, respectively, and ω is the angular frequency. V_{j0} is the dc component of the diode junction voltage, whereas

V_{j1} is its peak voltage. Additionally, ϕ is the phase delay between the incident voltage and the junction voltage and V_f is the build-in voltage when a diode is at ON state, respectively. The main SPICE parameters of the HSMS 2860 diode are: B_v = 7 V, V_f = 0.35 V, R_s = 6 V, C_j = 0.18 pF.

The impedance of the main rectifier is Z_{rect1} whereas the impedance of the driving rectifier is Z_{rect2}, respectively, are calculated by following the similar procedures as of [71].

$$Z_1 = Z_2 = \frac{1}{a^2+\omega^2 b^2}\{\pi a R_s - j\pi\omega b R_s\} \tag{3.4}$$

$$\text{where, } \begin{cases} a = \alpha_1 - \sin\alpha_1\cos\alpha_1 \\ b = R_s C_j\,(\pi - \alpha_1 + \sin\alpha_1\cos\alpha_1) \end{cases} \tag{3.5}$$

α_1 is turned-on angle for the main rectifier, expressed as,

$$\tan\alpha_1 - \alpha_1 = \frac{\pi R_s V_{out}}{R_L(V_{out}+V_f)} \tag{3.6}$$

From (3.4), Z_{rect1} is calculated as,

$$Z_{rect1} = Z_1 // Z_2 = \frac{1}{2(a^2+\omega^2 b^2)}\{\pi a R_s - j\pi\omega b R_s\} \tag{3.7}$$

Similarly,

$$Z_3 = \frac{1}{c^2+\omega^2 d^2}\{\pi c R_s - j\pi\omega d R_s\} \tag{3.8}$$

$$\text{where, } \begin{cases} c = \alpha_2 - \sin\alpha_2\cos\alpha_2 \\ d = R_s C_j\,(\pi - \alpha_2 + \sin\alpha_2\cos\alpha_2) \end{cases} \tag{2.9}$$

α_2 is turned-on angle for the driving rectifier, expressed as,

$$\tan\alpha_2 - \alpha_2 = \frac{\pi R_s V_B}{R_P(V_B+V_f)} \tag{3.10}$$

The impedance of the stub line (Z_0,θ) is calculated as,

$$Z_4 = Z_0 \left(\frac{Z_{out} + jZ_0 tan\theta}{Z_0 + jZ_{out} tan\theta}\right) \tag{3.11a}$$

$$\text{As, } Z_{out} = 0, \; Z_4 = jZ_0 tan\theta \tag{3.11b}$$

where, Z_0 is the characteristics impedance, and θ is the electric length of the stub. From (3.8) and (3.11b), Z_{rect2} is calculated as,

$$Z_{rect2} = Z_3 // Z_4 = \frac{Z_0 tan\theta \{\pi\omega d R_s + j\pi c R_s\}}{\pi c R_s + j\{(c^2+\omega^2 d^2) Z_0 tan\theta - \pi\omega d R_s\}} \tag{3.12}$$

From (3.7) and (3.12), the input impedance (Z_{in}) of the proposed rectifier becomes,

$$Z_{in} = Z_{rect1} // Z_{rect2}$$

$$Real(Z_{in}) = \frac{\pi R_s Z_0 tan\theta \{\omega M(bc+ad) + N(ac-\omega^2 bd)\}}{M^2+N^2} \tag{3.13}$$

$$Img(Z_{in}) = \frac{\pi R_s Z_0 tan\theta \{M(ac-\omega^2 bd) - \omega N(bc+ad)\}}{M^2+N^2} \tag{3.14}$$

where,

$$\begin{cases} M = \omega Z_0 tan\theta \{b(c^2+\omega^2 d^2) + 2d(a^2+\omega^2 b^2)\} + \pi R_s (ac - \omega^2 bd) \\ N = Z_0 tan\theta \{2(a^2+\omega^2 b^2) + a(c^2+\omega^2 d^2)\} - \pi\omega R_s (bc + ad) \end{cases}$$

To eliminate the imaginary part of Z_{in}, the following condition should be satisfied in (3.14),

$$M(ac - \omega^2 bd) = \omega N(bc + ad) \tag{3.15a}$$

$$(ac - \omega^2 bd) = \frac{\omega N(bc+ad)}{M} \tag{3.15b}$$

By substituting the values of M and N, (3.15a) can be expressed as,

$$Z_0 tan\theta = \frac{\pi R_s}{\omega}\left[\frac{\omega^2(bc+ad) + (ac-\omega^2 bd)^2}{O-P}\right] \tag{3.16}$$

where,

$$\begin{cases} O = (bc + ad)\{2(a^2+\omega^2 b^2) + a(c^2+\omega^2 d^2)\} \\ P = (ac - \omega^2 bd)\{b(c^2+\omega^2 d^2) + 2d(a^2+\omega^2 b^2)\} \end{cases}$$

After substituting the condition of (3.15b) on (3.13), Z_{in} is calculated as,

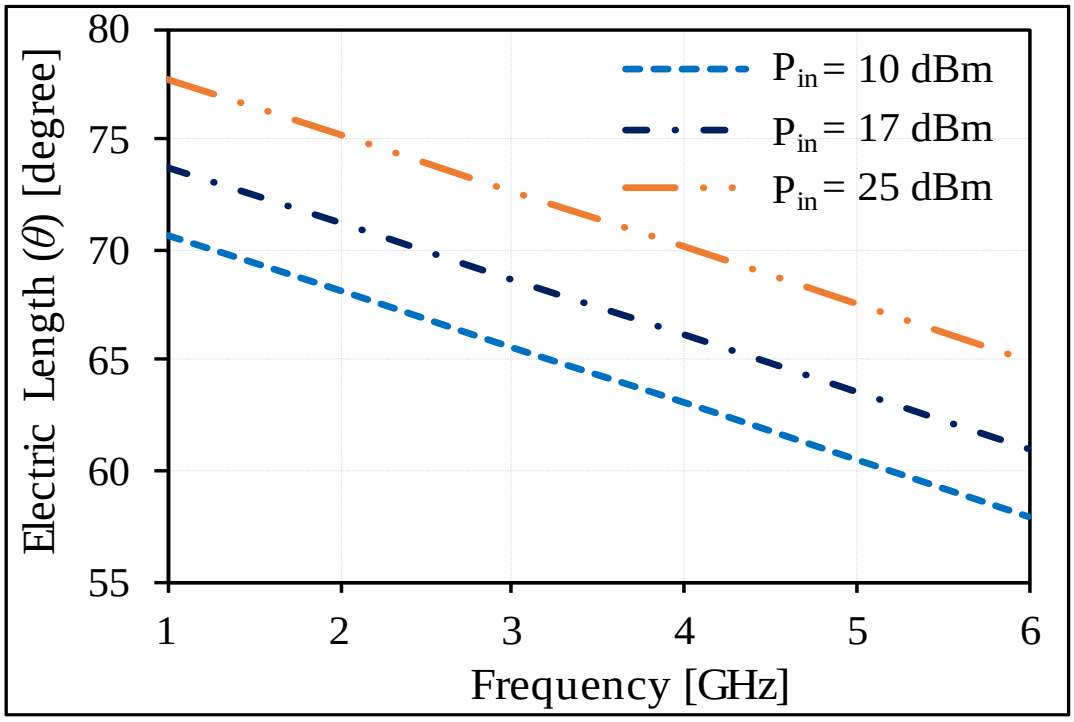
$$Z_{in} = Real(Z_{in}) = \left[\frac{\pi R_s \omega(bc+ad)}{M}\right] Z_0 tan\theta \tag{3.17}$$

with the value of M, (3.17) becomes,

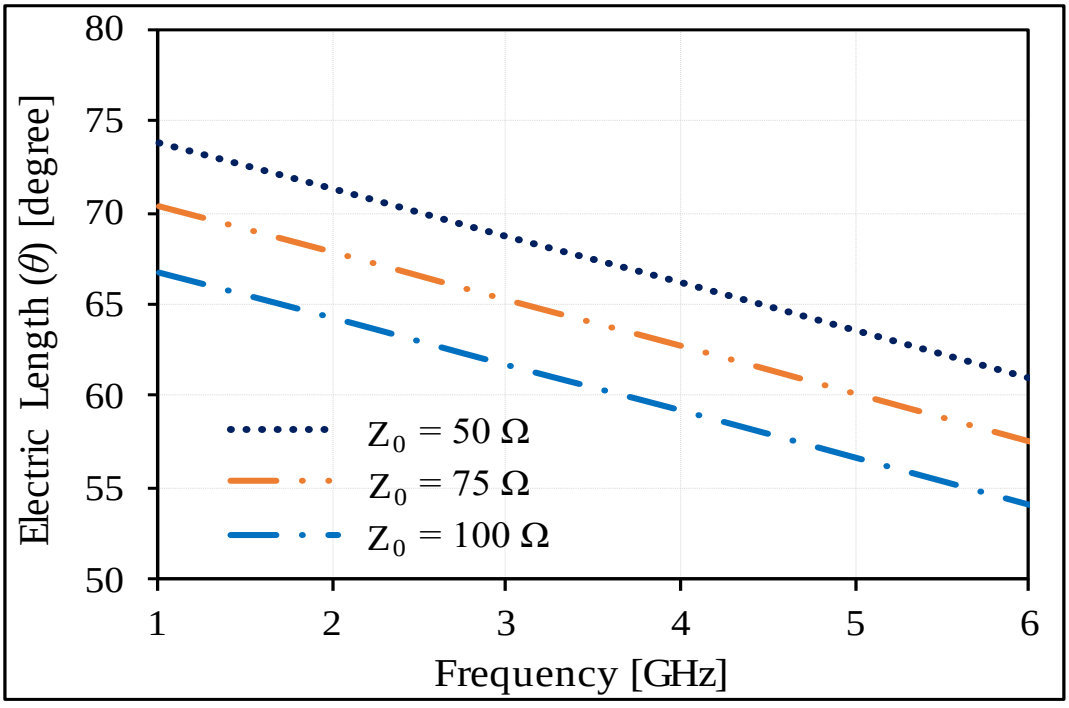
$$Z_{in} = \frac{\pi R_s\, \omega(bc+ad) Z_0 tan\theta}{\omega Z_0 tan\theta\{b(c^2+\omega^2 d^2)+2d(a^2+\omega^2 b^2)\}+\pi R_s(ac-\omega^2 bd)} \tag{3.18}$$

The characteristic of the proposed configuration is initially investigated through calculations. The values of a and b are obtained from (3.5) using α_1 which is computed from (2.6) with R_L = 450 Ω. Similarly, *c* and *d* are obtained from (9) using α_2 which is computed from (2.10), assuming R_P = 1 MΩ large impedance. By substituting these values into (3.16), $Z_0 tan\theta$ is obtained. For a perfect 50 Ω impedance, (3.15) is a condition that makes an imaginary part of Z_{in} equal to 0. Now, the final expression of the real part of Z_{in} is calculated in terms of ω and θ stated in (3.18). At the desired ω, the value of θ for Z_{in}= 50 Ω is obtained at particular Z_0 and P_{in} using (3.16) and (3.18). These calculations can be used to tune the input impedance of the proposed rectifier at a desired frequency. So, by a proper selection of Z_0 and θ, the frequency is decided as shown in Fig. 3.5.

Now, in Fig. 3.5(a), the different values of θ calculated from (3.16) to obtain real part of Z_{in} = 50 Ω from (3.18) for each frequency range from 1 GHz to 6 GHz under the condition of different input power levels at fixed Z_0 = 50 Ω is shown. Fig. 3.5(a) makes it clear that when power level is lower, small value of θ is required to make perfect 50 Ω matching. Similarly, in Fig. 3.5(b) the different values of θ calculated from (3.16) to obtain real part of Z_{in} = 50 Ω from (3.18) for each frequency range from 1 GHz to 6 GHz under the condition of different Z_0 at fixed input power P_{in} = 17 dBm is shown. Fig. 3.5(b) makes it clear that when stub impedance (Z_0) is higher, small value of θ is required, but large Z_0 makes the result in narrow transmission line which may have poor quality factor and higher losses. Considering these factors, we can select the stub line dimension to design the rectifier at the exact frequency and the power level that we need.



(a)



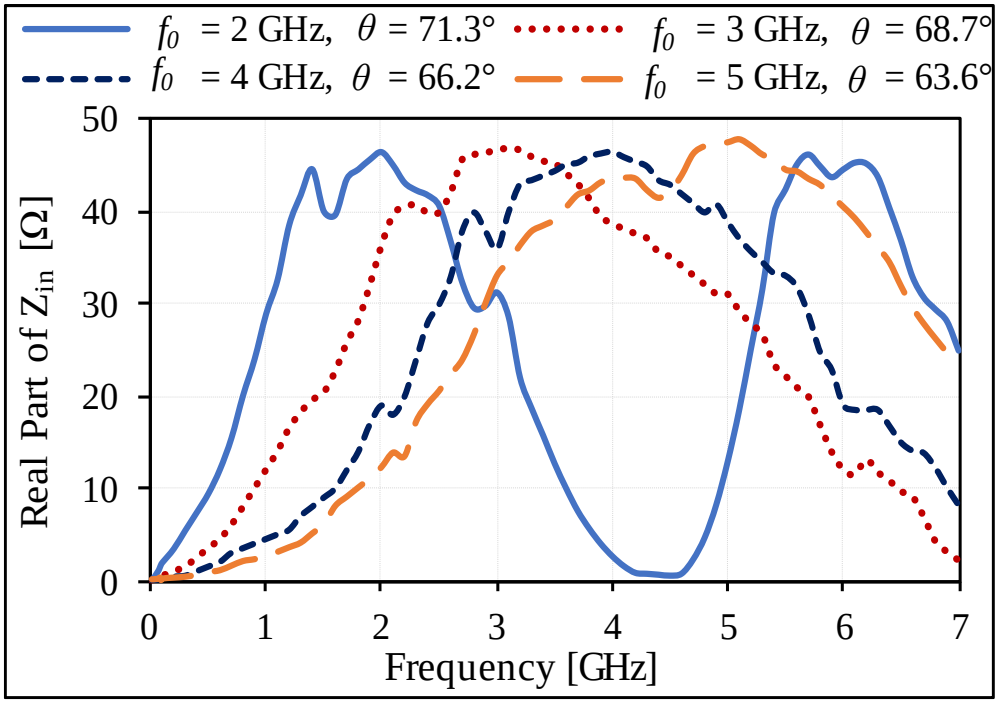
(b)

Fig. 3. 5: Example design: calculated values of θ to get real part of Zin= 50 Ω. (a) For different input power levels at fixed Z_0= 50 Ω. (b) For different Z_0 at fixed input power P_{in}= 17 dBm.

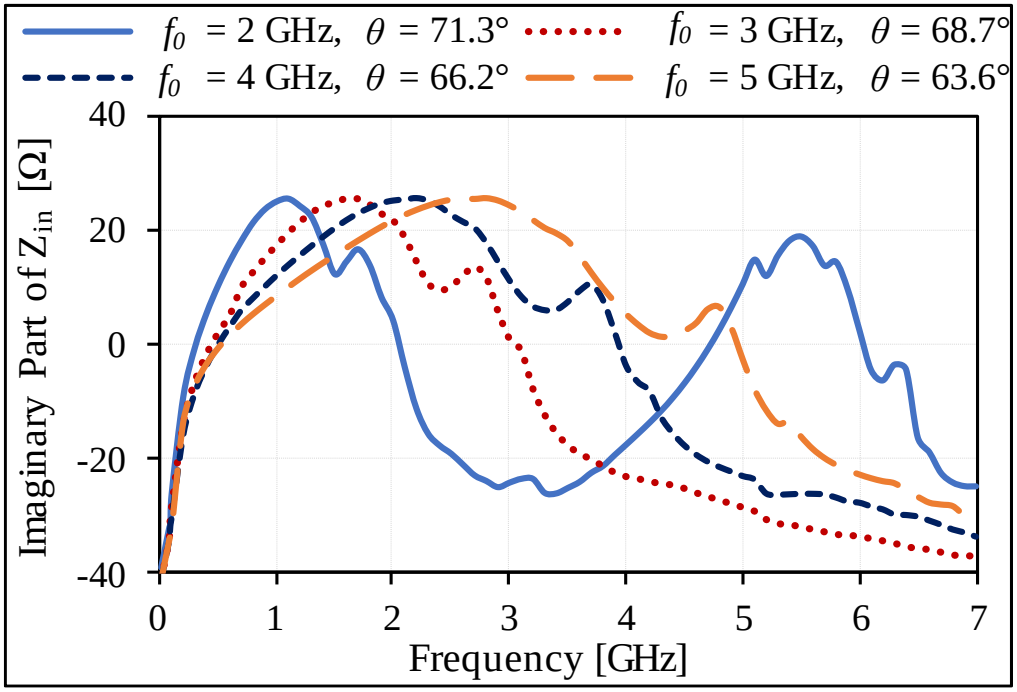
3.2.3 Schematic Simulation of the Proposed Rectifier with the Calculated θ values of the Stub Line

Using the calculated θ from (3.16), a schematic simulation of the proposed rectifier is performed in Keysight Advanced Design Structure (ADS #v2019.1) software. The simulated input of the proposed rectifier for different operating frequencies (f_0) and their respective calculated values of θ. of the stub is shown in Fig. 3.6.

Similarly, Fig. 3.7 shows the simulated reflection coefficient ($|S_{11}|$). Therefore, designer can carefully select θ at a specific f_0 with corresponding Z_0 and P_{in}, to design a self-impedance matching rectifier which work perfectly for the targeted frequency bandwidth and the target input power. Therefore, the guidelines presented from (3.1) to (3.18) best serve for estimating the initial parameters for designing the self-impedance matching rectifier.



(a)



(b)

Fig. 3. 6: Schematic simulated input impedance of the proposed rectifier with calculated θ for different designed f_0 of stub line at Z_0 = 50 Ω and P_{in}= 17 dBm (a) Real part (b) Imaginary part.

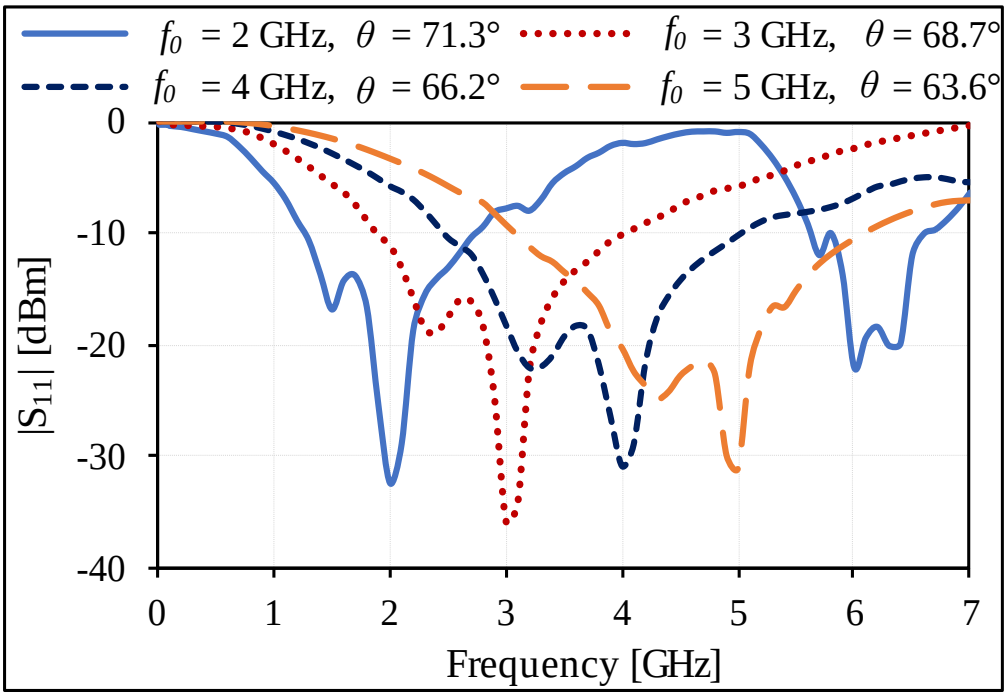


Fig. 3. 7: Example design: schematic simulated S-parameters for different designed (f_0) by changing the stub length (θ) at Z_0 = 50 Ω and P_{in}= 17 dBm.

3.2.4 Driving Rectifier as a Virtual dc Source

In [40], the present authors introduced the concept of a virtual dc voltage source by connecting the driving rectifier in parallel with the conventional voltage doubler. This approach generated virtual dc voltage from that parallel driving rectifier, which is sufficient to match the wide input impedance of the rectifier without the need of an external matching network at the input. However, [40] has the limitation of an uncontrolled frequency band and the requirement of relatively high input power to achieve peak PCE.

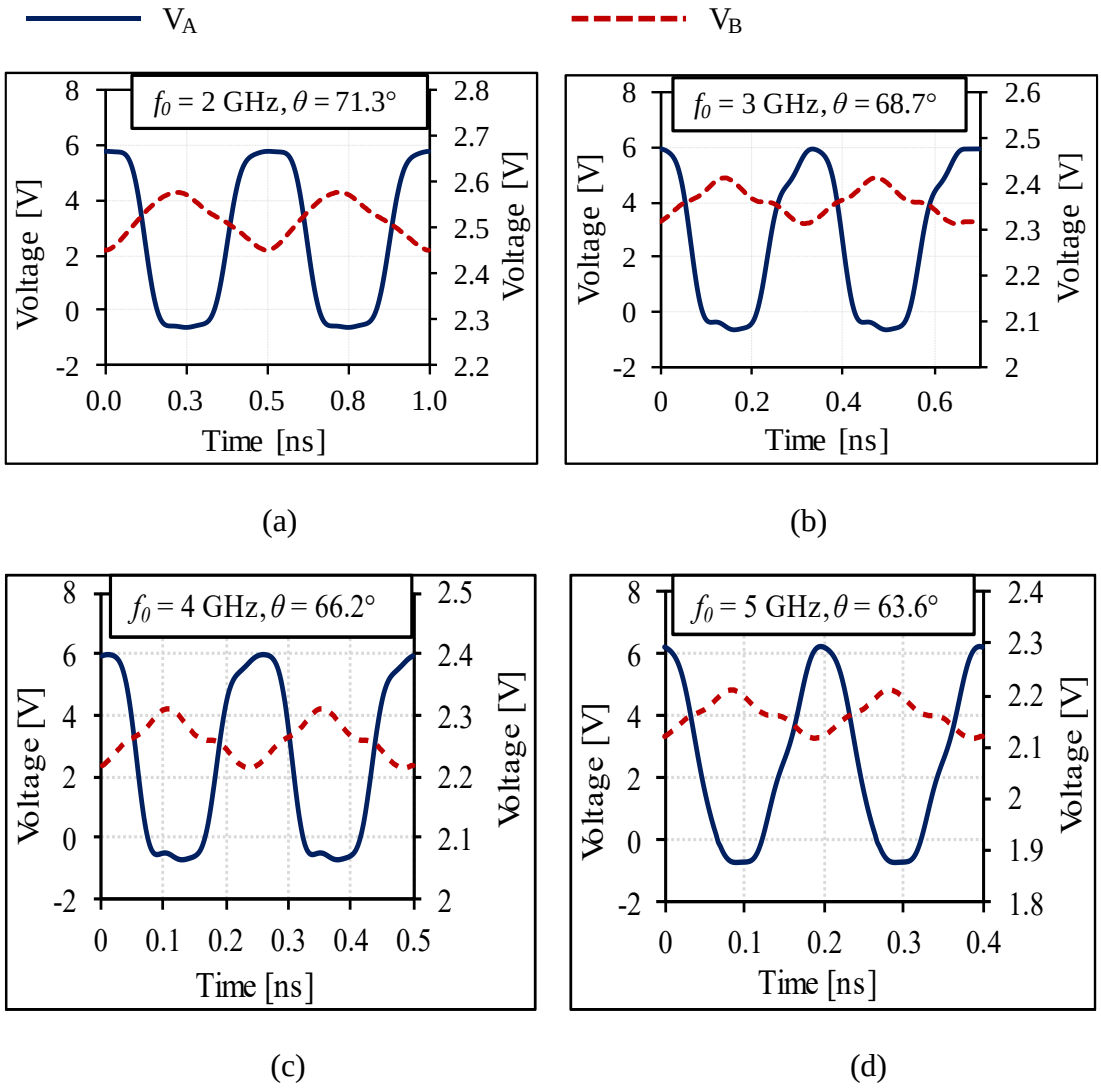
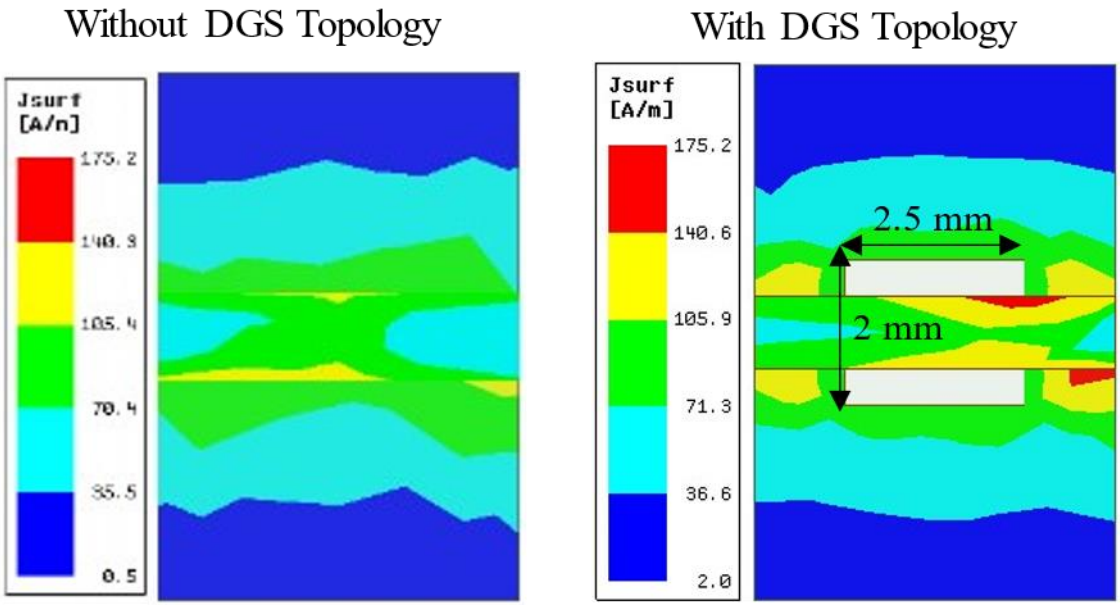


Fig. 3. 8: Simulated virtual dc voltage waveforms obtained at points A and B of the proposed rectifier (Fig. 3.3) for different designed (f_0) with their corresponding calculated θ at Z_0= 50 Ω and P_{in} = 17 dBm.

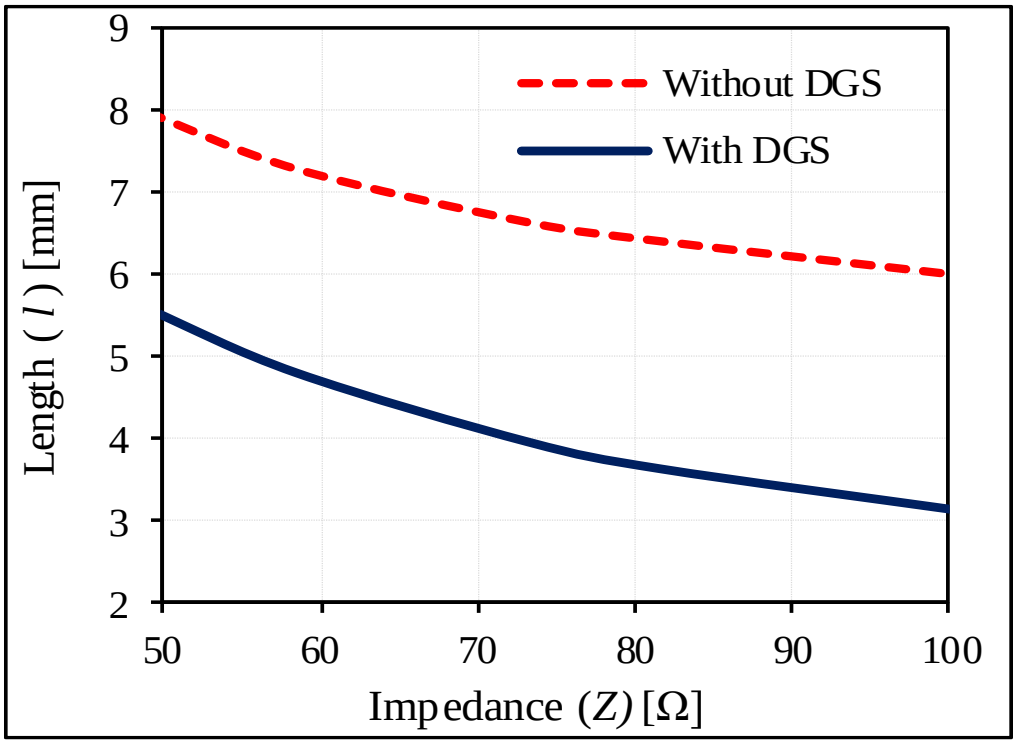
In this work, we utilize the similar concept of a virtual dc voltage source, but this time replace the series diode of the driving rectifier with a series stub line (Fig. 3.3). This proposal allows us to control both frequency and efficiency bandwidths simultaneously with reduced optimal input power required to achieve peak efficiency, as explained in Section II (B). Fig. 3.8 demonstrates simulated virtual dc voltage waveforms obtained at points A and B of proposed rectifier (Fig. 3.3) for different values of designed f_0 with corresponding calculated θ.

3.2.5 Design of High-impedance Stub Line using DGS Topology

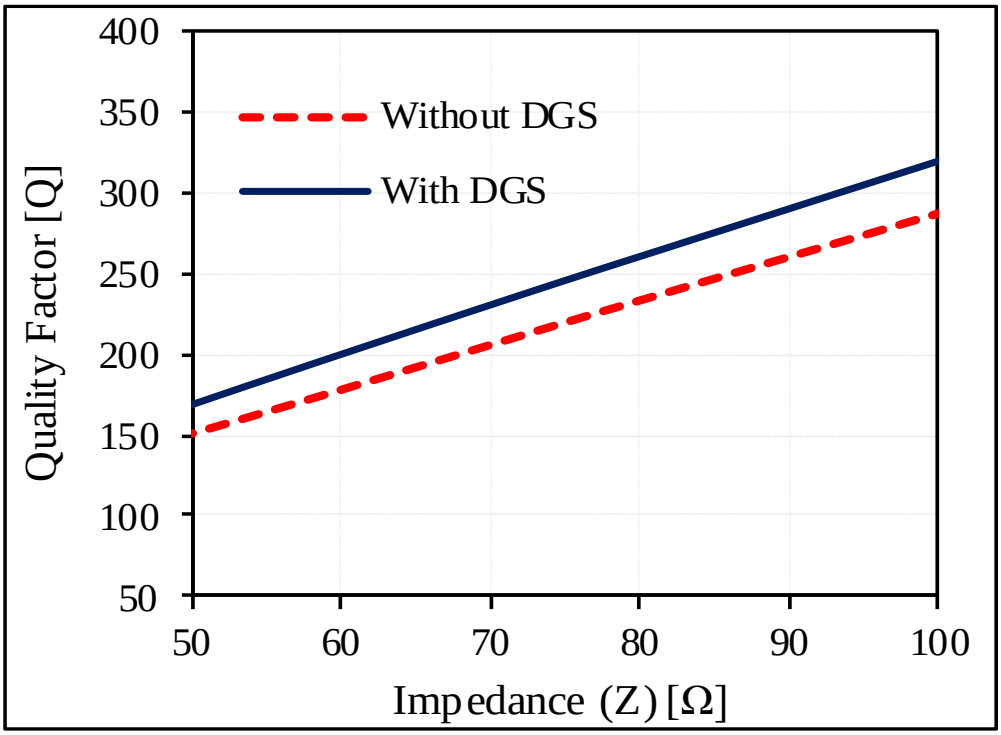
The use of large stub line will make the proposed circuit bulky and lossy. As an alternative, the DGS topology is employed to design high-impedance stub (Z_0, θ), which supports compact and low-loss circuits. In this work, DGS is achieved by making a small cut with the dimension of 2.5 mm × 2 mm in the ground plane. The current distribution in the stub for with and without DGS is shown in Fig. 3.9(a), which demonstrates that the DGS structure creates a disturbance in the current flow of the ground plane. Thus, with the DGS topology, the required stub length (l) becomes smaller with the improved quality (Q) factor, as shown in Fig. 3.9(b) and 3.9(c), respectively.



(a)



(b)



(c)

Fig. 3. 9: Performance comparison of the stub line design with and without DGS. (a) Current distribution. (b) Stub length vs. impedance graph. (c) Quality factor vs impedance graph.

3.3 Fabrication and Measurement of Miniaturized sub-6 GHz Rectification Circuit Utilizing Self-Impedance Matching

3.3.1 Layout Mask Preparation and Fabrication Prototype

All the simulation tasks of the proposed rectifier are performed in the ADS software. For the EM simulation and the layout preparation, the Ansys High-Frequency Structure Simulator (HFSS) software is used. The final layout of the proposed rectifier is shown in Fig. 3.10 and its dimensions are presented in Table 3.1. In the proposed rectifier, four lumped capacitors: C_1= C_2= C_3= C_4 = 100 pF are used where C_1 and C_3 for dc block and C_2 and C_4 for ac grounding. Similarly, three HSMS 2860 Schottky diodes D_1, D_2, and D_3 are used for the rectification purposes. To provide the ground during the measurement, the visa is necessary. In this work, multiple vias are used at a single place instead of a single via to reduce the effect of the via's inductance. The front and back side of the fabricated prototype of the proposed rectifier is shown in Fig. 3.11, which has the dimension of only 12mm × 6.3mm.

Table 3. 1: Design dimension of the Miniaturized sub-6 GHz Rectification Circuit Utilizing Self-Impedance Matching

L	W	L_1	L_2
12 mm	*6.3 mm*	*3 mm*	*1.8 mm*
L_3	$L_4 = L_9$	L_5	L_6
1 mm	*1.5 mm*	*1.4 mm*	*1.8 mm*
L_7	L_8	L_{10}	L_{11}
3.65 mm	*1.6 mm*	*3.75*	*2.3 mm*
W_1	L_{DGS}	W_{DGS}	D
0.8 mm	*2.5 mm*	*2 mm*	*0.25 mm*

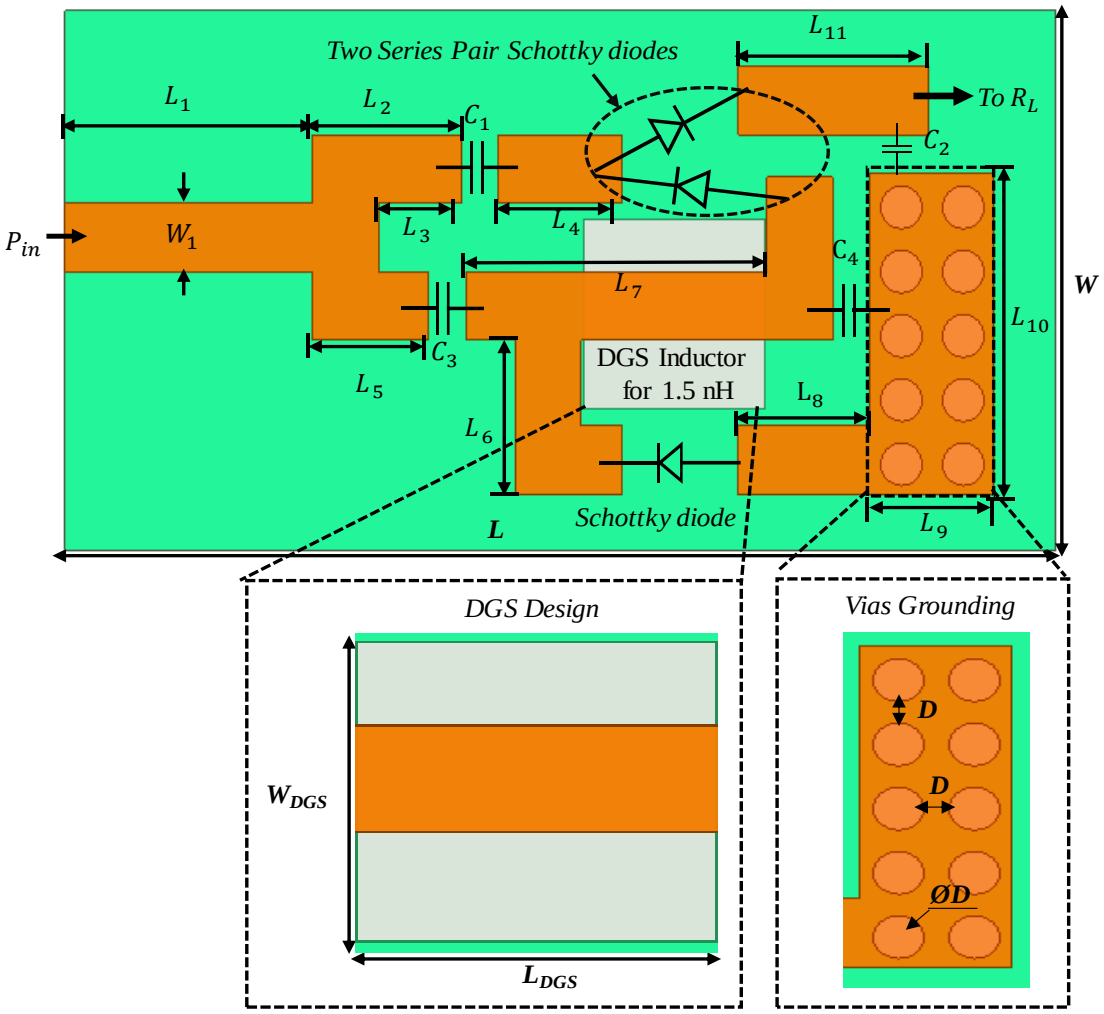


Fig. 3. 10: Layout preparation of the Miniaturized sub-6 GHz Rectification Circuit Utilizing Self-Impedance Matching.

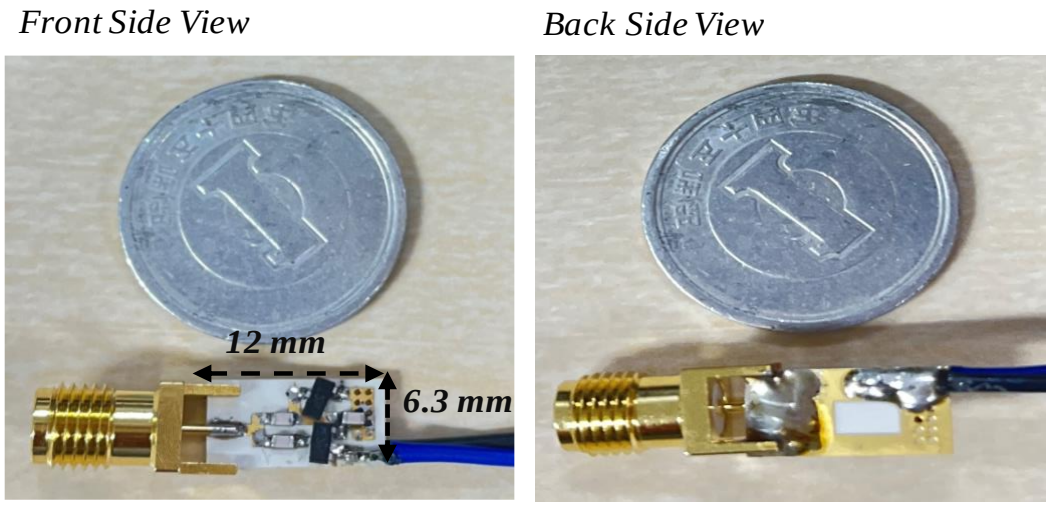


Fig. 3. 11: Fabricated prototype of the proposed rectifier

3.3.2 Simulation and Measurement Results

The setup for the measurement of reflection coefficient ($|S_{11}|$) and RF-to-dc PCE (η) of the proposed rectifier is shown in Fig. 3.12. $|S_{11}|$ is measured with a Keysight PNA series vector network analyzer (Part #N5222A). The simulated and the measured $|S_{11}|$ for different input power levels at their optimal efficiency conditions is shown in Fig. 3.13, where the measurement result accurately traces the simulation and stays well below -10 dB throughout the targeted bandwidth. For the output voltage measurement, an Anritsu vector signal generator (Part #MG3710A) and a digital multimeter were used.

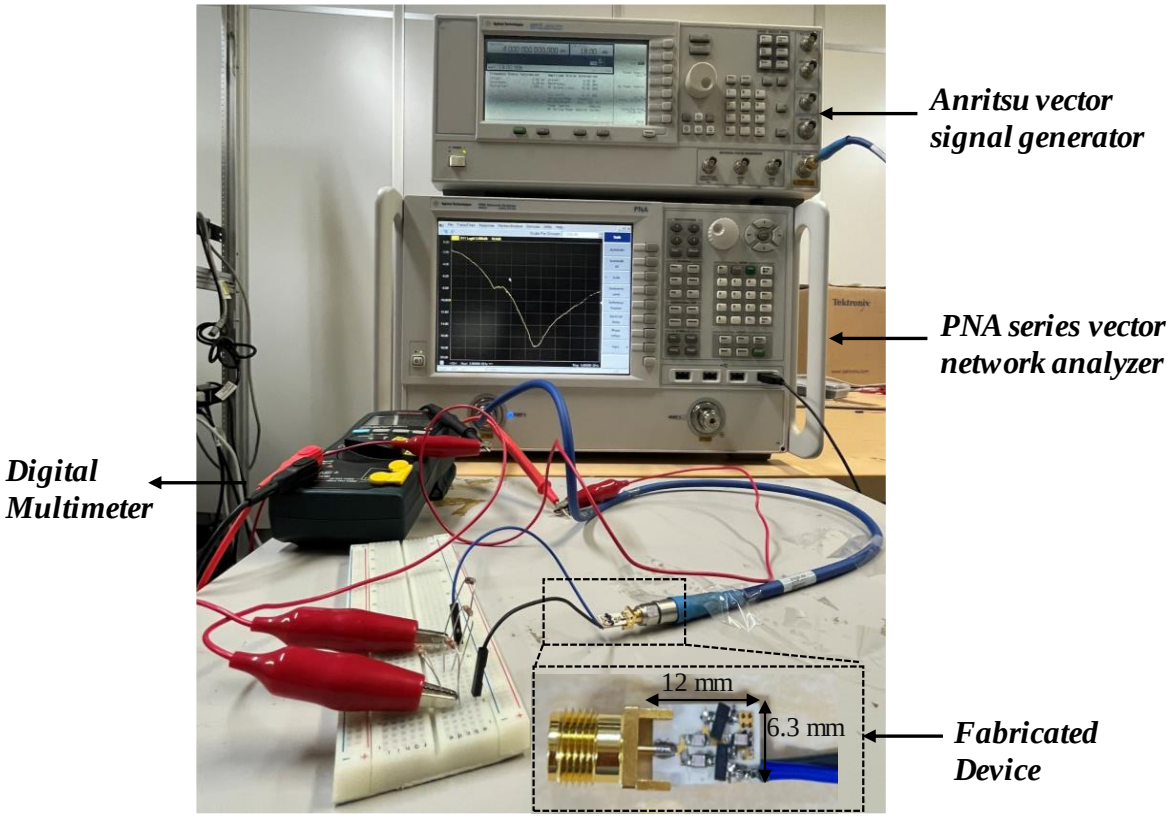


Fig. 3. 12: Measurement setup of the proposed rectifier.

The RF-to-dc PCE (η) of the proposed rectifier is calculated using:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\ \% = \frac{{V_{out}}^2}{R_L \times P_{in}} \times 100\ \% \tag{3.19}$$

where, P_{in} is input power, P_{out} is output power, V_{out} is output dc voltage, and R_L is load. The simulated and the measured PCE for different input power levels at optimal efficiency conditions is shown in Fig. 3.14.

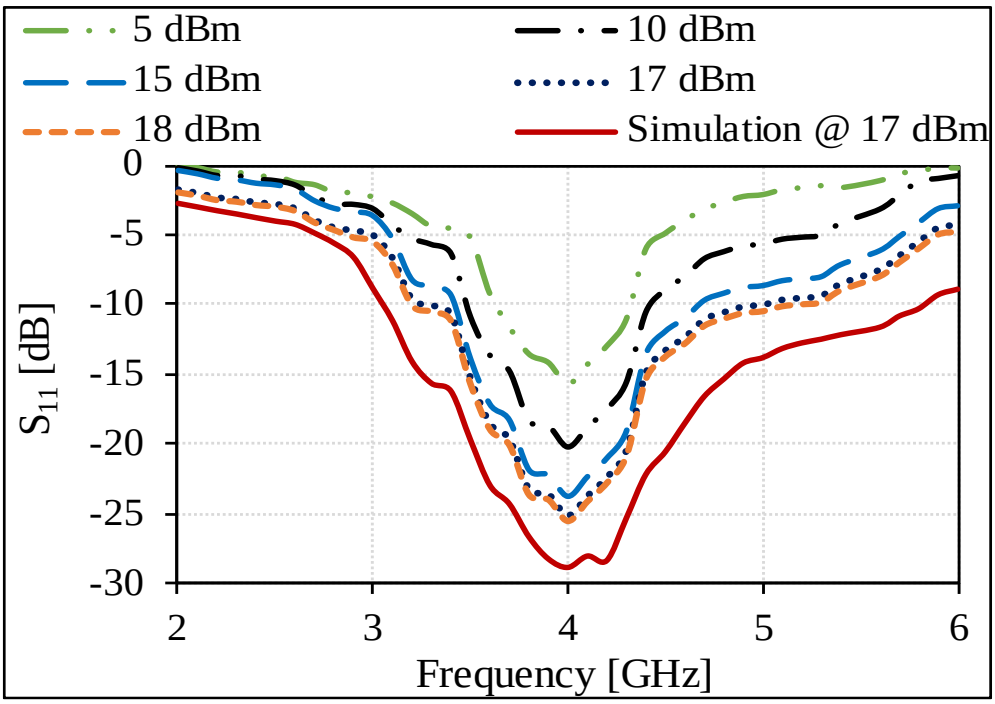


Fig. 3. 13: EM model simulated and measured $|S_{11}|$ for different input power levels at Z_0= 50 Ω, f_0 = 4 GHz and θ = 66.2°.

The maximum PCE achieved from overall EM simulation layout is 70.564% at optimal efficiency input power of 17 dBm and optimal efficiency load of 1.1 KΩ at 4 GHz optimal efficiency operating frequency, whereas the maximum PCE obtained from the measurement of fabricated prototype is 65.561% at the optimal efficiency input power of 18 dBm and the optimal efficiency load of 1.3 KΩ at 3.9 GHz optimal efficiency operating frequency, respectively. The measurement result shows that the proposed rectifier achieved a flat efficiency of more than 60% for the frequency bandwidth of 3.2 GHz to 5 GHz and 50% for the frequency bandwidth of 3 GHz to 5.8 GHz, respectively. Similarly, the simulated and the measured conversion efficiency for varying resistive loads are plotted at different input power levels shown in Fig. 3.15, which demonstrates that maximum efficiency is achieved at 1.3 KΩ of load for all input power levels during the measurement. The simulated and measured PCE for varying input power levels at optimal efficiency load and frequency conditions is shown in Fig. 3.16. The measurement results confirm that more than 50% of PCE is achieved for the

input powers from 10 dBm to 22 dBm. Similarly, the simulated and measured output dc voltage at optimal efficiency load and frequency conditions is shown in Fig. 3.17.

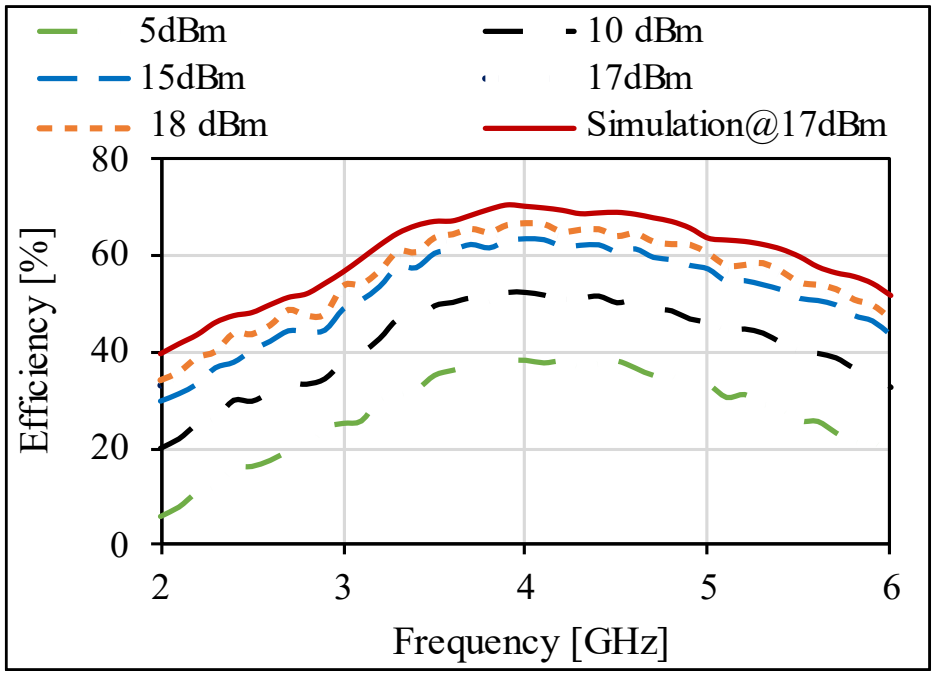


Fig. 3. 14: EM model simulated and measured PCE for different input power levels at Z_0 = 50 Ω, f_0 = 4 GHz and θ = 66.2°.

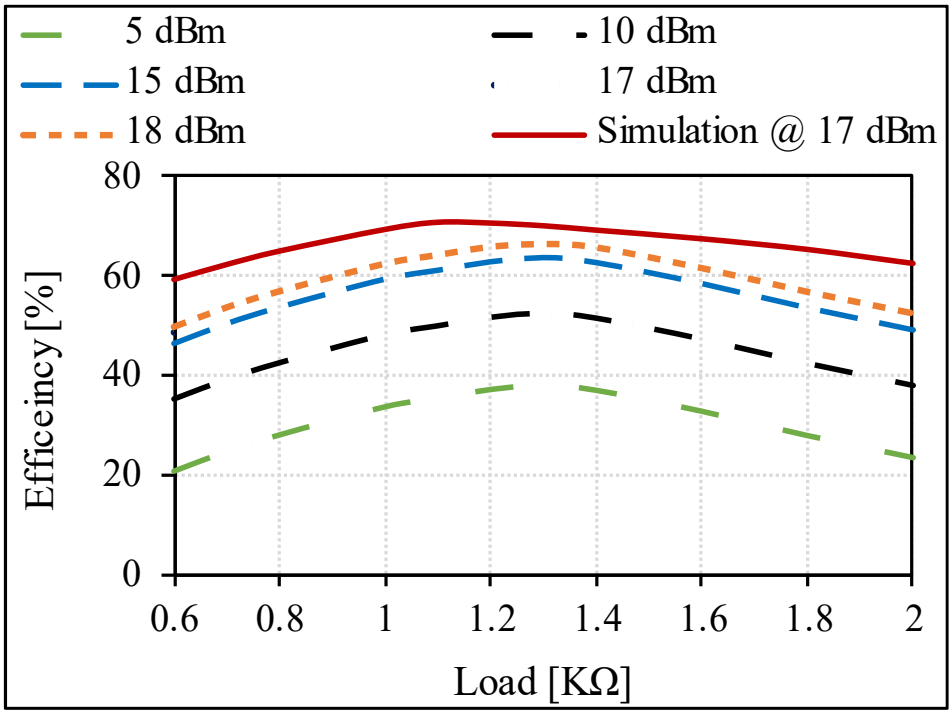


Fig. 3. 15: Simulated and measured PCE at 4 GHz and 3.9 GHz, respectively at different input power levels for varying loads.

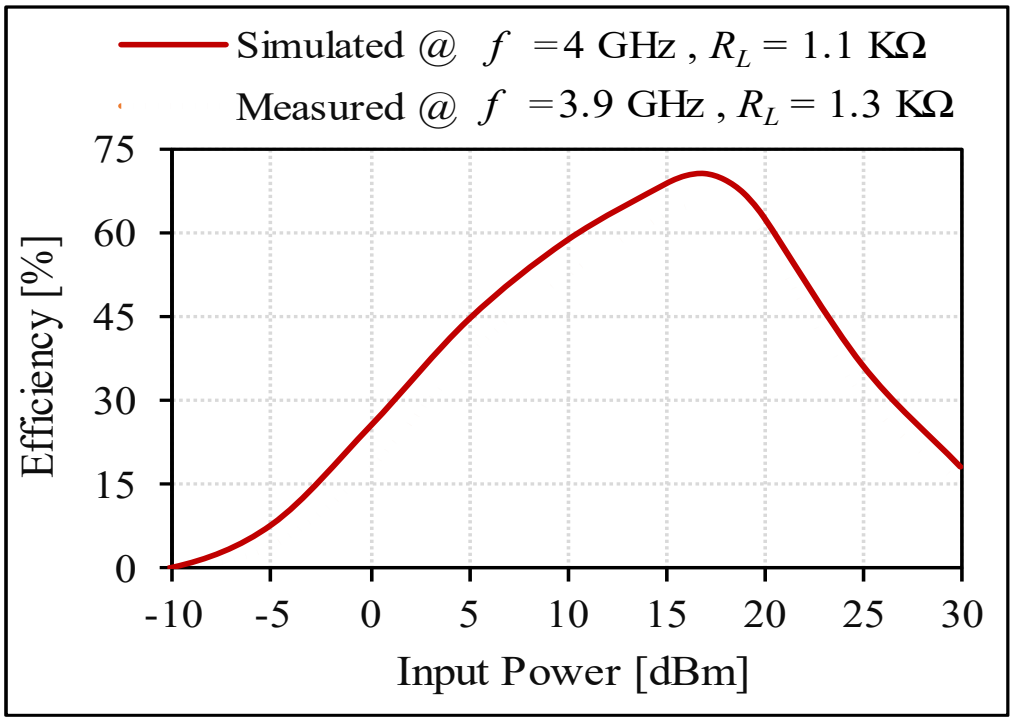


Fig. 3. 16: Simulated and measured PCE at optimal load and frequency condition for varying input power levels.

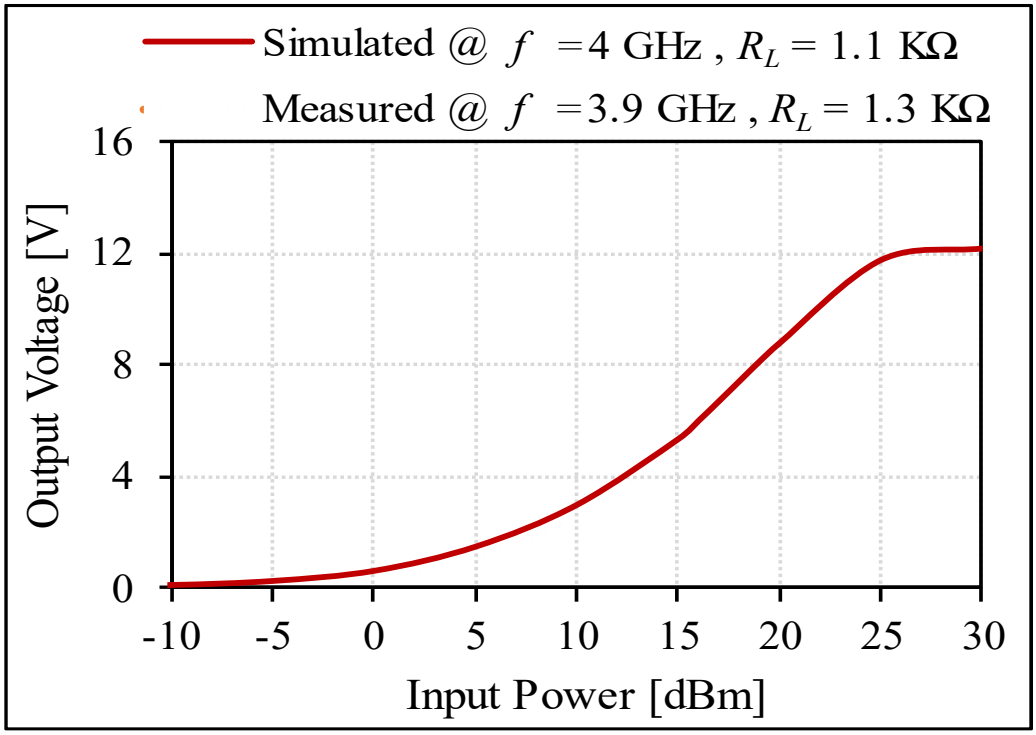


Fig. 3. 17: Simulated and measured PCE at optimal load and frequency condition for varying input power levels.

3.3.3 Performance Comparison

The measurement result of the proposed rectifier is compared with other related state-of-arts, as shown in the Table 3.2. The rectifier reported in [40] achieved ultra-wideband with higher PCE and compact circuit size, but it doesn't cover the targeted 5G frequency bands. Similarly, the rectifier presented in [71] obtained higher PCE for high frequencies but it has very narrow bandwidth and does not cover any frequency of 5G network. In [36], the rectifier achieved a good PCE for 3.7 GHz band of 5G, however, its circuit is bulky (approximately eleven times bigger than the proposed circuit) and does not cover 4.5 GHz band of the 5G. The rectifier reported in [72] covered the targeted frequency bandwidth with good PCE but its bandwidth for 50% efficiency is still lower and circuit size is approximately two times bigger as compared to the proposed rectifier.

Similarly, references [30] and [73], provided the maximum peak efficiency maintaining good PCE throughout the bandwidth but their circuits are bulky, approximately sixteen and seven times bigger than proposed rectifier, respectively and does not cover total available bandwidth of 5G.

Therefore, by employing new self-impedance matching technique, the miniaturized 5G rectifier is designed to cover total available frequency bandwidth of sub-6G band of the 5G network. The proposed rectifier covered 3 GHz to 5.8 GHz with fractional bandwidth (FBW) of 63.63 %. Beside this more than 50% of PCE is maintained in this bandwidth with the overall circuit size of only 0.756 cm^2 which is most compact due to the elimination of the matching circuit at input side which is usually done in traditional circuits.

The fractional bandwidth (FBW) is calculated using the following formula,

$$FBW = \frac{f_{u,\eta} - f_{l,\eta}}{\left(\frac{f_{u,\eta} + f_{l,\eta}}{2}\right)} \times 100\ \% \tag{3.20}$$

where, $f_{u,\eta}$ and $f_{l,\eta}$ are upper and lower frequency, respectively for greater or equal to specified PCE.

Table 3. 2: Performance Comparison of the proposed rectifier with other state-of-arts

Ref.	**Diode Type**	**Frequency [GHz]**	**RF-to-dc Conversion Efficiency (η)**	**Fractional Bandwidth (FBW)**	**Peak Efficiency (η_{max})**	**Size (cm^2)**
[30]	HSMS286	2.0 – 3.05 @ 10 dBm 1.8 – 3.3 @ 10 dBm	> 70% > 50%**	41.5% 58.8%	75.8% @ 14 dBm	12.6
[36]	HSMS286	1.75 – 3.55 @ 10 dBm 1.4 – 3.7 @ 10 dBm	> 70% > 50%	67.9% 90.196%	75%** @ 10 dBm	8.75
[40]	HSMS286	0.06 – 3.32 @ 10 dBm	> 50%	192.9%	77.3% @ 23 dBm	1.48
[71]	BAT15-03W	2.38, 4.99 1.78, 2.35, 4.97 @ 5 dBm	69.73%, 55.28% 60.95%, 71.37%, 54 %	N/A	69.73%, 55.28% 60.95%, 71.37%, 54% @ 5 dBm	N/A
[72]	HSMS286	3.0 – 5.1 @ 5 dBm	> 50%	51.8 %	55%** @ 5 dBm	1.5**
[73]	HSMS286	2.1– 3.3 @ 14 dBm 2– 3.3 @ 4 to 16 dBm	> 70% > 50%	44.4% 49.0%	76.3% @ 14 dBm	5.58
This work	**HSMS286**	**3.2 – 5 @ 18 dBm** **3 – 5.8 @ 18 dBm**	**> 60%** **> 50%**	**43.9%** **63.63%**	**65.56% @18 dBm**	**0.756**

N/A is not specified, ** Estimated from graphs.

3.4 Summary

In this chapter, a novel rectifier that employs the concept of self-impedance matching by connecting a driving rectifier in parallel with the conventional voltage doubler circuit is

proposed. The driving rectifier is designed with a half-wave rectifier and a series stub line realized as a virtual dc voltage source. The high-impedance stub line (Z_0, θ) of the driving rectifier is responsible for the frequency bandwidth adjustment of the proposed rectifier. The proposed concept makes the rectifier a most compact design by removing additional matching networks at the input and have simultaneous control on the frequency bandwidth and the peak efficiency. Such rectifier helps to effectively tune to design a desired rectifier at the target frequency band of the used 5G beamforming-based WPT system. The measurement result shows that the proposed rectifier covered all the accessible bandwidth of both 3.7 GHz and 4.5 GHz bands of 5G (from 3 GHz to 5.8 GHz) with more than 50% PCE with a circuit size of only 12mm × 6.3mm. Also, the use of DGS topology makes the proposed rectifier more compact and low-loss circuit. Such rectifiers can be applicable for beamforming-based WPT system of sub-6G signals from 5G network.

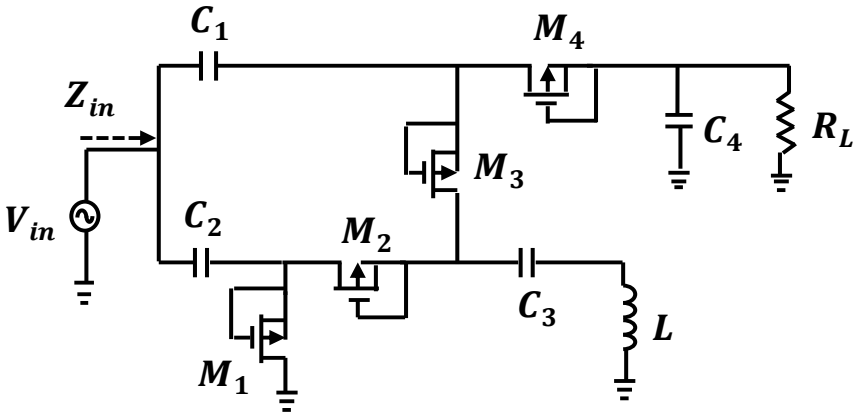
Chapter 4: Implementation of Self-Impedance Matching Rectifier in CMOS Technology

4.1 Introduction

For wireless power transfer in biomedical implants and some low power handheld gadgets like watches, IoTs devices, etc., compact size circuits are desired. The work presented in chapter 2 and chapter 3 which were designed in PCB technology are bulky comes int the cm^2 range and are lossy when the frequency comes to the GHz band. Complementary Metal-Oxide-Semiconductor (CMOS) circuits are more compact and present lower loss even at several GHz making them good for millimeter wave applications. The high-power CMOS rectifiers therefore are good candidates for the wireless power transfer system in biomedical and smaller gadgets applications. Especially, CMOS rectifier designed to cover a broadband with maximum efficiency, are applicable in harnessing energy from closer nano base stations that deliver high output power [74]. For such high-power rectifiers, achieving simultaneous high efficiency and circuit compactness in broadband range is challenging, primarily due to the requirements of input impedance matching network. Despite numerous reported ideas for high power CMOS rectifier, compromises often need to be made in terms of size, efficiency, or bandwidth. The CMOS rectifiers discussed in [75]-[78] present several rectification topologies suitable for higher frequencies; however, they are hindered by bulky circuits.

The rectifier presented in [79] offers circuit miniaturization but necessitates a compromise in efficiency. A rectifier with higher efficiency is reported in [80], [81], but they require off-chip external matching and cover a single frequency. Furthermore, the rectifier discussed in [40] employing the concept of a virtual dc source that demonstrates the ability to cover a broadband range with higher efficiency using discrete diodes. However, rectifier [40] was fabricated on Printed Circuit Board (PCB) technology, which makes the circuit bulky. To address this issue, same rectifier topology can be design in CMOS technology referred as Idea-I, depicted in Fig. 4.1(a), but this rectifier faces challenges such as i) no control over resonance due to the absence of passive matching element, ii) big inductor and iii) reduced efficiency. To achieve control over resonance, impedance matching network can be employed at input designed with C_M and L_M as Idea-II, depicted in Fig. 4.1(b); however, efficiency is still not improved a lot.

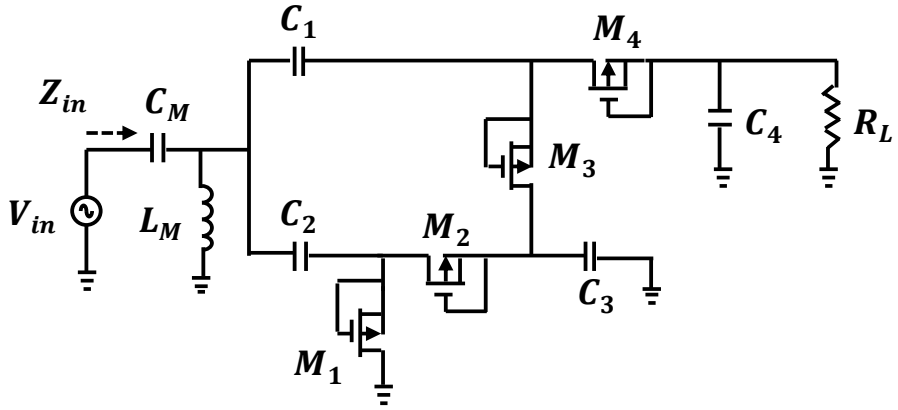
Idea-I



Disadvantages:
- Uncontrolled Resonance
- Big Inductor (L)
- Lower Efficiency

(a)

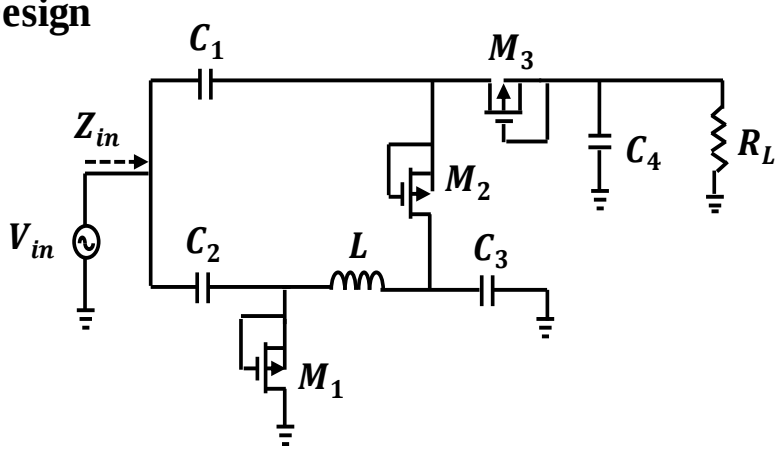
Idea-II



Disadvantages:
- Input Matching Required for Resonance Control
- Lower Efficiency

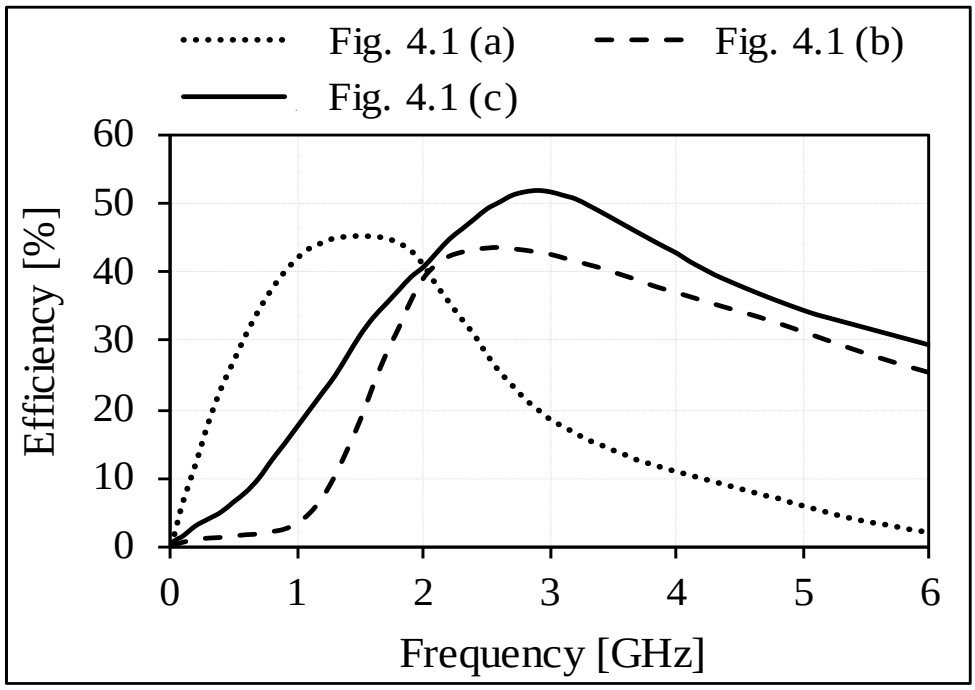
(b)

Proposed Design



Advantages:
- Resonance Controlled without Input Matching
- Improved Efficiency

(c)

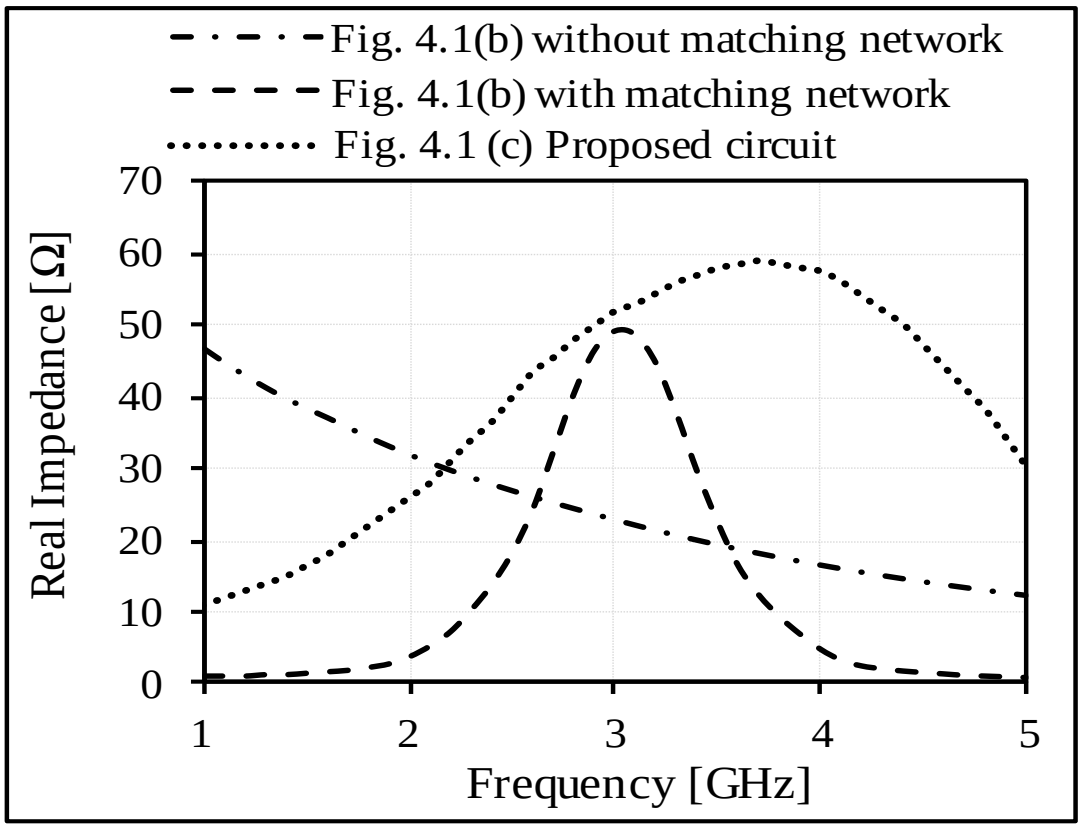


(d)

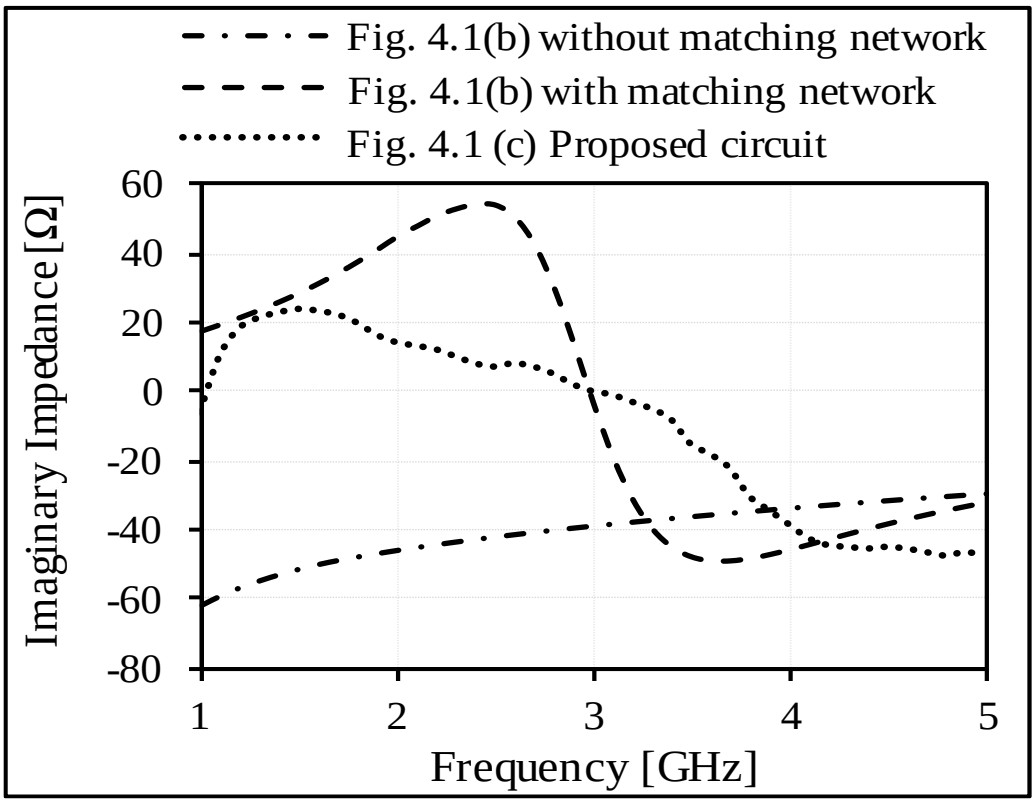
Fig. 4. 1: Performance comparison of different rectifier topology. (a) Rectifier circuit of Ref. [40] by replacing discrete diodes with CMOS transistors (b) Rectifier circuit of Fig. 4.1(a) substituting inductor (L) with input matching network (C_M and L_M) (c) Proposed CMOS rectifier (d) Comparison of simulated efficiency of Fig. 4.1(a), Fig. 4.1(b), and Fig. 4.1(c).

Till today, there are no reports of a CMOS rectifier capable of achieving broadband operation maintaining both maximum efficiency and compact circuit with control on resonance. Therefore, we proposed a novel rectifier design a solution to the problems arising from Idea-I and Idea II. In this work, a similar concept of a virtual dc source as in [40] is utilized, but with a major modification is to replace the series transistor of auxiliary rectifier with an inductor (*L*), as depicted in Fig. 4.1(c). In the proposed work, the key motivation of moving the inductor to the middle are:

i)**Resonance Control:** Using impedance matching network at input (Idea -II) i.e., Fig. 4.1(b), the control over resonance can be achieved, but such technique limits the operating bandwidth of the rectifier. But by moving the inductor to the middle, control over resonance is achieved maintaining the broadband operation, demonstrated through the impedance graph in Fig. 4.2.



(a)



(b)

Fig. 4. 2: Performance comparison of impedance of Idea-II (Fig. 4.1(b)) and proposed topology (Fig. 4.1(c)). (a) Real Impedance (b) Imaginary Impedance.

ii) Reduction in Losses due to Transistor: The rectifier circuits presented in Fig. 4.1(a) and Fig. 4.1(b) utilized four PMOS transistors (M_1, M_2, M_3, and M_4), but the proposed rectifier used only three PMOS transistors (M_1, M_2, and M_3), which means the voltage required to turn-on the transistors in proposed topology is less as compared to Idea-I and Idea-II, resulting more dc voltage generate at output, consequently improved the efficiency.

iii) Reduction in Losses due to Inductor: The design presented in Idea-II i.e., Fig. 4.1(b) used matching (C_M and L_M) at input, causing all the power is affected by inductor loss. However, in the proposed technique, half of the power goes to the main rectifier and suffers from transistor loss only, while the other half of the power goes to the auxiliary rectifier, which is affected by the inductor loss. This means that only half of the input power is affected by the inductor. Furthermore, the inductance required in the proposed rectifier is L = 4 nH, which is lower compared to the inductance required in the rectifier circuits topologies in Fig. 4.1(a) (L = 7 nH) and Fig. 4.1(b) (L_M= 5 nH), respectively. The reason for this is that the V_{DS} (drain-source

voltage) of output transistor in the proposed rectifier is higher compared to Fig. 4.1(a) and Fig. 4.1(b), resulting the proposed rectifier provides higher C_{gs} (gate-source capacitance) and C_{bs} (base-source capacitance) compared to topologies presented in Idea-I and Idea-II. In conclusion, the proposed design offers better efficiency for the same quality factor and smaller inductor size as compared to other design topologies as depicted in Fig. 4.3 and Table 4.1, respectively.

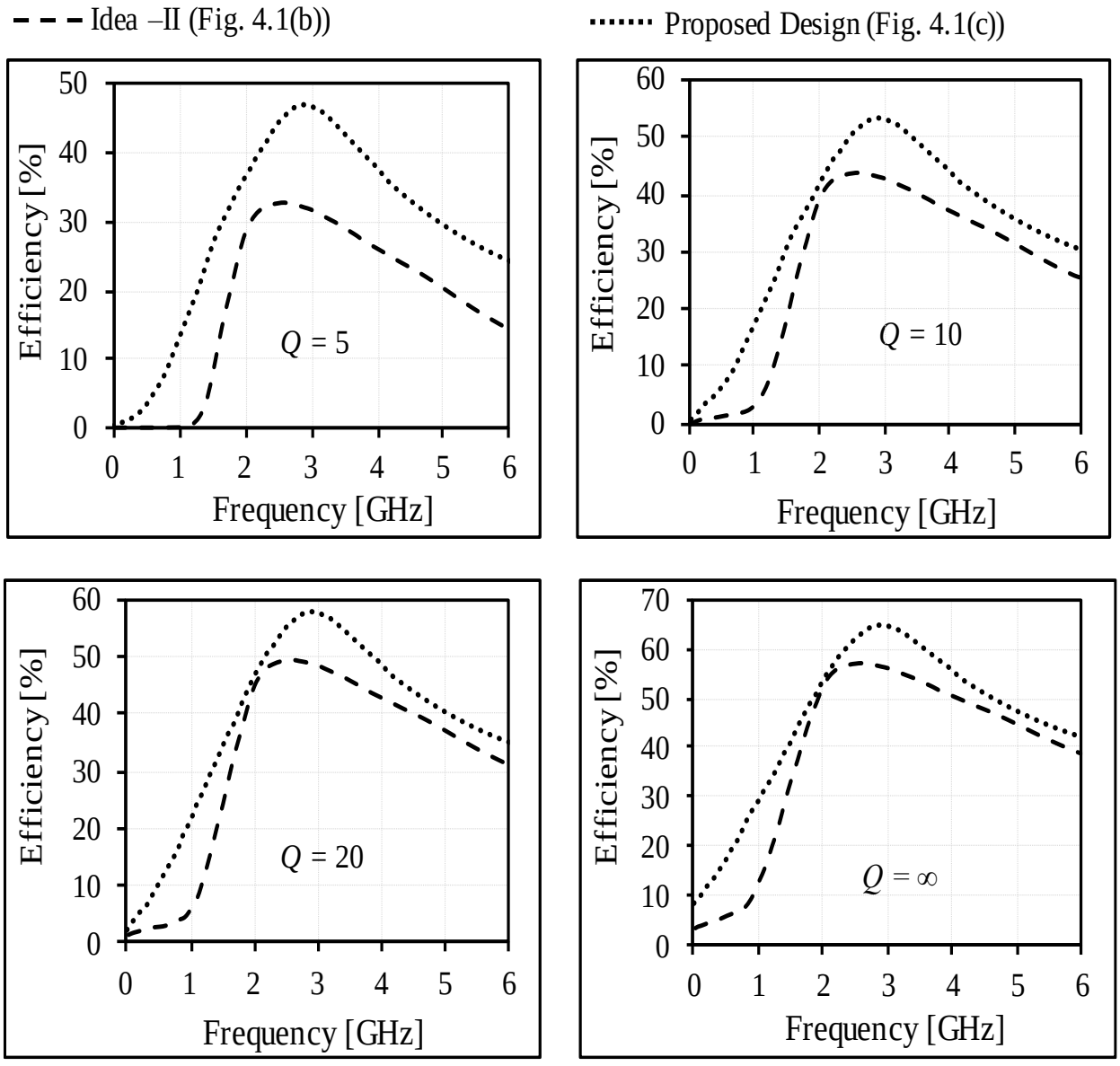


Fig. 4. 3: Efficiency comparison of proposed technique with convention design i.e., Idea-II at different values of quality factor.

Table 4. 1: Comparison between PCB and CMOS designs

Rectifier Topologies	**Inductance**	**Inductor Size**
Fig. 4.1(a)	L = 7 nH	0.168 mm^2 (1.8 times bigger than proposed)
Fig. 4.1(b)	L_M = 5 nH	0.120 mm^2 (1.3 times bigger than proposed)
Fig. 4.1(c)	L = 4 nH	0.093 mm^2 (Proposed)

4.2 Design of Compact and Efficient CMOS Rectifier

4.2.1 Design and Analysis of Proposed CMOS Rectifier Circuit

The proposed CMOS rectifier introduces the concept of a parallel rectifier by integrating the main rectifier (Rectifier-I) and auxiliary rectifier (Rectifier-II), as shown in Fig. 4.4. Rectifier-I is a conventional voltage doubler circuit solely dedicated to rectification designed with a dc block capacitor (C_1), two PMOS transistors (M_2 and M_3), and an ac ground capacitor (C_4).

Similarly, Rectifier-II is targeted for impedance matching purpose designed with half-wave rectifier composed of a dc-blocking capacitor (C_2), and a PMOS transistor (M_1), along with the integration of a single inductor (L) and an ac grounding capacitor (C_3). In CMOS circuit, the loss due from the chip inductor is highly dominant and covers the significant chip area when designing full circuit. For the rectifier design, inductors are inherent for the matching purposes. In this work, circuit size and efficiency is a highly dominant on to the on-chip inductor, so transistor is selected to optimize the layout size and performance while using the available foundry inductor.

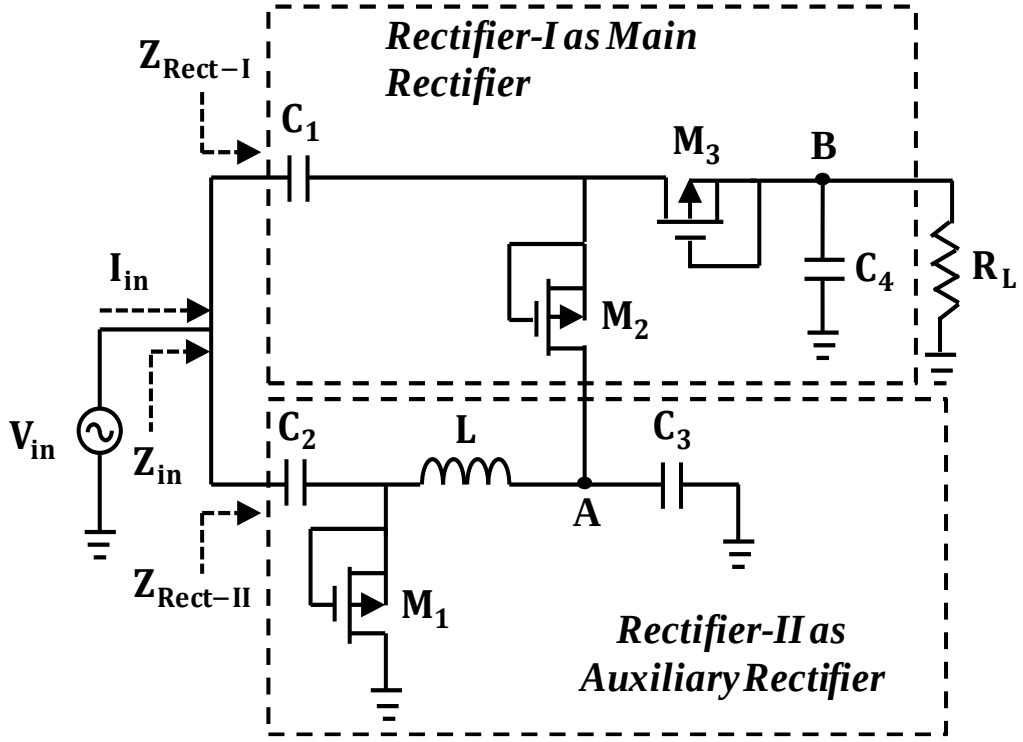
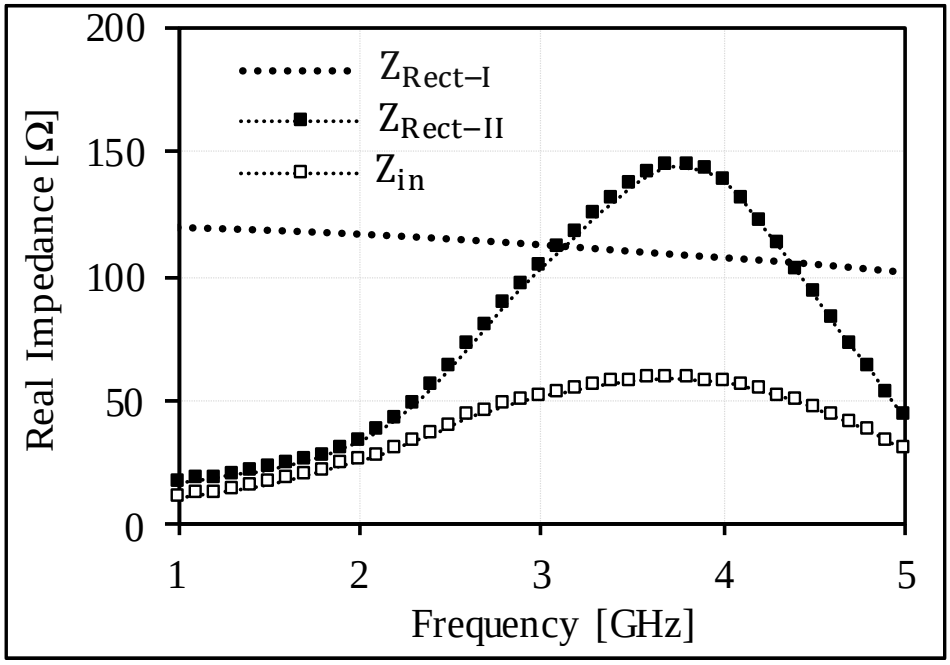
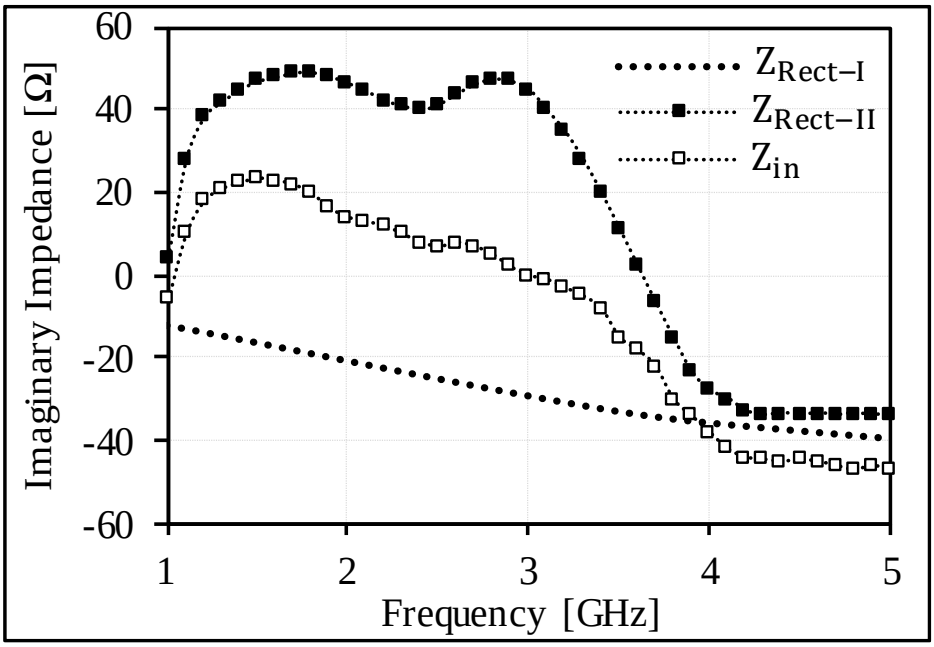


Fig. 4. 4: Schematic diagram of the proposed CMOS rectifier designed with C_1= C_2= C_4= 5pF, C_3= 2pF, and L = 4nH, where C_1 and C_2 are dc block capacitor, and C_3 and C_4 are low pass capacitor. Transistors M_1, M_2, and M_3 have same width of 330 µm whereas the length of each transistor is 0.18 µm.



(a)



(b)

Fig. 4. 5: Simulated impedance graphs of Fig. 4.2 at P_{in}= 20 dBm and R_L= 0.8 KΩ. (a) Real (b) Imaginary.

The impedances of Rectifier-I and Rectifier-II denoted as, Z_{Rect-I} and $Z_{Rect-II}$, respectively deviate from the ideal 50 Ω impedance. However, by connecting them in parallel sharing the same RF source, the equivalent impedance of the proposed rectifier comes closer to 50 Ω. The simulated input impedance graphs presented in Fig. 4.5, demonstrate that the impedance contributed from parallel connection of Rectifier-II effectively match both real and imaginary impedance of the proposed rectifier over a frequency range of 2.4 GHz to 3.5 GHz.

4.2.2 Inductor for Resonance and Bandwidth Control in the Proposed Rectifier

In CMOS technology, the transistor can be realized as a diode. The ac equivalent capacitance of the proposed rectifier as shown in Fig. 4.6 is expressed as $C_{eq} = (C_{M1} + C_{M2} + C_{M3})$ where C_{M1}, C_{M2}, and C_{M3} are parasitic capacitance of the transistors M_1, M_2, and M_3, respectively expressed as, $C_{M1} = C_{M2} = C_{M3} = (C_{db} + C_{gs})$. These parasitic capacitance values of the transistor remain constant, resulting C_{eq} of the proposed rectifier becomes fixed. Consequently, the sole parameter governing resonance of proposed rectifier is L, clear from input admittance (Y_{in}) analysis of the proposed rectifier in (20).

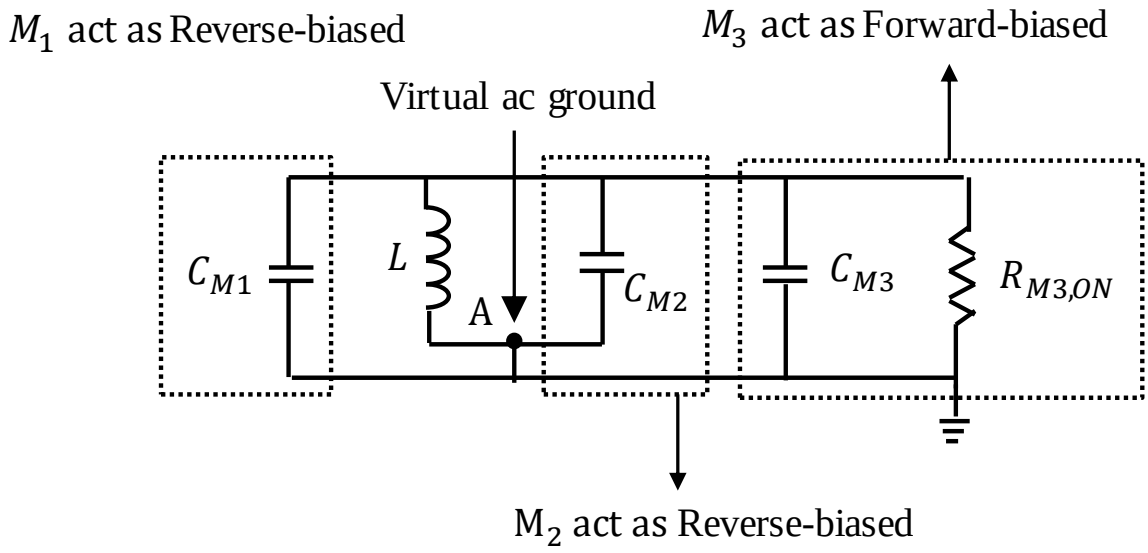


Fig. 4. 6: Ac equivalent circuit of the proposed CMOS rectifier (Fig. 4.2) where M_1 and M_2 are in reverse-biased and M_3 is in forward-biased. The parasitic capacitance of the transistors is, $C_{M1} = C_{M2} = C_{M3} = (C_{db} + C_{gs})$ where $R_{M3,ON}$ is the ON state resistance of the transistor M_3.

$$Y_{in} = \frac{1}{R_{M3,ON}} + \frac{1-\omega^2 LC_{eq}}{j\omega L} \tag{4.1}$$

where, ω is the angular frequency. To eliminate imaginary part in (4.1), following conditions should be satisfied,

$$1 - \omega^2 LC_{eq} = 0 \tag{4.2a}$$

$$L = \frac{1}{\omega^2 C_{eq}} \tag{4.2b}$$

As evidenced by (4.2), the only parameter responsible for resonance control of the proposed rectifier is *L*. Furthermore, corresponding fractional bandwidth (FBW) is determined by the *L*, since this rectifier can be considered as a first-order bandpass filter (tank circuit) as shown in Fig. 4.7, the FBW is proportional to the ratio $\sqrt{L/C}$ [82] as describe below:

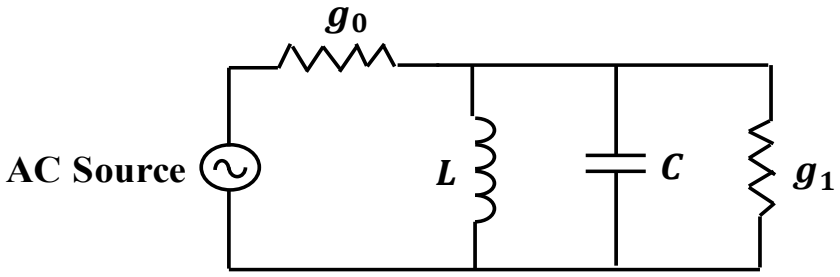


Fig. 4. 7: Equivalent circuit of the proposed CMSO rectifier.

Fractional Bandwidth (FBW) can be defined as,

$$FBW = \frac{g_0 g_1}{Q_{ex}} = \frac{2}{Q_{ex}} \tag{4.3}$$

where, g_0 = 1 and g_1 = 2 (Low-pass Filter Butterworth Coefficients)

Also, Q_{ex} is an external quality factor defined as,

$$Q_{ex} = \frac{b}{Y_0} \tag{4.4}$$

According to [82], the susceptance slope parameter to define the bandwidth in parallel resonant circuit is,

$$b = \frac{1}{\omega_0 L} \tag{4.5}$$

Substituting the value of b on (4.4),

$$Q_{ex} = \frac{1}{\omega_0 L Y_0} = \frac{Z_0}{\omega_0 L} \tag{4.6}$$

Now, substituting the value of Q_{ex} on (4.3), the FBW becomes,

$$FBW = \frac{2}{Q_{ex}} = \frac{2\omega_0 L}{Z_0} = \frac{2}{Z_0}\sqrt{\frac{L}{C}} \tag{4.7}$$

where L is the matching inductance, and C is the effective capacitance of the transistors.

From the above calculation, (4.7) shows the maximizing L will lead to maximaiztaion of the bandwidth. Also, in the proposed design we have not used any external capacitors to achieve the impedance matching. Therefore, FBW is maximized as anticipated from (4.7) based on the available parasitic capacitance from the transistors.

Furthermore, simulated $|S_{11}|$ of the proposed rectifier, as shown in Fig. 4.8 demonstrates that the inductance with all parasitic capacitances together act as a bandpass response and its resonance changes when value of L changes.

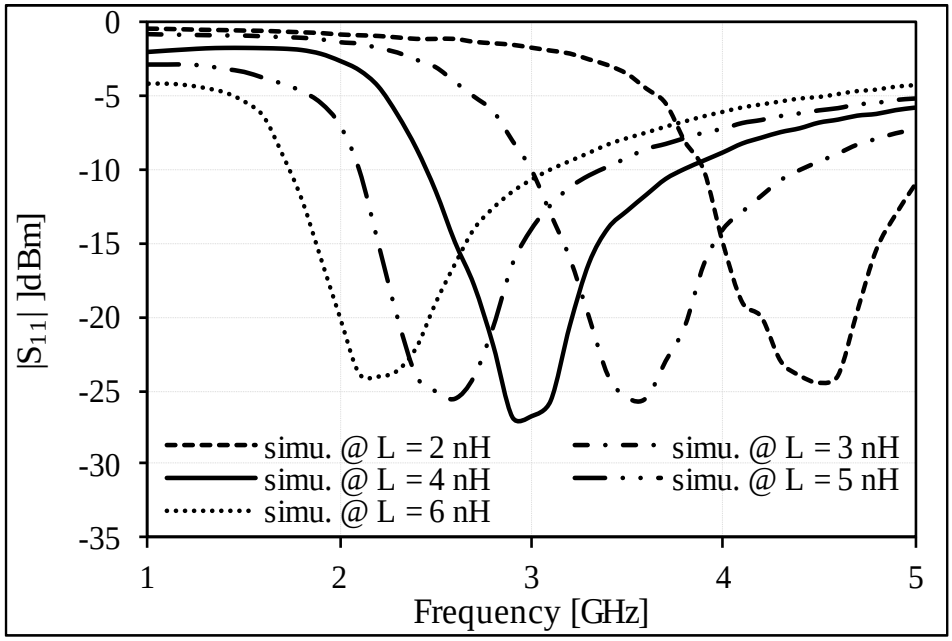


Fig. 4. 8: Simulated reflection coefficient $|S_{11}|$ of the proposed rectifier for different L at P_{in}= 20 dBm and R_L= 0.8 KΩ.

4.2.3 Selection of Transistor Size

A smaller transistor width can minimize the circuit size, but it increases the inductance value and results in a poor-quality factor, resulting in lower power conversion efficiency. Conversely, a larger transistor width reduces the inductance and maintains the quality factor; however, due to the increased transistor leakage, efficiency does not improve significantly, and the circuit size increases, as depicted in Table 4.2.

Table 4. 2: Comparison of inductance, quality factor and area for different width of transistors

Transistor Width (W)	Inductance (L)	Quality Factor (Q)	Circuit Area (A)
100 μm	7 nH	7	0.4146 mm^2
200 μm	5.8 nH	7.8	0.4182 mm^2
300 μm	4.2 nH	9	0.4215 mm^2
400 μm	3.4 nH	8.8	0.4220 mm^2
500 μm	2.8 nH	8.5	0.4224 mm^2

In this work, the selected width for each transistor 330 μm considering both size and efficiency of the proposed rectifier

4.3 Fabrication and Measurement of Compact and Efficient CMOS Rectifier

4.3.1 Layout Preparation and Prototype Fabrication

The layout mask for the proposed CMOS rectifier is designed using the Cadence Virtuoso IC6 Software, employing 0.18 µm CMOS technology. To validate its performance, the rectifier is fabricated and measured. The measurement setup for the proposed rectifier is shown in Fig. 4.9, which includes a probe station with one GSG infinity probe and one LGLLGL eye-pass DC probe, both from Formfactor. Digital multimeter, coaxial cable and the lumped component resistors are used for whole circuit build up. The measurement of reflection coefficient is performed using a Keysight PNA series vector network analyzer (Part #N5222A). The fabricated chip of the proposed rectifier, depicted in Fig. 4.10, exhibits an overall circuit area of 740 µm × 570 µm, with an active circuit area measuring 540 µm × 390 µm.

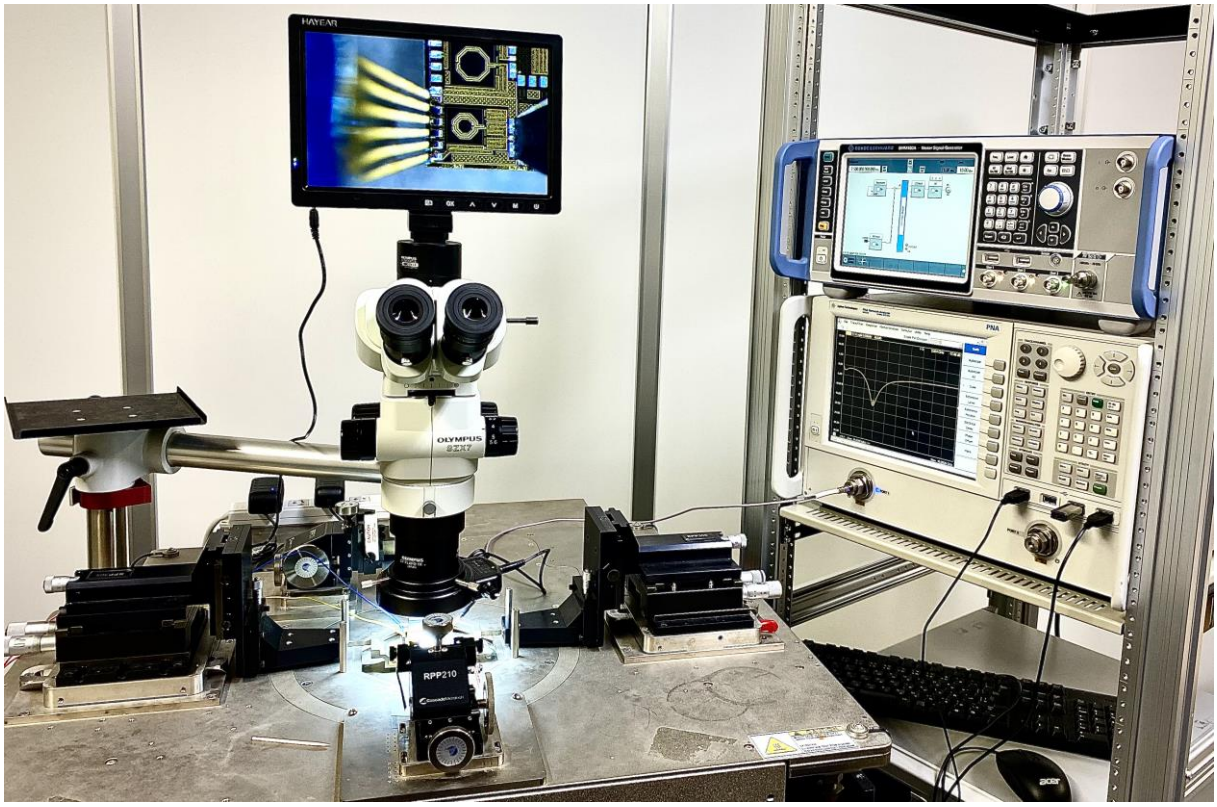


Fig. 4. 9: Fabricated proposed rectifier chip measurement setup.

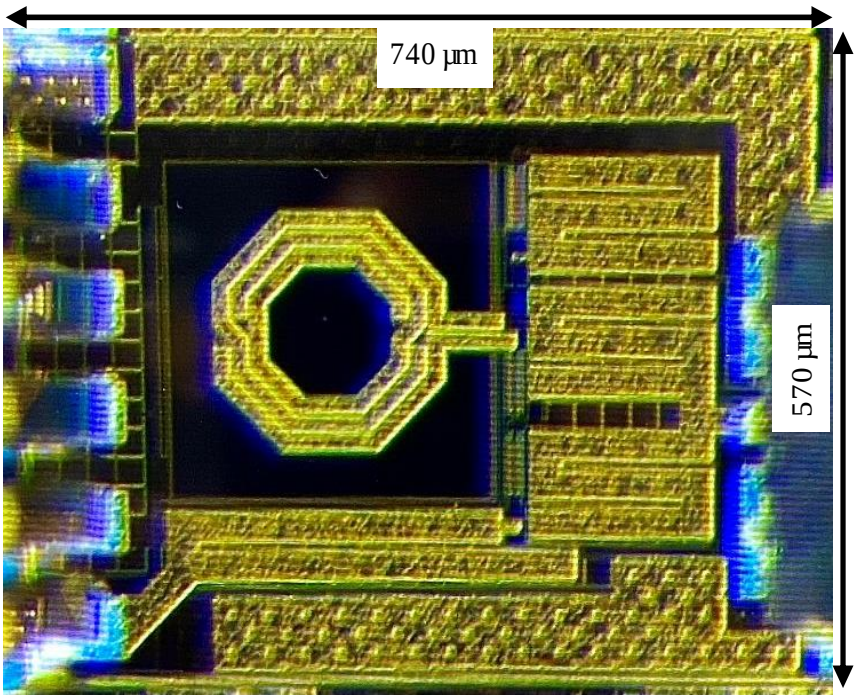


Fig. 4. 10: Fabricated chip of the proposed CMOS rectifier

4.3.2 . Simulation and Measurement Results

Fig. 4.11 shows the simulated and measured reflection coefficient $|S_{11}|$ for different input powers at their optimal efficiency load conditions. This graph shows that there is a good agreement simulation and the measurement results. Moreover, reflection coefficient stays well below than -10 dB throughout the measured bandwidth of 2.5 GHz to 3.5 GHz at 22 dBm input power.

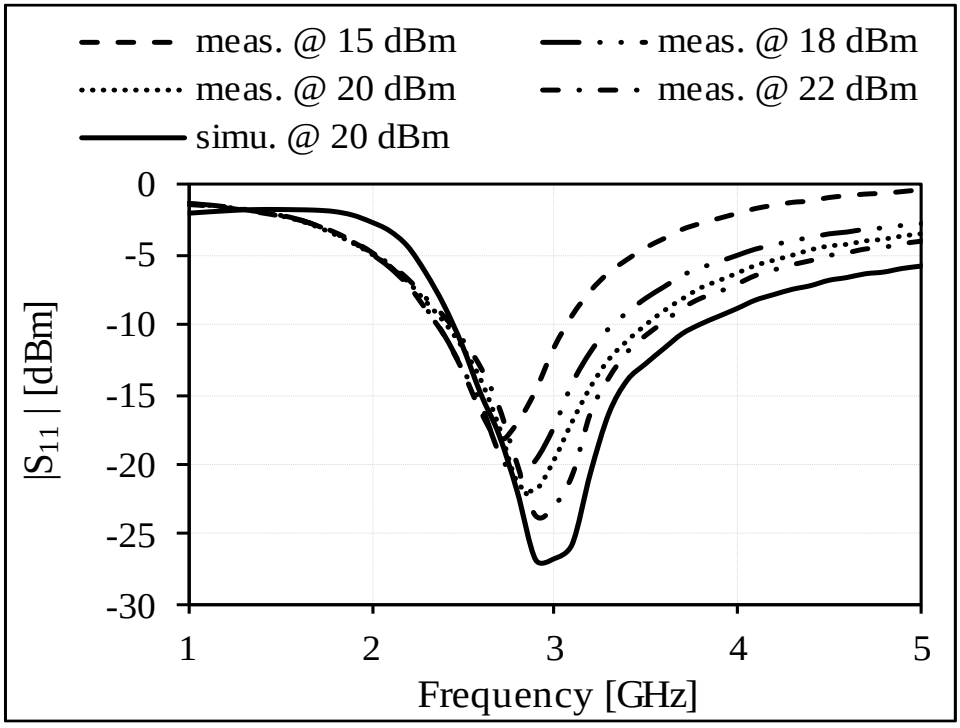


Fig. 4. 11: Simulated and measured $|S_{11}|$ for different input power at optimal efficiency load of 0.8 KΩ and 1 KΩ, respectively.

The RF-to-dc power conversion efficiency (PCE) of the proposed rectifier is measured using ROHDE & SCHWARZ SMM100A Vector Signal Generator and a digital multimeter. The RF-to-dc PCE (η) is calculated using (4.8),

$$\eta = \frac{P_{out}}{P_{in}} \times 100\ \% = \frac{{V_{out}}^2}{P_{in} \times R_L} \times 100\ \% \qquad (4.8)$$

where, P_{in} is input power, P_{out} is out power, V_{out} is output dc voltage and R_L is load. The PCE obtained from circuit simulation, post layout and measurement of the proposed rectifier for different input powers is illustrated in Fig. 4.12, demonstrate the maximum PCE achieved from the simulation is 51.5% at optimal efficiency load of 0.8 KΩ, and optimal efficiency input

power of 20 dBm whereas maximum PCE achieved from the measurement is 46.80% at optimal efficiency load of 1 KΩ, and optimal efficiency input power of 22 dBm, respectively. The slight discrepancy between the measurement and simulation is due to the various parasitic appearing from chip itself as there are fabrication tolerances that were not fully included in simulations. Also, some losses may be contributed from the measurement setup cable connections.

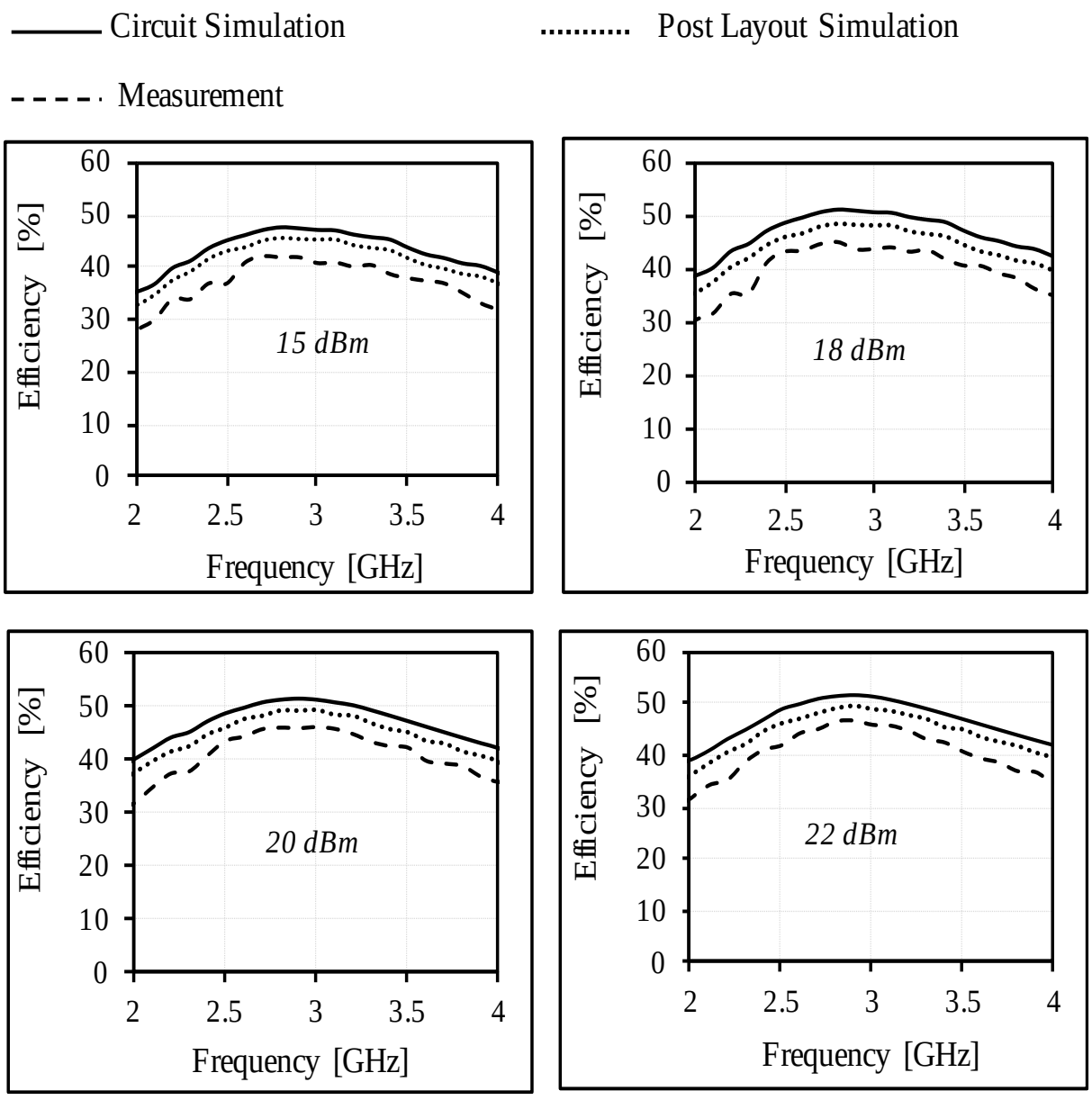


Fig. 4. 12: Simulated and measured PCE for different input power at optimal efficiency load of 0.8 KΩ and 1 KΩ, respectively.

However, more than 40% PCE is achieved from the measurement of proposed rectifier throughout the frequency bandwidth of 2.5 GHz to 3.5 GHz. There is various effect from the various corners and temperatures in the transistor circuits. So. to show process variation effect performance of proposed rectifier, simulated efficiency against various corners and temperature is shown in Fig. 4.13 for different input powers.

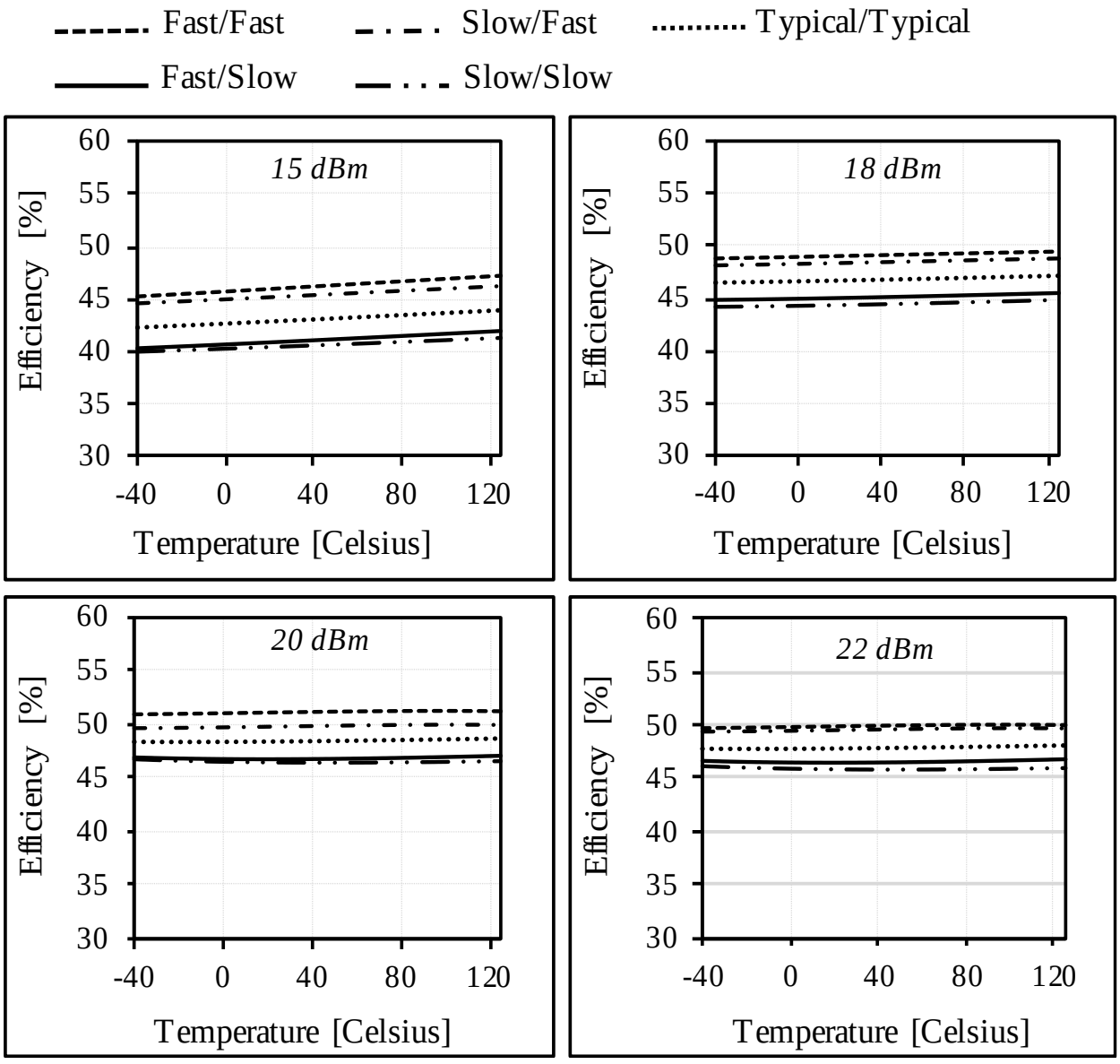


Fig. 4. 13: Simulated efficiency of the proposed rectifier for various corners and temperatures at different input powers.

Similarly, the measured PCE for varying resistive loads at different input powers is shown in Fig. 4.14, presents more than 40% PCE is achieved throughout load range from 0.6 KΩ to 1.2 KΩ at 22 dBm input power.

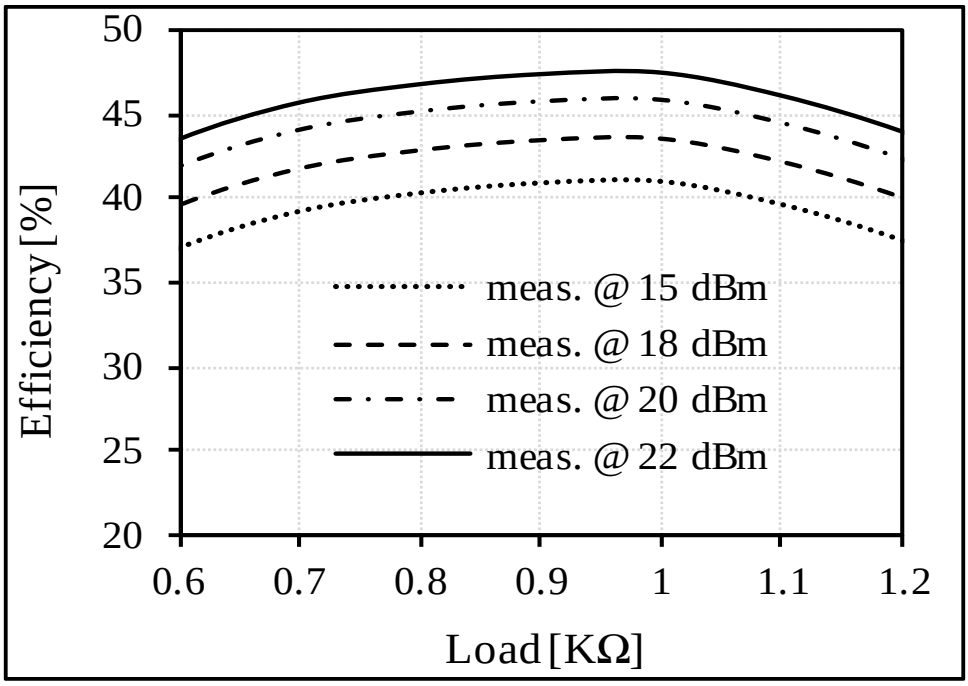


Fig. 4. 14: Measured PCE for varying loads at different powers.

Furthermore, Fig. 4.15 depicts measured PCE and output dc voltage for input power from -10 dBm to 24 dBm at optimal load of 1 KΩ. The results demonstrate that 30% and 40% PCEs are obtained for power range 8 dBm to 24 dBm and 14 dBm to 24 dBm, respectively.

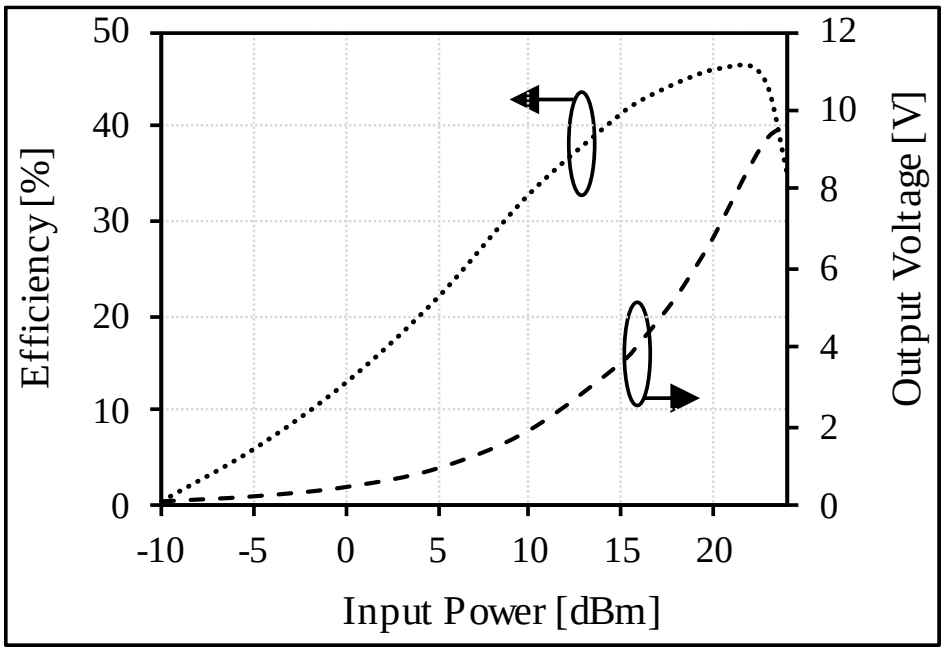


Fig. 4. 15: PCE and output voltage for varying powers at R_L of 1 KΩ.

Compared to the similar circuit topology in PCB technology [40], the proposed circuit has relatively higher efficiency and the major reasons for this are:

i) In reference [40], the rectifier was fabricated in PCB technology where Schottky diodes were used. But the proposed design is implemented in CMOS technology where we used PMOS transistor as a rectifying unit. It is known that the PMOS transistor has higher threshold voltage (V_{th}) when compared to the Schottky diode, that's why the efficiency getting from CMOS design is lower as compared to the PCBs.

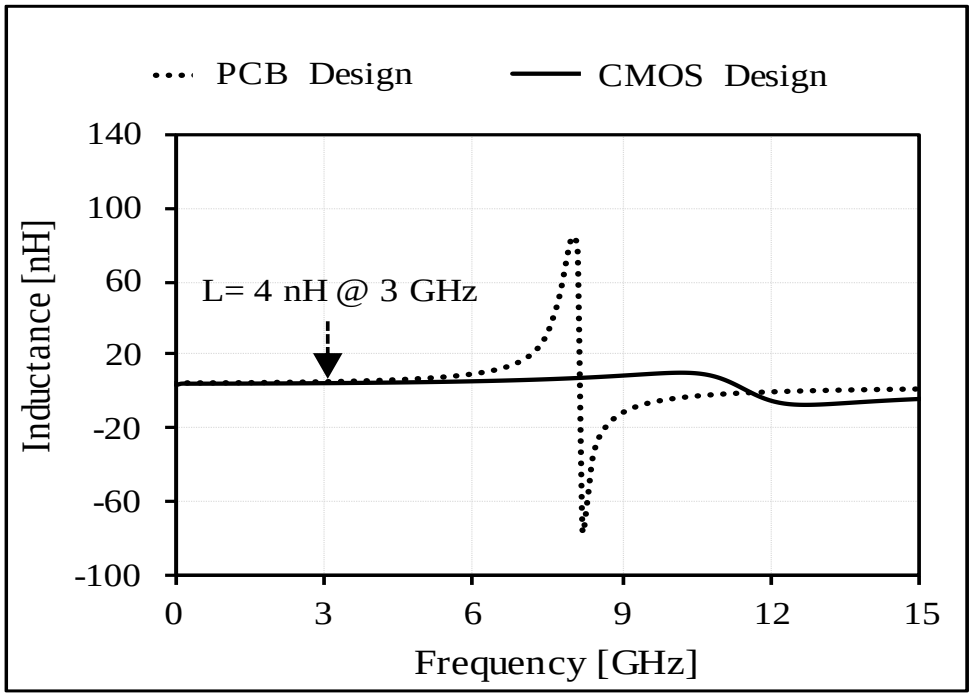
ii) Another reason is, the metal used in CMOS technology has lower conductivity (i.e., σ = 2.4 *10^7 S/m) with smaller thickness (i.e., t = 2.34 µm) but the metal used in PCB technology is pure copper with the conductivity of 5.8*10^7 S/m (which is more than twice as compared to CMOS technology) and the thickness of 16 µm (which is more than six times as compared to CMOS technology). So, the metal traces as well as the inductors in CMOS have higher conductive loss than the PCB one.

iii) Furthermore, the CMOS substrate has low resistivity. So, inductors tend to generate eddy current, which results in lower quality factor (Q)

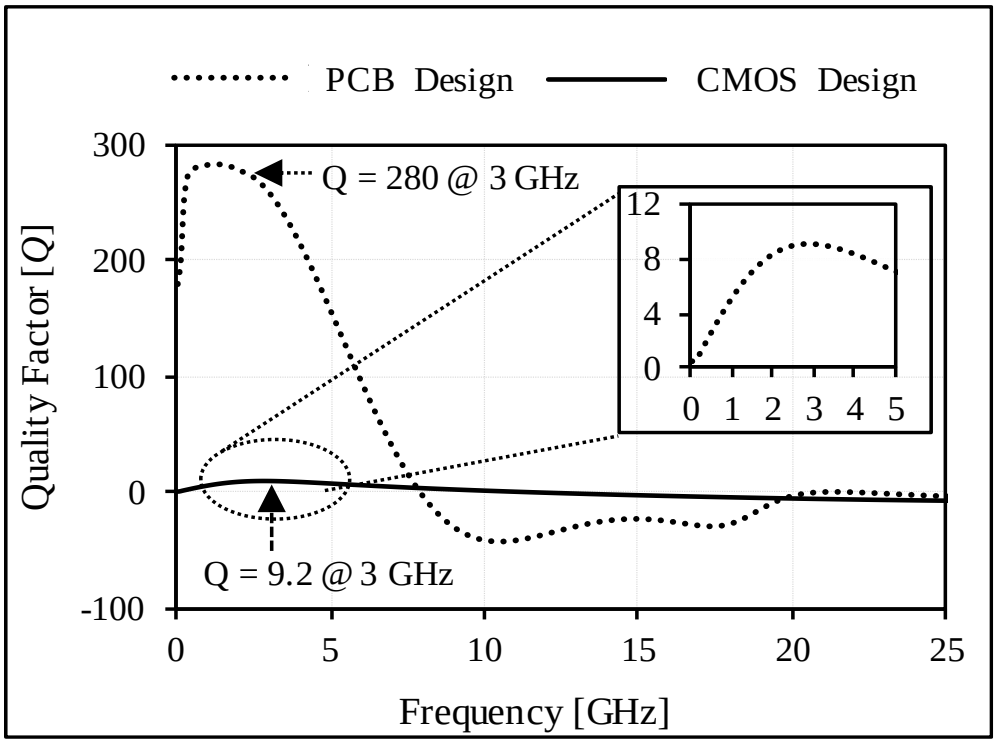
While designing an inductor, three important factors should be considered: a) quality factor, b) self-resonance and c) size. In this work, we design an inductor with maximum possible quality factor while considering its compactness. The comparison between the CMOS inductor and PCB inductor for their inductance values and quality factors over the frequency is shown here in Fig. 4.16 (a) and Fig. 4.16 (b), respectively. It is clearly visible that PCB inductors outperform CMOS ones. Still, as shown in Table 4.3, the CMOS inductor is 322 times smaller.

Table 4. 3: Comparison between PCB and CMOS designs

Technology	Inductance (L)	Self-resonance (f_{SR})	Quality Factor (Q) at 3 GHz	Size (mm^2)
PCB	4 nH	8 GHz	280	30
CMOS	4 nH	11.5 GHz	9.2	0.093



(a)



(b)

Fig. 4. 16: Comparison between PCB and CMOS technology (a) Inductance comparison (b) Quality factor comparison.

Now to confirm the performance of the proposed topology, breakdown of the transistor. is checked which is defined the drain-source voltage (V_{DS}) As shown in Fig. 17, 1.8 V transistor is used and to avoid breakdown, maximum V_{DS} should not exceed 3.3 V, that means breakdown occurs if V_{DS} > 3.3 V. In the proposed topology shown in Fig. 4.16, the V_{DS} value of each transistor; $V_{DS}\ (M_1) = V_{A'}$ = 3.23 V, $V_{DS}\ (M_2) = V_{B'} - V_A$= 3.10 V, and $V_{DS}\ (M_3) = V_B - V_{B'}$ = 2.56 V does not exceed 3.3 V. In short, at output voltage $V_{out} = V_{DS}\ (M_1) + V_{DS}\ (M_2) + V_{DS}\ (M_3) \approx 10$ V, none of the transistors entered breakdown. But, beyond this, transistors start to breakdown from M_1 and leakage may occur, resulting in efficiency degradation.

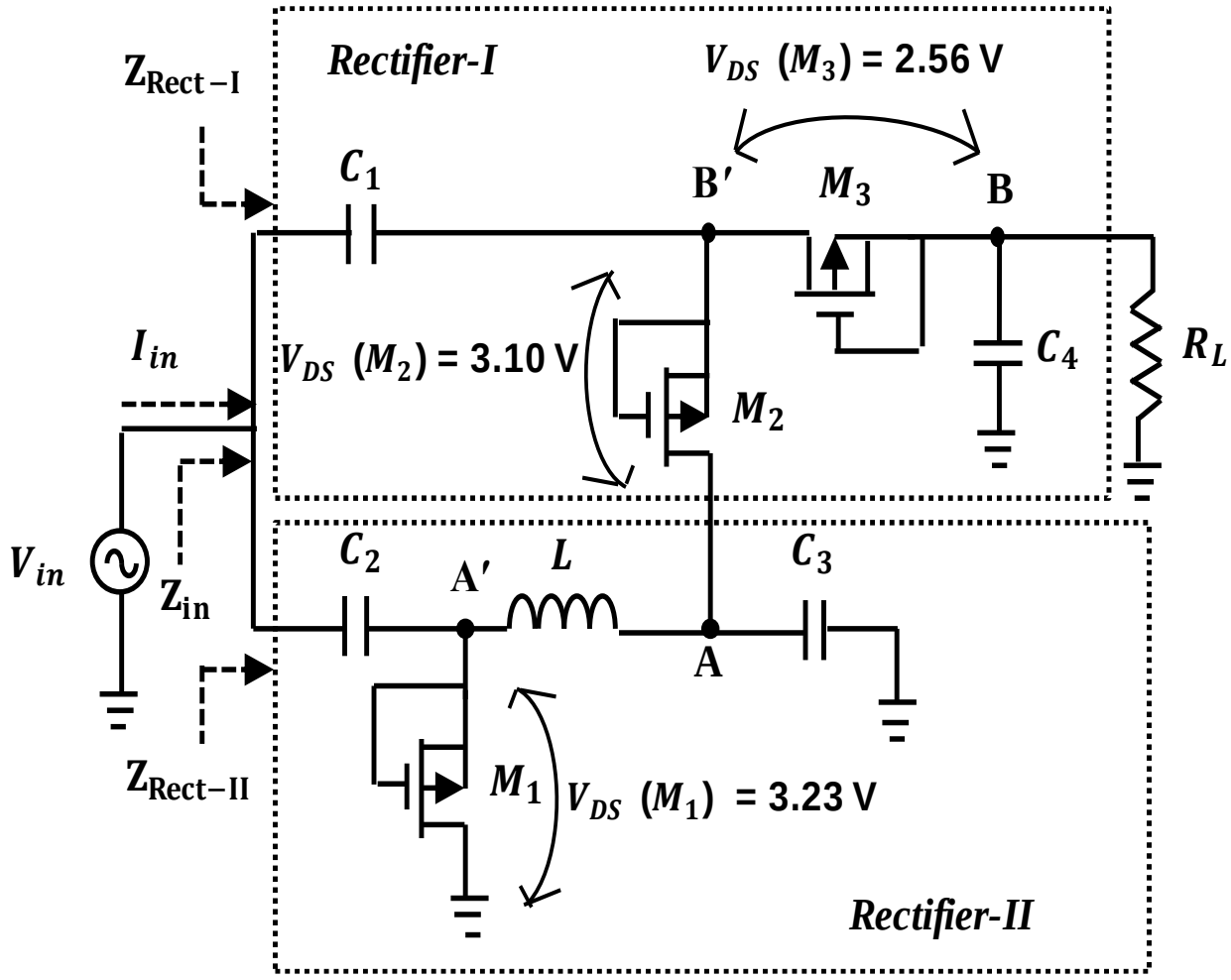


Fig. 4. 17: Schematic diagram of the proposed CMOS rectifier with V_{DS} value of each transistor.

4.3.3 . Performance Comparison

The performance comparison of the proposed rectifier is shown in Table 4.4, which demonstrates the proposed CMOS rectifier achieved more than 40% PCE throughout the

broadband frequency range from 2.4 GHz to 3.5 GHz with a peak efficiency of 46.8% maintaining a compact circuit size compared to other state-of-the-art designs.

The Figure of Merit (FoM) is calculated using the following formula:

$$\text{FoM} = \frac{\eta_{max} \times FBW}{Area(cm^2)} \times f_o \tag{4.9}$$

where, center frequency (f_o) = $\frac{f_H + f_L}{2}$, fractional bandwidth (FBW) = $\frac{f_H - f_L}{f_o}$, f_H , f_L are high, low frequencies.

Table 4. 4: Performance comparison of proposed rectifier with other related state-of-arts

Ref.	Frequency (GHz)	Conversion Efficiency (%)	Input Power (dBm)	Output Load Resistance	Technology	Area {active area} (mm^2)	Figure of Merit (FoM)
[30]	2.0-3.05	70	10	400 Ω	PCB	1260	0.063
[36]	1.75-3.55	70	10	N/A	PCB	875	0.154
[73]	2.1-3.3	70	14	500 Ω****	PCB	558	0.164
[75]	2.4	15.9	0	10 MΩ	CMOS 0.13 μm	2.08*	-
[76]	5.8	14	0	1 MΩ	CMOS 0.13 μm	1.036**	-
[77]	2.4	30	10	250 Ω	CMOS 0.13 μm	0.7395	-
[79]	2.4	10.2	6	N/A	CMOS 0.13 μm	0.216	-
[80]	2.4	46	25.5	24 Ω	CMOS 28 nm	0.705***	-
[81]	2.4	47	8.9	2 KΩ	CMOS 0.18 μm	0.057***	-
This work	**2.4 - 3.5**	**> 40**	**22**	**1 KΩ**	**CMOS 0.18 μm**	**0.4218 {0.2106}**	**122.04**
	2.9	**46.8 (peak)**					

*Includes transceiver, **includes T/R switch, ***required off chip matching, ****estimated from graph, N/A is not available.

4.4 Summary

In this chapter, a compact CMOS rectifier is proposed and designed. The proposed circuit employs the concept of parallel rectifier by integrating two rectifiers i.e., main rectifier and auxiliary rectifier named as Rectifier-I and Rectifier-II, respectively. In this work, the main rectifier was specially targeted for rectification whereas the auxiliary rectifier was designated for impedance matching, resulting in no need of any matching circuits at input. Additionally, the auxiliary rectifier is responsible for controlling the resonance of the proposed rectifier. The measurement results demonstrate more than 40% PCE throughout the frequency bandwidth of 2.4 GHz to 3.5 GHz, with a peak efficiency of 46.8%. The proposed circuit maintains compactness with an active area size of $0.21 mm^2$. This highly efficient compact on-chip rectifiers are advantageous for the beamforming-based WPT systems that are applicable to power the smaller gadgets circuits which has constraints for high performance in the lower aspect ratio in terms of the circuit size.

Chapter 5: Wideband CMOS Rectifier with Higher Efficiency and Compact Size using Parasitic Cancellation Technique

5.1 Introduction

The rectifier proposed in chapter 4 has bandwidth 1.1 GHz. This is the maximum ultrawideband that is possible to achieve from the on-chip rectifier till date above 1 GHz. Now, to achieve ultrawideband operation above 2 GHz bandwidth, a conventional π-matching technique can be used at input as shown in Fig. 5.1(a) is checked. Using π-matching at input, wideband operation can be achieved but maintaining maximum efficiency throughout the bandwidth is difficult as shown in Fig. 5.1(c). So, there is always a compromise either on bandwidth or efficiency when designing the ultrawideband rectifier circuit.

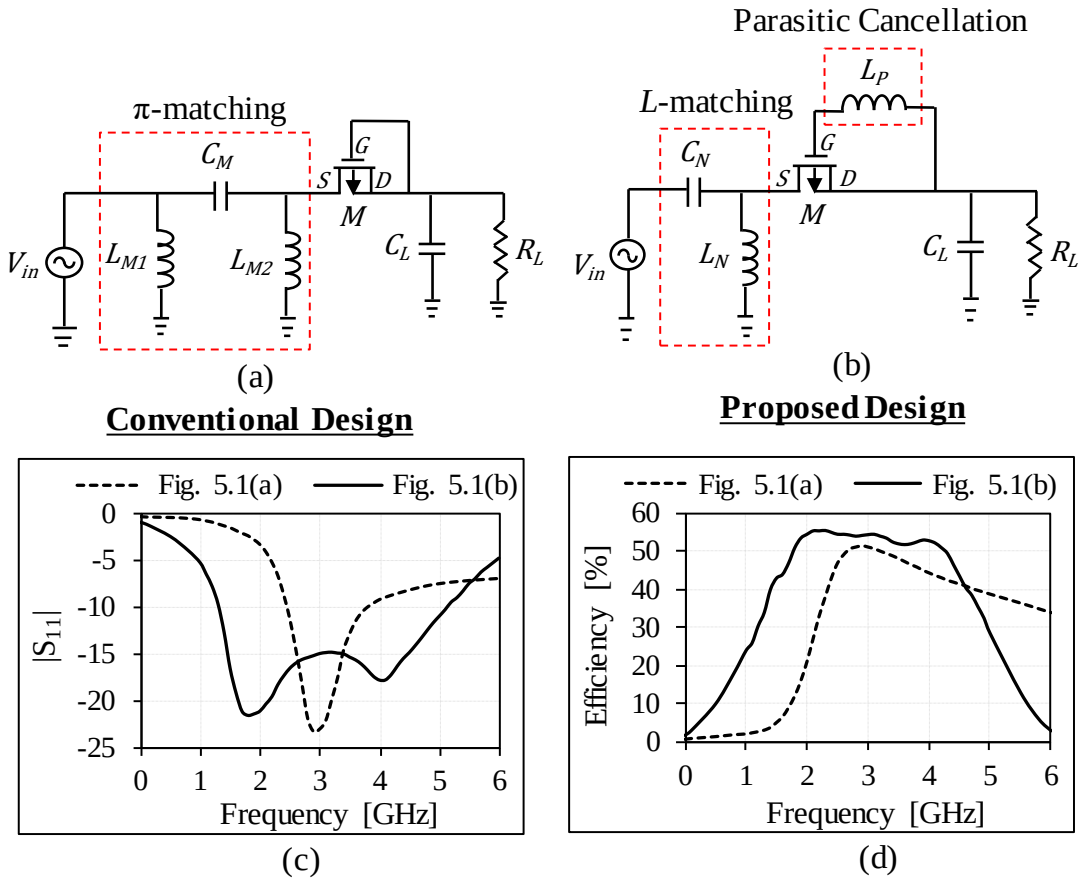


Fig. 5. 1: Wideband rectifier design with different matching topologies and their performance comparison (a) Rectifier with π-matching at input (b) Rectifier with combined *L*-matching at input and parasitic cancellation technique (c) Reflection coefficient comparison and (d) Conversion efficiency comparison of Fig. 5. 1(a) and 1(b).

To the best of author's knowledge, there are no reports of a CMOS rectifier capable of achieving wideband operation targeting higher frequency maintaining both maximum efficiency and compact circuit. Therefore, in this work, a novel parasitic cancellation technique is proposed employing a single inductor (L_p) at gate-side of the transistor (M) along with the L-matching at input as shown in Fig. 5.1(b), resulting ultra-wideband operation is achieved with maximum flat efficiency throughout the bandwidth as shown in Fig. 5.1(c).

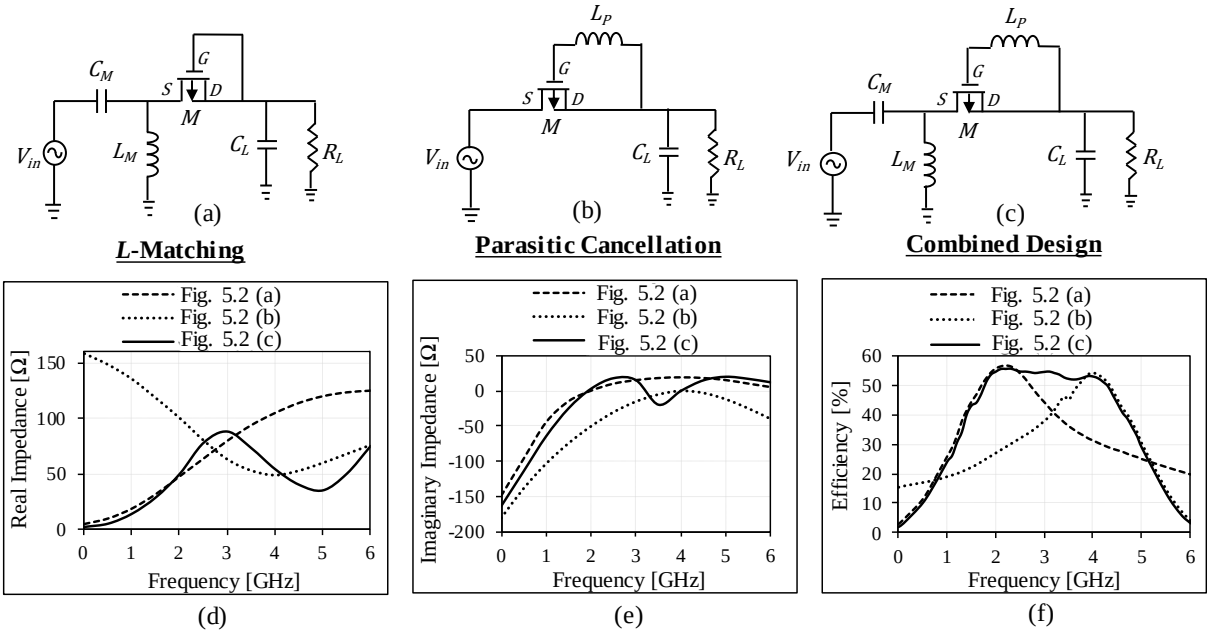


Fig. 5. 2: Rectifier design with different impedance matching topologies. (a) with L- matching (b) with gate-biasing (parasitic cancellation technique) (c) with combination of L- matching and parasitic cancellation real impedance comparison (e) imaginary impedance comparison (f) efficiency bandwidth comparison.

5.2 Design of Proposed Wideband CMOS Rectifier

5.2.1 Design Analysis of Wideband CMOS Rectifier Circuit

To achieve ultra-wideband operation maintaining maximum flat efficiency, the proposed CMOS rectifier is designed using a single transistor (M) with two impedance matching circuits, i) L-matching at input and ii) Gate-biasing of the transistor (parasitic cancellation). To analyze the ultra-wideband performance of the rectifier due to the combination of L- matching and gate-biasing of transistor, the individual rectifiers i) with L- matching at input (designed with C_M and L_M) and ii) gate-biasing of the transistor (M) (designed with L_P at the gate of M) are investigated as shown in Fig. 5.2(a) and 5.2(b), respectively. The real impedance as shown in Fig. 5.2(d) and imaginary impedance as shown in Fig. 5.2(e) illustrated that the L-matching at

input is responsible for the resonance at f_1 = 2 GHz, whereas the parasitic cancellation technique is responsible for the resonance at f_2 = 4 GHz, respectively. When both matching techniques (Fig. 5.2(a) and 5.2(b)) are combined together as shown in Fig. 5.2(c), the impedance graph depicted that both frequencies, f_1 and f_2 can be covered maintaining near 50 Ω impedance throughout the bandwidth of 2 GHz to 4 GHz. The efficiency bandwidths obtained from *L*-matching, parasitic cancellation technique, and combined deign are shown in Fig. 5.2 (f), illustrate that combined design (proposed technique) significantly improves the efficiency in between the resonances f_1 and f_2 and achieved maximum flat efficiency throughout the operational bandwidth. The voltage waveforms obtained from *L*-matching, parasitic cancellation technique, and combined deign at 3.2 GHz (frequency in between f_1 and f_2) for C_L = 0.6 pF and C_L = 100 pF are shown in Fig. 5.3, depicts that output voltage obtained from the proposed design is significantly higher as compared to the *L*-matching and parasitic cancellation technique only.

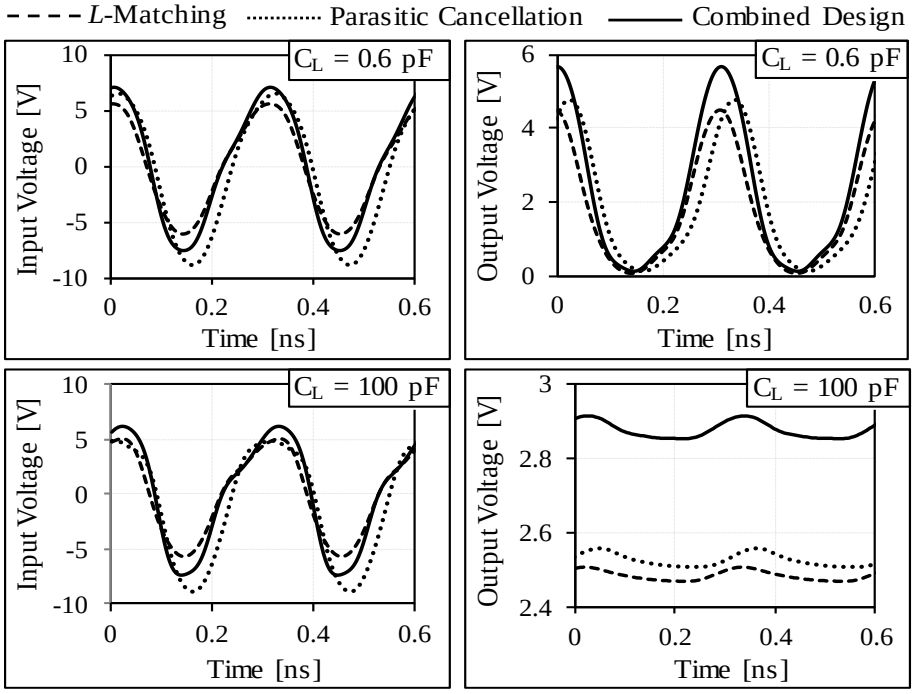


Fig. 5.3. Voltage waveforms obtained from Fig. 5.2(c) at 3.2 GHz for C_L = 0.6 pF and 100 pF.

5.2.2 Rectifier Circuit Analysis with and with Gate-biasing

The rectifiers with and without parasitic cancellation technique with their ac equivalent circuits are as shown in Fig. 5.4(a) and 5.4(b) respectively.

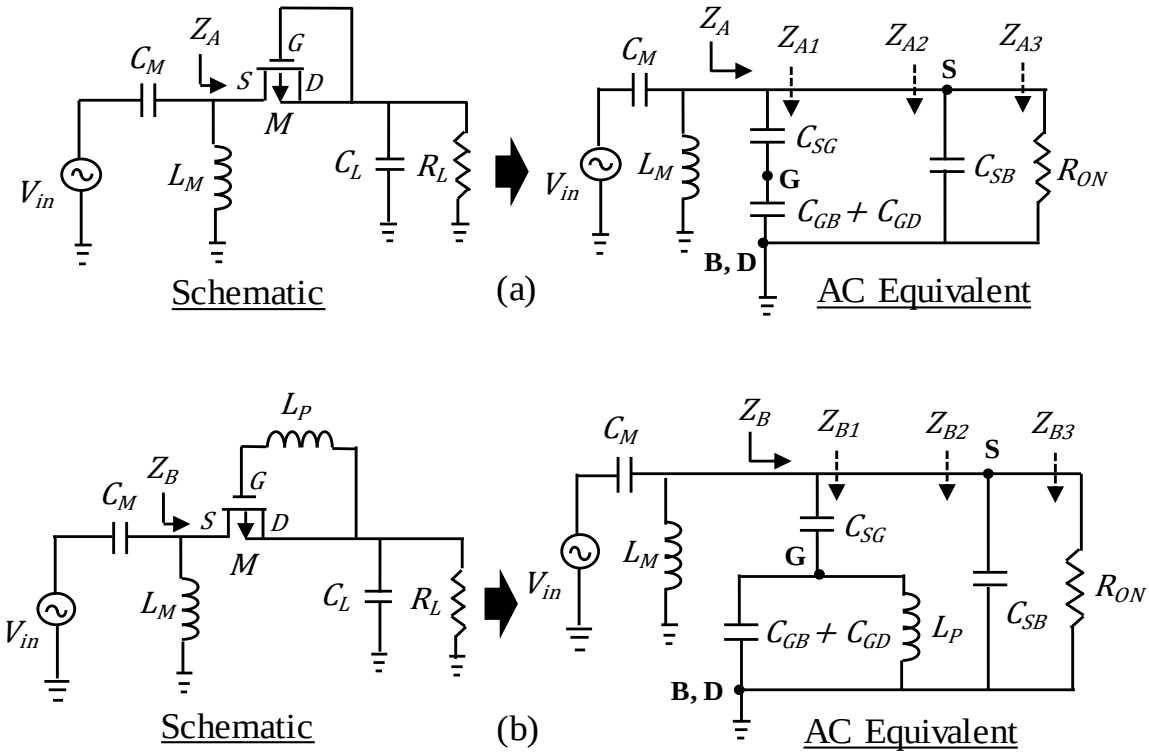


Fig. 5. 4: Rectifiers with their ac equivalent circuits (a) without parasitic cancellation technique (b) with parasitic cancellation technique.

From Fig. 5.4(a),

$$Z_A = Z_{A1}//Z_{A2}//Z_{A3}$$

$$Z_A = R_{ON}// \frac{1}{j\omega C_{eq}} \tag{5.1}$$

where,

$$C_{eq} = C_{SG} + C_{GB} + C_{GD} + C_{SB}$$

$$Z_A = \frac{(1-j\omega R_{ON} C_{eq})R_{ON}}{1+ \omega^2 {R_{ON}}^2 {C_{eq}}^2} \tag{5.2}$$

From Fig. 5.4(b),

$$Z_B = Z_{B1}//Z_{B2}//Z_{B3} \tag{5.3}$$

$$Z_{B1} = \frac{1}{j\omega C_{SG}} + \frac{j\omega L_P}{1-\omega^2 L_P(C_{GB}+C_{GD})} \tag{5.4a}$$

$$Z_{B2} = \frac{1}{j\omega C_{SB}} \tag{5.4b}$$

$$Z_{B3} = R_{ON} \tag{5.4c}$$

From (5.3),

$$Z_B = \frac{(P-\omega^2 L_P C_{SG})R_{ON}}{-\omega^2 C_{SG}\, C_{SB}\, R_{ON}\, P + j\omega\,(PC_{SG}+PC_{SB}-\omega^2 L_P C_{SG} C_{SB})} \tag{5.5}$$

where,

$$P = 1 - \omega^2 L_P (C_{GB} + C_{GD}) \tag{5.6}$$

Solving (5.5),

$$Z_B = \frac{(\omega^2 L_P C_{SG}-P)(Q+j\omega R)R_{ON}}{Q^2+\omega^2 R^2} \tag{5.7}$$

where,

$$Q = -\omega^2 C_{SG} C_{SB} P R_{ON} \tag{5.8}$$

$$R = PC_{SG} + PC_{SB} - \omega^2 L_P C_{SG} C_{SB} \tag{5.9}$$

From (5.7), it can be understood that the cancellation circuit determined the input impedance of the proposed rectifier. Now to achieve ultra-wideband operation, previously *L*-matching can be designed at a lower frequency (f_1) and then parasitic cancellation technique can be employed at a higher frequency (f_2) as shown in Fig. 5.4 (b). In the optimized design, the inductance values L_M and L_P are 7 nH and 4 nH, respectively.

5.3 Fabrication and Measurement

5.3.1 Implementation and Prototype Fabrication

The proposed broadband CMOS rectifier layout mask in this work is prepared using Cadence Virtuoso IC6 Software in a 6-metal/1-poly (6M1P) CMOS process where the metal-1 to metal-6 are referred to as M1 to M6. The inductors and the capacitors used are standard foundry inductors and capacitors that are selected from the optimization. The prototype of the proposed rectifier is fabricated for checking its validation. The prototype chip photo is shown in Fig. 5.5. Inside the chip, some excess metal was added to satisfy the design rules of the foundry. The chip size is 1050 µm × 760 µm, with an active circuit area measuring 850 µm × 610 µm without ground-signal-ground (GSG) measurement pads.

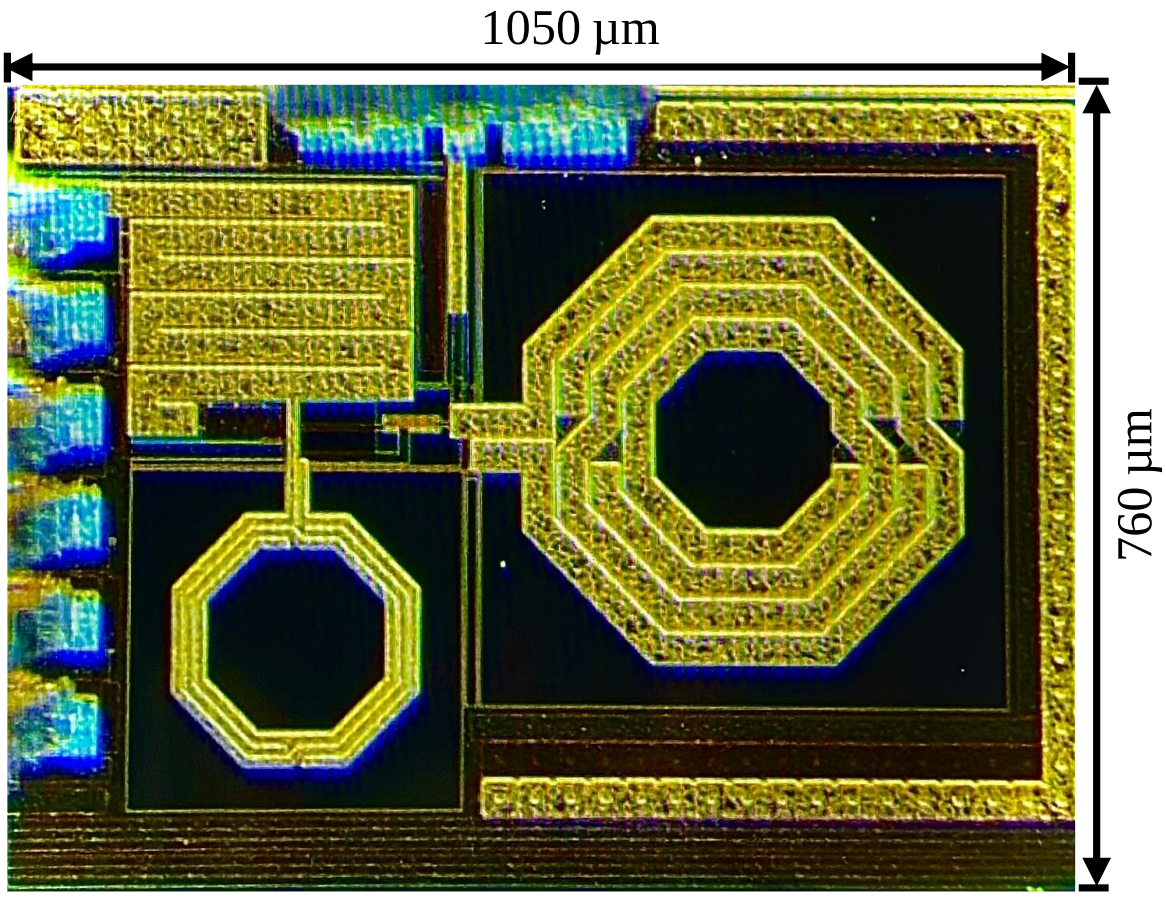


Fig. 5. 5: Fabricated chip of the proposed CMOS rectifier.

5.3.2 Measurement of Return Loss $|S_{11}|$ and RF-to-dc Conversion Efficiency (η)

The measurement setup consisted of CASCADE Microtech Summit 11000 M probe station equipped with one on-wafer infinity RF probe to input RF signal and one LGLLGL eye-pass DC probe for DC output measurement, and both are from Formfactor. The RF input signal is generated using ROHDE & SCHWARZ SMM100A Vector Signal Generator, the return loss is measured using Agilent Technologies N5222A PNA Network Analyzer. For the output voltage measurement, a digital multimeter is used.

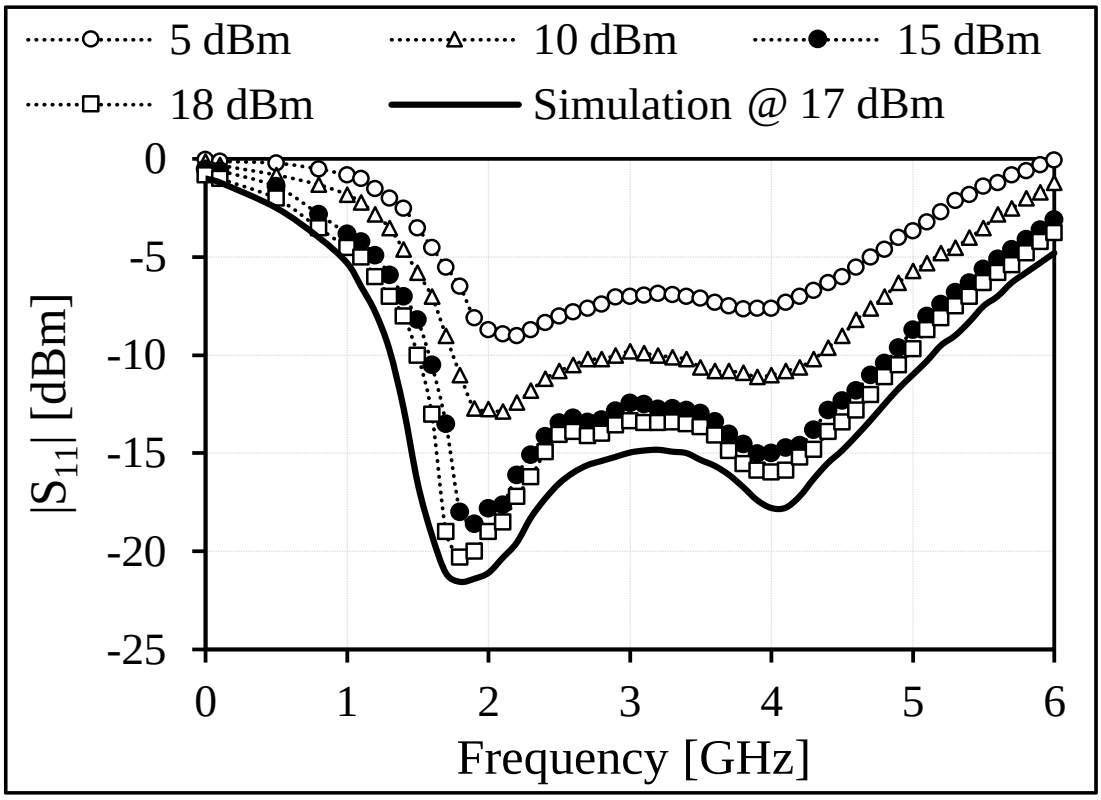


Fig. 5. 6: Simulated and measured $|S_{11}|$ for different input powers at optimal R_L of 300 Ω and 500 Ω, respectively.

The simulated and measured S-parameters of the proposed CMOS rectifier, shown in Fig. 5.6, demonstrate good agreement between simulation and measurement. The measured return loss $|S_{11}|$ stays well below -10 dB throughout the bandwidth of 1.5 GHz to 5 GHz at an input power of 18 dBm. The measured return loss shows about a 2 dB difference from the simulated results. This discrepancy may be due to the tolerance of the metal conductance in the used technology and other parasitic that were not included during the simulations.

The RF-to-dc Power Conversion Efficiency (PCE) of the proposed CMOS rectifier is calculated using the following formula,

$$\eta = \frac{P_{out}}{P_{in}} \times 100\ \% = \frac{{V_{out}}^2}{P_{in} \times R_L} \times 100\ \% \tag{5.10}$$

where, P_{in} is input power, P_{out} is out power, V_{out} is output dc voltage and R_L is load. The PCE obtained from the simulation and measurement of the proposed rectifier for different input power levels at their optimal efficiency load conditions is shown in Fig. 5.7. From simulation, more than 50% PCE is obtained for the operating bandwidth of 1.8 GHz to 4.2 GHz at optimal efficiency load of 300 Ω and optimal efficiency input power of 17 dBm, respectively with 55.5% of peak efficiency. Similarly, from measurement, more than 48% PCE is obtained for the operating bandwidth of 1.9 GHz to 4.1 GHz to 4.1 GHz at optimal efficiency load of 500 Ω and optimal efficiency input power of 18 dBm, respectively with 52.80% of peak efficiency. Similarly, the simulated and measured PCE and output voltage with respect to input power level are shown in Fig. 5.8(a) and Fig. 5.8(b), respectively. Furthermore, Fig. 5.9, shows the simulated and measured PCE with respect to output load for different input power levels.

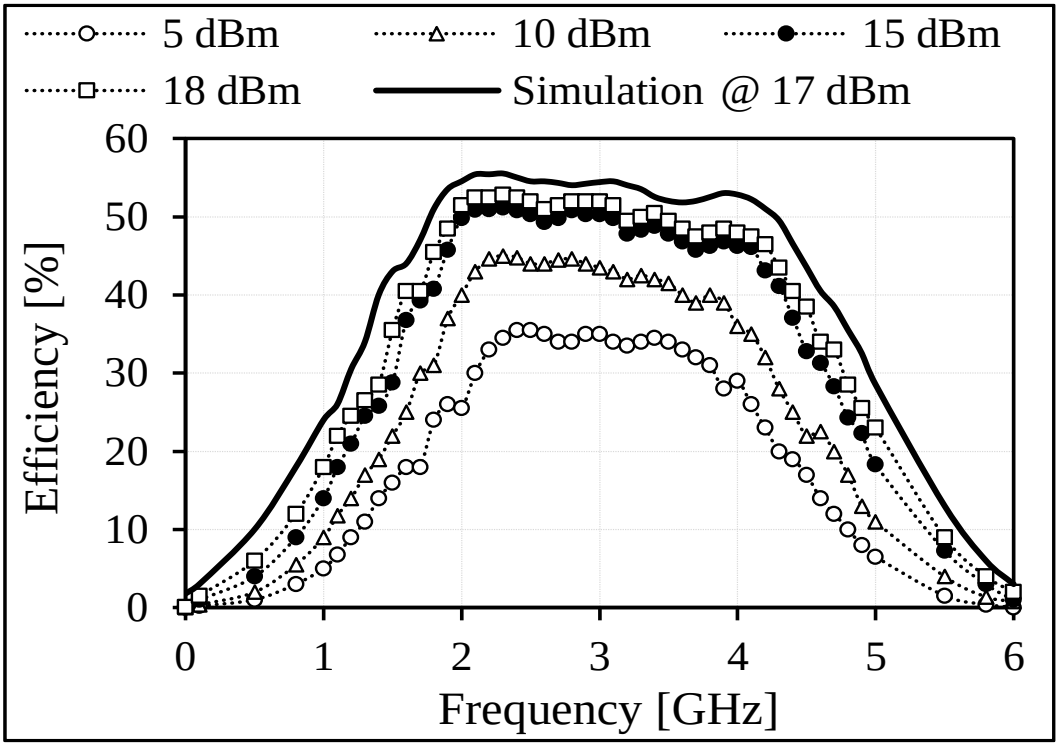
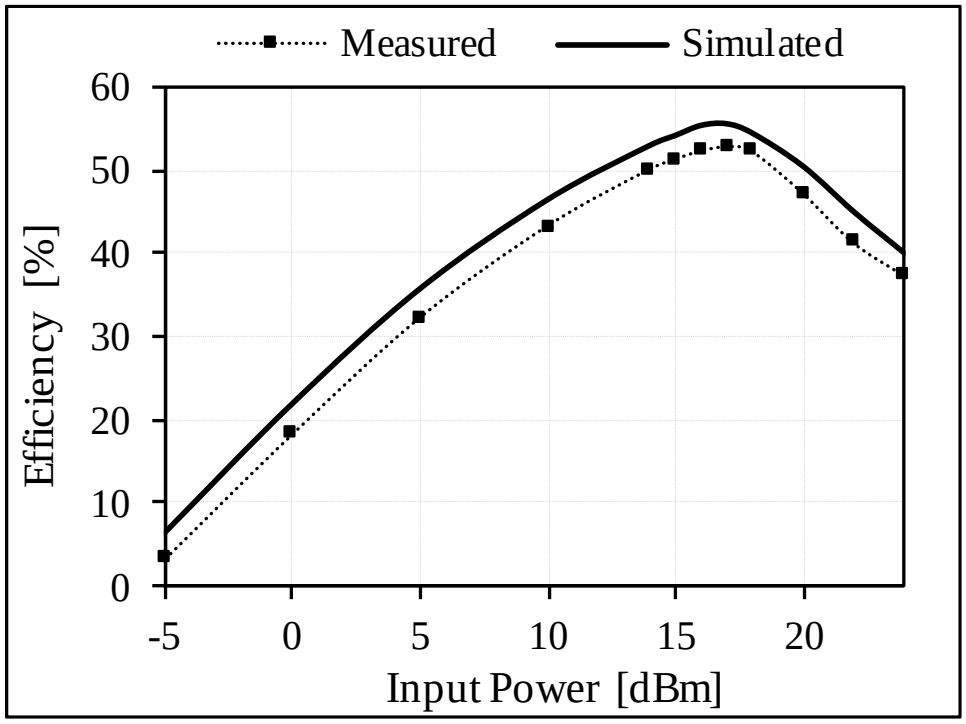
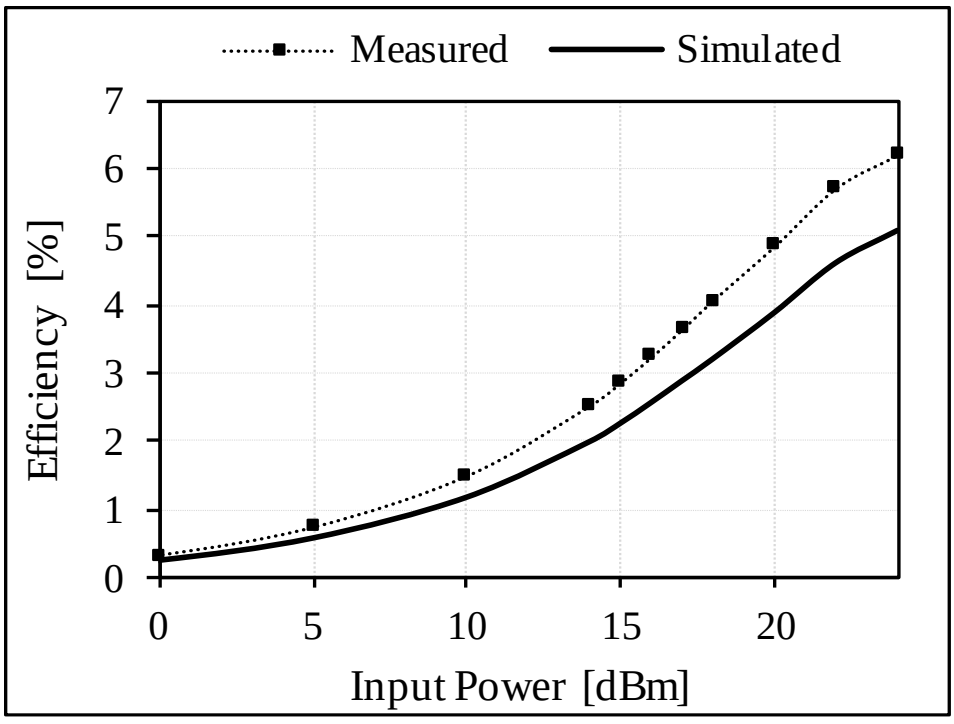


Fig. 5. 7: Simulated and measured PCE with respect to frequency for different input powers at optimal R_L of 300 Ω and 500 Ω, respectively.



(a)



(b)

Fig. 5. 8: Simulated and measured results at R_L of 300 Ω and 500 Ω, respectively (a) PCE (b) output voltage, with respect to input power.

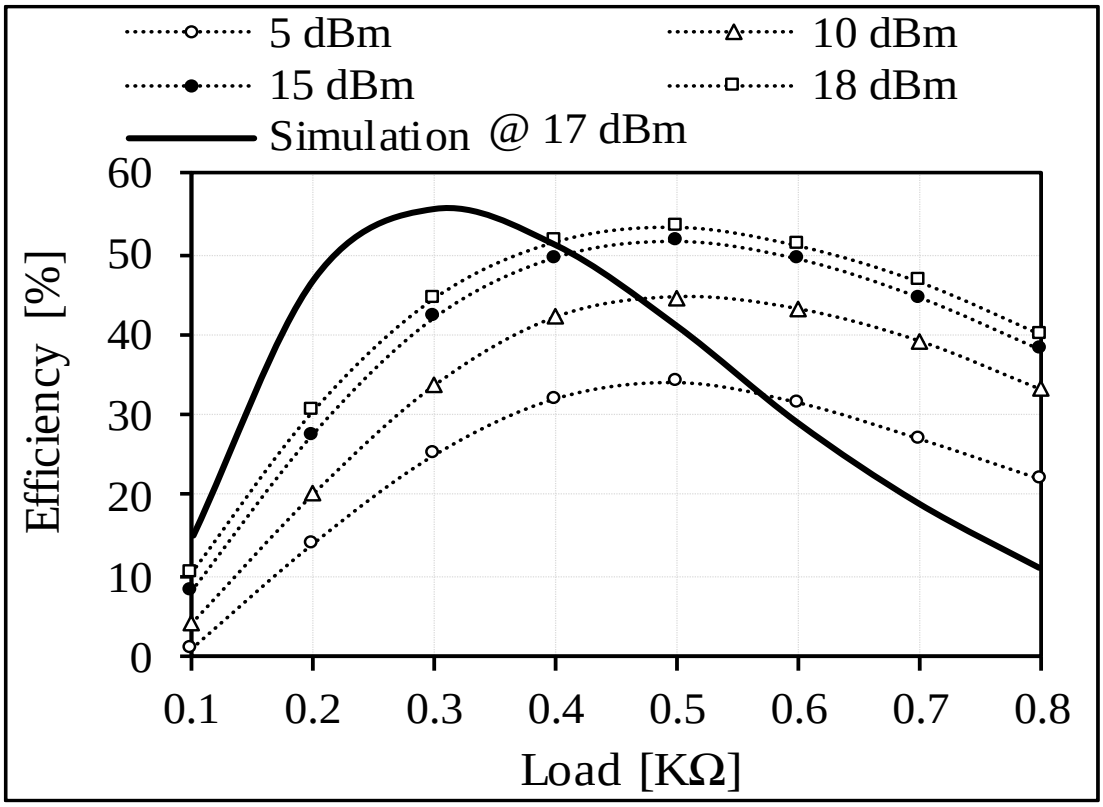


Fig. 5. 9: Simulated and measured PCE with respect to load at different input power levels.

5.3.3 Performance Comparison

The performance comparison of the proposed wideband rectifier is shown in TABLE 5.1, which demonstrates the proposed CMOS rectifier achieved more than 48% PCE for the frequency bandwidth of 1.9 GHz to 4.1 GHz at 500 Ω and 18 dBm of optimal efficiency condition with peak efficiency of 52.8% and active area of 0.51 mm^2. The proposed work achieved ultra-wideband operation in CMOS ever reported as compared to related state-of-arts.

Table 5. 1: Performance comparison of proposed rectifier with other related state-of-arts

Ref.	Frequency (GHz)	Conversion Efficiency (%)	Output Load Resistance	CMOS Technology	Area {active area} (mm^2)
[75]	2.4	15.9 @ 0 dBm	10 MΩ	0.13 μm	2.08*
[76]	5.8	14 @ 0 dBm	1 MΩ	0.13 μm	1.036**
[77]	2.4	30 @ 10 dBm	250 Ω	0.13 μm	0.7395
[80]	2.4	46 @ 25.5 dBm	24 Ω	28 nm	0.705***
[81]	2.4	47 47 @ 8.9 dBm	2 KΩ	0.18 μm	0.057***
[83]	2.4 - 3.5	> 40 @ 22 dBm	1 KΩ	0.18 μm	0.4218 {0.2106}
This work	**1.9 - 4.1**	**> 48 @ 18 dBm**	**0.5 KΩ**	**0.18 μm**	**0.798 {0.5185}**
	2.1	**52.8 (peak) @ 18 dBm**			

*Required transceiver, **required T/R switch, ***required off chip matching.

5.4 Summary

In this chapter, a compact ultra-wideband CMOS rectifier is proposed and designed. The proposed circuit employs the concept of parasitic cancellation techniques cascaded with the conventional *L*-matching to achieve ultra-wideband operation at targeted range. The measurement results demonstrate more than 48% PCE throughout the frequency bandwidth of 1.9 GHz to 4.1 GHz, with a peak efficiency of 52.8% at 18 dBm of input power and 500 Ω of load. The proposed circuit maintains compactness with an active area size of 0.51 mm^2. This highly efficient compact ultra-wideband on-chip rectifier are advantageous for the beamforming-based WPT systems that are applicable to power the smaller gadgets circuits which has constraints for high performance in the lower aspect ratio in terms of the circuit size.

Chapter 6: Conclusion and Future Prospect

The thesis has outlined the design of various rectification circuits that would be applicable for the beamforming-based WPT system ranging from the larger devices to the smaller devices meeting the constraints for effective wireless energy transfer. Major requirements of the rectifier for such applications as working for dual power band, reconfigurable frequency band, and the size requirements are featured. By employing DGS topology, high quality factor inductors are achieved which replace the use of conventional lossy lumped inductor, resulting in improvement efficiency. Furthermore, the concept of self-impedance matching is introduced for wideband rectification having the control over resonance which maintains good efficiency throughout the total available bandwidth of the 5G network. Additionally, to make the circuit more compact, the rectifier is designed in CMOS technology.

6.1 Conclusion

The main contributions in this thesis are summarized as follows:

- Firstly, by tuning the operating frequency at input, dual power bands are obtained from a single rectifier circuit with higher efficiency. In the proposed rectifier, frequency f_1 = 900 MHz is selected for low-power applications whereas f_2 = 2.4 GHz is selected for low-power applications. For impedance matching of the Rectifier-I and Rectifier-II, the required inductance values of 34 nH and 5 nH respectively are realized using DGS topology, resulting in reduced inductor loss and improved efficiency. The proposed rectifier covered the input power range from -18 dBm to 2 dBm, 8 dBm to 20 dBm maintaining more than 50% of RF-to-dc conversion efficiency with overall circuit size of 35mm × 30mm.

- Secondly, the concept of self-impedance matching is employed by connecting a driving rectifier in parallel with the conventional voltage doubler circuit. The driving rectifier is designed with a half-wave rectifier and a series stub line realized as a virtual dc voltage source. The high-impedance stub line (Z_0, θ) of the driving rectifier is responsible for the frequency bandwidth adjustment of the proposed rectifier. The proposed concept makes the rectifier a most compact design by removing additional matching networks at the input and have simultaneous control on the frequency

bandwidth and the peak efficiency. The measurement result shows that the proposed rectifier covered all the accessible bandwidth of both 3.7 GHz and 4.5 GHz bands of 5G (from 3 GHz to 5.8 GHz) with more than 50 % PCE with a circuit size of only 12mm × 6.3mm. Also, the use of DGS topology makes the proposed rectifier more compact and low-loss circuit. Such rectifiers can be applicable for EH of sub-6G signals from 5G network.

- Thirdly, the concept of parallel rectifier by integrating two rectifiers i.e., main rectifier and auxiliary rectifier named as Rectifier-I and Rectifier-II, respectively is employed. In this work, the main rectifier was specially targeted for rectification whereas the auxiliary rectifier was designated for impedance matching, resulting in no need of any matching circuits at input. Additionally, the auxiliary rectifier is responsible for controlling the resonance of the proposed rectifier. The measurement results demonstrate more than 40% PCE throughout the frequency bandwidth of 2.4 GHz to 3.5 GHz, with a peak efficiency of 46.8%. The proposed circuit maintains compactness with an active area size of 0.21mm^2.

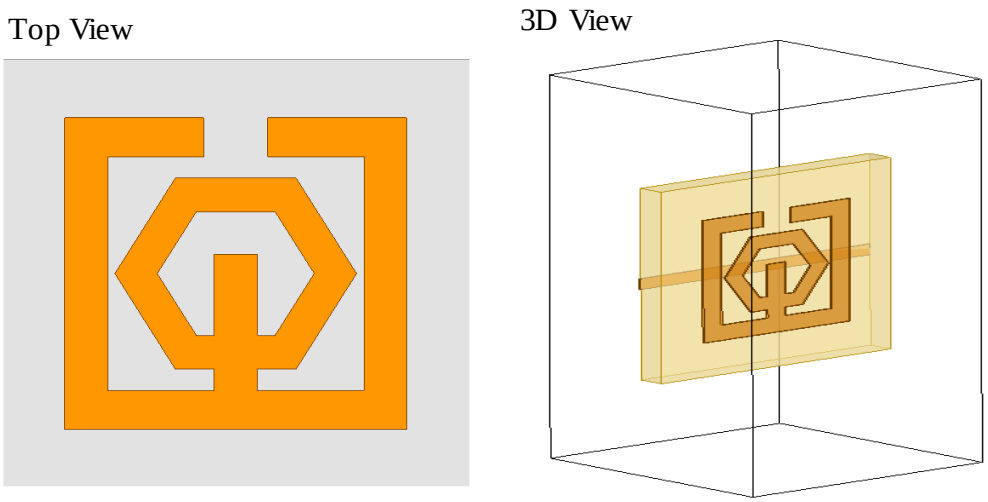
- Finally, an ultra-wideband CMOS rectifier was proposed employing a novel parasitic cancellation technique using a single inductor (L_p) at the gate side (G) of the transistor (M) along with the L-matching at the input. The proposed technique significantly improves the efficiency between the resonances due to L-matching and parasitic cancellation, resulting maximum flat efficiency is obtained throughout the ultra-wideband range. The proposed design achieves more than 48% conversion efficiency at 18 dBm optimal input power and 500 Ω optimal load conditions for the broadband range from 1.9 GHz to 4.1 GHz, with an active circuit size of 0.51 mm^2.

6.2 Future Prospects

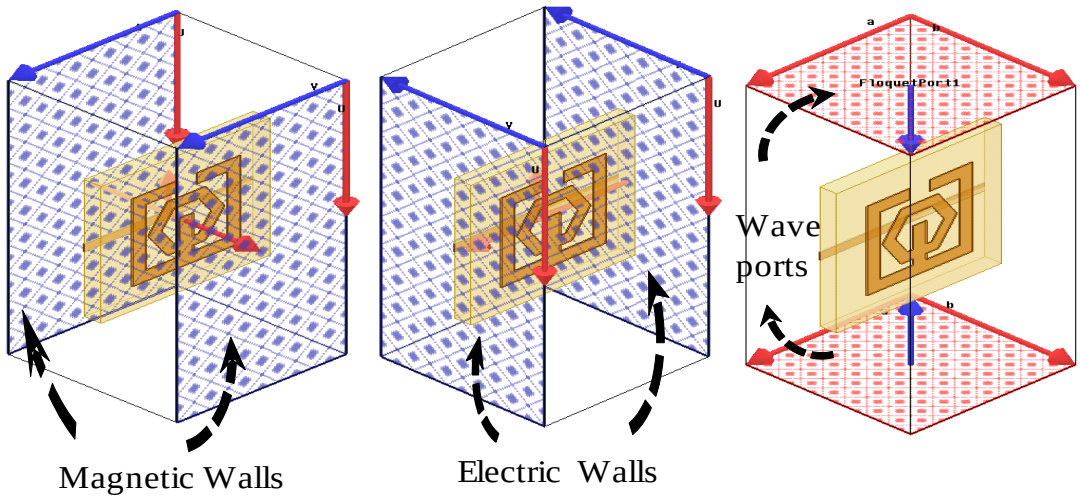
In this thesis we were successful to develop various rectifiers that are able to work in various power levels, frequencies, and are compact to be implement in compact circuit requirements. Now, to implement the thesis outcomes, the future prospects would be to build the beamforming based WPT system employing beamforming antennas the developed rectification circuits, which will be as follows:

I. Design of beamforming antennas using metamaterial for WPT:

Beamforming antennas are indispensable to achieve beamforming-based WPT. Metamaterial ae engineered structures that can manipulate the EM fields and offer an innovative solution for improving the efficiency and the directivity of the antenna array system. So, utilizing the advantages of the metamaterial, metamaterial-based beamforming antenna development will be effective for beamforming WPT system design. Fig. 6.1 shows a metamaterial structure unit cell. By arranging these metamaterials in planar configuration, metamaterial sheets can be designed as shown in Fig. 6. 2. A good point of this unit cell metamaterial is that it can be used as a basic antenna unit structure to design high gain unit cell antenna.



(a)



(b)

Fig. 6. 1: Unit metamaterial structure (a) Layout view (b) simulation model in HFSS software representing magnetic walls, electric walls, and wave ports.

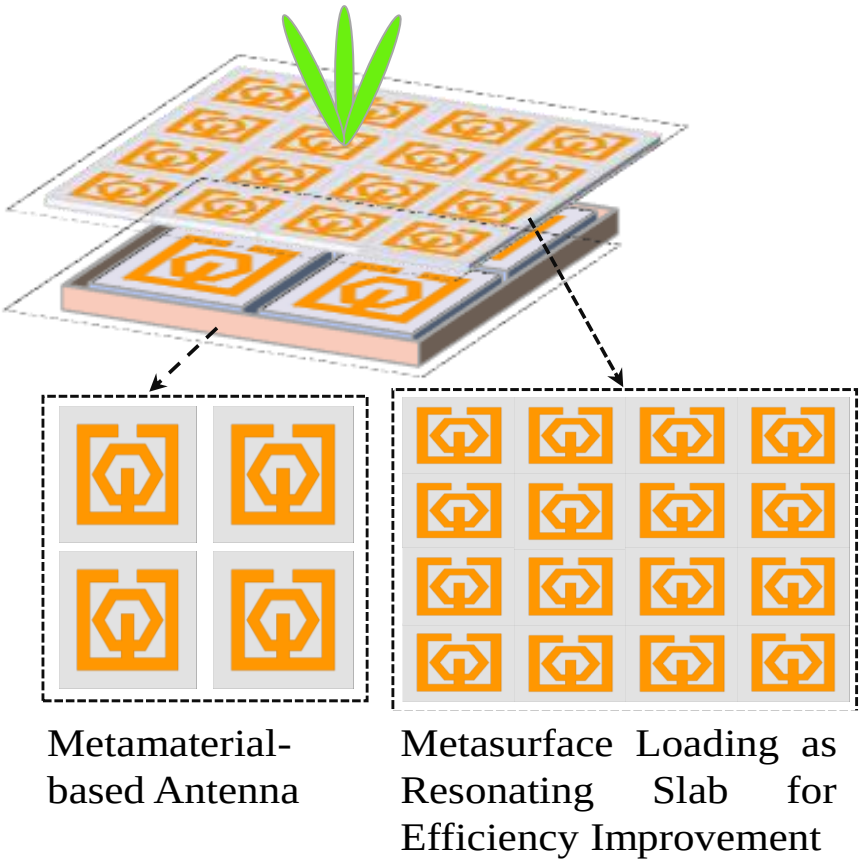


Fig. 6. 2: Metamaterial-based beamforming antenna design.

II. Integration of metamaterial-based beamforming antenna with proposed CMOS rectifier

The overall beamforming-based WPT system will finally be designed by the integration of the developed CMOS rectifier and metamaterial-based beamforming antenna. This system will be capable of operating for various power levels at the target operating frequency.

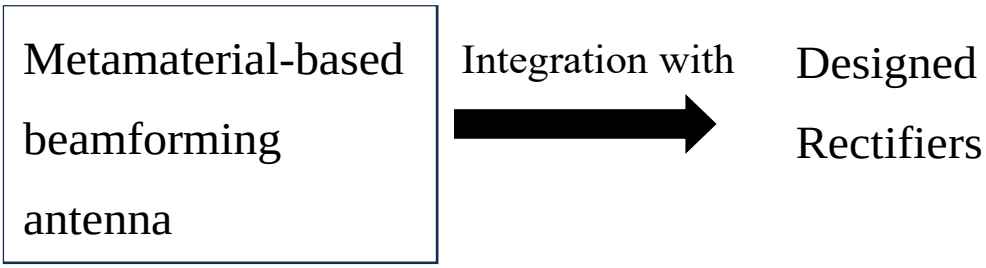


Fig. 6. 3: Metamaterial-based beamforming antenna integration with proposed rectifiers.

References

[1] A. Petritz, et al, “Imperceptible energy harvesting device and biomedical sensor based on ultra fexible ferroelectric transducers and organic diodes,” *Nature Communication*, vol.12, 2399 (2021).

[2] R. K. Pokharel, A. Barakat, S. Alshhawy, K. Yoshitomi, and C. Sarris, “Wireless power transfer system rigid to tissue characteristics using metamaterial inspired geometry for biomedical implant applications,” *Scientific Reports*, vol. 11, 5868 (2021).

[3] S. Hekal, A. B. Abdel-Rahman, H. Jia, A. Allam, A. Barakat, and R. K. Pokharel, “A Novel Technique for Compact Size Wireless Power Transfer Applications Using Defected Ground Structures,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 591-599, Feb. 2017, doi: 10.1109/TMTT.2016.2618919.

[4] R. Sharma, et al, “Electrically connected spin-torque oscillators array for 2.4 GHz Wi-Fi band transmission and energy harvesting,” *Nature Communication*, vol. 12, 2924 (2021).

[5] S. Assawaworrarit, and S. Fan, “Robust and efficient wireless power transfer using a switch-mode implementation of a nonlinear parity–time symmetric circuit,” *Nature Electron*, vol. 3, 273–279 (2020).

[6] A. Barakat, K. Yoshitomi, and R. K. Pokharel, “Design Approach for Efficient Wireless Power Transfer Systems During Lateral Misalignment,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 9, pp. 4170-4177, Sept. 2018, doi: 10.1109/TMTT.2018.2852661.

[7] H. J. Visser and R. J. M. Vullers, "RF Energy Harvesting and Transport for Wireless Sensor Network Applications: Principles and Requirements," in *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1410-1423, June 2013, doi: 10.1109/JPROC.2013.2250891.

[8] Z. Hameed and K. Moez, "Design of impedance matching circuits for RF energy harvesting systems", *Microelectron. J.*, vol. 62, pp. 49-56, Apr. 2017.

[9] C. Wang, N. Shinohara, and T. Mitani, "Study on 5.8-GHz Single-Stage Charge Pump Rectifier for Internal Wireless System of Satellite," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 4, pp. 1058-1065, April 2017, doi: 10.1109/TMTT.2017.2672552.

[10]T. Ngo, A. Huang, and Y. Guo, "Analysis and Design of a Reconfigurable Rectifier Circuit for Wireless Power Transfer," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7089-7098, Sept. 2019, doi: 10.1109/TIE.2018.2875638.

[11]Y. Huang, N. Shinohara, and T. Mitani, "A Constant Efficiency of Rectifying Circuit in an Extremely Wide Load Range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 986-993, April 2014, doi: 10.1109/TMTT.2013.2287676.

[12]S. Muhammad, J. Jiat Tiang, S. Kin Wong, A. Iqbal, M. Alibakhshikenari, and E. Limiti, "Compact Rectifier Circuit Design for Harvesting GSM/900 Ambient Energy," *Electronics*. 2020; 9(10):1614. https://doi.org/10.3390/electronics9101614.

[13] Q. W. Lin and X. Y. Zhang, "Differential Rectifier Using Resistance Compression Network for Improving Efficiency Over Extended Input Power Range," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 9, pp. 2943-2954, Sept. 2016, doi: 10.1109/TMTT.2016.2592531.

[14] S. D. Assimonis, V. Fusco, A. Georgiadis, et al., "Efficient and Sensitive Electrically Small Rectenna for Ultra-Low Power RF Energy Harvesting'" *Scientific Reports*, vol. 8, 15038 (2018). https://doi.org/10.1038/s41598-018-33388-w.

[15] M. Aboualalaa, I. Mansour, A. B. Abdelrahman, A. Allam, M. Abo-zahhad, H. Elsadek, and R. K. Pokharel, "Dual-band CPW rectenna for low input power energy harvesting applications," *IET Circuits, Devices & Systems*, 2020, 14, (6), p. 892-897, DOI: 10.1049/iet-cds.2020.0013.

[16] N. Shariati, W. S. Rowe, J. R. Scott, and K. Ghorbani, "Multi-service highly sensitive rectifier for enhanced RF energy scavenging," *Scientific Reports*, vol. 5 2015 May 7, 9655. doi: 10.1038/srep09655.

[17] J. Liu, M. Huang, and Z. Du, "Design of Compact Dual-Band RF Rectifiers for Wireless Power Transfer and Energy Harvesting," IEEE Access, vol. 8, pp. 184901-184908, 2020, doi: 10.1109/ACCESS.2020.3029603.

[18] H. Tafekirt, J. Pelegri-Sebastia, A. Bouajaj, and B. M. Reda, "A Sensitive Triple-Band Rectifier for Energy Harvesting Applications," *IEEE Access*, vol. 8, pp. 73659-73664, 2020, doi: 10.1109/ACCESS.2020.2986797.

[19]C. Song, Y. Huang, P. Carter, J. Zhou, S. D. Joseph, and G. Li, "Novel Compact and Broadband Frequency-Selectable Rectennas for a Wide Input-Power and Load Impedance Range," *IEEE Transactions on Antennas and Propagation*, vol. 66, no. 7, pp. 3306-3316, July 2018, doi: 10.1109/TAP.2018.2826568.

[20] J. -J. Lu, X. -X. Yang, H. Mei, and C. Tan, "A Four-Band Rectifier With Adaptive Power for Electromagnetic Energy Harvesting," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 10, pp. 819-821, Oct. 2016, doi: 10.1109/LMWC.2016.2601294.

[21] V. Kuhn, C. Lahuec, F. Seguin, and C. Person, “A Multi-Band Stacked RF Energy Harvester With RF-to-DC Efficiency Up to 84%,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 5, pp. 1768-1778, May 2015, doi: 10.1109/TMTT.2015.2416233.

[22] C. Song et al., “A Novel Six-Band Dual CP Rectenna Using Improved Impedance Matching Technique for Ambient RF Energy Harvesting,” *IEEE Transactions on Antennas and Propagation*, vol. 64, no. 7, pp. 3160-3171, July 2016, doi: 10.1109/TAP.2016.2565697.

[23] M. M. Mansour, X. L. Polozec, and H. Kanaya, “Compact and Wide-band Efficiency Improved RF Differential Rectifier for Wireless Energy Harvesting,” in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 972-975, doi: 10.1109/MWSYM.2018.8439427.

[24] L.-F. Li, X. Yang, and E.-J. Liu, “A Broadband High-Efficiency Rectifier Based on Two-Level Impedance Match Network,” *Progress In Electromagnetics Research Letters*, vol. 72, pp. 91-97, 2018.

[25]M. M. Mansour and H. Kanaya, “Compact and Broadband RF Rectifier With 1.5 Octave Bandwidth Based on a Simple Pair of L-Section Matching Network,” *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 4, pp. 335-337, April 2018, doi: 10.1109/LMWC.2018.2808419.

[26]Mei-Juan Nie, Xuexia Yang, and Jia-Jun Lu, “A Broadband Rectifying Circuit with High Efficiency for Microwave Power Transmission,” *Progress In Electromagnetics Research Letters*, vol. 52, pp. 135-139, 2015.

[27]M. Nie, X. Yang, G. Tan and B. Han, “A Compact 2.45-GHz Broadband Rectenna Using Grounded Coplanar Waveguide,” *IEEE Antennas and Wireless Propagation Letters*, vol. 14, pp. 986-989, Dec. 2015, doi: 10.1109/LAWP.2015.2388789.

[28]D. Wang, X. A. Nghiem, and R. Negra, “Design of a 57 % bandwidth microwave rectifier for powering application,” in *2014 IEEE Wireless Power Transfer Conference*, 2014, pp. 68-71, doi: 10.1109/WPT.2014.6839596.

[29]H. S. Park and S. K. Hong, “Broadband RF-to-DC Rectifier With Uncomplicated Matching Network,” *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 1, pp. 43-46, Jan. 2020, doi: 10.1109/LMWC.2019.2954594.

[30]P. Wu *et al*., “Compact High-Efficiency Broadband Rectifier With Multi-Stage-Transmission-Line Matching,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 8, pp. 1316-1320, Aug. 2019, doi: 10.1109/TCSII.2018.2886432.

[31]S. Zheng, W. Liu, and Y. Pan, “Design of an Ultra-Wideband High-Efficiency Rectifier for Wireless Power Transmission and Harvesting Applications,” *IEEE Transactions on Industrial Informatics*, vol. 15, no. 6, pp. 3334-3342, June 2019, doi: 10.1109/TII.2018.2874460.

[32]X. Y. Zhang, Z. Du, and Q. Xue, “High-Efficiency Broadband Rectifier With Wide Ranges of Input Power and Output Load Based on Branch-Line Coupler,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 731-739, March 2017, doi: 10.1109/TCSI.2016.2614331.

[33]Y. L. Lin, X. Y. Zhang, Z. Du, and Q. W. Lin, “High-Efficiency Microwave Rectifier With Extended Operating Bandwidth,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 7, pp. 819-823, July 2018, doi: 10.1109/TCSII.2017.2716538.

[34]C. Song *et al*., "Matching Network Elimination in Broadband Rectennas for High-Efficiency Wireless Power Transfer and Energy Harvesting," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3950-3961, May 2017, doi: 10.1109/TIE.2016.2645505.

[35]J. Kimionis, A. Collado, M. M. Tentzeris, and A. Georgiadis, "Octave and Decade Printed UWB Rectifiers Based on Nonuniform Transmission Lines for Energy Harvesting," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4326-4334, Nov. 2017, doi: 10.1109/TMTT.2017.2697851.

[36]P. Wu, S. Y. Huang, W. Zhou, and C. Liu, "One Octave Bandwidth Rectifier With a Frequency Selective Diode Array," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 11, pp. 1008-1010, Nov. 2018, doi: 10.1109/LMWC.2018.2869281.

[37]H. Zhang, and X. Zhu, "A broadband high efficiency rectifier for ambient RF energy harvesting," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, pp. 1–3 (IEEE, 2014).

[38]J. D. Ryder, Electronic Fundamentals & Applications (Pitman Publishing, 1970).

[39]W. Kester, B. Erisman, and G. Tandi, "Switched Capacitor Voltage Converters. Technical Report," *Analog Devic*es (1998). http://www. analog.com/media/en/training-seminars/design-handbooks/Practical-Design-Techniques-Power-Termal/Section4.pdf. (Accessed 10 September 2021).

[40] B. Gyawali, S. K. Thapa, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Analysis and design of diode physical limit bandwidth efficient rectification circuit for maximum flat efficiency, wide impedance, and efficiency bandwidths," *Scientific Reports*, vol. 11, Art. No. 19941, 2021.

[41]H. Sun, Z. Zhong, and Y. Guo, “An Adaptive Reconfigurable Rectifier for Wireless Power Transmission,” *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 9, pp. 492-494, Sept. 2013.

[42]A. M. Almohaimeed, R. E. Amaya, J. A. Lima, and M. C. E. Yagoub, “An Adaptive Power Harvester with Active Load Modulation for Highly Efficient Short/Long Range RF WPT Applications,” *Electronics*, vol. 7, no. 125, Jul. 2018.

[43]P. Lu, C. Song, F. Cheng, B. Zhang, and K. Huang, “A Self-Biased Adaptive Reconfigurable Rectenna for Microwave Power Transmission,” *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7749- 7754, Aug. 2020.

[44]P. Lu, X. Yang, J. Li, and B. Wang, “Polarization Reconfigurable Broadband Rectenna With Tunable Matching Network for Microwave Power Transmission,” *IEEE Transactions on Antenna Propagation*, vol. 64, no. 3, pp. 1136-1141, March 2016.

[45]P. Lu, K. M. Huang, Y. Yang, F. Cheng, and L. Wu, “Frequency Reconfigurable Rectenna With an Adaptive Matching Stub for Microwave Power Transmission,” *IEEE Antennas and Wireless Propagation Letters*, vol. 18, no. 5, pp. 956-960, May 2019.

[46]D. Khan et al., “An Efficient Reconfigurable RF-DC Converter With Wide Input Power Range for RF Energy Harvesting,” IEEE Access, vol. 8, pp. 79310-79318, 2020.

[47]A. Mabrouki, M. Latrach and V. Lorrain, “High efficiency low power rectifier design using zero bias schottky diodes,” in IEEE Faible Tension Faible Consommation, Monaco, Monaco, 2014, pp. 1-4.

[48]B. Gyawali, R. K. Pokharel, S. K. Thapa, M. Aboualalaa, A. Barakat, and K. Yoshitomi, “Broadband and Compact 3-Bit Digitally-Controlled Reconfigurable Rectification Circuit,” in Proc. 2022 Wireless Power Week (WPW), Bordeaux, France, 2022, pp. 780–783.

[49]B. Gyawali, S. K. Thapa, M. Aboualalaa, A. Barakat, K. Yoshitomi and R. K. Pokharel, “Design of Self-Impedance Matching Ultra-Wideband Rectification Circuit,” in Proc. 2022 Asia-Pacific Microw. Conf. (APMC), Yokohama, Japan, 2022, pp. 671-673.

[50]Z. Zhong, H. Sun, and Y. Guo, “Design of rectifier with extended operating input power range,” Electron. Lett., vol. 49, no. 18, pp. 1175–1176, Aug. 2013.

[51] A. A. R. Haeri, M. G. Karkani, M. Sharifkhani, M. Kamarei, and A. Fotowat-Ahmady, “Analysis and design of power harvesting circuits for ultra-low power applications,” IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 64, no. 2, pp. 471-479, Feb. 2017.

[52] P.-H. Hsieh, C.-H. Chou, and T. Chiang, “An RF energy harvester with 44.1% PCE at input available power of −12 dBm,” IEEE Trans. Circuits Syst. I Reg. Papers, vol. 62, no. 6, pp. 1528-1537, Jun. 2015.

[53] P. Saffari, A. Basaligheh, V. J. Sieben, and K. Moez, “An RF-powered wireless temperature sensor for harsh environment monitoring with non-intermittent operation,” IEEE Trans. Circuits Syst. I Reg. Papers, vol. 65, no. 5, pp. 1529-1542, May 2018.

[54] P. Saffari, A. Basaligheh, and K. Moez, “An RF-to-DC rectifier with high efficiency over wide input power range for RF energy harvesting applications,” IEEE Trans. Circuits Syst. I Reg. Papers, vol. 66, no. 12, pp. 4862-4875, Dec. 2019.

[55] K. Niotaki et al., “RF Energy Harvesting and Wireless Power Transfer for Energy Autonomous Wireless Devices and RFIDs,” IEEE J. Microwaves, vol. 3, no. 2, pp. 763-782, April 2023.

[56] K. Miwatashi, T. Hirakawa, N. Shinohara, and T. Mitani, “Development of High-Power Charge Pump Rectifier for Microwave Wireless Power Transmission,” IEEE J. Microwaves, vol. 2, no. 4, pp. 711-719, Oct. 2022.

[57] K. Dang et al., “A 5.8-GHz High-Power and High-Efficiency Rectifier Circuit With Lateral GaN Schottky Diode for Wireless Power Transfer,” IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2247-2252, March 2020.

[58] J. Liu, Y. Z. Xiu, and C. L. Yang, “Analysis and design of dual-band rectifier using novel matching network,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 4, pp. 431–435, Apr. 2017.

[59] S. Shen, C.-Y. Chiu, and R. D. Murch, “A Dual-Port Triple-Band L-Probe Microstrip Patch Rectenna for Ambient RF Energy Harvesting,” IEEE Antenna Wireless Propag. Lett., vol. 16, pp. 3071-3074, 2017.

[60] S. Shen, Y. Zhang , C.Y. Chiu, and R. Murch , “A Triple-Band High-Gain Multibeam Ambient RF Energy Harvesting System Utilizing Hybrid Combining,” IEEE Trans. Ind. Electron., vol. 67, no. 11, pp. 9215-9226, Nov. 2020.

[61] H. Sun, Y. X. Guo, M. He, and Z. Zhong, “A dual-band rectenna using broadband Yagi antenna array for ambient RF power harvesting,” IEEE Antenna Wireless Propag. Lett., vol. 12, pp. 918-921, Aug. 2013.

[62] V. Palazzi et al., “A Novel Ultra-Lightweight Multi-band Rectenna on Paper for RF Energy Harvesting in the Next Generation LTE Bands,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 1, pp. 366-379, Jan. 2018.

[63] J. Liu, M. Huang, and Z. Du, “Design of Compact Dual-Band RF Rectifiers for Wireless Power Transfer and Energy Harvesting,” IEEE Access, vol. 8, pp. 184901-184908, 2020.

[64] F. Bolos, D. Belo, and A. Georgiadis, “A UHF rectifier with one octave bandwidth based on a non-uniform transmission line,” in Dig. IEEE MTT-S Int. Microw. Symp. Dig., May 2016, pp. 1–3.

[65]W. Liu, K. Huang, T. Wang, Z. Zhang, and J. Hou, “A Broadband High-Efficiency RF Rectifier for Ambient RF Energy Harvesting,” IEEE Microw. Wireless Compon. Lett., vol. 30, no. 12, pp. 1185-1188, Dec. 2020.

[66] C. -H. Du, F. Cheng, and C. Gu, “Efficient Tri-Band Rectifier Using Multistub Matching Network for WPT Applications,” IEEE Microw. Wireless Techn. Lett., vol. 33, no. 9, pp. 1361-1364, Sept. 2023.

[67] Z. Yue, X. Xu, S. Li, Y. H. Zhu, and X. Q. Lin, “Efficient and Compact Tri-Band Rectifier With Large Frequency Ratio for WPT,” IEEE Microw. Wireless Compon. Lett., vol. 32, no. 11, pp. 1355-1358, Nov. 2022.

[68] P. Lu, X. -S. Yang, J. -L. Li, and B. -Z. Wang, “A Compact Frequency Reconfigurable Rectenna for 5.2- and 5.8-GHz Wireless Power Transmission,” IEEE Trans. Power Electron., vol. 30, no. 11, pp. 6006-6010, Nov. 2015.

[69]X. Wang, B. Jin, L. Huang, M. Zhang, and M. Fang, “A Novel High-Sensitivity Broadband Rectifier for Ambient RF Energy Harvesting,” Radioengineering, vol. 31, no. 3, pp. 331-338, Sep. 2022.

[70] S. Yu, F. Cheng, C. Gu, C. Wang, and K. Huang, “Compact and Efficient Broadband Rectifier Using T-type Matching Network,” IEEE Microw. Wireless Compon. Lett., vol. 32, no. 6, pp. 587-590, June 2022.

[71]S. H. Wang, S. Y. Zheng, K. W. Leung, and M. H. Xia, “A Self-Matched Multi-Band Rectifier for Efficient Electromagnetic Energy Harvesting,” IEEE Trans. Circuit Syst. I: Reg. Pap., vol. 68, no. 11, pp. 4556-4565, Nov. 2021.

[72] M. A. Halimi, P. P. Shome, T. Khan, and S. R. Rengarajan, “Efficient single and broadband microwave rectifiers for RFEH/WPT enabled low power 5G sub-6 GHz devices,” AEU-Intl. J. Electron. Commn., vol. 165, Art. no. 154645, Jun. 2023.

[73]Z. He and C. Liu, “A compact high-efficiency broadband rectifier with a wide dynamic range of input power for energy harvesting,” IEEE Microw. Wireless Compon. Lett., vol. 30, no. 4, pp. 433–436, Apr. 2020.

[74] NanoStationM & NanoStationlocoM Datasheet. https://dl.ubnt.com/datasheets/nanostationm/nsm_ds_web.pdf (Accessed 26 March 2024).

[75] J. Masuch, M. Delgado-Restituto, D. Milosevic, and P. Baltus, “Co-integration of an RF energy harvester into a 2.4 GHz transceiver,” IEEE J. Solid-State Circuits, vol. 48, no. 7, pp. 1565–1574, Jul. 2013.

[76] W. Lerdsitsomboon and K. Kenneth, “Technique for integration of a wireless switch in a 2.4 GHz single chip radio,” IEEE J. Solid-State Circuits, vol. 46, no. 2, pp. 368–377, Feb. 2011.

[77] S. Dehghani and T. Johnson, “A 2.4-GHz CMOS Class-E Synchronous Rectifier,” IEEE Trans on Microw. Theory and Techn., vol. 64, no. 5, pp. 1655-1666, May 2016.

[78]B. Li, X. Shao, N. Shahshahan, N. Goldsman, T. Salter, and G. M. Metze, “An Antenna Co-Design Dual Band RF Energy Harvester,” IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 60, no. 12, pp. 3256-3266, Dec. 2013.

[79] J. Pandey, Y.-T. Liao, A. Lingley, R. Mirjalili, B. Parviz, and B. Otis, “A fully integrated RF-powered contact lens with a single element display,” IEEE Trans. Biomed. Circuits Syst., vol. 4, no. 6, pp. 454–461, Dec. 2010.

[80] X. Li, Y. Lu, M. Huang, and R. P. Martins, “A 2.4-GHz Mid-Field CMOS Wireless Power Receiver Achieving 46% Maximum PCE and 163-mW Output Power,” IEEE Trans. Circuits Syst. II: Exp. Brief., vol. 67, no. 2, pp. 360-364, Feb. 2020.

[81] C.-J. Li and T.-C. Lee, “2.4-GHz high-efficiency adaptive power,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 2, pp. 434–438, Feb. 2014.

[82] G. L. Matthaei, L. Young, and E. M. T. Jones, “Microwave Filters, Impedance-Matching Network, and Coupling Structures” Artech House, 1980.

[83] B. Gyawali, R. K. Pokharel, S. K. Thapa, A. Barakat, and N. Shinohara, “New Rectification Technique Employing Auxiliary Rectifier for Resonance Control Achieving Compact Size and High Efficiency in CMOS,” *IEEE Solid-State Circuits Letters*, vol. 7, pp. 187-190, 2024, doi: 10.1109/LSSC.2024.3409710.

List of Publications

Journal Publications

[J1] **B. Gyawali,** R. K. Pokharel, S. K. Thapa, A. Barakat and N. Shinohara, "New Rectification Technique Employing Auxiliary Rectifier for Resonance Control Achieving Compact Size and High Efficiency in CMOS," *IEEE Solid-State Circuits Letters*, vol. 7, pp. 187-190, 2024, doi: 10.1109/LSSC.2024.3409710.

[J2] **B. Gyawali,** M. Aboualalaa, A. Barakat and R. K. Pokharel, "Design of Miniaturized Sub-6 GHz Rectifier With Self-Impedance Matching Technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 7, pp. 3413-3422, July 2024, doi: 10.1109/TCSI.2024.3397810.

[J3] **B. Gyawali,** S. K. Thapa, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Analysis and design of diode physical limit bandwidth efficient rectification circuit for maximum flat efficiency, wide impedance, and efficiency bandwidths", *Nature Scientific Reports* 11, 19941 (2021), doi: https://doi.org/10.1038/s41598-021-99405-7.

Conference Publications

[C1] **B. Gyawali,** M. Aboualalaa, A. Barakat, and R. K. Pokharel, "Frequency Switching Dual Power Band Rectifier with Load-Modulation Technique," in *Proc. IEEE Wireless Power Technology Conference and Expo 2023 (WPTCE2023),* San Diego, CA, USA, 2023, pp. 1-4, doi: 10.1109/WPTCE56855.2023.10216256.

[C2] **B. Gyawali,** M. Aboualalaa, A. Barakat, and R. K. Pokharel, "Design of Low Efficiency Variation 5G Rectifier without External Matching Circuits," in *Proc. 2022 Asian Wireless Power Transfer Workshop (AWPT2022),* Kyoto, Japan, 2022, Dec. 5-6.

[C3] **B. Gyawali,** S. K. Thapa, M. Aboualalaa, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Design of Self-Impedance Matching Ultra-Wideband Rectification Circuit," in *Proc. 2022 Asia-Pacific Microwave Conference (APMC2022)*, Yokohama, Japan, 2022, pp. 671-673. DOI: https://doi.org/10.23919/APMC55665.2022.9999810.

[C4] **B. Gyawali,** R. K. Pokharel, S. K. Thapa, M. Aboualalaa, A. Barakat, and K. Yoshitomi, "Broadband and Compact 3-Bit Digitally-Controlled Reconfigurable Rectification Circuit," in *Proc. 2022 IEEE Wireless Power Week (WPW 2022)*, Bordeaux, France, 2022, pp. 780-783. DOI: https://doi.org/10.1109/WPW54272.2022.9901332.

Awards

[A1] ***"Student Award"*** in 2022 Asian Wireless Power Transfer Workshop (AWPT), 2022.

[A2] ***"Presentation Award"*** in the 2nd Thailand-Japan Microwave Student Workshop (TJMW), 2021.