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Low temperature (210 °C) fabrication of Ge MOS capacitor and controllability of its flatband voltage

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ABSTRACT

Germanium (Ge) and germanium tin (GeSn) are strong candidate materials for novel electronic device such as spin MOS field-effect transistor (FET) or flexible devices. A high-quality insulating layer on Ge(Sn) should be formed at low temperatures to realize these applications. In this study, we fabricated a Ge MOS capacitor (CAP) and n-MOSFET with a SiO_2/GeO_2 gate dielectric using an electron cyclotron resonance plasma process and subsequent post-deposition annealing at a low temperature of 210 °C. The MOSCAPs show the typical electrical characteristics without significant degradation compared with the samples fabricated at a higher temperature of 450 °C. The n-MOSFET shows distinct output characteristics with clear saturation behavior and high current drivability. From the flatband voltage comparison among different annealing temperatures, high-temperature annealing induces the interface dipole formation in the gate insulator, significantly shifting flatband voltage to a negative direction. X-ray photoelectron spectroscopy analysis suggests that the origin of the interface dipole is oxygen atom movement at a SiO_2/GeO_2 interface. This information will be an important guideline for fabricating a high-quality insulator on Ge(Sn) at low temperatures.

1. Introduction

Germanium (Ge) has many exciting material characteristics, such as high carrier mobility, long spin diffusion length, and high-quality polycrystalline formation at relatively low temperatures [1–6]. By adding tin (Sn) into Ge, we can modulate its band structure from indirect to direct [7]. Thus, Ge and GeSn are suitable for various applications, such as complementary metal-oxide-semiconductor (CMOS) channels [1,2], spin MOS field-effect transistor (MOSFET) channels [3,8], flexible electronics devices [9–11], and near/mid-infrared optical devices [7,12]. A high-quality insulating film on Ge as a gate insulator or passivation layer is required to successfully apply Ge to these devices. Concerning spin MOSFET application, as a ferromagnetic source/drain (S/D) electrode, we focus on Heusler alloy (ex. CoFeAlSi (CFAS) and Co_2MnSi (CMS)) due to its excellent spin injection/detection efficiency [3,8]. However, when these Heusler alloy/Ge contact is annealed at above 250 °C, this interface and spin injection/detection characteristics deteriorate significantly due to interdiffusion of the constituent elements [13]. Similarly, glass or plastic substrates that will be used in the flexible electronics field have weak heat-resisting properties [10,14]. On the other hand, previously reported fabrication processes of the insulating layer on Ge require a relatively high process temperature of 400–550 °C, particularly gate stack fabrication steps [1,2,15]. Therefore, these methods are hard to apply for Heusler alloy/Ge-based spin MOSFET or flexible electronic devices, and process temperature reduction is strongly required.

We have demonstrated Ge n-MOSFET operation with ferromagnetic Heusler alloy S/D [8]. In this previous paper, we used SiO_2/GeO_2 structure as a gate insulator. However, the fabrication temperature of its gate stack using the electron cyclotron resonance (ECR) plasma process and subsequent post-deposition annealing was 250 °C. As mentioned above, the temperature is still high for spin MOSFET or flexible electronics applications. Furthermore, GeSn requires a lower process temperature to prevent Sn precipitation at high temperature. Of course, we should avoid degradation of dielectric properties such as interface state density or leakage current characteristics in low-temperature process.

Based on these backgrounds, we studied a high-quality insulating layer fabrication on Ge at low process temperature. We used the MOS capacitor (CAP) as a sample structure for evaluation. The Ge MOS capacitor fabricated at 210 °C showed typical properties without degradation of electrical properties compared with the samples at a higher process temperature. In addition, a n-channel Ge MOSFET with

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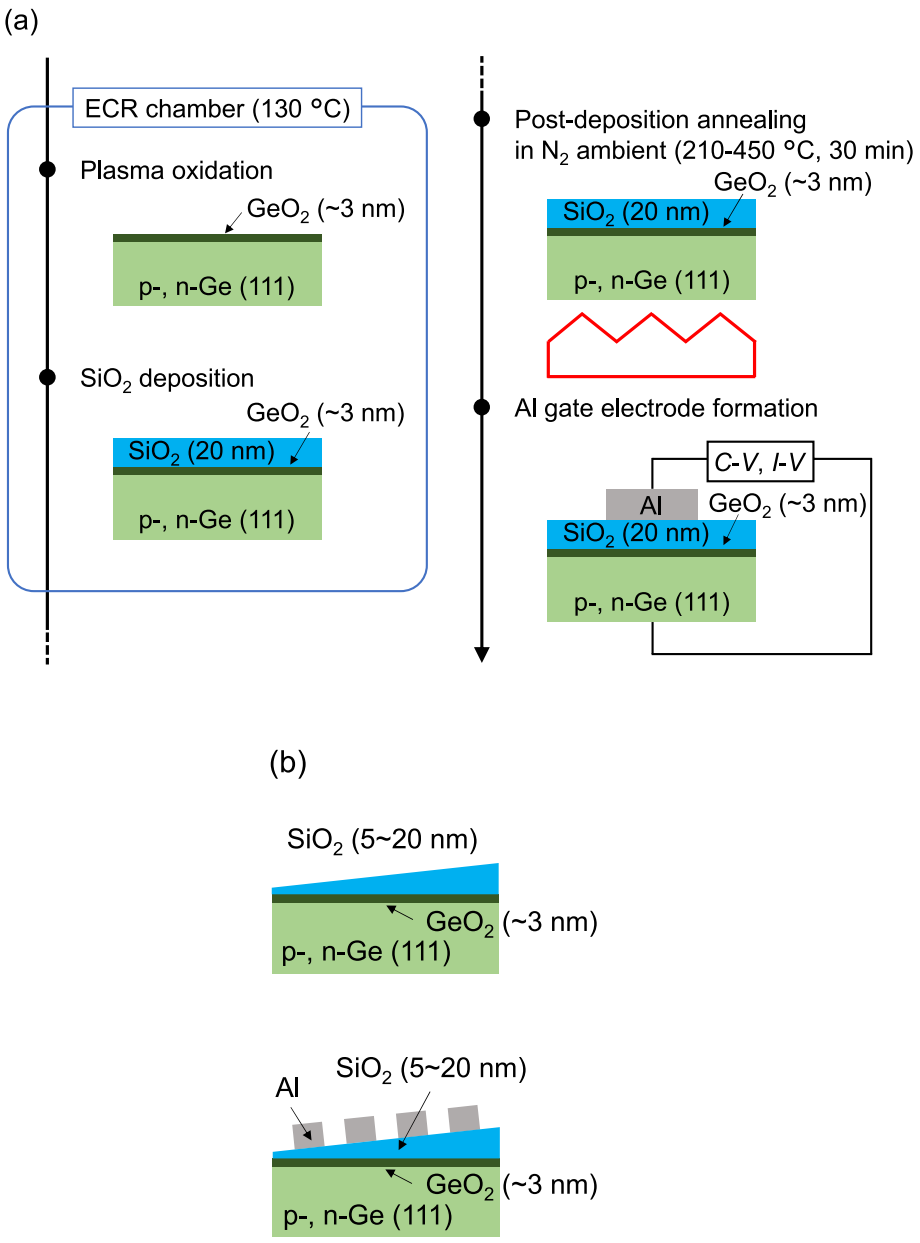

Fig. 1. (a) Fabrication procedure of Ge MOSCAPs in this study. (b) The cross-sectional illustration of the MOSCAP sample with SiO_2 thickness gradient.

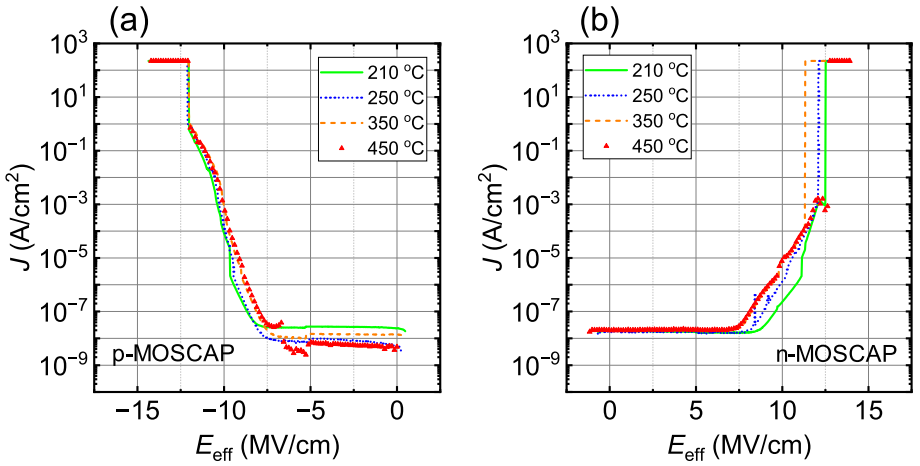

Fig. 2. Leakage current characteristics of Ge (a) p-MOS capacitors and (b) n-MOS capacitors with PDA temperature range of 210–450 °C.

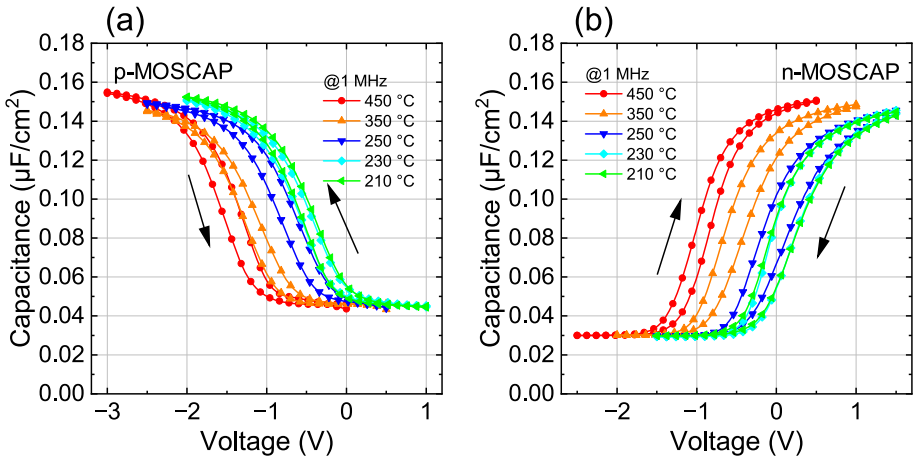

Fig. 3. High-frequency (1 MHz) roundtrip *C–V* characteristics of Ge (a) p-MOS capacitors and (b) n-MOS capacitors with a PDA temperature range of 210–450 °C.

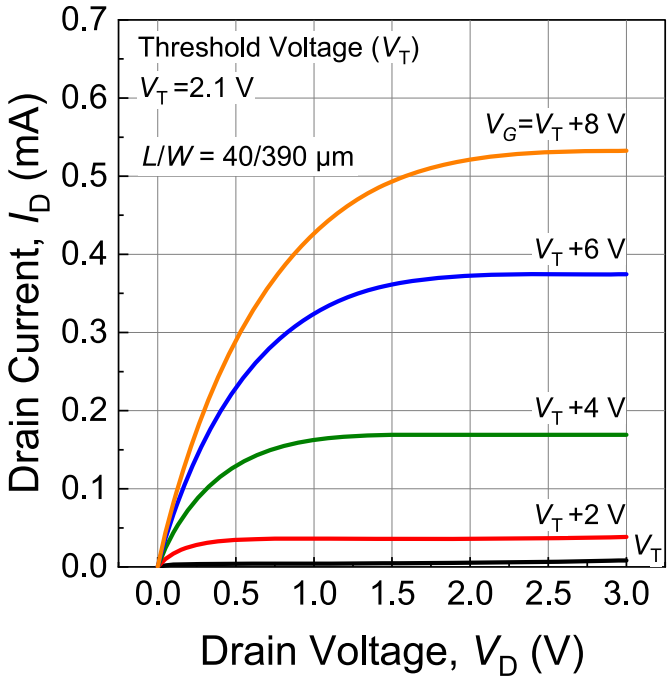

Fig. 4. Output characteristics of a Ge n-MOSFET with the SiO_2/GeO_2 gate insulator fabricated at 210 °C.

the same gate stack operated successfully. Comparing the electrical characteristics of Ge MOS capacitors fabricated at different temperatures, we found the negative shift of flatband voltage (V_{FB}) for the sample with high fabrication temperature. Through the electrical and structural analysis, oxygen-related interface dipole may have an important role in this phenomenon. This information will be helpful in surface potential control for Ge and GeSn advanced electronic devices.

2. Experimental

In this study, we used (111) oriented p- and n-Ge substrates because they are epitaxial growth orientations for ferromagnetic Heusler alloys [8]. And we used SiO_2/GeO_2 structure as a gate insulator similar to the previous study [8]. One of the reasons for using SiO_2/GeO_2 structure is GeO_2/Ge interface shows excellent electrical characteristics [16,17]. However, it needs to be passivated by other stable dielectrics due to its high water solubility and poor chemical instability [18,19]. Based on these reasons, we used sputter-deposited SiO_2 as a capping layer for plasma-oxidized GeO_2 because it can be formed at low temperatures, and both layers can be formed sequentially in the same vacuum chamber without breaking the vacuum by ECR plasma process [20]. The surface of the Ge substrate was ultrasonically cleaned with acetone and de-ionized water. Subsequently, the native oxide of the surface was removed by cyclic cleaning with diluted HF and de-ionized water. After substrate chemical cleaning, the sample was loaded into the vacuum chamber of the ECR system immediately. ECR plasma oxidation was performed at 130 °C on the Ge surface for a gate stack's interlayer formation [20]. Through the plasma oxidation, ~3 nm-thick GeO_2 grows on the Ge surface. Then, SiO_2 (20 nm) was deposited by an ECR plasma sputtering at the same temperature without breaking the vacuum. Post-deposition annealing (PDA) was performed at 210, 230, 250, 350, or 450 °C for 30 min in N_2 ambient. Al was deposited using thermal evaporation and patterned as a gate electrode. Fig. 1(a) shows MOSCAP sample preparation procedure. We measured the leakage current and high-frequency roundtrip capacitance-voltage (*C–V*) property as electrical characterizations. We calculated the capacitance equivalent thickness (*CET*), V_{FB}, and hysteresis (*HT*) from *C–V* characteristics.

To clarify the dominant component of V_{FB}, V_{FB} thickness dependence was studied. After the formation of a 20 nm-SiO_2/GeO_2 stacked structure and PDA at 210 or 450 °C with the method mentioned above, a SiO_2 thickness gradient (5–20 nm) was made by time-dependent wet etching by ultra dilute HF solution. Then, Al gate electrode was formed by thermal evaporation. The cross-sectional sample illustration is shown in Fig. 1(b).

The n-MOSFET was fabricated on (111) p-Ge using the gate-last process [21]. After forming a heavy-doped S/D region by thermal diffusion of phosphorous from a solid-state diffusion source (spin-on dopant) [22], the $Al/SiO_2/GeO_2$ gate stack was formed using the abovementioned method with PDA temperature of 210 °C. Al contact metal for S/D was formed and annealed at 200 °C. The channel length (*L*) and width (*W*) are 40 and 390 μm, respectively.

3. Results

Fig. 2 shows the leakage current characteristics (leakage current density *J* vs effective electric field E_{eff} (≡ gate voltage (V_G)/*CET*)) of the samples (a) p-MOS and (b) n-MOS. All samples show almost the same *J*-E_{eff} curves without significant temperature dependence. Specifically, the effective breakdown fields ($E_{B,eff}$) of the p-MOS and n-MOS samples with PDA temperature of 210 °C were 12.0 MV/cm and 12.5 MV/cm, respectively. These values are comparable with thermally oxidized SiO_2 on Si [23]. Moreover, the leakage currents were well suppressed at applied fields lower than $E_{B,eff}$. Fig. 3(a) and (b) show the high-frequency (1 MHz) roundtrip *C–V* characteristics of p-MOS and

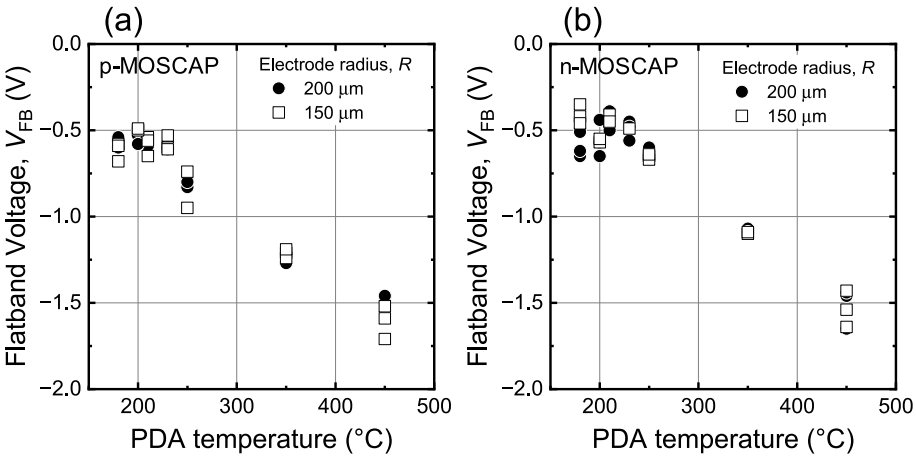

Fig. 5. V_{FB} dependence of PDA temperature. (a) p-MOS and (b) n-MOS capacitors.

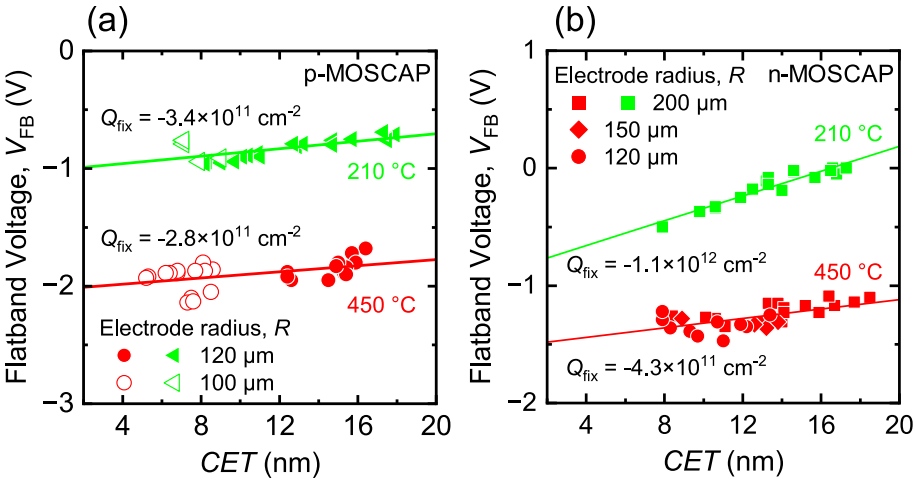

Fig. 6. V_{FB} – CET plots for Q_{fix} and δ_{dipole} estimation. (a) p-MOS and (b) n-MOS. A cross-sectional illustration of the sample is shown in Fig. 1(b).

Table 1
Q_{fix} and δ_{dipole} obtained from V_{FB}-*CET* plots.

PDA	Q_{fix} [cm^{-2}]		δ_{dipole} [eV]	
	p	n	p	n
210 °C	−3.4 × 10^{11}	−1.1 × 10^{12}	0.94	0.98
450 °C	−2.8 × 10^{11}	−4.3 × 10^{11}	1.81	1.70

n-MOS capacitors with different PDA temperatures, respectively. Even at a low PDA temperature of 210 °C, both p- and n-MOS capacitors show typical high-frequency *C*–*V* curves. Fig. 4 shows the output characteristics of the Ge n-MOSFET with the SiO_2/GeO_2 gate insulator fabricated at 210 °C. We can find a well-behaved FET operation curve. The peak value of the field-effect mobility was 154 cm^2/Vs. Figs. 2–4 suggest that the SiO_2/GeO_2 gate stack fabricated using the ECR method can work as a MOS gate on Ge even by low-temperature fabrication.

From Fig. 3(a) and (b), we can find that *C*–*V* curves shift to a positive direction with decreasing PDA temperature. At high PDA temperatures such as 450 °C, V_{FB} is negatively high, which is unfavorable in terms of low voltage operation of MOS devices. Therefore, low-temperature PDA can potentially tune V_{FB} for operation voltage control. The V_{FB} and PDA temperature relationship was visualized in Fig. 5(a) for p-MOSCAP and 5(b) for n-MOSCAP. Similar process temperature dependence of V_{FB} has been reported for thermally oxidized GeO_2/Ge structures (400–500 °C) [24] and HfO_2/GeO_2/Ge structures (350–400 °C) [25].

To clarify the main component of V_{FB}, we extract fixed charges and interfacial dipoles of SiO_2/GeO_2/Ge gate stacks based on the *C*–*V* characteristics of the sample with SiO_2 thickness gradients. In general, the V_{FB} of a MOS is determined by the work function difference between the gate electrode metal and the semiconductor and the fixed charge distributed in the dielectric film. Fixed charges in the dielectric film can be divided into three types: interface-localized fixed charges, uniformly distributed fixed charges in the film, and dipoles at the interface between different dielectrics. Of these, the interface-localized fixed charge changes V_{FB} linearly with *CET*, while the uniformly distributed fixed charge in the film changes V_{FB} with the square of *CET*. The change in V_{FB} due to the dipole is independent of *CET*. From this, the presence of each charge can be inferred from the shape of the V_{FB}–*CET* plots. V_{FB}–*CET* plots for these samples are summarized in Fig. 6. All plots show a good linear relationship, which means the effect of uniformly distributed fixed charges in SiO_2 and GeO_2 can be negligible. In this case, the V_{FB} can be expressed as follows:

$$V_{FB} = (\Phi_M - \Phi_{Ge}) - \frac{Q_{fix}}{\varepsilon_{SiO_2}\varepsilon_0} CET + \delta_{dipole} \quad (1)$$

where Φ_M (4.28 eV) and Φ_{Ge} (4.51 eV for p-Ge and 4.17 eV for n-Ge) are work functions of Al gate electrode and Ge, respectively [26]. Φ_{Ge}s were obtained from the acceptor or donor concentration of the Ge substrates. δ_{dipole} is the total dipole in the gate stack. Q_{fix} are areal densities of interfacial fixed charges near the dielectric/Ge interface. We can obtain

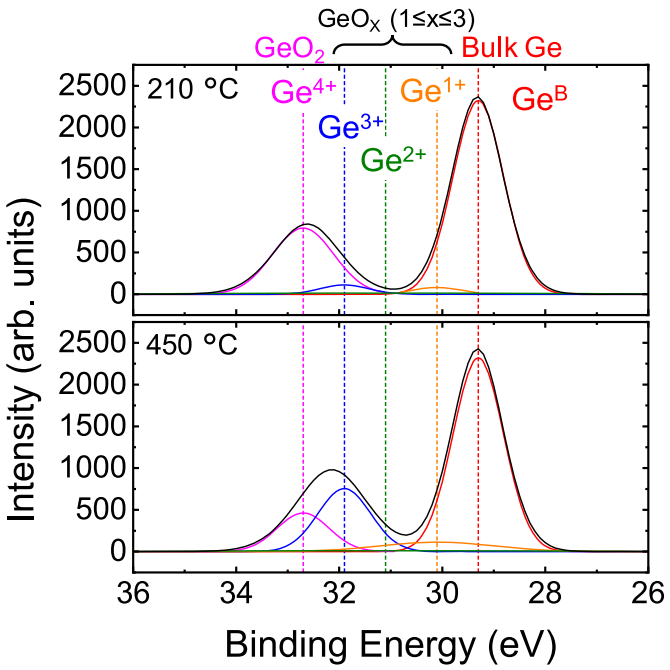

Fig. 7. Ge 3d XPS spectra for $SiO_2/GeO_2/Ge$ stacks with (a) 210 °C and (b) 450 °C PDA.

Q_{fix} and δ_{dipole} from the slope and y-axis interception of the fitting line of Fig. 6, respectively. The calculated Q_{fix} and δ_{dipole} are summarized in Table 1. In the p-MOS case, Q_{fix} shows almost the same value in different PDA temperatures (imperceptibly high in the 210 °C-PDA sample). On the other hand, the δ_{dipole} drastically increased at high PDA temperatures. Although the n-MOS shows a slight Q_{fix} change, the dominant V_{FB} change component is δ_{dipole}, the same as the p-MOS case.

4. Discussion

To clarify the origin of δ_{dipole} modulation by different PDA temperatures, X-ray photoelectron spectroscopy (XPS) measurement was carried out. Fig. 7 shows the Ge 3d XPS spectra of 1.5-nm SiO_2/3 nm-GeO_2/Ge structures with (a) 210 °C and (b) 450 °C PDA at a photoelectron take-off angle of 90°. The spectra were calibrated with a Ge 3d core level (29.3 eV). Compared with 210 °C-PDA sample, the Ge oxide peak located 32–33 eV of 450 °C-PDA sample shifts to a low energy direction. For further discussion, the spectrums for both samples were deconvoluted into a bulk-related component and four oxide-related components corresponding to specific Ge oxidation states of Ge^{1+}, Ge^{2+}, Ge^{3+}, and Ge^{4+}. The dominant component of the 210 °C-PDA sample is Ge^{4+}, corresponding GeO_2. On the other hand, sub-oxide (Ge^{3+} and Ge^{1+}) components increase for the 450 °C-PDA sample. Such temperature-dependent tendency was reported in Refs. [27,28]. The origin is considered the volatilization of O from GeO_2.

Kita et al. suggested that the origin of interface dipole in gate stack is an areal density difference of oxygen atoms at the interface of different insulating layers [29]. We try to explain the δ_{dipole} modulation in our experiment using this model. As shown in Fig. 7, high-temperature PDA reduces GeO_2 and brings on Ge sub-oxide formation. It is considered volatilization of GeO_2. This high-temperature PDA generates positively charged oxygen vacancy (O_V^+) in GeO_2. And excess oxygen atoms diffuse to the SiO_2 side and stay as negatively charged interstitial (O_I^-). As a result, the V_{FB} negatively shifts by δ_{dipole} formation at SiO_2/GeO_2 for MOS capacitors with PDA at 450 °C. It is illustrated in Fig. 8. It is attractive from the viewpoint of the V_{FB} control of Ge-MOS devices. In other words, low-temperature PDA for SiO_2/GeO_2 stacked gate dielectric suppresses the interface dipole formation efficiently, and this method can help control the surface potential of the Ge and threshold voltage of Ge-based MOS devices. In actual Ge and GeSn device applications, introducing a high-k gate insulator instead of SiO_2 will be necessary, similar to Si or other semiconductor materials [29–32]. We consider that the behavior of SiO_2/GeO_2 interface obtained in this study could be applied to discuss the high-k/GeO_2 interface.

5. Conclusion

For novel Ge-based electronic devices requiring low-temperature formation, we fabricated and characterized Ge MOSCAPs with a process temperature of 210 °C. From the leakage current and C–V characteristics, the MOSCAP fabricated at 210 °C does not degrade it electrical characteristics significantly compared with the samples with a higher fabrication temperature. The n-MOSFET fabricated at a low temperature of 210 °C also successfully operated with clear saturation behavior and high current drivability. We found that the V_{FB} drastically shifted by changing the PDA temperature. From the detailed V_{FB} analysis using the SiO_2 thickness gradient sample, it is clarified that the dominant component was the interface dipole at the gate stack. According to the XPS analysis, the origin of the interface dipole is considered the oxygen atom movement at the SiO_2/GeO_2 interface during high-temperature PDA. In other words, low-temperature PDA effectively suppresses the interface dipole formation, which will help control the surface potential of the Ge underlying insulator.

CRediT authorship contribution statement

Hajime Kuwazuru: Writing – original draft, Methodology, Investigation, Formal analysis, Data curation. **Taisei Aso:** Investigation, Formal analysis, Data curation. **Dong Wang:** Supervision, Project administration. **Keisuke Yamamoto:** Writing – review & editing, Writing – original draft, Supervision, Project administration, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests.

Keisuke Yamamoto reports financial supports were provided by Japan Society for the Promotion of Science, New Energy and Industrial Technology Development Organization, Tohoku University Research Institute of Electrical Communication. The other authors declare that

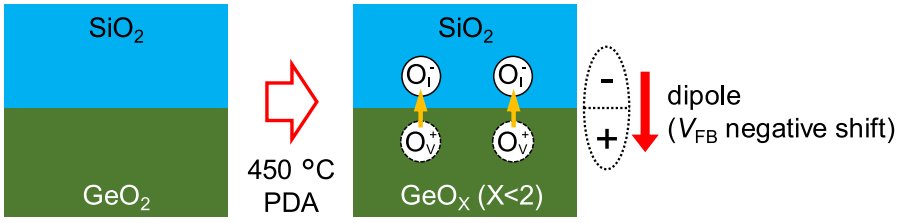

Fig. 8. Schematic illustration of dipole formation at SiO_2/GeO_2 interface during 450 °C PDA.

they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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