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A Novel Capacitorless Low-Dropout Regular (LDO) Design for High-Performance System-on-Chip Applications Using 180nm CMOS Process

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Abstract: *This paper presents the design and validation of a capacitorless low-dropout regulator (LDO) using 180nm CMOS technology, targeting low power consumption, high power supply rejection ratio (PSRR), and stability for system-on-chip (SoC) applications. Unlike traditional LDOs, which rely on bulky external capacitors, this design eliminates them, reducing size and cost. Key components include a bandgap voltage reference (BGR), startup circuit, error amplifier, and power core, all meticulously designed and simulated. The integrated LDO exhibited excellent performance: a low quiescent current of 78.9µA, near-zero shutdown current, superior line, load regulation, and a PSRR of -61dB at 100kHz. Power gating further reduced idle power consumption. Extensive simulations validated the design's efficiency and stability, making it suitable for portable, low-power applications. This work addresses conventional LDO limitations and lays the foundation for future capacitorless LDO designs, promoting more compact and efficient power management solutions.*

Keywords: Capacitorless Low-Dropout Regulator (LDO); CMOS Technology; System-on-Chip (SoC); Power Supply Rejection Ratio (PSRR); Power Management.

1. INTRODUCTION

The increasing demand for efficient power management solutions, particularly in system-on-chip (SoC) applications, has significantly influenced the semiconductor industry [1]. Traditional low-dropout regulators (LDOs) rely on external capacitors to achieve stability and a high-power supply rejection ratio (PSRR) [2]. However, these capacitors are bulky, expensive, and degrade over time, reducing the LDO's long-term stability and performance. Consequently, there is a growing interest in developing capacitorless LDOs, which eliminate the need for external components, reducing board space and overall system cost [3],[4]. Despite these advantages, capacitorless LDOs present substantial design challenges, particularly in maintaining stability and frequency response [5]-[7].

The semiconductor industry is currently experiencing rapid growth and significant transformation, driven by technological advancements and the increasing demand for high-performance, energy-efficient devices [8]-[11]. The proliferation of portable electronic devices and the integration of digital and analog circuits on a single chip underscore the need for robust and efficient power management solutions [12]-[15]. However, the industry also faces challenges such as supply chain disruptions, rising production costs, and the need for sustainable manufacturing practices [16]-[18]. These factors highlight the importance of innovative solutions, such as capacitorless LDOs, which can meet stringent performance requirements while addressing cost and environmental concerns [19]-[22].

Ensuring a stable voltage supply regardless of changes in input voltage, supply current, output load, or temperature is crucial in power management [23]-[24]. LDOs are popular for on-chip power management because they provide accurate and clean supply voltages, suitable for SoC applications [25]-[27]. The trend toward high-performance LDOs with high PSRR specifications is driven by the widespread use of portable applications, which necessitate the coexistence of digital and analog circuits within the same die [28]. Additionally, reducing power consumption is a significant trend established by the growth of mobile applications, emphasizing the necessity for stable and power-efficient LDO designs [29]-[31].

LDOs are categorized into conventional and capacitorless types. Conventional LDOs typically employ high-value external capacitors to enhance stability and PSRR performance [32]-[33]. However, these capacitors occupy additional board space, require extra pins in SoC devices, and degrade over time, which can compromise long-term stability. The shift towards capacitorless LDOs addresses these drawbacks by eliminating the need for external capacitors, thereby reducing system size and cost. This makes capacitorless LDOs attractive for applications where efficiency and compactness are critical [34]-[38]. Nevertheless, capacitorless architectures present significant challenges, particularly in achieving stable operation and maintaining adequate frequency response [39]-[45].

This research aims to address the limitations of conventional LDOs by proposing a capacitorless LDO design that offers low power consumption and high PSRR performance. The significance of this work lies in its potential to provide a more efficient and cost-effective solution for power management in SoC applications. By eliminating the need for external capacitors, the proposed design can significantly reduce the overall size and cost of the system, making it suitable for a wide range of

applications. Moreover, the implementation of Miller compensation topology and an on-chip capacitor is intended to enhance the stability and frequency response of the LDO, overcoming the traditional challenges associated with capacitorless designs.

The specific objectives of this research are: to design and develop a capacitorless LDO regulator using 180nm CMOS process technology, tailored to provide stable and efficient power management for SoC applications; to optimize the LDO's performance by achieving high PSRR and low quiescent current, which are crucial for minimal power consumption and enhanced noise rejection; to maintain stability and improve frequency response through the implementation of Miller compensation topology and an on-chip capacitor; to incorporate power gating techniques to further reduce power consumption by turning off circuit blocks when not in use; and to simulate the proposed design using HSpice tools and validate its performance through extensive testing and analysis.

This study proposes an improved capacitorless LDO that is low-power and has a high PSRR performance while maintaining the fast frequency response required by SoC applications. The circuit is designed with a Miller Compensation topology to compensate for the absence of an output capacitor. This topology is a robust and effective compensation technique well-suited for capacitorless LDOs. An added on-chip capacitor of 10pF is also implemented to achieve better line and load regulation. Additionally, power gating is implemented to reduce power consumption by turning off a circuit block when it is not in use. The overall system is designed and simulated using HSpice 180nm CMOS technology.

2. METHODOLOGY

The methodology for designing a capacitorless low-dropout regulator (LDO) focused on achieving low power consumption, high power supply rejection ratio (PSRR), and stability without relying on external capacitors. Key steps in the process included setting design objectives, selecting suitable CMOS process technology, designing and simulating individual components, and integrating these components into a complete LDO system. The performance of the design was rigorously validated through simulations under various conditions, which were presented in Chapter III, Results and Discussion.

The primary goals of the design were to develop an LDO that could efficiently function within system-on-chip (SoC) applications, providing stable output voltage, low power consumption, and high PSRR. Specific targets included achieving low quiescent current, minimal shutdown current, excellent line and load regulation, and superior noise rejection capabilities. Additionally, the design aimed to incorporate power gating techniques to minimize power consumption during idle periods.

Figure 1 illustrates the proposed Bandgap Voltage Reference (BGR) circuit used in the design of the capacitorless low-dropout regulator (LDO). The BGR circuit is essential for providing a stable reference voltage, which is critical for the accurate operation of the LDO. The diagram shows the key components of the BGR, including transistors, resistors, and a current mirror configuration. The transistors are configured to create a temperature-compensated voltage reference, ensuring that the output remains stable across varying supply voltages and temperatures. The resistors are carefully selected to achieve the desired voltage levels and temperature coefficients. This conventional BGR design is chosen for its reliability and effectiveness in maintaining a consistent reference voltage, which is crucial for precisely regulating the LDO. The figure visually represents the layout and connections of the BGR components, highlighting the intricate design necessary to achieve high performance in the capacitorless LDO.

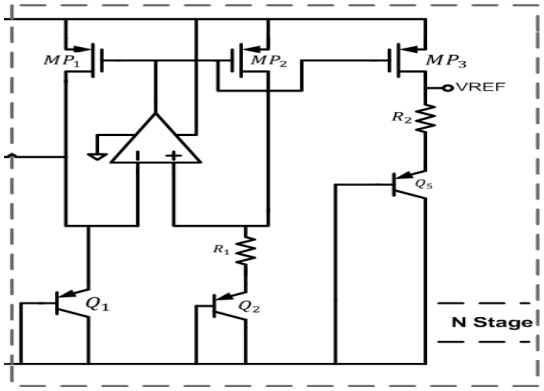

Fig 1 Proposed BGR circuit design.

To properly size the resistor value of the bandgap voltage reference, the resistor ratio must be set as with respect to equation 1 below: This ratio is set such that the PTA voltage (generated by the difference in base-emitter voltages V_{BE} of two transistors operating at different current densities) compensates for the temperature variation of the diode voltage drop.

$$V_{ref} = V_{BE} + \frac{R_2}{R1} + \Delta V_{BE} \quad (1)$$

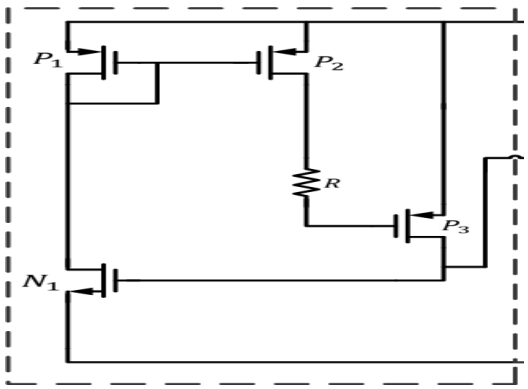

Fig. 2. Proposed Startup Circuit

The startup circuit (Figure 2) ensures that the BGR reaches its stable operating point quickly after power-up. This circuit was designed to provide an initial voltage close to the desired reference voltage, allowing the BGR to take over and stabilize the system. Without an effective startup circuit, the reference voltage might take longer to stabilize, potentially causing inaccuracies in the LDO's output. The proposed startup circuit was simulated and demonstrated rapid and reliable performance, ensuring

the BGR's stability from the moment the device was powered on.

The error amplifier is a critical component that regulates the output voltage by comparing it with the reference voltage and generating an error signal (Figure 3). This signal adjusts the pass transistor to maintain the desired output voltage. The chosen topology for the error amplifier featured high gain, wide bandwidth, and high slew rate, essential for precise voltage regulation and fast response times. The design also included a constant current reference (Figure 4) to provide a stable bias current unaffected by variations in voltage and temperature. The error amplifier was simulated to evaluate its DC gain, phase margin, unity gain bandwidth, and common-mode rejection ratio (CMRR). The results indicated excellent performance, with high gain and stability across different process corners.

The power core consists of the pass transistor, feedback resistors, Miller compensation, and an on-chip capacitor. The pass transistor, a PMOS type, was chosen for its low dropout voltage and low current consumption. The feedback resistors create a voltage divider network that compares the output voltage with the reference voltage, providing feedback to the error amplifier. Miller compensation involves adding a small capacitor to the regulator's feedback loop, counteracting positive feedback caused by the Miller effect and enhancing stability. The on-chip capacitor further improves line and load regulation by providing additional stability without the need for bulky external capacitors.

Power gating is a technique used to reduce power consumption by turning off specific circuit blocks when they are not in use. This technique was implemented to minimize power usage during idle periods, significantly extending battery life in portable applications. The design incorporated power gating in such a way that it did not compromise the LDO's performance during active operation.

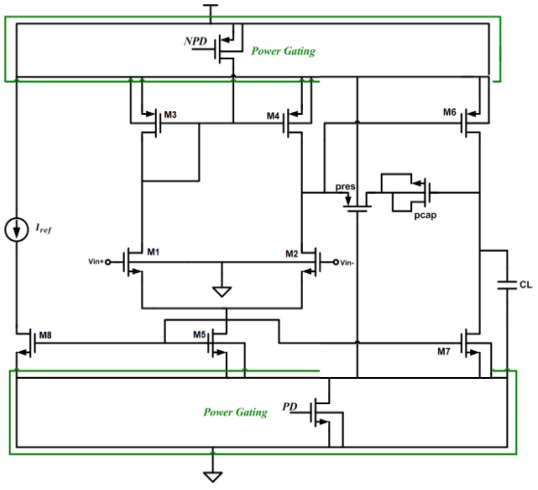

Fig. 3. Proposed Error Amplifier Circuit

Once the individual components were designed and validated through simulations, they were integrated into a complete LDO system.
The integrated design (Figure 5) was then simulated using HSpice to evaluate its overall performance under various conditions, including different supply voltages, temperatures, and load conditions.
The integrated LDO was tested for key performance parameters such as dropout voltage, quiescent current, shutdown current, line regulation, load regulation, and PSRR.

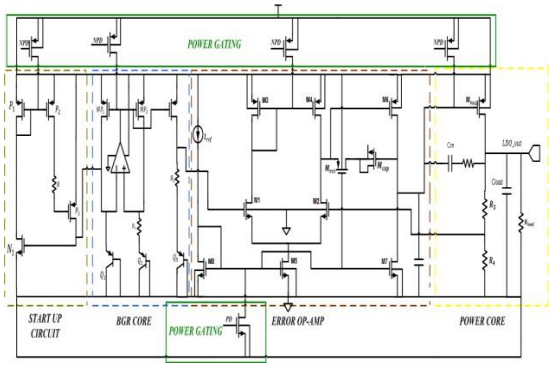

Fig. 4. Proposed Constant Current Reference Circuit

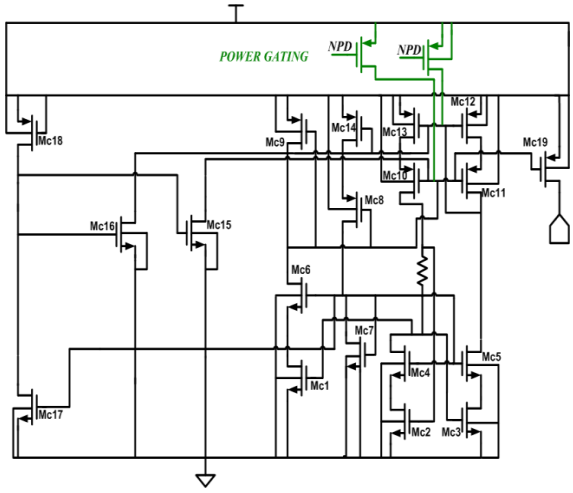

Fig. 5. The LDO Schematic Design.

The dropout voltage, the minimum difference between the input and output voltages for the LDO to maintain regulation, was measured under various conditions. The LDO maintained a dropout voltage of 300mV at the typical and fast corners but increased to 500mV at the slow corner due to the lower supply voltage and higher temperature conditions. These results are within acceptable limits for the targeted applications.

Line regulation measures the LDO's ability to maintain a consistent output voltage despite variations in the input voltage, while load regulation measures the ability to maintain output voltage as the load changes.

The methodology for designing the capacitorless LDO involved a systematic approach to achieving high performance and stability while eliminating external capacitors. By carefully selecting the 180nm CMOS process technology and designing robust components such as the BGR, startup circuit, error amplifier, and power core, the LDO met the stringent requirements for SoC applications. The integrated design demonstrated excellent performance across various metrics, validated through extensive simulations. The implementation of power gating further enhanced the design's efficiency, making it suitable for low-power, portable applications. Future work could explore additional compensation techniques and noise-immune architectures to improve

further the performance and applicability of capacitorless LDOs in various electronic devices.

3. Results and Discussion

The results and discussion section provides an analysis of the performance of the proposed capacitorless low-dropout regulator (LDO) based on simulation and measurement results. This section evaluates the LDO's key performance parameters, including the bandgap voltage reference (BGR), error amplifier, and overall LDO performance, focusing on metrics such as quiescent current, line regulation, load regulation, and power supply ratio (PSRR).

A. Bandgap Voltage Reference (BGR) Simulation Results

The BGR is a critical component in the LDO, responsible for providing a stable reference voltage across various conditions. To evaluate the performance of the BGR, simulations were conducted under different process corners, including typical (TT), fast (FF), and slow (SS) corners, with variations in supply voltage and temperature. The BGR's temperature coefficient (TC) and sensitivity were measured to assess its stability and accuracy.

Figure 6 and Table 1 show the simulation results indicating that the BGR maintained a stable reference voltage with minimal deviation across the different process corners. At the typical corner (vdd = 1.8V, temp = 25°C), the BGR exhibited a TC of 2.5087 ppm/°C and a sensitivity of 0.68. Under fast corner conditions (vdd = 1.98V, temp = 0°C), the TC was 2.3972 ppm/°C with a sensitivity of 0.51, while at the slow corner (vdd = 1.62V, temp = 85°C), the TC increased to 24.8620 ppm/°C with a sensitivity of 1.09. These results demonstrate that the BGR design effectively provides a stable reference voltage, with only slight variations under extreme conditions.

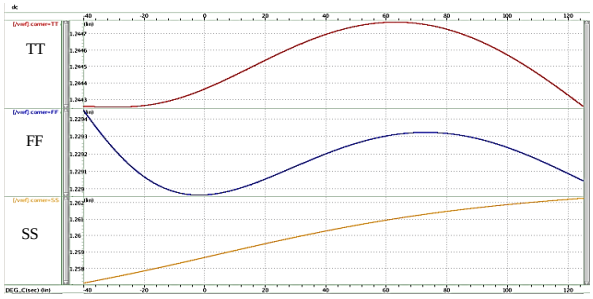

Fig 6 Voltage Reference Output Waveform vs. Temperature Sweep

Table.1 Temperature Coefficient of BGR

PROCESS CORNERS	V_{min}	V_{max}	Voltage @ 300K	TC (ppm/°C)
TT (vdd = 1.8 V, temp = 25 °C)	1.2442527318 V	1.244767908 V	1.24458007 V	2.5087
FF (vdd = 1.98 V, temp = 0 °C)	1.228962810 V	1.229448939 V	1.22902976 V	2.3972
SS (vdd = 1.62 V, temp = 85 °C)	1.2570913412 V	1.262258888 V	1.25969088 V	24.8620

*Temperature is sweep from -40 °C to 125 °C

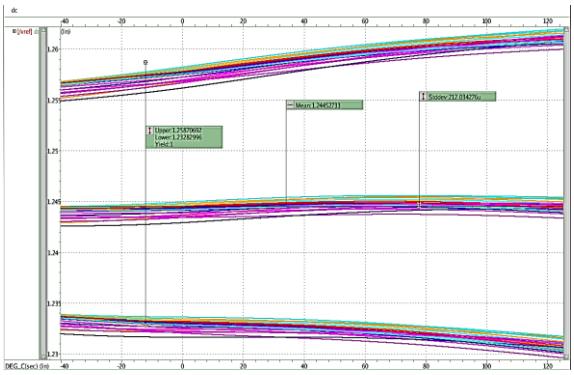

Fig 7 Monte Carlo Analysis Voltage Reference Output Waveform vs Temperature Sweep

Figure 7 shows the Monte Carlo Analysis of voltage reference with 30 iterations. The Monte Carlo analysis of the voltage reference circuit, conducted over 30 iterations, shows a mean output voltage of 1.2452733V, closely aligning with the target of around 1.25V. The standard deviation of 212.034276µV indicates minimal variation in the output voltage due to component tolerances and temperature changes, ranging from approximately -40°C to 120°C. This low deviation suggests that the design is stable and robust, maintaining consistent performance across the specified temperature range.

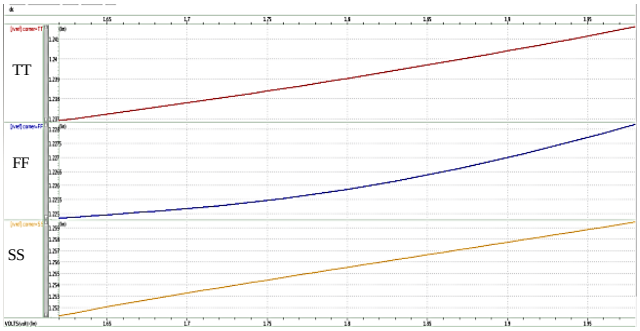

Fig 8 Voltage Reference Output Waveform vs. Voltage Supply Sweep

Table 2. Sensitivity Result of BGR

PROCESS CORNERS	V_{ref} @ 1.8 V	$\frac{dV_{dd}}{dV_{ref}}$	SENSITIVITY (%)
TT (vdd = 1.8 V, temp = 25 °C)	1.24458007 V	5.46473466 m	0.68
FF (vdd = 1.98 V, temp = 0 °C)	1.2289636 V	4.21555299 m	0.51
SS (vdd = 1.62 V, temp = 85 °C)	1.26157198 V	8.68057987 m	1.09

*Voltage supply (V_{dd}) is a sweep from 1.62V to 1.8V

Figure 8 shows the simulation of V_{ref} across voltage supply sweeps, with a sensitivity of 0.68% at the "TT" (typical), 1.09% at the "SS" (slow), and 0.51% at the "FF" (fast) corners. These small sensitivity values indicate that the voltage reference is minimally affected by supply variations. Table 2 summarizes these results. Figure 9 presents the Monte Carlo analysis, revealing slight changes in the output but remaining close to the expected value.

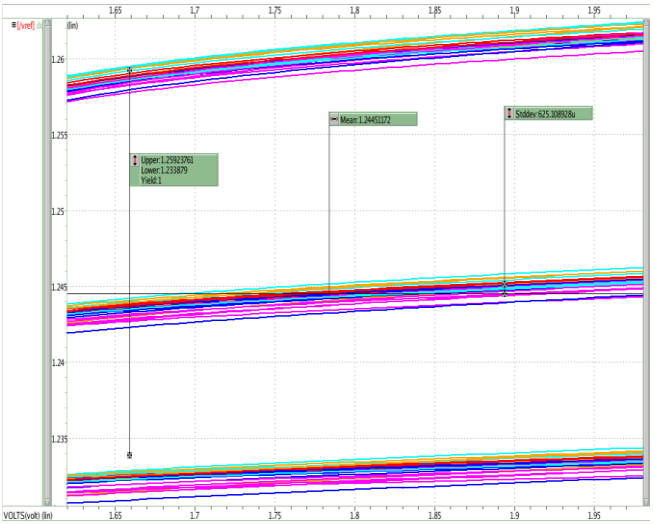

Fig 9 Monte Carlo Analysis of Voltage Reference Output Waveform vs. Voltage Supply Sweep

B. Error Amplifier Simulation Results

The error amplifier plays a crucial role in regulating the output voltage of the LDO by comparing it with the reference voltage and generating an error signal. The performance of the error amplifier was evaluated through frequency response analysis, common-mode rejection ratio (CMRR), slew rate, and PSRR measurements as provided in Figures 10-13 and Table III).

The error amplifier showed impressive performance across various parameters. The DC gain analysis revealed a high gain, essential for precise voltage regulation. Specifically, the gain values were 85.37 dB at the typical corner, 80.08 dB at the fast corner, and 83.24 dB at the slow corner. The phase margin, which indicates the stability of the amplifier, was 71.6° at the typical corner, 60.0° at the fast corner, and 76.5° at the slow corner.

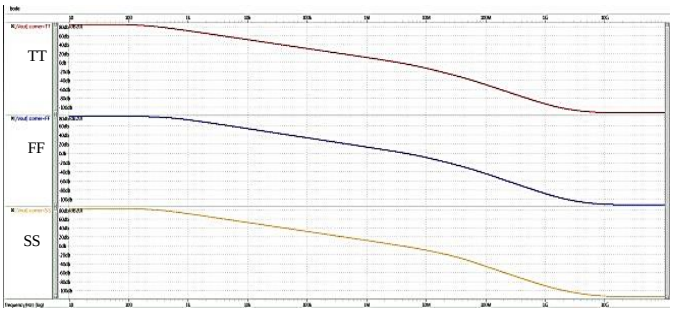

Fig. 10 DC Gain Analysis of Error Amplifier

The unity gain bandwidth, crucial for fast response times, measured 3.27 MHz, 4.37 MHz, and 3.65 MHz for the typical, fast, and slow corners, respectively. Additionally, the CMRR values were 92.80 dB, 87.55 dB, and 91.93 dB across the respective corners, indicating excellent noise rejection capabilities.

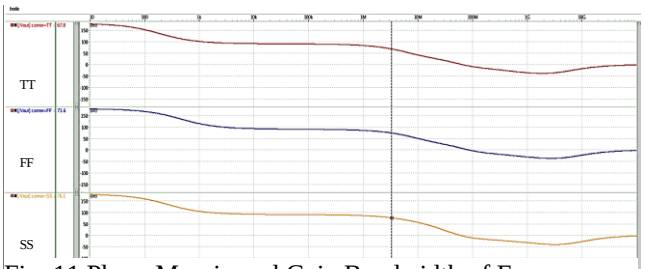

Fig. 11 Phase Margin and Gain Bandwidth of Error Amplifier

The graph shows the error amplifier's transient response, illustrating a high slew rate as the output voltage rises quickly with a rate of 251V/us. This indicates the amplifier's ability to rapidly respond to input changes, which is essential for applications requiring fast settling times and accurate signal tracking.

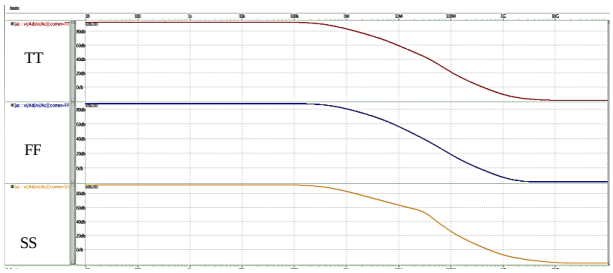

Fig. 12 CMRR of Error Amplifier

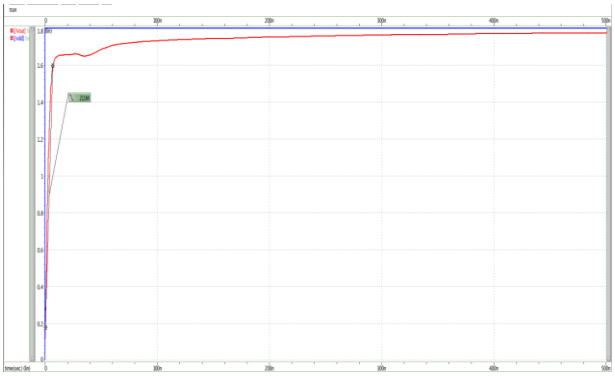

Fig. 13 Slew Rate of Error Amplifier

Table. 3 Summary Result of Error Amplifier

PARAMETERS	PROCESS CORNERS		
	TT (vdd = 1.8V, temp = 25°C)	**FF** (vdd = 1.98V, Temp = 0°C)	**SS** (vdd = 1.62V, Temp = 85°C)
Gain	85.37 dB	80.08 dB	83.24 dB
Phase Margin	71.6°	60.0°	76.5°
Unity Gain Bwth	3.27MHz	4.37MHz	3.65MHz
CMRR	92.80 dB	87.55 dB	91.93 dB

C. *Overall LDO Performance*

The overall performance of the LDO was assessed by evaluating key parameters such as dropout voltage, quiescent current, shutdown current, line regulation, load regulation, and PSRR.

The dropout voltage, which is the minimum difference between the input and output voltages for the LDO to maintain regulation, was measured under various conditions (Figure 14). The LDO maintained a dropout voltage of 300mV at the typical and fast corners, but it increased to 500mV at the slow corner due to the lower supply voltage and higher temperature conditions.

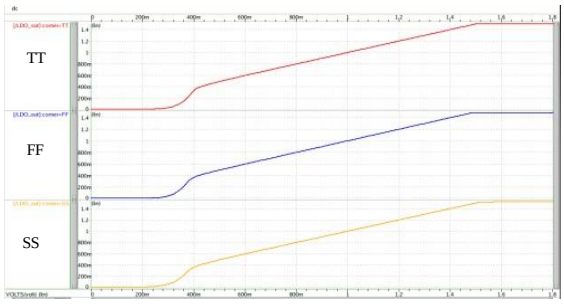

Fig. 14. Dropout Voltage of LDO.

Quiescent current (Figure 13), the current consumed by the LDO when it is in standby mode with no load, is a critical parameter for low-power applications. The LDO achieved a low quiescent current of 78.9µA at the typical corner, 82.3µA at the fast corner, and 86.6µA at the slow corner. These values indicate that the LDO design is highly efficient, consuming minimal power when not actively regulating a load.

D. *Shutdown Current*

The shutdown current (Figure 14), which is the current consumed when the LDO is in a disabled state, was also shutdown current of 30.1623nA at the typical corner, 213.64nA at the fast corner, and 3.0905µA at the slow corner. These low values ensure that the LDO does not significantly drain the battery when not in use.

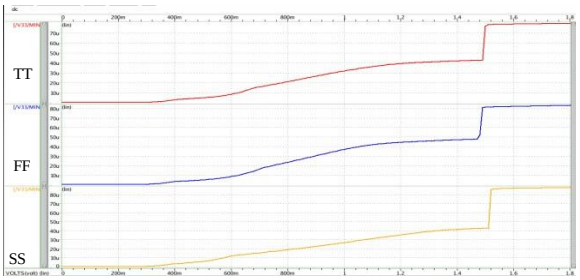

Fig. 15. Quiescent Current of LDO.

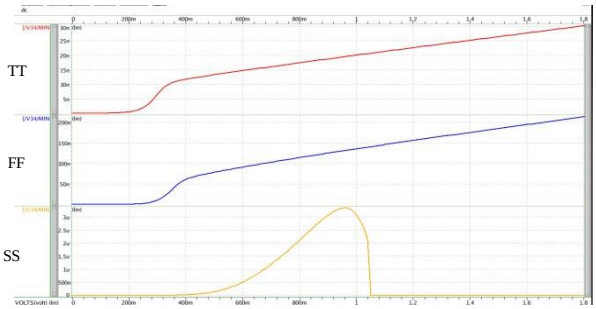

Fig. 16. Shutdown Current of LDO

E. *Line Regulation*

Line regulation measures the LDO's ability to maintain a constant output voltage despite variations in the input voltage (Figures -17-19). The LDO demonstrated excellent line regulation, with values of 0.00845mV/V, 0.00572mV/V, and 0.0148mV/V for the input voltage ranges of 1.62V to 1.8V across the typical, fast, and slow corners, respectively. For the input voltage range of 1.8V to 1.98V, the line regulation values were 0.00592mV/V, 0.0538mV/V, and 0.00879mV/V, respectively.

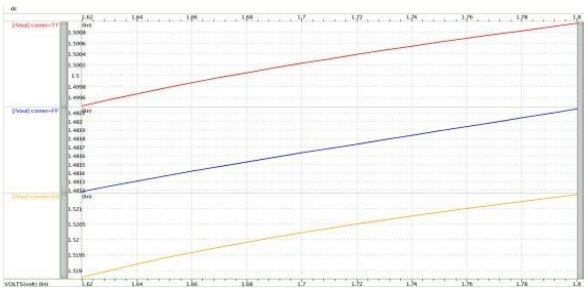
Fig. 19. LDO Line Regulation Input Voltage between 1.62V to 1.8V

Load regulation, the ability to maintain a constant output voltage as the load changes, was another critical parameter evaluated. The LDO achieved load regulation values of 0.04921mV/mA, 0.08425mV/mA, and 0.06856mV/mA for the load range of 0A to 1mA across the typical, fast, and slow corners, respectively. These results indicate that the LDO can effectively regulate the output voltage even as the load varies.

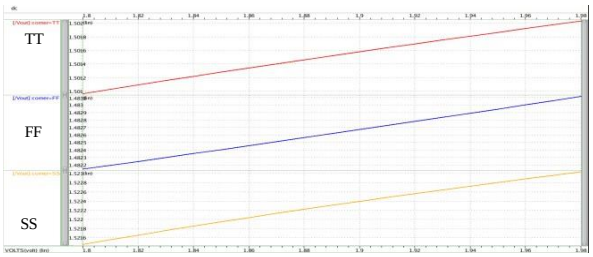

Fig. 18 LDO Line Regulation Input Voltage between 1.8V to 1.98V

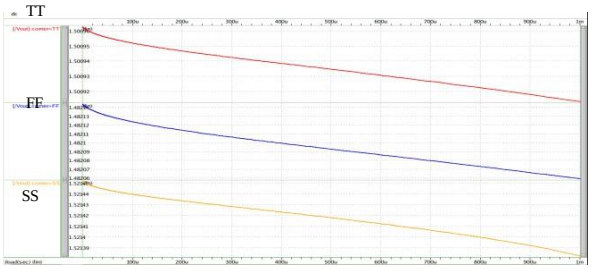

Fig. 19. LDO Load Regulation Waveform Result from 0A to 1mA.

F. *Power Supply Rejection Ratio (PSRR)*

PSRR is a measure of the LDO's ability to reject changes in the input voltage and maintain a stable output voltage. The LDO exhibited high PSRR values, measuring -61dB, -62dB, and -57dB at the typical, fast, and slow corners, respectively, at a frequency of 100kHz (Figure 18). These high PSRR values indicate that the LDO can effectively filter out noise from the input power supply, ensuring a clean and stable output voltage.

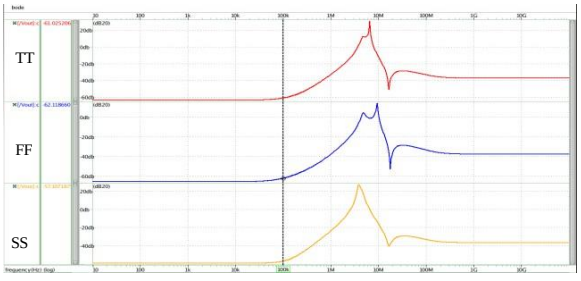

Fig. 20. LDO PSRR Result.

G. *Power Gating*

Power gating is a technique used to reduce power consumption by turning off specific circuit blocks when they are not in use. The LDO implemented power gating effectively, resulting in a significantly reduced power consumption of 54.6327nW in the disabled state. This feature is particularly beneficial for portable devices, as it helps extend battery life by minimizing power usage during idle periods.

H. *Summary of LDO Performance*

The LDO's performance was compared to previously reported LDO designs, highlighting its superior efficiency and stability. Table IV summarizes the key performance parameters of the proposed LDO across different process corners and compares them with desired values and previously reported designs.

Table.4 Results of the LDO Performance for Difference Corner Analyses

PARAMETERS V = Voltage; I = Current	**DESIRED VALUE**	**PROCESS CORNERS TT (vdd = 1.8V, temp = 25°C)**	**FF (vdd = 1.98V, temp =0°C)**	**SS (vdd = 1.62V, temp = 85°C)**
Output V	1.50V	1.50V	1.48V	1.52V
Dropout Voltage	300mV	300mV	500mV	100mV
Quiescent I	<100µA	78.9µA	82.3µA	86.6µA
Shutdown I	<5µA	30.1623 349 nA	213.642811 nA	3.09054951 nA
Line Regulation (1.62V to 1.8V)	<2mV/V	0.008 mV/V	0.00572 mV/V	0.0148 mV/V
Line Regulation (1.8V to 1.98V)	<2 mV/V	0.00592 *mV /V*	0.0538 *mV/V*	0.00879 *mV/V*
Load Regulation (0A to 1mA)	<1 mV/mA	0.04921 *mV/mA*	0.08425 *mV/mA*	0.06856 *mV/mA*
PSRR	*-60.00 dB @ 100kHz*	*−61.0 dB*	*−62.1 dB*	*−57.1 dB*
Power Consumption at Normal State	<2 mW	349.7070 µW	349.7070 µW	349.7070 µW
Power Consumption at Disabled State	-	54.6327 nW	54.6327 nW	54.6327 nW

Table.5 Performance Comparison with Previously Reported LDO Design

PARAMETERS	[11]	[12]	[13]	[14]	[15]	**THIS WORK**
CMOS Process	CMOS 40nm	CMOS 180nm	CMOS 350nm	CMOS 180nm	CMOS 40nm	CMOS 180nm
Supply Voltage	1.09 V	1.1 V	3.0 V	1.8 V	1.1 V	1.8 V
Dropout Voltage	0.21	0.2	0.2 V	0.2 V	0.2 V	0.3 V
Quiescent Current	76 µA	65 µA	65 µA	55 µA	57 µA	78.9 µA
Shutdown Current	-	-	-	-	-	30.162334 9 nA
Line Regulation (mV/V)	0.6 mV/V	0.857 mV/mA	4.1 mV/V	3.9 mV/V	0.5 mV/V	0.00845 *mV/V*
Load Regulation (mV/mA)	0.015 V/mA	0.2 mV/mA	4 mV/mA	7 mV/mA	3.89 mV/m A	0.04921 *mV/mA*
PSRR @100kHz	-70 dB	-68 dB	-26 dB	-50 dB	-35 dB	−61.0 *dB*
On-chip Capacitor	1 µF (Off-chip	1 µF (Off-chip	100 pF (On-chip)	100 pF (On-chip)	50 pF (On-chip)	10 pF
Power Consumption at Normal State	23 mW	20 mW	10 mW	10 mW	20 mW	349.70 µW
Power Consumption at Disabled State	-	-	-	-	-	54.63 nW

Table IV demonstrated that this LDO has excellent line regulation values of 0.00845mV/V, 0.00572mV/V, and 0.0148mV/V for the input voltage ranges of 1.62V to 1.8V across the typical, fast, and slow corners, respectively. Load regulation values were 0.04921mV/mA, 0.08425mV/mA, and 0.06856mV/mA for the load range of 0A to 1mA across the respective corners. These results indicate that the LDO can effectively regulate the output voltage under varying conditions.

The proposed capacitorless LDO regulator designed in 180nm CMOS technology demonstrates excellent performance across various parameters. The design achieves low quiescent current, near-zero shutdown current, excellent line and load regulation, and high PSRR, making it a highly efficient and stable solution for system-on-chip applications.

Compared to the other architectures, as shown in Table V, the designed LDO exhibits a better result for the parameters except for the quiescent current. Since the

designed LDO uses a constant current reference, it caused a slight increase in the quiescent current compared to an ideal biasing circuit. However, the constant current reference is less sensitive to process and temperature variations than the ideal biasing circuit. The designed LDO is the only architecture that measures the shutdown current since power gating is implemented in the system. The related architectures were designed with a fixed bias current that was always present even when it was in shutdown mode, it was not well-documented because the fixed bias current is much greater than the shutdown current. However, since minimizing power consumption has become important, shutdown current needs to be measured and optimized.

4. CONCLUSION

This study presents the design and validation of a capacitorless low-dropout regulator (LDO) using 180nm CMOS technology, specifically tailored for system-on-chip (SoC) applications. The primary objectives were to achieve low power consumption, high power supply rejection ratio (PSRR), and stability without relying on external capacitors. By adopting a systematic methodological framework, we successfully addressed the challenges associated with capacitorless LDO designs.

The key components of the LDO, including the bandgap voltage reference (BGR), startup circuit, error amplifier, and power core, were meticulously designed and simulated. The BGR provided a stable reference voltage under varying conditions, while the startup circuit ensured rapid stabilization. The error amplifier delivered high gain and wide bandwidth, essential for precise voltage regulation. The power core, incorporating a PMOS pass transistor, feedback resistors, Miller compensation, and an on-chip capacitor, maintained stability and improved line and load regulation. Additionally, the implementation of power gating significantly reduced power consumption during idle periods.

Extensive simulations of the integrated LDO system demonstrated excellent performance across various metrics. The LDO achieved a low quiescent current of 78.9μA, near-zero shutdown current, and excellent line and load regulation. The PSRR was measured at -61dB at 100kHz, indicating high noise rejection capability. The power gating feature effectively minimized power usage during idle periods, making the LDO highly efficient for portable applications.

The proposed capacitorless LDO design meets the stringent requirements for modern SoC applications. The successful integration of advanced techniques, such as Miller compensation and power gating, ensures high performance and efficiency. This work not only addresses the limitations of conventional LDOs but also sets a foundation for future research in capacitorless LDO designs. Further exploration of additional compensation techniques and noise-immune architectures could enhance the performance and applicability of these regulators in various electronic devices, paving the way for more compact and efficient power management solutions.

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