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A Multilevel Supply Modulator for RF Power Amplifier using 130nm CMOS Technology: Comparator Based Approach

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Abstract: Energy-efficient power amplifiers (PAs) that preserve battery life for extended periods of time, without sacrificing linearity are becoming increasingly important for mobile devices. The supply modulator in the envelope tracking (ET) design affects the efficiency enhancement in radio frequency (RF) PAs. This paper presents design of a comparator-based supply modulator that dynamically controls the supply voltage required to drive the PA. A preamplifier has been designed to amplify the RF input signal and an envelope detector tracks the amplified signal within the comparator's swing of 0 - 3.3 V. A single-bit comparator has been designed that works at 2.1 GHz frequency with a minimal rise-time delay of 0.2 ns and it is cascaded to operate as an 8-bit comparator. The multilevel supply modulator receives the input from the 8-bit comparator. This determines the amount of current flow to the PA by limiting current flow through the transistors that are turned OFF by the comparator. Hence the comparator based envelope tracking system is aimed at designing the ET circuit and improving the power added efficiency to approximately 45% Moreover the ET circuit does not comprise of bulky components like the inductors, thus expected to consume lesser chip area.

Keywords: Radio Frequency Power Amplifier; 5G mobile communication; 130nm CMOS; eight-bit comparator; envelope tracking; multilevel supply-modulator; linearity; efficiency

1. Introduction

Modern technology electronic circuits have shrunk in size during the past century, but their power density has grown dramatically as the industry shifted toward digitization and miniaturization. In modern electronic industry, designing an effective thermal management system to transfer heat away from the electronic chips becomes crucial [1)]. High battery power consumption has been a major concern apart from low quality signals when using data services in mobile technology. The reason for high battery power consumption at specified output power level is due to poor efficiency of power amplifier in the mobile transceiver, which dissipates a major portion of the power drawn from the battery in the form of heat and goes unutilized. It has therefore become necessary to reduce power dissipation by controlling the power drawn by the transceiver circuit in the mobile phones. Mobile communication has gained a great momentum since the 80's and has been evolving itself in decades. The use of mobile phones and internet has increased rapidly in the past two to three years in India [2)] , thus looking into implementing 5G has become a need to maintain the requirement of the consumers. Mobile technology has evolved from using analog technology (1G) in the 80's to successive usage of digital technology (2G, 3G, 4G and 5G) supporting additional features[3)]. The vast opportunities for optimization and efficiency gains will be the next area of study for widely used smart devices and a variety of applications in 5G networks [4)]. Therefore to stay active in the market, data service providers have to ensure high signal strength and the mobile companies have to take care of the high power consumption without compromising on the features provided by them like usage of social networking, video streaming, web browsing, music downloads, and many more to attract market. Long Term Evolution (LTE), which is the actual 4G used technologies like orthogonal frequency division multiplexing (OFDM), multiple input multiple output (MIMO), adaptive beam-foaming antennas that help reducing network congestion [5)].

Linearity of the transmitter is compromised upon due to the high peak to average power ratio (PAPR) due to which the PA is forced to work in the back-off region resulting in high power consumption [6)]. This has led to research in the areas of efficient power enhancement techniques in the power back-off region. In the work depicted in [7)] the supply

voltage was varied using DC – DC converter to modulate the supply voltage to the RF power amplifier (PA) and showed that the efficiency of the RF PA can be improved effectively. Power amplification is the final stage in the transceiver block which deals with high power level signals for transmission [8] and dissipates about 50% [9] of the total power, hence reducing the power efficiency and in turn the battery life. The performance of a power amplifier is characterized by the output power and gain without compromising on the linearity and efficiency. Studies have revealed that envelope tracking [6] [10] is a reliable method to improve the efficiency of the power amplifier, where the principle adopted is "tracking the RF signal voltage and modulating the supply voltage according to the signal power" as shown in Fig. 1. The envelope tracking further operate a supply modulator circuit which is responsible to dynamically control the current to the power amplifier and in this way the power efficiency is improved.

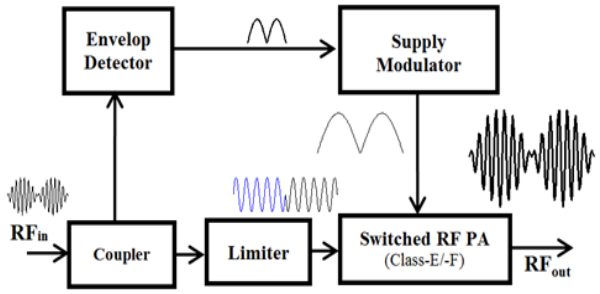

Fig. 1: Conventional ET system

Two primary considerations in any circuit design, whether digital or analog, are power efficiency and speed [11] [12]. The most effective strategies to obtain low power are to lower the supply voltage (V_{DD}) and have all chip components function in the subthreshold zone [13] CMOS transistors have been considered as most reliable in the design of high performance IC such as transceivers, analog to digital converters, memories etc.[14]. With the advent of 4G and moving towards 5G, there is an involvement of complex modulation methods like CDMA, OFDM etc. The RF transmitter has been becoming more and more complex while moving from 3G to 5G and future generation communication system which requires further miniaturization of transceivers, high data rates, high modulation bandwidth etc. [6]. In analog design scaling of transistors cannot be done abruptly, as intrinsic circuit capacitances and interconnect parasitic capacitances play a major role in reducing the speed and bandwidth of analog circuits [15].

A wide bandwidth hybrid supply modulator for LTE-A application was designed by [16], using 0.18 µm CMOS technology, which tracks the envelope at a speed of 100MHz and also controls the bandwidth at low bandwidth envelope region. Since the modulator controls the power loss in the PA, the overall efficiency of the ET PA is the product of the RF power amplifier efficiency and the modulator efficiency. In the architectures [17] [18], the switching transistor, employed as the power modulator has higher switching losses resulting in decreased overall efficiency. A review conducted by [17] on various architectures integrated with Pas indicate that ET is preferable over EER or the Doherty methods when used in linear mode and 5G technologies, due to the wide intermediate frequency requirements. Moreover, when the RF amplifier is operated near the maximum output power region, the output power is more sensitive to drain bias; and any noise developed by the supply modulator at the drain of the RF power amplifier, possibly fall into the receiver band [19], which requires a low noise supply modulator design. Recently work done by [20] used a modulated rapid load pull system which showed good linearity, but with reduced efficiency.

.The focus in this work is the design of a comparator based supply modulator. The emphasis lies in the concept of turning only appropriate number of transistors ON to control the current flowing through the load

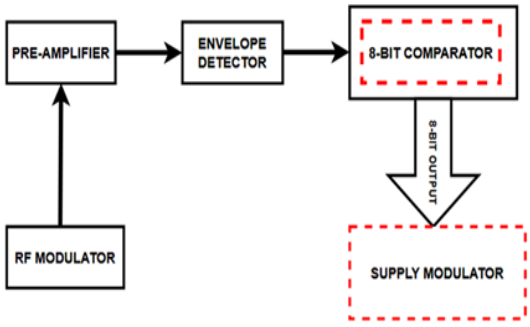

Fig. 2: Block Diagram of proposed system

The proposed design as shown in Fig. 2 is suitable for implementation in a conventional radio frequency integrated circuit (RFIC) design flow using CADENCE platform.

2. Methodology

For supply modulation in PA architecture, two well-known techniques have been found in the literature, namely envelope elimination and restoring (EE&R) and envelope tracking (ET). The EE&R works better on constant amplitude non-linear PAs with dynamically controlled supply voltage. The ET is preferable for the linear Pas whose poor power efficiency especially at low power levels can be mitigated by applying the supply voltage accordingly [21]. The main challenges that have to be overcome for an ET circuit are:

- A high efficiency supply modulator has to be designed

- Has to consider the fact that the efficiency at lower envelope voltage is low in comparison to high envelope voltage due to its inability to compress the low power region.
- Minor distortion in the supply modulator will be modulated on to the output of the RF PA. Hence the supply modulator has to be designed with high precision.

In essence, an ET circuit is made up of a PA circuit and a bias modulator. The supply modulator is in charge of dynamically regulating the bias voltage applied to the PA. In order to keep up with the rapid variations in voltage levels, the supply modulator needs to be extremely effective and quick. Simultaneously, the switching frequency must be kept constant to accommodate the signal's instantaneous variations in voltage level. Furthermore, it is also important to keep in view that the change in supply voltage is appropriate with the transistor operating conditions [18]. Ensuring compliance with all of these is also essential to guarantee that the PA's linearity is not compromised.

The proposed system in Fig. 2 shows that the input RF signal is amplified by a preamplifier circuit to make it compatible with the comparator circuit which is designed to compare voltage levels from 0-3.3V. This signal is then passed through an envelope detector circuit which captures the voltage level of the signal from the preamplifier, thus forming an envelope over the bandwidth of the RF signal. The amplitude of the envelope is compared by a high speed 8-bit comparator that turns on individual output bits based on the input amplitude of the envelope. The 8 output bits of the 8-bit comparator controls the bias conditions of the transistorized supply modulator circuit. The supply modulator circuit controls the current flowing into the PA circuit, thus reducing the power loss by reducing the DC input power to the PA prior to being consumed.

2.1 Preamplifier and envelope detector circuit

It was noticed that when the input RF signal of the range from -20 dBm to 10 dBm was applied to the envelope detector circuit, its output was not sufficient enough to be compared with the reference voltage levels of the – 8-bit comparator circuit. The comparator operates at the reference voltage range from 0 V to 3.3 V. Therefore, a single stage Cascode Class AB amplifier as shown in Fig.3 has been designed to amplify the input RF signal into the desired range from 0 V to 3.3 V.

The purpose of using an envelope detector is to lock the signal voltage by continuously monitoring RF signal voltage fluctuations. Envelope shaping is seen to be a crucial component for increasing linearity and efficiency while reducing the load on the supply modulator. [22] Envelope detectors designed in [19) 23)] have emphasized on maintaining the supply voltage greater than the knee voltage in order to avoid nonlinearities in the PA characteristics. The envelope detector designed in this work comprises of a diode acting as a rectifier and a resistor-capacitor combination acting as a filter.

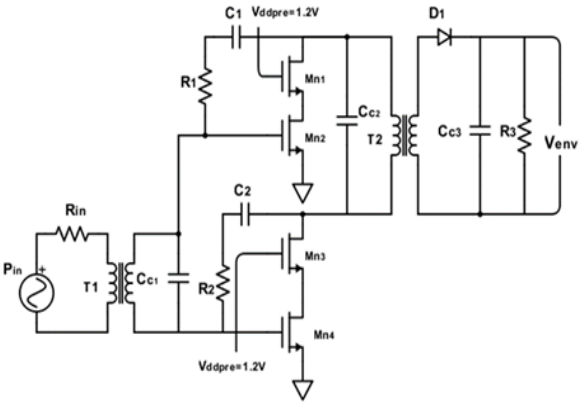

Fig. 3: Pre-amplifier and Envelope Detector

The envelope detector designed can track the input RF signal up to the modulation bandwidth of 40MHz and is much above the suggested bandwidth of the LTE signal. The diode acts as a rectifier which allows positive signals to pass through it and the conduction has been optimized for 0 V to 3.3 V by adjusting the device area to 200 μm^2 (square micrometers) with a W/L ratio of 100 µm by 2 µm for the diode.

The resistor and capacitor which contributes to the RC time constant is adjusted so that the capacitor discharges slowly. The W/L ratio for both the components has been adjusted to obtain a resistance of 258Ω and a capacitance of 40pF respectively.

2.2 Single bit high speed comparator

Analog comparators act as checkers which are basically cascaded inverters followed by latches [24). 25)] proposed an analog comparator which uses as many as 24 transistors resulting in device degradation and transient faults leading to large circuit size.

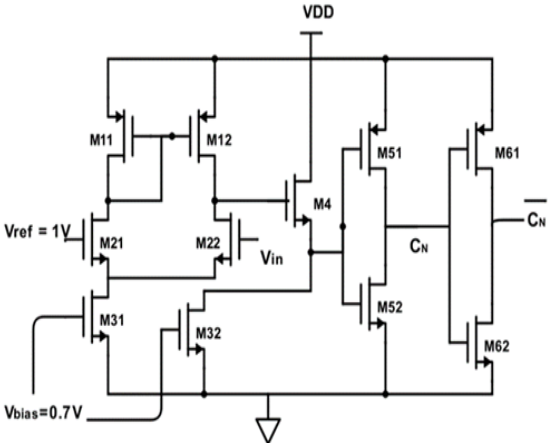

Fig. 4: Single-bit comparator

In this work, a comparator design using as low as 7 transistors is proposed as shown in Fig.4, in a 130 nm CMOS technology providing smaller sized foot print, and still yielding compatible results. The comparator output is followed by two inverters to provide inverted and buffered output needed for the supply modulator circuit. The comparator compares the envelope signal input (V_{env}) (represented as V_{in} in the Fig.4) with the pre-determined reference voltage (V_{ref}) which is equal to 1V. If V_{env} is greater than V_{ref}, the comparator circuit goes to saturation thus producing an output which is `1', or else the output is `0'The reference value is finalised as 1V by varying the operating frequencies upto 100 MHz.

For comparator design, the permissible delay for the rise time is 10% of the total time. The RF signal for LTE modulation has a maximum bandwidth of 40 MHz; giving 2.5 ns delay time with 25 ns total time. The work in [26] confirms that propagation delay of up to 10 ns is acceptable for RF communication applications at high frequencies..

2.3 8-bit comparator circuit

The 8-bit comparator circuit comprises of 8 single-bit comparator circuits cascaded together as shown in Fig. 5. It was noticed that the value of V_{ref} in the single bit comparator affected the output adversely in a way that when it was increased beyond 2.7V the maximum output saturation voltage started reducing. Hence the reference voltage for the cascaded 8-bit comparator is set to 2.7V which is divided by a potential divider circuit to provide 8 levels of reference voltages to the individual comparator. The output of the envelope detector (V_{env}) is applied as the input to the comparator. We will compare the input, which is the output signal from the envelope detector circuit, to the reference voltage at each comparator block. The comparator outputs are saturated to 3.3 V, logic "1" is produced for all of the outputs where the reference signal is greater than or equal to the envelope signal value. These are the inputs that the supply modulator receives.

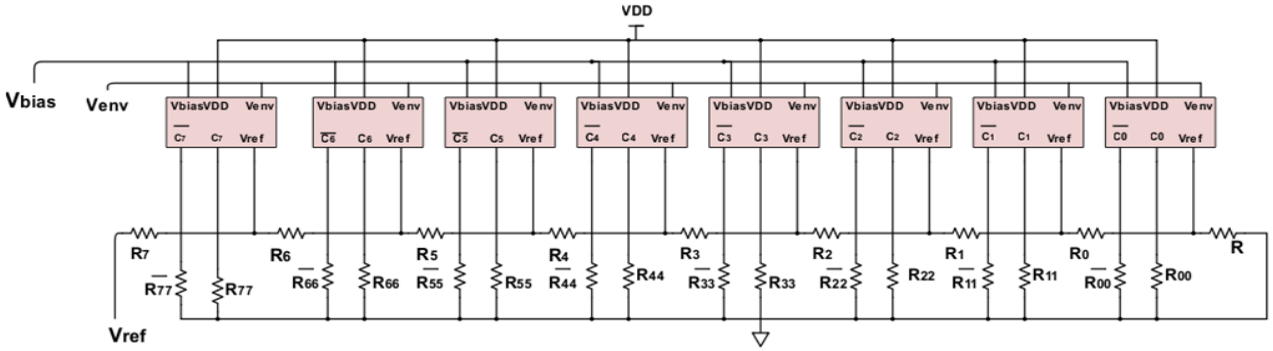

Fig 5: 8 - bit comparator circuit

2.4 Supply modulator

In ET PA circuits, supply modulator design is regarded as a key technique. Supply modulators can be classified as linear and discrete. Linear modulators which are designed as Class AB/B and Class G/H amplifiers requires differential input excitation and very good symmetry both in matching circuits and active devices. Discrete modulators, on the other hand can use pulse width modulation techniques. Multilevel discrete supply modulators are based on multiple switching levels and is advantageous for ET circuits due to high efficiency and high bandwidth tracking [27].

The supply modulator circuit design comprises of two arrays of 8 NMOS transistors as shown in Fig. 6. The uncomplemented and complemented outputs from the – 8-bit comparator circuit serve as inputs to the transistors. The output is measured across a tank circuit comprising of a resistor (R_L) and a capacitor (C_L). By this arrangement of the transistors discrete levels of voltage are obtained at the output. The output signal strength is determined by the number of transistors that are ON at a particular instant of time.

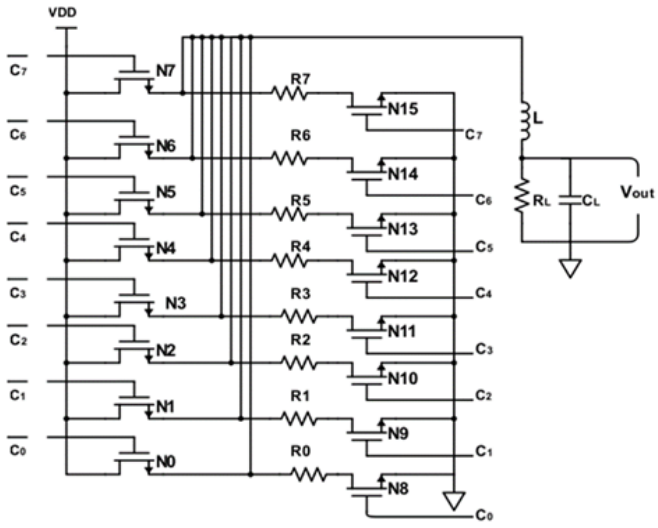

Fig 6: Supply modulator circuit

Table 1: Device sizes and values

Device	Preamplifier	Envelope Detector	Comparator	Supply modulator
Transistor	Mn1, Mn3 (W = 120µm, L= 130nm		M11, M12. M51, M61 (W = 5µm, L = 130nm	N0 -N15 (W = 1µm, L = 130nm)
	Mn2, Mn4 (W = 120µm, L = 130nm)		M21, M22, M31, M32, M52, M62 , M4 (W= 2.5µm, L= 130nm)	
Resistor	R1, R2 = 1KΩ	280Ω		R_L = 10Ω
Capacitor	C1, C2 = 2 pF, Cc1= 1pF, Cc2 = 0.64pF	40pF		C_L = 1pF
Diode		W = 100µm , L = 2µm		
Inductor				L = 190pH

3. Results and discussion

Varying voltage levels and sources (AC/DC) are needed for different power utilities to function. Because switching and conduction losses in components lose a significant amount of power, an alternative method is required [1]. The whole idea of carrying out this work has been aimed at designing a supply modulator that would dynamically control the current flowing into the PA circuit. As expected the supply modulator has been designed using an 8-bit comparator approach.

3.1 Preamplifier and envelope detector

An Amplitude Modulated RF signal has been provided at the input of the preamplifier. The input signal strength was varied from -12 dBm to 6 dBm (105 mv to 765 mV approx.). It was noticed that the signal strength increased from 1.4 V to 5.1 V peak for the corresponding signal inputs as shown in Table 2.

Table 2: Preamplifier and Envelope detector

P_{in} (dBm)	V_{in} (mv)	$V_{(pre)}$ (V)	V_{env} (V)
-12	105	1.4	0.8
-10	175	2.3	1.25
-8	205	2.6	1.5
-6	276	3.1	1.75
-4	336	3.4	2
0	395	3.8	2.37
4	595	4.6	2.9
6	765	5.1	3.2

The envelope detector circuit is used to process the pre-amplifier's output. For every value of the input RF signal the output of the envelope detector is measured. The observations are recorded in Table 1 and the two waveforms for minimum value and maximum value of the input signals can be viewed in the Fig. 7. As observed the output voltage of the envelop detector exactly follows the input signal voltage. In Fig. 7 (a) and (b), it can be noticed that for the input power, Pin = -12 dBm, the envelope voltage is 0.8 V and for Pin = 6dBm the envelope voltage is 3.2 V, and so it is for the intermediate readings

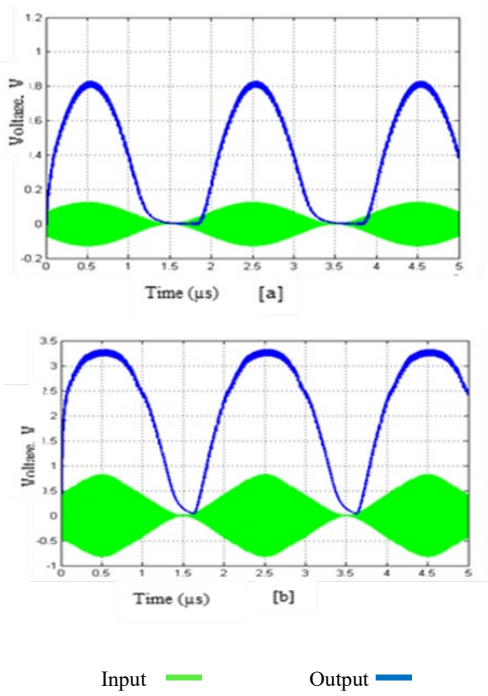

Fig. 7: RF input and envelope output for (a) Pin = -12 dBm (b) Pin = 6 dBm

The linearity graph in Fig. 8. shows that the output voltage of the envelope detector (V_{env}) circuit varies almost linearly with the input signal power (P_{in}). This is a basic requirement to ensure that the supply modulator and the PA outputs are linear, thus improving the efficiency of the PA. The green dash line graph indicates the expected linear plot and the red line plot with blue dots indicate the output plot obtained from the envelope detector circuit and the two plots almost overlap each other

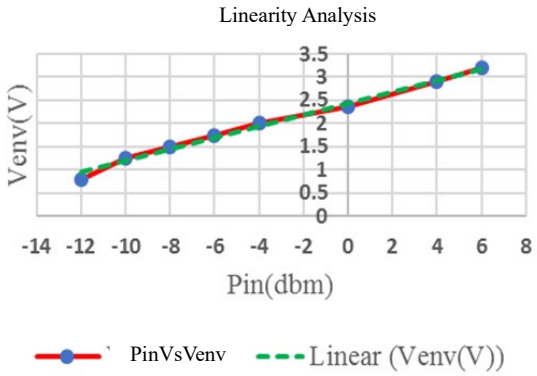

Fig. 8: Linearity graph for the envelope detector

3.2 Single bit comparator results

The reference voltage determines how wide the pulses produced by the single-bit comparator circuit are. 1 volt is the fixed reference voltage. Figure 9 shows that the comparator output saturates at the reference voltage with a delay as short as 0.2 ns. The time it reaches saturation is 1.079 ns, and the time measured at the reference voltage of 1 V is 0.838 ns. In response to variations in the RF signal's input signal power, the delay is thus roughly 0.2 ns, demonstrating a very rapid switching speed with a very minimal delay. The comparator's efficacy is confirmed for frequencies up to 2.1 GHz, and it has been noticed that the switching delay is less than 10ns. performance for ET application. The switching speed of the comparator in this design is very high, with a rise time delay approximately 0.2 ns and thus is found suitable for the intended envelop tracking design.

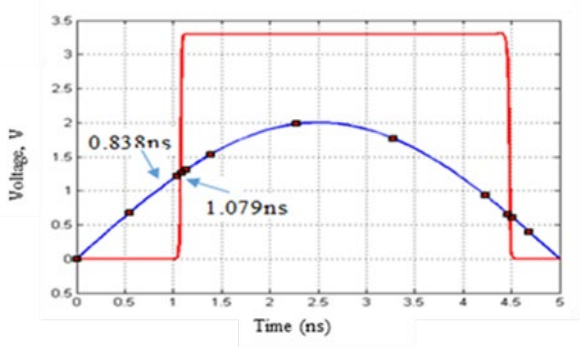

Fig. 9: Single bit comparator propagation delay

3.3 8-bit comparator results

The 8-bit comparator circuit was tested by applying input signals with signal power varying from -12 dBm to 6 dBm. As the signal strength increases, more number of comparators tend to turn ON, until all the comparator outputs are ON, indicating maximum signal strength. It has been noticed from the graphs in Fig. 10 that for an input signal voltage as low as 100 mV only one comparator output is ON and for the input signal approximately equal to 765mV all the comparators turn ON.

Table 3 shows the outputs as the input signal strength varies from approximately 100 mV to 800 mV. The plot in Fig. 10 reflects the condition when all the comparator's outputs are ON for the maximum input signal of 765 mv (≈ 6 dBm recorded from the CADENCE).

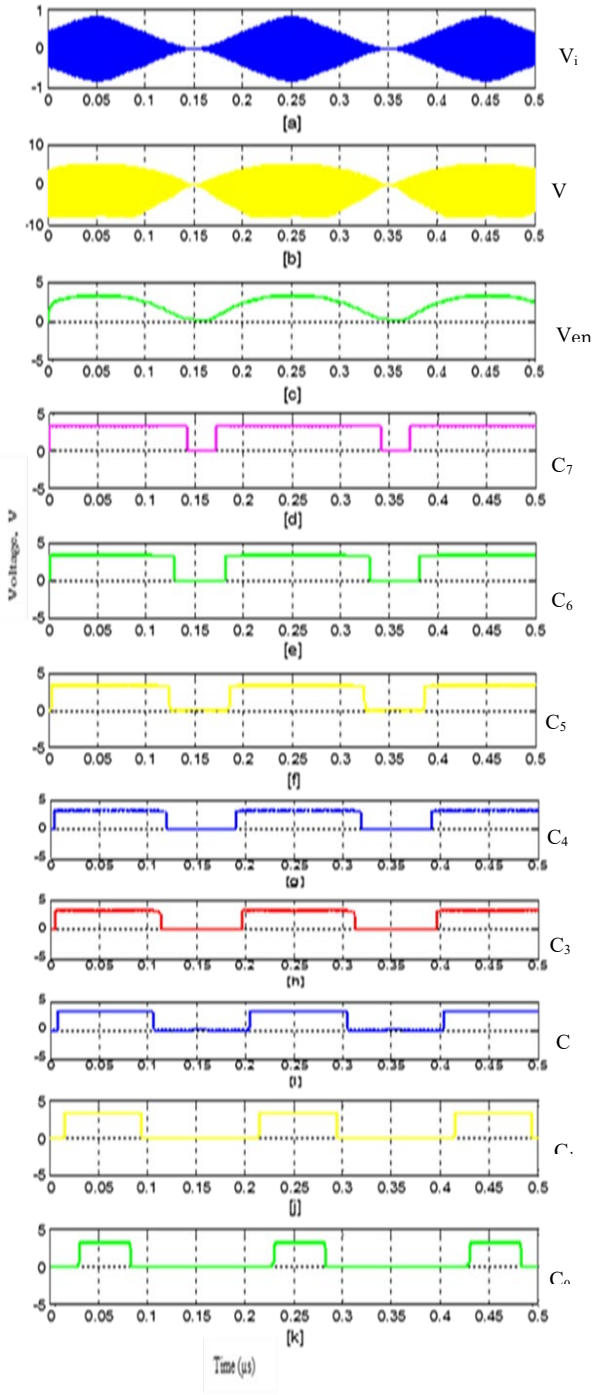

Fig. 10: 8 - bit comparator outputs for Pin = 6 dBm (a) input RF signal; (b) preamplifier output; (c) envelope detector output (d) - (k) 8-bit comparator outputs C0 through C7

Table 3: Comparator output for varying input voltage

Pin (dBm)	Vin (mv)	V(pre) (V)	Venv (V)	Comparator output							
				C0	C1	C2	C3	C4	C5	C6	C7
-12	105	1.4	0.8	1	0	0	0	0	0	0	0
-10	175	2.3	1.2	1	1	0	0	0	0	0	0
-8	205	2.6	1.5	1	1	1	0	0	0	0	0
-6	276	3.1	1.7	1	1	1	1	0	0	0	0
-4	336	3.4	2	1	1	1	1	1	0	0	0
0	395	3.8	2.3	1	1	1	1	1	1	0	0
4	595	4.6	2.9	1	1	1	1	1	1	1	0
6	765	5.1	3.2	1	1	1	1	1	1	1	1

3.4 Results from the Supply modulator

All the outputs from the 8-bit comparator are fed to the input of the supply modulator as shown in Fig. 6. After performing the simulation, the required input and output waveforms are selected from the Cadence Virtuoso simulation window for every value of the input signal. These selected waveforms are extracted in the .csv form from cadence and further processed in the MATLAB to generate the waveforms as shown in Fig. 11.

From Fig. 11 (a) it is noted that for an input equal to -8dBm (205mV), there are only two steps indicating that only two transistors are ON and the maximum output voltage is 1.72V as also recorded in Table 3. Similarly, in the subsequent Figures (b) and (c) it has been noticed that as the input voltage increases the number of steps in the output signal increases indicating the number of transistors that are active at that value of input power. It can also be noted that at ascending levels of input power the output voltage at the supply modulator also increases from 1.05V to 3.2V which is an indication of dynamic supply voltage that has been obtained.

In Table 3 the value of the output voltage corresponding to the input voltage has been recorded. The output voltage (V_{out}) gradually increases with increase in input voltage (V_{in}). It is clear that only the transistors that get the active signal from the comparator are activated, and that the supply modulator's output determines the voltage applied to the PA. As the equivalent input voltage rises, it has been observed that the output power increases steadily. The input voltage displayed in Table 3 and Fig. 12 is derived from the waveforms acquired by CADENCE analysis.

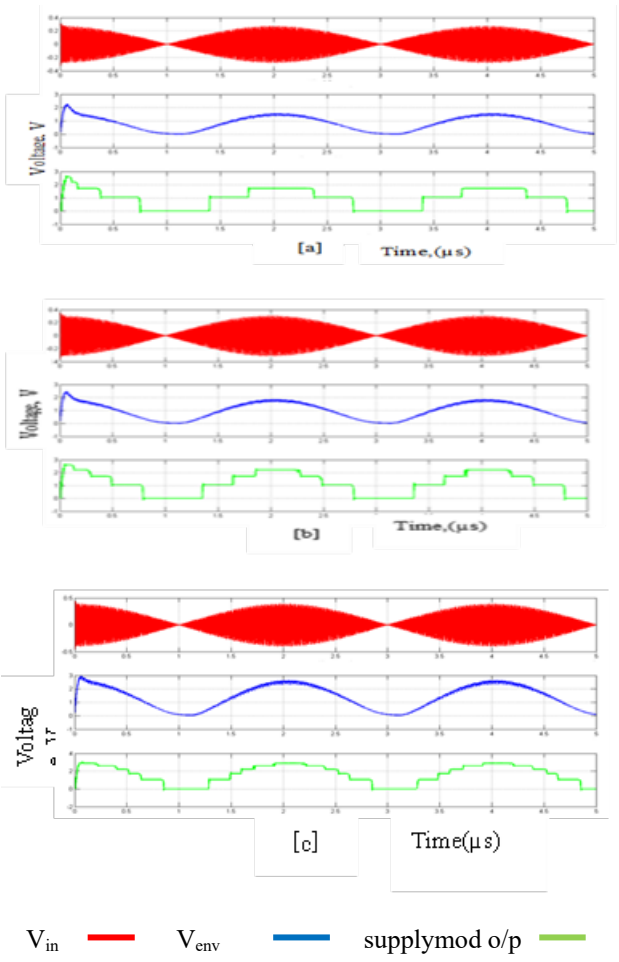

Fig. 11: Supply modulator results for : (a) Pin=-8dBm (b) Pin=-7dBm (c) Pin=-5dBm

Table 4: Supply modulator results

V_{DD} = 3.3 V					
P_{in} (dBm)	V_{in} (mv)	$V_{(pre)}$ (V)	V_{env} (V)	Steps	V_{out} (V)
-10	175	2.3	1	1	1.05
-8	205	2.6	1.5	2	1.72
-7	237	2.9	1.6	3	2.21
-6	276	3.1	1.75	4	2.5
-5	330	3.4	2.3	5	2.8
-4	336	3.4	3	6	3
-3	395	4	3.3	7	3.1
-2	412	5.3	3.6	8	3.2

A graph is obtained by plotting the values of the input power to the output voltage of the supply modulator, using Excel and the values recorded from the results which are tabulated in Table 3. The outputs seem to be following the reference linearity plot as can be seen in Fig. 12. the The output voltage varies linearly and in proportion to the input power (Pin). The green dotted line in the plot in Fig. 12 is the linearity analysis plot from Excel which indicates if the

inputs and outputs are linear in their responses. The plot of the input power to the preamplifier to the output voltage at the supply modulator almost coincide with each other which is a clear indication of linearity of the circuits involved.

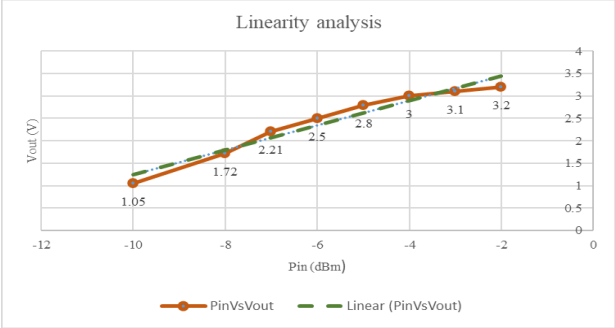

Fig. 12: Linearity Graph for supply modulator

3.5 Results from PA with dynamic supply

The output from the supply modulator was provided as V_{DD} to the PA. For experimental purpose the preamplifier circuit itself was used as the PA. The results were obtained for fixed supply voltage and dynamic supply voltage. This was done in order to obtain the power added efficiency (PAE) which is calculated as shown in equation 1 for the dynamic PA supply. For the fixed DC supply voltage biased PA the denominator is the P_{dcPA} alone.

$$PAE = {P_{out} - P_{in}}/{P_{dcPA} - P_{dc}} \qquad \text{equ 1}$$

where,

P_{out} is the power obtained at the output of PA

P_{in} is the RF input power

$P_{dcPA} - P_{dc}$ is the difference in the power with varying supply voltages (referred as Pdc (dynamic) in Table 5.

This has been calculated after each iteration using the calculator function in the Cadence Virtuoso. It can be noticed in Table 5 that the PAE of the dynamically controlled PA is comparatively higher than the one using fixed VDD. The PAE is approximately 45% which is higher than the fixed biased PA by approximately 10%. It is also noticed that depending on the number of comparators that are turned ON, the dynamic input DC power also increases. The PA performs linearly upto 6dBm and then saturates.

Table 5: Comparative analysis for fixed and dynamic PA

V_{DD} = 3.3 V									
P_{in} (dBm)	P_{in} (mW)	P_{out} (fixed) (W)	P_{out} (dynamic) (W)	P_{dc} (fixed Vdd) (W)	P_{dc} (dynamic) (W)	PAE (fixed) (%)	PAE (dynamic) (%)	Comp. ON	Output (S/L)
-10	0.1	68.5m	19.12m	2.027	711.9m	3.3	2.6	1	L
-8	0.158	99.1m	39.41m	2.028	782.6m	4.8	5	2	L
-6	0.25	118.4m	72.22m	2.028	856.9m	5.8	8.3	3	L
-5	0.3	141.1m	93.17m	2.028	894.3m	6.9	10.41	4	L
-4	0.4	167.6m	123.4m	2.028	959.7m	8.2	12.81	5	L
-3	0.5	198.6m	151.6m	2.027	995.3m	9.7	15.23	6	L
-2	0.63	234.8m	189.9m	2.027	1.052	11.56	17.9	7	L
0	1	323.5m	259.3m	2.027	1.103	16.03	23.41	8	L
2	1,59	478.9m	354.3m	2.027	1.185	23.06	29.7	8	L
4	2.5	523m	438.2m	2.027	1.247	26.96	34.9	8	L
6	3.98	556m	516.5m	2.025	1.32	27.2	38.8	8	L
8	6.3	643m	590.7m	2.021	1.373	31.5	42.5	8	S
10	10	694.5m	663m	2.011	1.464	34.03	44.6	8	S
S- PA goes into Saturation L – PA remains Linear									
Comp. ON indicates the number of comparators in ON state									
Fixed refers to Fixed V_{DD} and dynamic refers to results after supply has been modulated									

Table 6: Comparison with previous work

Ref	Technology	Power(Psat) (dBm)	Gain (dB)	PAE (%)	Frequency (GHz)	Bandwidth (MHz)	Efficiency (%)
[28]	65nm CMOS	19.2	16	55	2.4-2.6	-	-
[29]	65nm CMOS	24.5	-	-	2.4	-	52
This Work	130nm CMOS	28.21	18.21	44.6	2.1	40	66.3

4. Conclusion

The objective of the paper was to design – 8-bit comparator based multilevel supply modulator for envelop tracking in RF power amplifier which has been successfully demonstrated. The whole circuit was designed on a 130 nm CMOS framework and simulated using CADENCE tools. Transient analysis was carried out and the output of each block in the circuit has been tested. The envelope detector circuit had been tested for various values of the input voltages and it could ceil the output at the required value of voltage. The 8-bit comparator could turn ON the output lines in accordance to the input power in order to activate the corresponding transistors in the supply modulator circuit. The output of the supply modulator has shown that the output voltage dynamically changes with change in the input signal strength. This work thus, puts light on a very efficient method to modulate the supply voltage to the PA. The Envelope Tracking circuit was tested on a PA circuit and the results obtained are quite encouraging with a good efficiency of 66.3%, maximum saturated power equal to 28.21 dBm, power gain of 18.21dB and a PAE of 44.6%. The future work will focus on designing a PA suitable for this envelope tracking model so that the PAE can be further increased. Efforts will be towards designing PA by eliminating the transformer so as to reduce bulkiness and reduce chip area.

Acknowledgements

NIL

Nomenclature

G	Generation
CMOS	Complementary Metal Oxide Semiconductor
nm	Nano meter
RF	Radio Frequency
PA	Power Amplifier
GHz	Giga Hertz
PAE	Power Added Efficiency
ET	Envelope Tracking
LTE	Long Term Evolution
MIMO	Multiple input multiple output
OFDM	Orthogonal Frequency Division Multiplexing
$C_0 - C_7$	Comparator Outputs
V	Voltage
dBm	Millimeter-decibel
P	Power
G	Generation

Greek symbols

μs	Unit of time
Ω	unit of resistnce

Subscripts

pre	Preamplifier
env	envelope
in	input
out	output
L	detector

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