Development of High Q Circuit Components in CMOS Technology for Millimeter Wave and Sub-THz Band Applications

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By

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ABSTRACT

Nowadays, the use of Complementary Metal-Oxide Semiconductor (CMOS) technology for millimeter and sub-terahertz (sub-THz) bands applications has attracted many researchers due to its low cost and easy integration into next-generation wireless communication systems, which are expected to achieve wireless communication links of more than 100 Gbps. In every wireless communication system, several passive elements are present, such as transmission lines, filters, antennas, resonators, etc. The performance of these wireless system is greatly influenced by these passive devices. However, the conventional on-chip designs of passive elements, which are typically made of microstrip and coplanar waveguide (CPW) structures, suffer from higher radiation, conductor, and dielectric losses at frequencies above the millimeter wave range. Alternatively, Defected Ground Structure (DGS) and Substrate Integrated Waveguide (SIW) structures have gained attention for high-frequency applications due to their low profile and high quality (Q) factors. Although these structures perform well in high-frequency applications, their circuit size remains a challenging issue for their on-chip implementation. Therefore, this thesis aims to design and fabricate compact size, low-loss, high-Q factors resonators, filters, and transmission lines using DGS and SIW topology in millimeter wave and sub-THz band in the commercial 0.18 μm CMOS technology.

In this dissertation, firstly, high Q DGS-based band stop filters (BSF) were designed and implemented in CMOS technology for millimeter wave applications. Besides their filtering purpose to eliminate unwanted signals from communication paths, these high Q BSFs are also suitable for realizing low phase noise voltage-controlled oscillators. The proposed two transmission poles (TPs) DGS-based band-stop filters (BSFs) utilize a novel concept of capacitively loaded T-shaped resonators embedded inside the original big DGS resonator, resulting in two high-Q factor small loop resonators. This structure, when combined with the feedline and series capacitor, allows independent control of the positions of the two TPs on each side of the parallel resonance without increasing the layout size. As a result, sharp scattering (S-) parameter response is achieved. Consequently, the loaded Q-factor and negative group delay of the band-stop filters are significantly improved at the designed frequency band. Two prototypes of the proposed band-stop filter with symmetric and asymmetric structures are designed and fabricated. The measurement results for these designs show good return losses at their center stopband frequencies with high Q values. Moreover, the respective chip areas are most compact, using only 0.024 mm² and 0.0129 mm².

Above millimeter wave band, DGS suffers from the issue of imperfect grounding, higher radiation, and interference with the adjacent components. To overcome these issues, SIW-based designs were explored, which is also a planer structure that can be designed in any substrate technology like CMOS and are more closed structures than DGS, less affected by the adjacent components, and presents low radiation loss. So, we utilized SIW topology to design and fabricate on-chip SIW cavity resonators for the millimeter wave band at 60 GHz resonance frequency. When implementing SIW-based cavities in CMOS technology, several challenges arise, including bulky size, transition loss, and matching circuit issues. To address these challenges, sub-modes SIW structures with folded ridge structures are implemented inside the proposed cavities, resulting in a significant size reduction. Experimental work is also conducted to study the effects of microstrip and blind via transitions feedings in these designs. Moreover, Complementary Split Ring Resonators (CSRRs) are incorporated into the design to achieve internal matching within the SIW cavities, eliminating the need for external matching circuits. The designed ultraminiaturized cavities have a compact size of less than 1% of a standard SIW design at the same resonance frequency of 60 GHz, while maintaining good return loss and high external Q-factor.

Above millimeter wave, sub-terahertz (sub-THz) band (90 ~ 300 GHz) are recently proposed for applications like communication and medical imaging due to their non-ionic (non-harmful) nature and higher penetration depth (can penetrate human skin easily). In addition, sub-THz band designs are relatively most compact. So, to design high Q passive designs in sub-THz band, SIW-based resonators and transmission lines are proposed and designed at 200 GHz. In this thesis, a new set of design equations specially tailored for SIW designs in sub-THz band was proposed and verified through simulations. Various compact and miniaturized SIW resonators, covering standard to sub-modes (standard SIW, half mode SIW, half mode with folded ridge SIW, half mode with folded ridge and CSRR loading, quarter mode with folded ridge, and quarter mode with folded ridge and CSRR loadings) are proposed, designed, fabricated, and validated based on these proposed equations. All these designs exhibit lower return loss, high Q-factor, and compact chip area. The measurement results are obtained by performing multi-line thru-reflect-line (m-TRL) de-embedding to remove the effect of the pads in such high-frequency designs. Moreover, leveraging the same design equations, a 200 GHz band half mode SIW transmission line is designed and fabricated. The simulation results of this design demonstrate a promising insertion loss of 1.1 dB in the frequency band ranging from

150 GHz to 280 GHz, making it suitable for various sub-THz band applications. To the author's knowledge, this is the first realization of resonators and interconnects line in commercial CMOS technology for sub-THz band applications with such ultra-miniaturized dimensions and excellent performance characteristics.

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Abbreviations

ADS	:	Advanced Design System
BAW	:	Bulk Acoustic Waves
BPF	:	Band Pass Filter
BSF	:	Band Stop Filter
CMOS	:	Complementary Metal Oxide Semiconductor
CPW	:	Coplanar Waveguide
CSRR	:	Complementary Split Ring Resonator
DGS	:	Defected Ground Structure
EM	:	Electromagnetic
EMSIW	:	Eighth Mode Substrate Integrate Waveguide
GSM	:	Global System for Mobile Communication
DC	:	Direct Current
EMSIW	:	Eighth Mode Substrate Integrate Waveguide
HFSS	:	High Frequency Structure Simulator
HMSIW	:	Half Mode Substrate Integrate Waveguide
LC	:	Inductor Capacitor
LPF	:	Low Pass Filter
LTCC	:	Low Temperature Co-Fired Ceramic
MIM	:	Metal Insulator Metal
m-TRL	:	Multi line Thru-Reflect-Line
PCB	:	Printed Circuit Board
PWW	:	Post Wall Waveguide
QMSIW	:	Quarter Mode Substrate Integrated Waveguide
RF	:	Radio Frequency
SAW	:	Surface Acoustic Waves
SiO_2	:	Silicon Dioxide
SIW	:	Substrate Integrated Waveguide
TE	:	Transverse Electric
TM	:	Transverse Magnetic
TPs	:	Transmission Poles
TZs	:	Transmission Zeros
VCO	:	Voltage Controlled Oscillator

Chapter 1: Introduction

1.1 Overview

The advancement of wireless communication in the 21st century has revolutionized the way we communicate and access information. The historical timeline, as shown in Figure 1.1, illustrates the significant growth in wireless traffic data rate since the 1980s. The first generation (1G) of wireless communication was based on analog systems and primarily supported voice communication at a speed of just 2 Kbps. However, subsequent generations, including 2G, 3G, and 4G, brought about substantial improvements in capacity and data transfer rates. The evolution of these technologies paved the way for faster and more efficient wireless communication for public use.

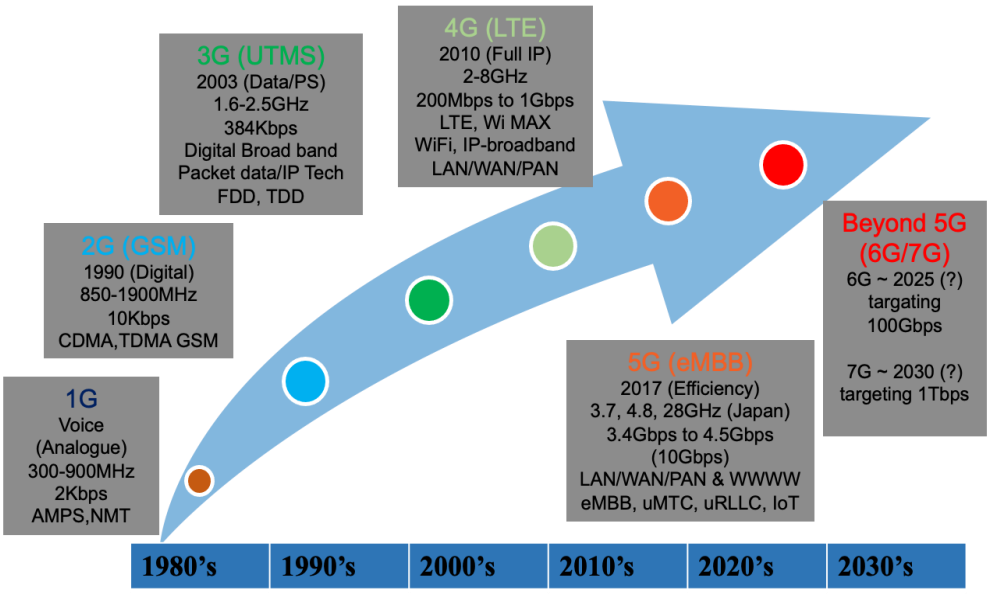


Fig. 1. 2: Wireless communication system timeline

With the advent of the fifth generation (5G) of wireless communication, which is currently being deployed in various parts of the world, the target data speed has reached 10 Gbps [1]. This remarkable increase in speed enables users to experience high-speed internet connectivity and seamless communication with minimal data delays. The impact of advanced communication networks extends beyond terrestrial applications. Today, we can explore far-reaching areas such as space and deep undersea beds, thanks to the advancements in wireless

communication. Even in Japan, 5G communication has been officially introduced in multiple frequency bands, ranging from 3.7 to 28 GHz, with current data speeds of 3.4 to 4.5 Gbps.

The widespread adoption of 5G technology has empowered individuals to access high-speed internet and communicate effectively, regardless of their location. A single handheld device now allows us to explore and connect with different parts of the world, making communication more efficient and convenient. This rapid progress in wireless communication drives researchers in the field to continuously strive for improvements. The focus of telecommunication and wireless system research includes developing better, smaller, and more affordable devices that offer reliable and faster communication capabilities. These efforts aim to meet the growing demands of an increasingly interconnected world.

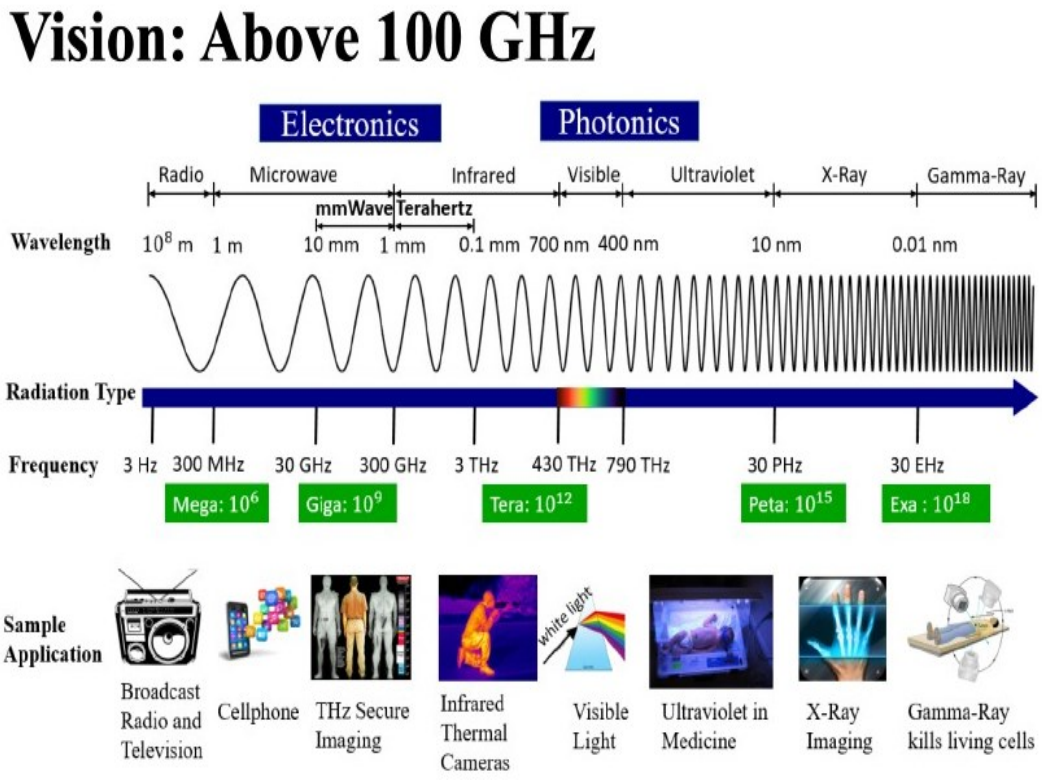


Fig. 1. 3: Above 100 GHz band application vision [2]

Indeed, complementary metal-oxide semiconductor (CMOS) technology has garnered significant attention from researchers in the field of millimeter and terahertz (THz) wireless communication systems. CMOS offers several advantages such as low fabrication cost and easy

planer integration, making it an attractive choice for next-generation wireless communication systems aiming for Terabit-per-second (Tbps) links [1]-[2].

To transmit high-power signals effectively, it is crucial to have low-loss signal paths or transmission lines. Traditionally, microstrip lines and coplanar waveguides (CPWs) have been utilized as transmission lines. These conventional transmission lines suffer from radiation loss and conductor loss, which tend to increase at high frequencies. These losses can significantly impact the overall performance of the system. To establish an efficient wireless communication system, it is essential to design not only the active devices like oscillators and power amplifiers on-chip but also strive to integrate everything on a single chip. By integrating all the components on-chip, including transmission lines, it becomes possible to minimize losses associated with interconnects in high-frequency applications. This approach helps to mitigate the issues caused by radiation loss and conductor loss, ultimately enhancing the overall performance of the system.

Therefore, the recent trend in CMOS millimeter and THz wireless communication research is to explore on-chip integration of all the necessary components, enabling the realization of efficient and high-performance wireless communication systems with reduced losses and improved overall system performance.

1.2 Problem Definition and Conventional Studies

For the low loss high speed communication systems, the bottle neck for those designs are the passive designs. Designing on-chip passive components such as filters, resonators, and transmission lines in millimeter wave and sub-THz bands using available CMOS technology presents several challenges like higher loss, lower performance, circuit size, etc. These components are crucial in many wireless system designs and are often utilized in the design of other circuits like oscillators and amplifiers.

In conventional designs, resonators often rely on inductor-capacitor (LC) combinations to achieve the desired oscillation frequency. However, at high frequencies above 25 GHz, the inductor itself starts to radiate, leading higher losses and lower quality factor (Q-factor). The Q-factor of resonators and filters is a dominant factor in determining the phase noise of oscillators, as described by Leeson's equations [3]. Consequently, high-frequency oscillators designed with inductor-based resonators suffer from higher phase noise and lower output power

and are unusable in the higher frequencies like above K-bands [3]-[9]. Alternative solutions are needed to address this issue.

To overcome these problems, it is crucial to design resonator structures that can maintain a high *Q*-factor even at very high frequencies. Researchers are exploring alternative resonator designs, such as those based on bulk acoustic waves (BAWs), surface acoustic waves (SAWs), and other innovative structures. These alternative designs aim to achieve high *Q*-factors and minimize radiation losses, thereby improving the performance of high-frequency oscillators and other circuits. Still such structures are only applicable in lower frequency limited to C-band and are unable to fulfil the demand of high frequency applications.

Similarly, microstrip transmission lines above the K-band exhibit high losses and possess low *Q*-factors, leading to performance degradation in the implemented systems. These losses are inherent in these conventional design topologies. To address this issue, researchers are investigating alternative transmission line structures and materials, such as coplanar waveguides (CPWs), substrate-integrated waveguides (SIWs), and advanced dielectric materials in printed circuit board technology. These innovations aim to reduce losses and enhance the performance of low frequencies upto sub-terahertz band but are still limited by the performance of available materials.

Therefore, there is a requirement of the low-loss and high frequency designs topology of the passive circuits in CMOS technology to improve the performance and efficiency of future wireless communication systems operating at these high frequencies.

1.3 Research Motivation and Objective

Recently, Defected Ground Structure (DGS) and low-profile Substrate Integrated Waveguide (SIW)-based resonators and filters garnered attention than conventional lumped elements-based components, microstrip-based components, and coplanar waveguides (CPW)-based components due to their low conduction loss, high *Q*-factor, and easy integration with planar circuits in integrated designs. In our laboratory, we successfully implemented DGS filters in CMOS technology to design low phase noise voltage-controlled oscillators (VCOs) in various band applications [10]-[18]. This achievement has motivated us to explore the use of DGS filters for designing miniaturized, low-loss on-chip filters in the millimeter-wave band.

The high unloaded *Q* factor of SIW-based resonators and filters makes them particularly appealing for low-loss designs in PCB technology. We have successfully demonstrated low-loss resonator and filter designs in PCB technology in previous works [18]-[19]. In this work we aim to design on-chip SIW based resonators and interconnects for millimeter wave and sub-THz band applications. Taking advantage of the on-chip high-*Q* SIW-based structures in millimeter-wave and sub-THz bands for future wireless communication serves as the motivation for this research. These low loss high Q passive designs are advantageous for improving the performance of future high frequency band wireless communication systems finding their application as shown in block diagram in Fig. 1.3.

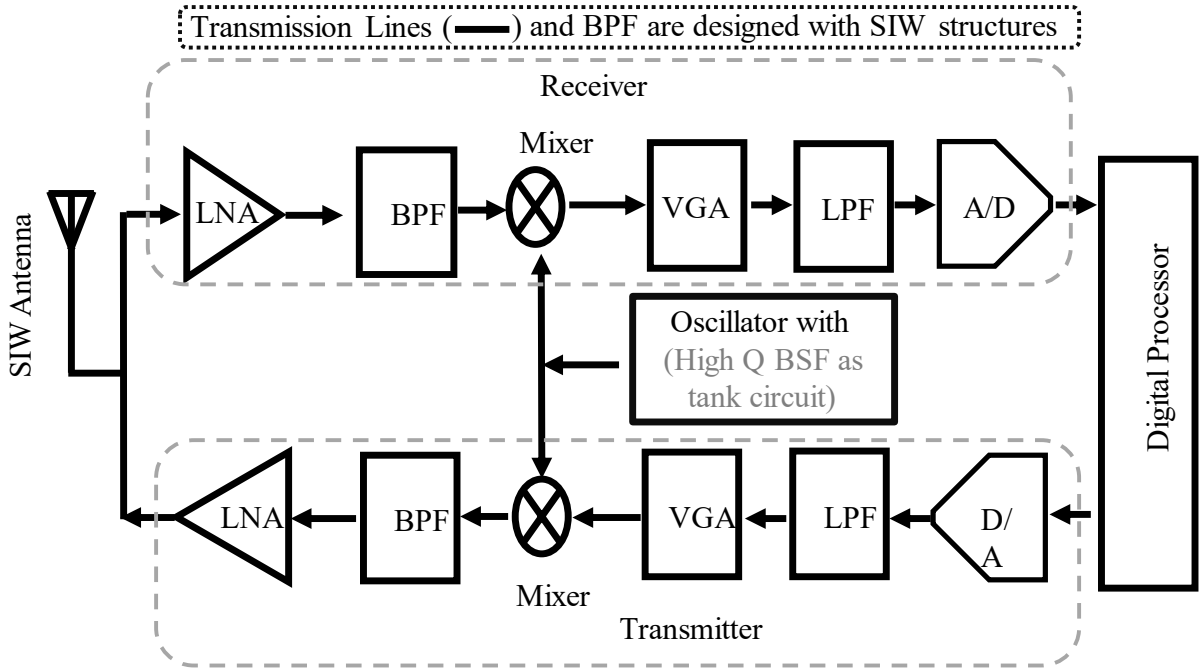


Fig. 1. 4: Block diagram of wireless communication system with high Q passive components integration

The research aims to achieve the following objectives:

- Enhancing the filter response of millimeter-wave DGS band stop filters (BSF) by generating transmission poles around the center frequency with full controllability.

- Analyzing, implementing, prototyping, and experimenting with 60 GHz band millimeter-wave miniaturized SIW resonators in CMOS technology for millimeter-wave applications.
- Designing, analyzing, and implementing low-loss sub-THz band on-chip miniaturized resonators and transmission lines in commercial CMOS technology.

By addressing these objectives, the research aims to contribute to the development of improved filters, resonators, and transmission lines with high Q for millimeter-wave and sub-THz band applications, particularly in the context of on-chip integration using CMOS technology.

1.4 Thesis Outline

The key accomplishments of this thesis are organized as follows in Chapters 2-5:

Chapter 2 discusses the DGS structure and its application for filter design. The design and implementation of the DGS filter for a 52 GHz band application are presented. This chapter includes the design theory, working principle, and fabrication and measurement of two prototypes of the proposed filters.

Chapter 3 describes the theory and implementation of the SIW structure, along with its wave propagation characteristics. Various miniaturized designs for the 60 GHz millimeter-wave band application are presented, including different prototypes with various feeding structures, folded ridge, and complementary split ring resonators for miniaturization and impedance matching.

In Chapter 4, design guides for sub-THz band SIW in commercial CMOS technology are proposed and discussed. Given the lack of proper theory for SIW design in higher frequencies in existing literature, this chapter provides detailed guidelines for designing sub-THz band SIW vias in commercial CMOS technology. Various prototypes of resonators, ranging from standard to sub-modes, and transmission lines covering the entire D-band are designed based on the proposed design guides. The chapter also includes a discussion on sub-THz band de-embedding.

Finally, Chapter 5 summarizes the conclusions of the overall thesis work, highlighting the major contributions. It also includes a discussion on future research ideas.

Chapter 2: Two Transmission Poles Millimeter Wave High-*Q* Defected Ground Structure-Based Filter Designs

2.1 Introduction

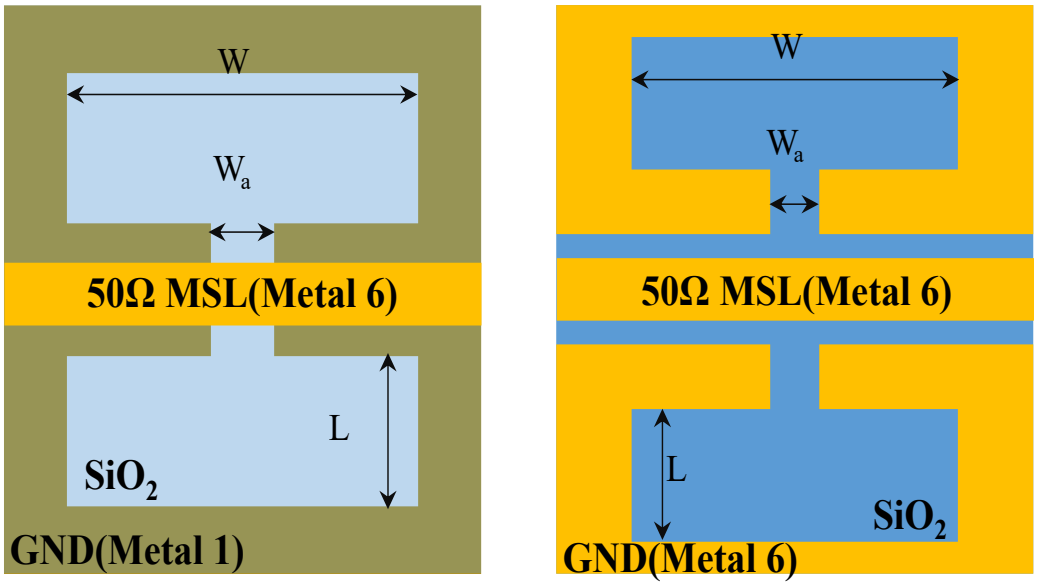
In most communication devices, filters/resonators have a significant role in selecting desired signals by filtering the unwanted signals from the path. Nevertheless, the large active area of these filters/resonators is trouble for their implementation in high-performance technologies like Gallium Nitride (GaN), complementary metal-oxide-semiconductor (CMOS), etc. However, after the introduction of defected ground structure (DGS) by C. S. Kim et al. [20] in the early 2000s, there has been a significant improvement in performance and circuit size of RF/microwave components like filters, resonators, antennas, etc. [21]-[24]. DGS is just a reshaping of the ground plane that alters the current distribution on the ground plane. Due to this, the effective capacitance and inductance of circuit changes and the performance of filters and other microwave circuits are enhanced.

Bandstop filters (BSF)/notch filters are vital elements whenever specific band signals must filter out from the communication paths. Many literatures on DGS-based BSF have been reported in printed circuit board technologies [25]-[31]. However, to the author's best knowledge, DGS BSF in the CMOS technology has not been reported to date. Besides, the first on-chip tunable absorptive BSF has been investigated for lower frequency band (2.9 - 4.3 GHz) application using the lumped elements [32]. Similarly, 24.5 GHz on-chip absorptive BSF was reported in the 0.13 μm (Bi)-CMOS process [33]. A dual-band BSF filter in the CMOS process using thin-film microstrip structure open stepped impedance resonator has been reported with two different designs at 30/85 GHz and 30/80 GHz band [34]. But both reported designs possess wider stop bandwidth and larger circuit size. Previously, Jahan et al. [10]-[16] have proposed DGS-based BSF in commercial CMOS technology for application to design low phase noise voltage-controlled oscillators (VCO) in various frequencies bands. However, in all these VCO designs, implemented BSFs were presented only with the simulation results.

2.2 DGS Implementation

A DGS resonator is created by making some pattern on the grounding plane of the conventional transmission lines. Usually, conventional DGS resonators are designed using the top metal as a standard transmission and bottom metal as a ground plane where defects are created. Few

examples of the DGS resonators using such topology are (i) H-shaped DGS resonator [12] in which signal path is designed in top layer metal and the grounding return path is designed with bottom layer metal and (ii) H-shape coplanar waveguide type DGS resonator [13], where both the signal path and the grounding plane are made on the top layer metal. The main disadvantage of former topology is that it offers the different metal thickness between the used metal layers i.e., top metal is much thicker than bottom metal. The later one takes the advantage of the thickest metal layer. Both resonators have been implemented on the CMOS technology to design a K-band VCOs. However, both these designs have significant disadvantages: (i) they are bulky, (ii) they present the effect of long interconnects requirements to be implemented in the VCO designs, and (iii) They present only the band stop response due do which they are not sensitive enough to be implemented for the filtering applications.

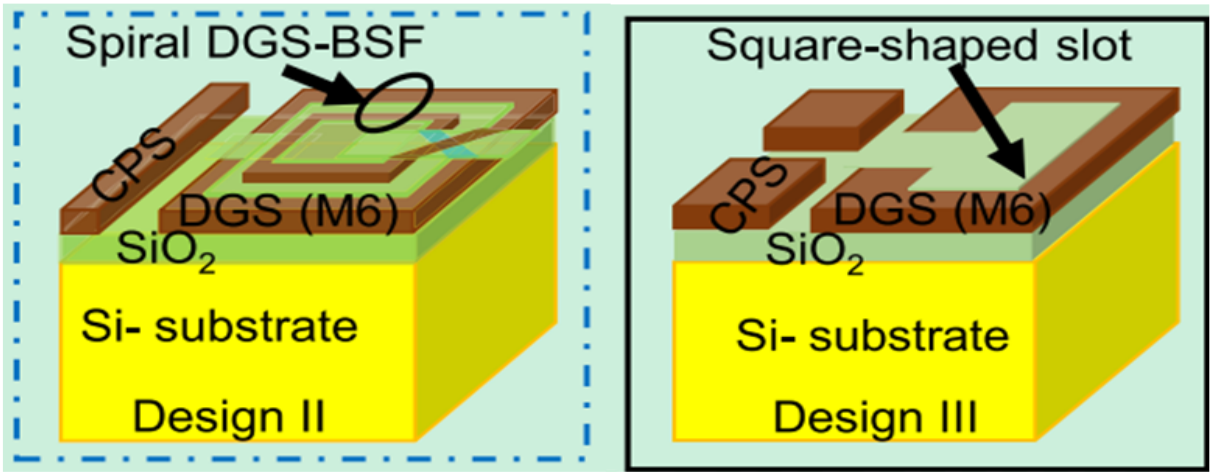


(a) *(b)*

Fig. 2. 1: Traditional DGS BSFs. (a) H-shaped DGS BSF [12]. (b) H-shaped CPW DGS BSF [13].

Different types of minimal size DGS resonators like spiral DGS band stop filter, square shaped slot DGS filters are presented in the low phase noise VCO design in [16]. These structures have successfully demonstrated the compact design of the DGS-BSF designs. Fig. 2.2 (b) is a dual series resonance type DGS BSF which is implemented to K-band VCOs designs. Here, DGS-

based BSF with a small circuit size were realized by placing a capacitor in the excitation gap of DGS. Although both transmission poles are created around the parallel resonance, they are not effectively adjustable due to the filter geometry and single capacitor used in the excitation gap.



(a) *(b)*

Fig. 2. 2: Dual resonance DGS resonators. (a) spiral DGS resonator . (b) Square-shaped DGS resonator [16]

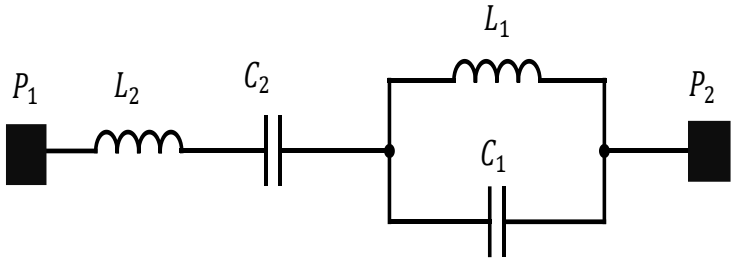


Fig. 2. 3: Lumped elements based BSF circuit with both the lower and the upper band TPs.

2.3 BSF Circuit Realization with Two TPs

A BSF circuit with simple parallel resonance has self-resonance only without the TPs. However, such circuits act like a simple series inductor ($\overline{L_1}$) before its self-resonance frequency and a simple series capacitive ($\overline{C_1}$) that after it [14]. So, when some inductances/capacitances are attached in series, TPs appears around this self-resonance frequency of the BSF. Fig. 2.3 shows

the first order lossless circuit which creates both lower and the upper band TPs, and these resonances can be calculated as $\omega_{s1} = \frac{1}{\sqrt{(L_2+\overline{L_1})C_2}}$ and $\omega_{s2} = \frac{1}{\sqrt{L_2(\overline{C_1}+C_2)/(\overline{C_1}+C_2)}}$, respectively.

Fig. 2.3 input impedance can be represented by:

$$Z = j\omega L_2 + \frac{1}{j\omega C_2} + \frac{j\omega L_1}{1-\omega^2 L_1 C_1}, \tag{2.1}$$

and its susceptance parameter (B) can be obtained,

$$B = \frac{\omega C_2(1-\omega^2 L_1 C_1)}{\omega^2 L_1 C_2 - (1-\omega^2 L_1 C_1)(1-\omega^2 L_2 C_2)}. \tag{2.2}$$

Now, by making $B = 0$, the parallel resonance frequency is obtained ($\omega_o = \frac{1}{\sqrt{L_1 C_1}}$) whereas by equating $B = \infty$, two frequencies of series resonance (ω_{s1} and ω_{s2}) are obtained that can be obtained by,

$$\omega_{s1}{}^2, \omega_{s2}{}^2 = \frac{(L_2C_1+L_1(C_2+C_1)) \pm \sqrt{C_1^2(L_2+L_1)^2 + L_2{}^2 C_2^2}}{2L_1C_1L_2C_2}. \tag{2.3}$$

Now, the susceptance slope (b) parameter is obtained by the method in reference [35], as:

$$b = \frac{\omega_o}{2}\frac{\partial B}{\partial \omega}\Big|_{\omega=\omega_o} = \omega_o C_1. \tag{2.4}$$

Using b from (2.4), the external quality factor (Q_{ex}) is calculated as [5], [35]:

$$Q_{ex} = \frac{b}{Y_o} = \frac{g_o g_1}{FBW}. \tag{2.5}$$

where, FBW is the fractional bandwidth, g_o and g_1 are the low pass prototype parameters. Solving (2.4) and (2.5), C_1 and L_1 are obtained as,

$$C_1 = \frac{Y_o g_o g_1}{\omega_o FBW}, \quad L_1 = \frac{1}{\omega_o^2 C_1}. \tag{2.6}$$

Now, the equivalent series inductor ($\overline{L_1}$) that is before its parallel resonance frequency and the series equivalent capacitor ($\overline{C_1}$) that is after its parallel resonance of Fig. 1(a) are calculated by,

$$\overline{L_1} = \frac{L_1\omega_o^2}{\omega_o^2-\omega_{s1}^2}, \quad \overline{C_1} = \frac{C_1(\omega_{s2}^2-\omega_o^2)}{\omega_{s2}^2}. \tag{2.7}$$

Finally, the equivalent C_2 and L_2 are obtained as,

$$L_2 = \frac{1}{\omega_{s1}^2 C_2} - \overline{L_1}\,, \; C_2 = \frac{\omega_{s2}^2 L_{42}\overline{C_1}}{\overline{C_1} - \omega_{s2}^2 L_2}. \tag{2.8}$$

Table 2.1 presents the calculated lumped components values for the various TPs positions at the same stopband frequency using equations (2.6)–(2.8). The response of simulated S-parameter of these scenarios is illustrated in Fig.2.4. The existence of two TPs in the near vicinity of self-resonance reduce 3-dB bandwidth and enhance the quality factor Q_l as presented in Table I. The $loaded\ Q$ is calculated from methodology described in [5], [31], [35].

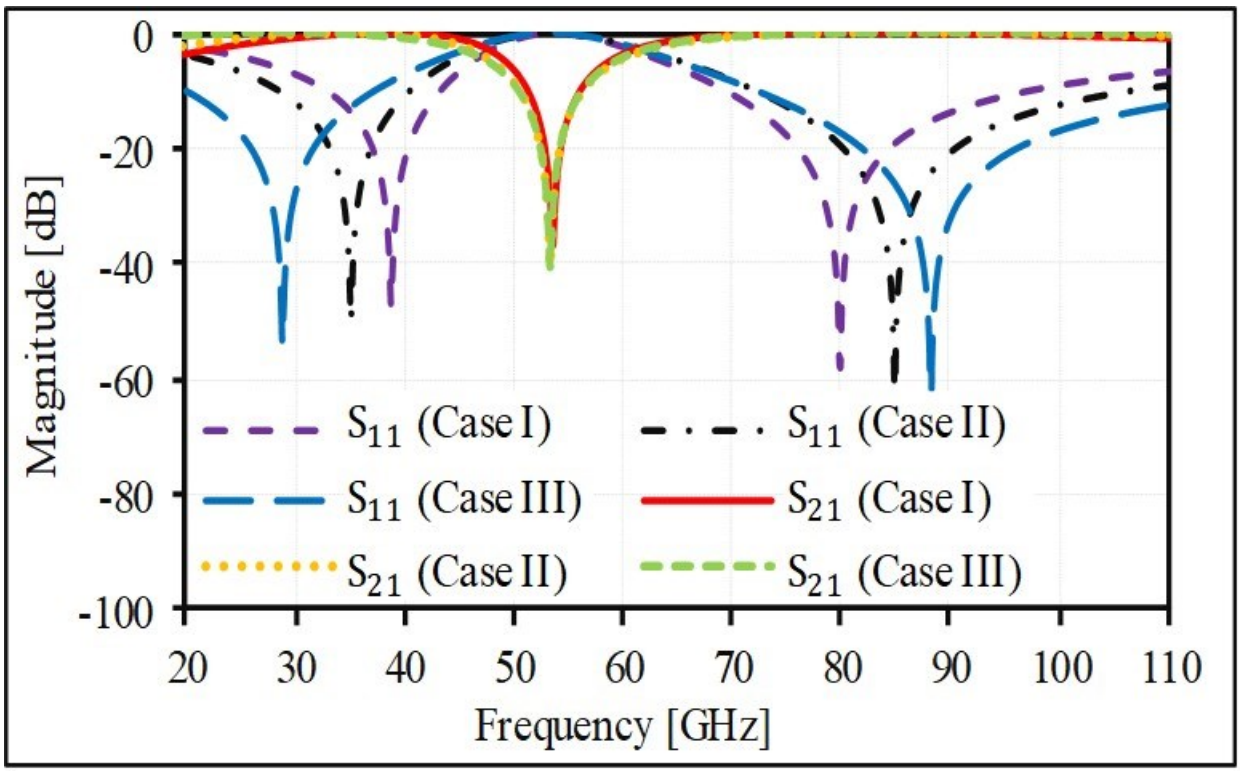


Fig. 2. 4: S-parameters simulation results of two TPs BSF in Fig. 2.3 for various cases listed on Table 2.1.

Table 2. 1: Calculated lumped elements parameters of BSF for different position of TPs (ω_{s1} and ω_{s2}) at ω_o = 54 GHz center stopband frequency

	ω_{s1} and ω_{s2} [GHz]	FBW	L_1 [pH]	C_1 [fF]	L_2 [pH]	C_2 [fF]	$Q_l = \left[\frac{\omega_o}{\omega_{c2} - \omega_{c1}}\right]$
I	39, 80	0.244	81	109	138	55	4.09
II	35, 85	0.293	99	90	113	72	3.41
III	29, 88	0.301	95	94	80	140	3.32

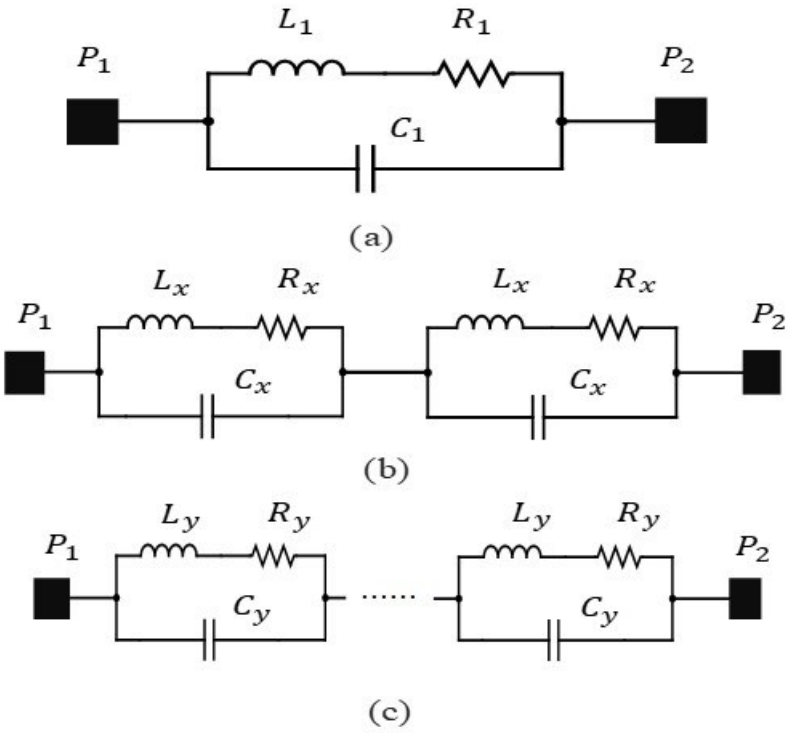


Fig. 2. 5: Simple lumped elements based BSF circuit with (a) Single resonator. (b) Two-resonators series cascaded design. (c) n-resonator series cascaded design.

2.4 Design of Proposed Two TPs DGS-based BSF Filter and its Implementation in commercial CMOS Technology

The proposed two TPs BSF is designed with *n* smaller series connected resonators elements with same parameters having high-Q factor, which therefore leads to realize high *Q*-factor design.

2.4.1 Analysis of a Lossy Parallel LC Resonance Circuit

Fig. 2.5(a) illustrates a parallel simple resonance circuit with a lossy element. The cascaded arrangements of multiple parallel resonance designs are presented in Fig.2.5(b) and Fig.2.5(c), respectively. The input impedance (Z_{in}) of Fig. 2.5(a) is as follows:

$$Z_{in} = \frac{R_1 + j\omega L_1}{1 - \omega^2 L_1 C_1 + j\omega R_1 C_1}. \tag{2.9}$$

Likewise, the Z_{in} of the series connected resonant circuit having *n* small resonators in Fig.2.5(c), is expressed as follows:

$$Z_{in} = \frac{R_y + j\omega L_y}{1 - \omega^2 L_y C_y + j\omega R_y C_y} \times n. \tag{2.10}$$

$$Z_{in} = \frac{nR_y + j\omega(nL_y)}{1 - \omega^2(nL_y)(C_y/n) + j\omega(nR_y)(C_y/n)} \tag{2.11}$$

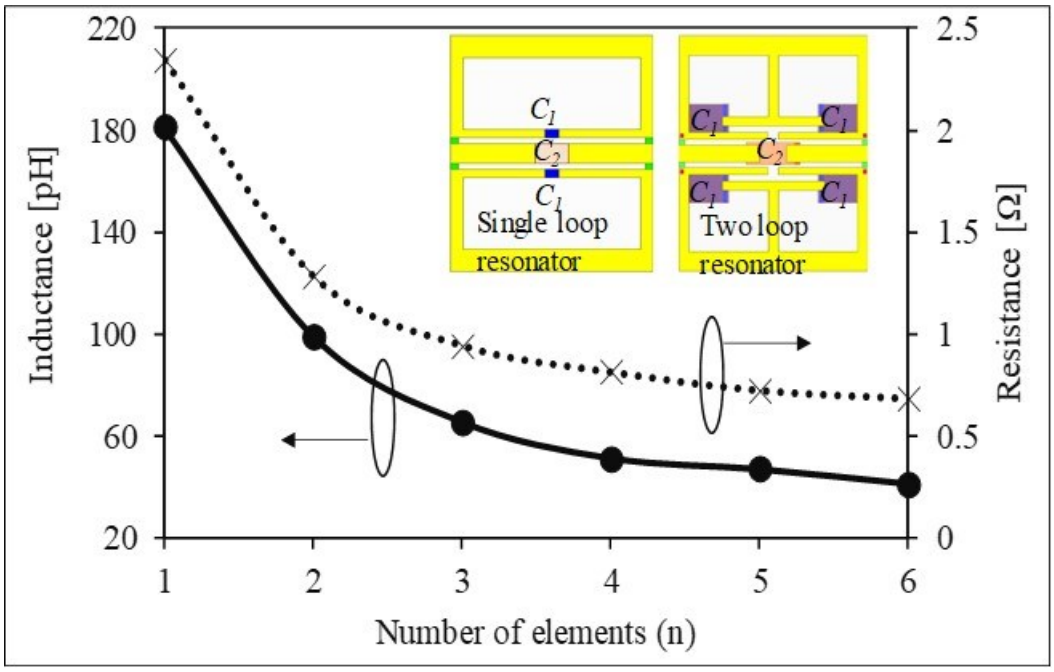
From (2.9) and (2.11) to the same resonant frequency condition, Fig.2.5(a) and Fig.2.5(c) becomes equivalent with $R_y = R_1/n$, $L_y = L_1/n$ and $C_y = nC_1$. For instance, when two-resonators are cascaded as in Fig. 3(b), the equivalent condition becomes $R_x = R_1/2$, $L_x = L_1/2$ and $C_x = 2C_1$. That implies that to achieve same resonance using two smaller cascaded resonators, we only require half of the inductance compared to a single resonator. Also, using (2.11), the *Q* unloaded (Q_u) [5], [35] is obtained as,

$$Q_u = \frac{\omega(nL_x)}{(nR_x)} = \frac{\omega L_x}{R_x}, \tag{2.12}$$

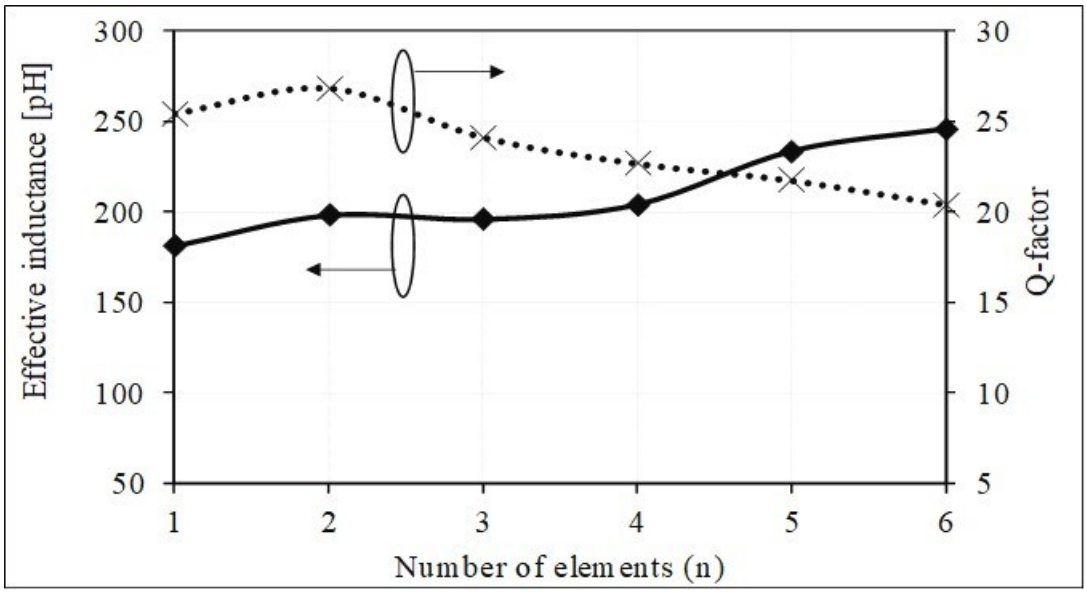
which shows that if high Q resonators are utilized in designing the cascaded series resonator structure, it is possible to obtain a higher Q design for the entire structure compared to using a single bulky resonance circuit. So, by implementing multiple high Q-factor resonators in a cascaded arrangement, the overall filter performance can be significantly enhanced, allowing for better signal filtering and improved circuit efficiency in various RF/microwave applications.

The DGS-based BSFs that are used to design K-band VCOs employ a single loop big resonator However, at higher frequencies such as the V-band, designing a BSF with same topology, i.e., a single loop big resonator with tiny capacitor, becomes challenging. The use of a tiny capacitor makes the filter vulnerable to additional parasitic capacitance that appears from interconnects

lines and other design circuit elements, making it hard to accurately realize the filter resonance frequency, especially in CMOS processes.



(a)



(b)

Fig. 2. 6: Interpretation of HFSS simulation result at 52 GHz frequency for (a) nth loop unit cell inductance and resistance (b) total effective inductance and the Q-factor of overall proposed DGS filter.

Additionally, at higher frequencies, the single loop inductor exhibits a low Q-factor due to higher resistive loop losses, which ultimately impacts the overall performance of the resonator. To address these challenges, the study focused on the total effective inductance (*Leff*) and the Q-factor of the n^{th} section of cascaded series smaller resonators with n-elements. Fig.2.6(a) presents the inductance (L) and resistance (R) of a single nth loop resonator in a cascaded DGS design constructed with n smaller resonator sections that is obtained through EM simulation using High-Frequency Structure Simulator (HFSS v2018.01).

Fig. 2.6 (b) illustrates *Leff* and the Q-factor of the full resonant circuit when designed by employing n resonators in series. *Leff* is computed by multiplying the unit cell inductance with the number of resonators employed. For this specific design structure, the Q-factor is maximum when n=2. Moreover, *Leff* is higher than that of the single big resonator. As the number of resonators increases, *Leff* increases significantly, but the Q-factor decreases beyond this value. This suggests that using two resonator sections in series can provide the highest Q-factor and improved performance for the filter design.

2.5 Implementation of the Proposed Two TPs DGS-based BSF in commercial CMOS Technology

As previously mentioned, we used n = 2 for this design. Fig. 2.7 shows the equivalent circuit of Fig. 2.5(a). Fig. 2.8 shows its EM model implementation in 0.18-um CMOS technology. The signal path and grounding plane are implemented with the thickest layer metal (M6). Within the layout size of the original single DGS loop, as shown in Fig. 2.8(a), two small inductive loops are created by using a T-shape line structure inside of it. The capacitors (C_1) are loaded and placed to close the loop of T-structure at the end.

The equivalent circuit shown in Fig. 2.7 for the proposed DGS has lumped elements L_{DGS}, C_{DGS}, and R_{DGS}. The capacitor C_{DGS} is relatively small. When the additional capacitance C_1 is introduced, the DGS loop becomes smaller, and the parallel resonance frequency occurs at the frequency $\omega_o = \frac{1}{\sqrt{L_{DGS}(C_{DGS}+C_1)}}$. By adjusting size (here the length) of the proposed T-shape (p) that is inside the DGS structure, it is possible to achieve variation in DGS inductance. Similarly, L_{CPS} and C_{CPS} represents the equivalent elements of feedline. The equivalent series inductance ($\overline{L_{DGS}}$) and series capacitor ($\overline{C_s}$) in combination with L_{CPS} and $C_S = C_{CPS} + C_2$, determines the

TPs positions. The lower band TP (ω_{s1}) and the upper band TP (ω_{s2}) are represented by $\frac{1}{\sqrt{(L_{CPS}+\overline{L_{DGS}})C_p}}$ and $\sqrt{\frac{\overline{C_s}C_p}{L_{CPS}(\overline{C_s}+C_p)}}$, respectively. By using the equations described in references [10]–[16], the values of L_{DGS}, R_{DGS}, and C_{DGS} are calculated. Similarly, L_{CPS}, and C_{CPS} are calculated using (2.1)–(2.8) where the terms L_{DGS}, C_{DGS}, L_{CPS}, and C_{CPS} are represented by L_1, C_1 $(= C_s)$, L_2, and C_2 $(= C_p)$ as also described in the references [14] and [16] as in equation (2.13)-(2.16).

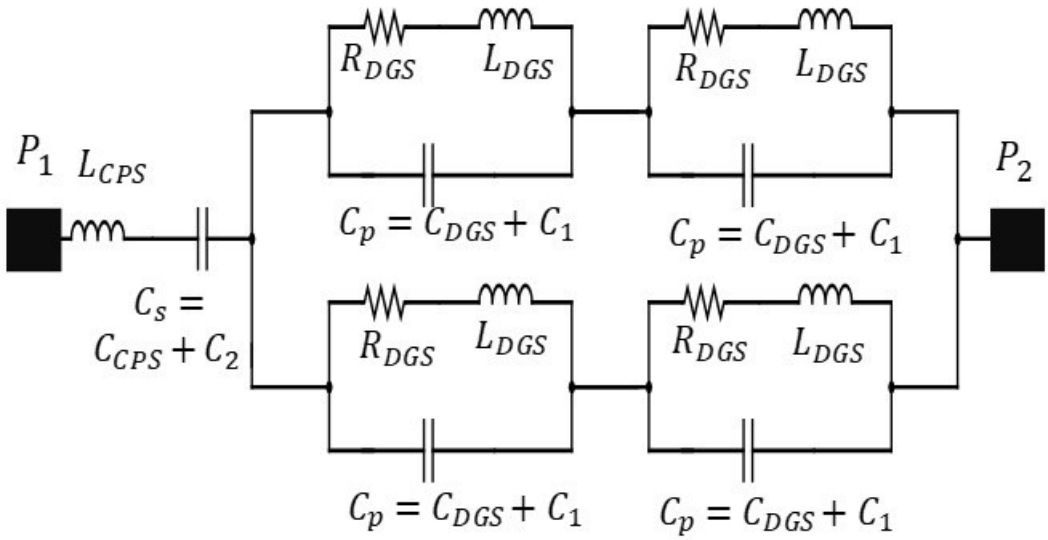


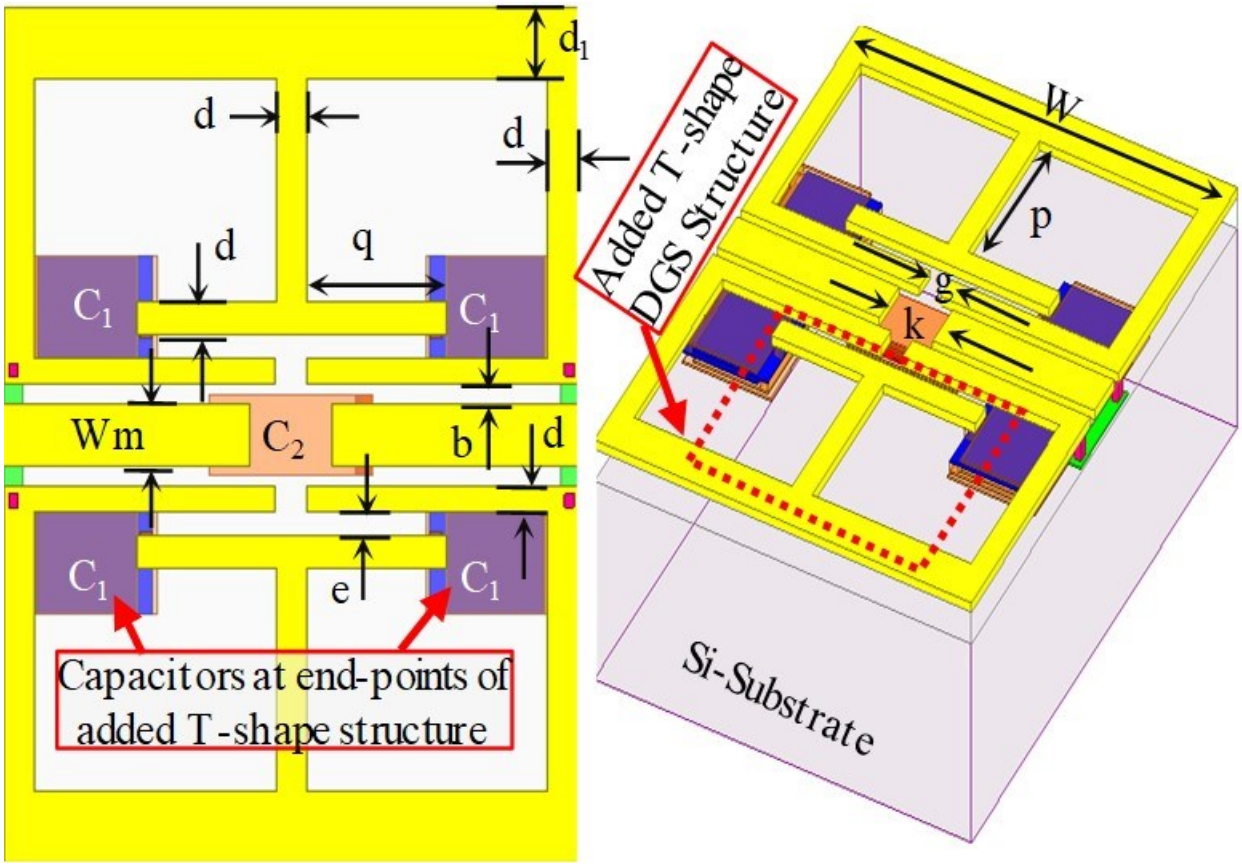
Fig. 2. 7: The equivalent circuit of the proposed BSF with n cascaded resonator circuit connected in series connection. $C_P = 109\ fF$, $L_{CPS} = 130\ pH$, $C_s = 63\ fF$, $L_{DGS} = 82\ pH$, $R_{DGS} = 1.26\ pH$, *and* P_1 *and* P_2 *are ports.*

$$C_{DGS} = \frac{\omega_c}{2Z_o(\omega_o^2-\omega_c^2)} \quad L_{DGS} = \frac{1}{\omega_o^2 C_{DGS}} \tag{2.13}$$

$$R_{DGS} = \frac{1}{\sqrt{\left(\frac{1}{|S_{11}(\omega_o)|^2}\right)-\left(2Z_o\left(\omega C-\frac{1}{\omega L}\right)\right)^2-1}} \tag{2.14}$$

$$L_{CPS} = \frac{1}{(\omega_o^2-\omega_{s1}^2)} - \overline{L_{DGS}}\,, \quad C_p = \frac{\overline{C_s}}{\omega_{s2}^2 L_{CPS}\overline{C_s}-1} \tag{2.15}$$

$$\overline{L_{DGS}} = \frac{L_{DGS}\omega_o^2}{\omega_o^2-\omega_{s1}^2}, \quad \overline{C_s} = \frac{C_s(\omega_{s2}^2-\omega_o^2)}{\omega_{s2}^2} \tag{2.16}$$



(a) (b)

Fig. 2. 8: The proposed DGS-based BSF EM model. (a) Top view. (b) 3D view.

2.6 Analysis of the Controllable Transmission Poles

Different variations in the structure of the proposed BSF design are examined to validate the independent selection of transmission poles at the target frequency. Initially, the impact of introducing a T-shape structure is investigated. As shown in Fig. 2.9, altering the length of the T-shape leads to changes in the self-resonance frequency. A slight adjustment in the position of the lower transmission poles results in a significant enhancement in insertion loss in the stopband frequency. This is because the inductance L_{DGS} varies and from (2.1)–(2.8), [14], [16], the self-resonance depends directly on this L_{DGS} and the series resonances depend on effective value of inductance at the self-resonance.

Subsequently, by varying the capacitors C_1, the lower TP position can be changes, with only a

smaller change in the center stopband frequency and upper band TP, as depicted in Fig. 2.10. Finally, capacitor C_2 plays an important role for determining the position of the TP in upper band, as illustrated in Fig. 2.11. It also influences the center resonance frequency. The alteration in the center resonance frequency when using capacitor C_2 with MIM (Metal-Insulator-Metal) capacitor is attributed by the change in the effective capacitance that is at the resonator excitation gap, resulting from the proximity of the metal layers M5 to M2 and M6 metals in the DGS. Consequently, through the careful optimization of T-shaped length, capacitors C_1 and C_2, an optimized DGS BSF with controllable TPs can be achieved, exhibiting sharp S-parameter characteristics. Table 2.2 provides a summary of the analysis.

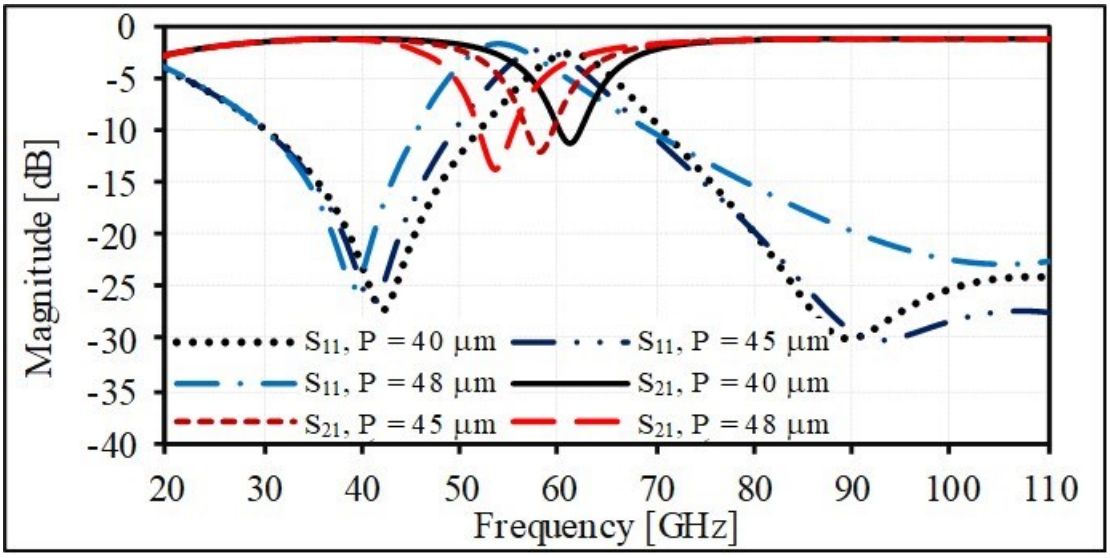


Fig. 2. 9: S-Parameters results with the length of T-shape structure.

Table 2. 2: Analysis of capacitors C1 and C2 with respect to position of TPs (ω_{s1} and ω_{s2}) around ω_o = 53.2 GHz stopband frequency

ω_{s1} and ω_{s2} [GHz]	Added T-shape Structure Length [µm]	C_1 [fF]	C_2 [fF]
40 & 89	45	70	50
39 & 92	47	70	60
36 & 92	48	94	50
35 & 86	48	116	60

The optimized dimensions of the proposed BSF are embedded in Fig. 2.8, which are shown in Table 2.3. Fig. 2.12 shows S-parameter simulation results of the proposed BSF EM model, which agrees well with the equivalent circuit results. The performance comparison of Q-factors of the proposed BSF design with the conventional DGS-based BSF having two transmission poles is presented in Table 2.5, which shows that the proposed DGS-based BSF has a higher Q_u and Q_l than its conventional BSF counterparts.

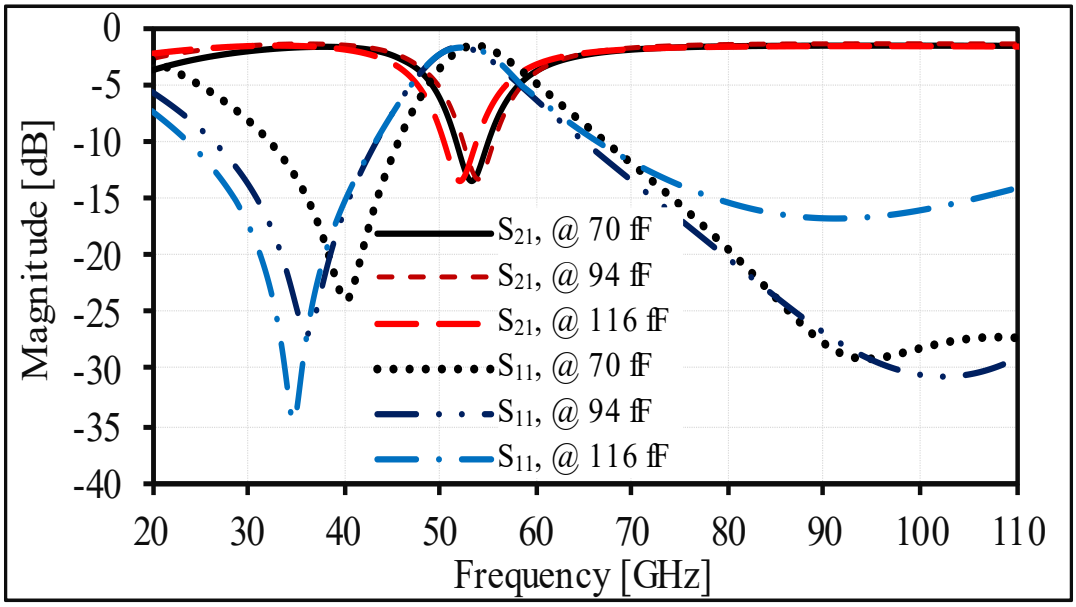


Fig. 2. 10: S-Parameters results with capacitor C1 variation.

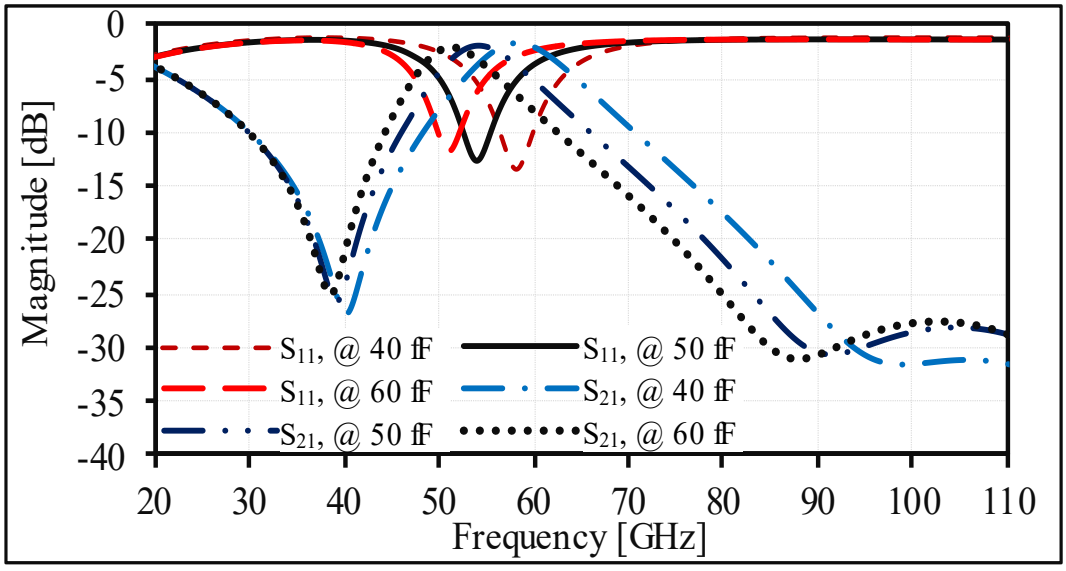


Fig. 2. 11: S-Parameters results with capacitor C2 variation.

Table 2. 3: Optimized dimension of the proposed DGS-based BSF in Fig. 2.8 (in micrometers)

b	d	d_1	e	g	k
6	7.5	10	4	8	20
Wm	p	q	W	C_1	C_2
14	46.5	30	135	are MIM capacitors	

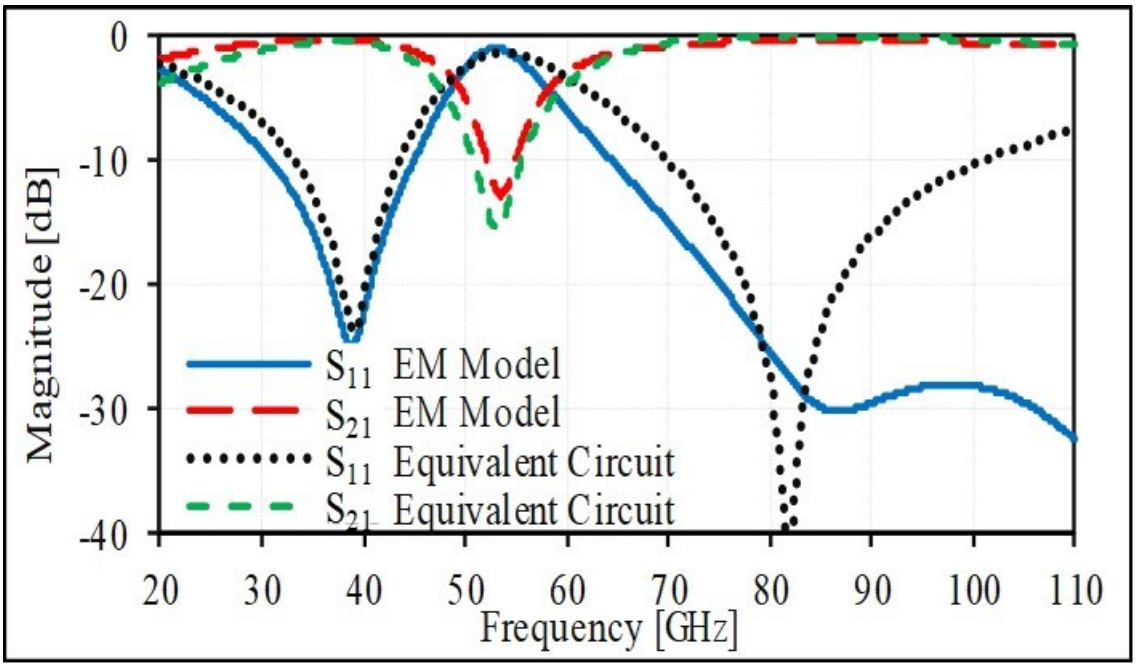


Fig. 2. 12: Proposed DGS-based BSF S-parameter simulation results.

Table 2. 4: The Q-factors comparison of DGS-based BSF design with two TPs

BSF Designs	f_o [GHz]	ω_{s1}, and ω_{s2} [GHz]	Dimension ($\lambda_g \times \lambda_g$)	Q_l	Q_u
Design [11]	33*	17*, 61*	0.053 × 0.053	4.6*	24*
Proposed Design	53.2	40, 86	0.037 × 0.045	4.91	26.8

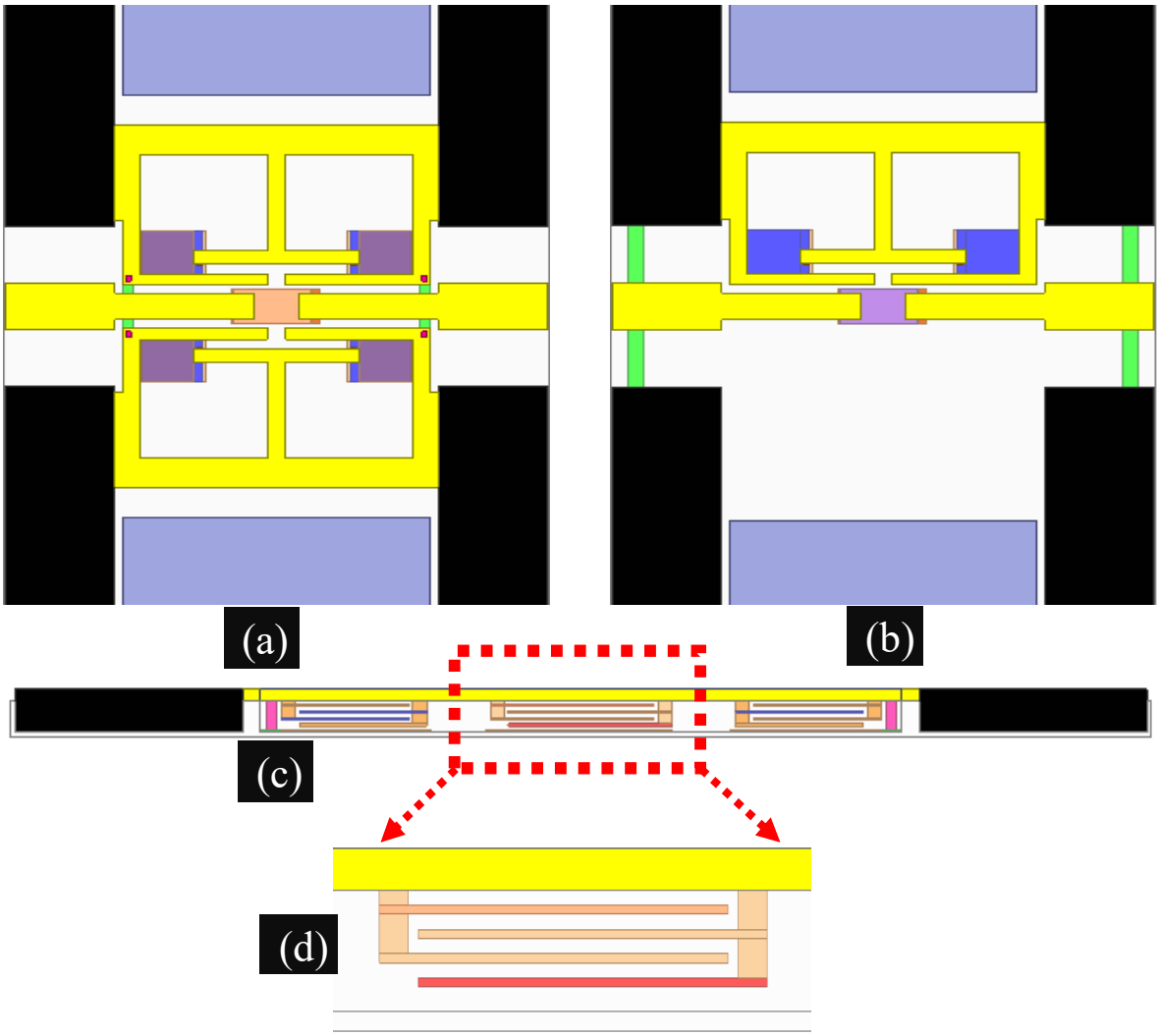


Fig. 2. 13: Layout of the proposed DGS-based BSF prototype (a) symmetric structure. (b) Asymmetric structure. (c) Side View. (d) MIM Capacitors.

2.7 Fabrication and Measurement

2.7.1 Fabrication and Measurement Setup

The proposed design of DGS-based BSF was implemented in 1P6M layer 0.18-µm CMOS technology. The layout of the proposed designs is shown in Figure 2.13. All the signal and the ground metals are made in top metal layer whereas MIM capacitors are designed using the stacked materials. Two prototypes of proposed BSF (a) symmetric and (b) asymmetric are Fig. 2.14 and Fig 2.15 are fabricated. The intrinsic dimensions of proposed DGS-BSF are most

compact among the literatures; symmetric BSF is $0.037\lambda_g \times 0.045\lambda_g$, whereas assymmetric BSF is $0.037\,\lambda_g \times 0.024\,\lambda_g$. The fabricated chips were measured in the measurement environment setup consisting of a Keysight N5227B PNA microwave network analyzer, two Keysight N5293AX03 110 GHz frequency extenders, and two 150 µm GSG probes.

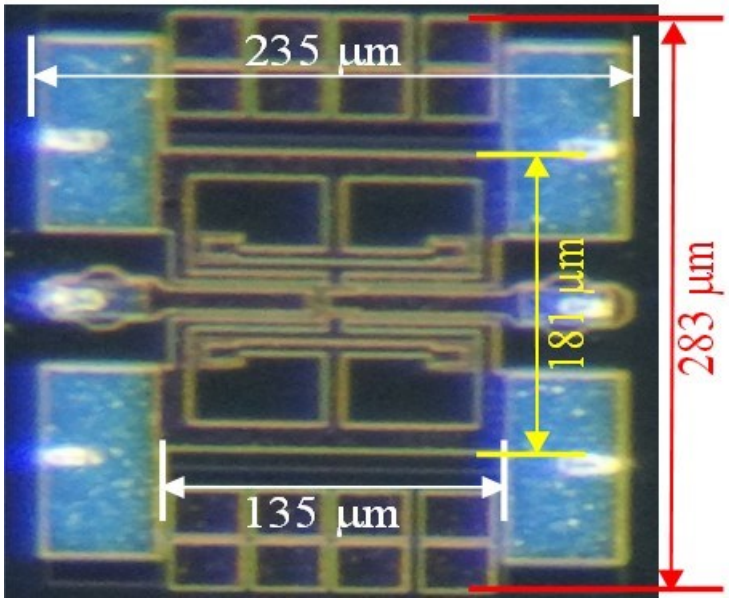


Fig. 2. 14: Proposed DGS-based BSF prototype micrograph of symmetric structure.

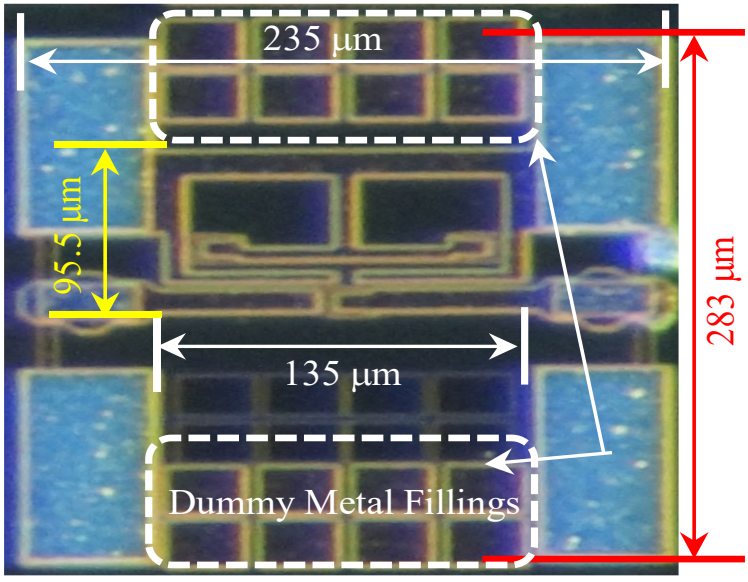


Fig. 2. 15: Proposed DGS-based BSF prototype micrograph of asymmetric structure.

2.7.2 Measurement Results

Measurement setup presents the results from 20 GHz to 110 GHz. The simulations are done without including measurement pads, whereas measured results are shown after performing L-2L de-embedding. The returned loss (magnitude of reflection coefficient) measurement result of the proposed symmetric BSF demonstrates 1.78 dB at 53.2 GHz stopband frequency as shown in Fig. 2.16. Similarly, Fig. 2.17 shows that the maximum negative group delay is measured 161 pS. The calculated value of Q_l and Q_u are found to be 4.91 and 26.2, respectively. Moreover, it is noteworthy that the S-parameters and negative group delay results obtained from measurements accurately align with the nature of the simulation results across the entire frequency range of measurement.

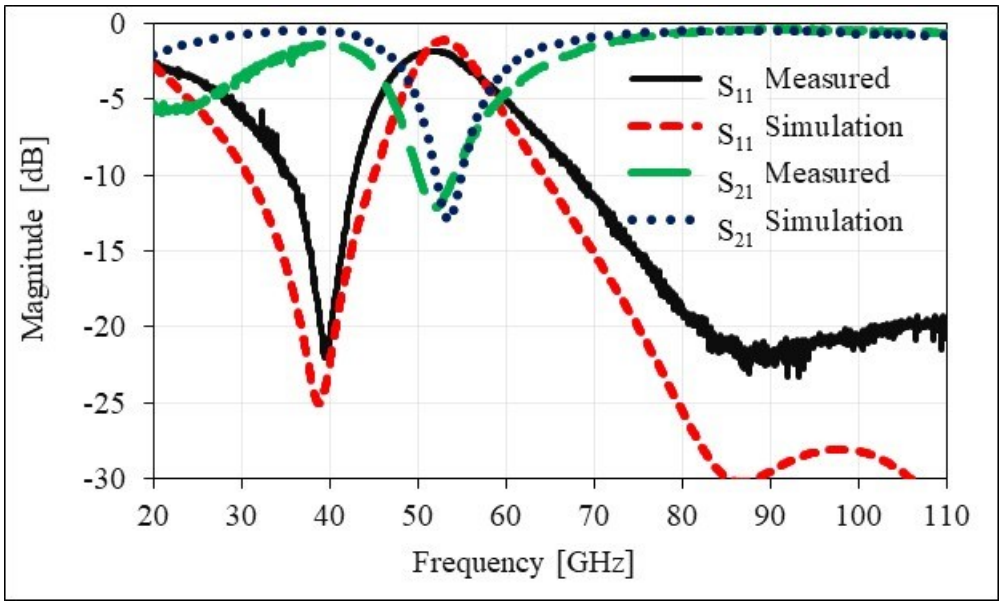


Fig. 2. 16: Simulated and the measured S-parameters results of the proposed symmetric DGS-based BSF.

Similarly, the measured return loss result of the proposed asymmetric design at stopband frequency of 52 GHz is 2.2 dB. Similarly, the measured maximum negative group delay is 118 pS, as shown in Fig. 2.18 and 2.19. The measured Q_l and Q_u are obtained as 4.57 and 20.55, respectively. The higher loss attributed by the asymmetric design is mainly due to the loss from the open structure in signal line side. In both these designs the group delay is computed by method in [5], [35] as;

$$group\ delay = t_{gd} = -\frac{\partial(\angle S_{21})}{\partial\omega}. \tag{2.17}$$

where, $\angle S_{21}$ is the phase of the transmission coefficient and the ω is the angular frequency.

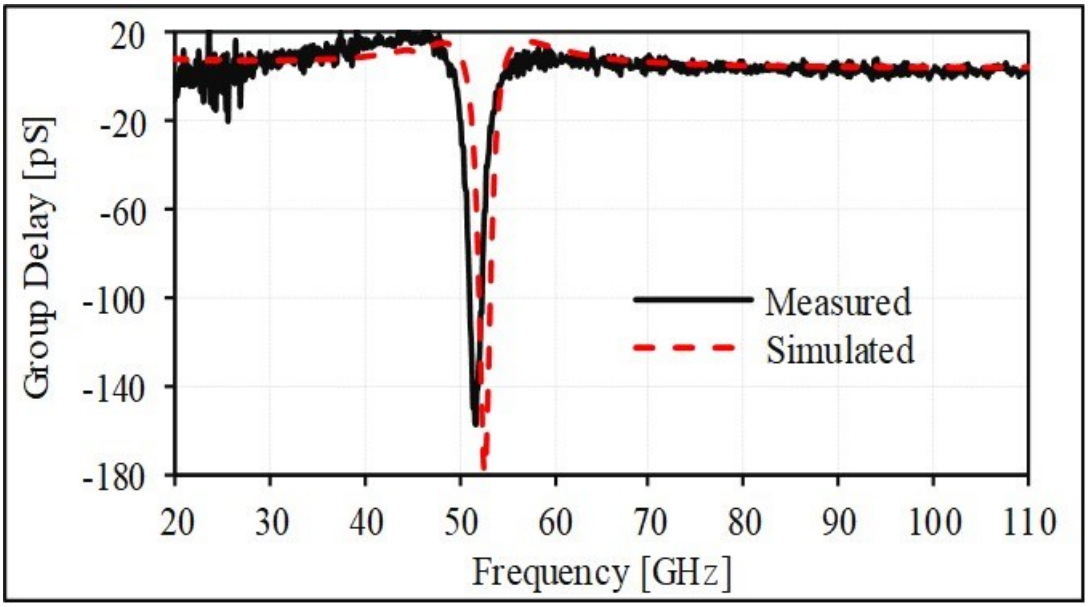


Fig. 2. 17: Simulated and the measured negative group delays results of the proposed symmetric DGS-based BSF.

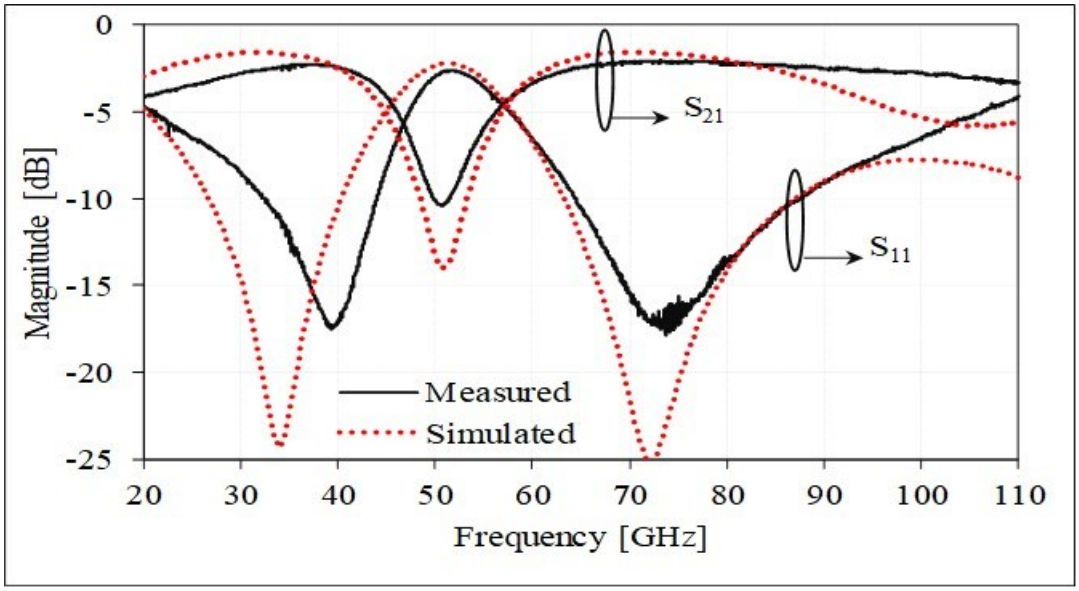


Fig. 2. 18: Simulated and the measured S-parameters results of the proposed asymmetric DGS-based BSF.

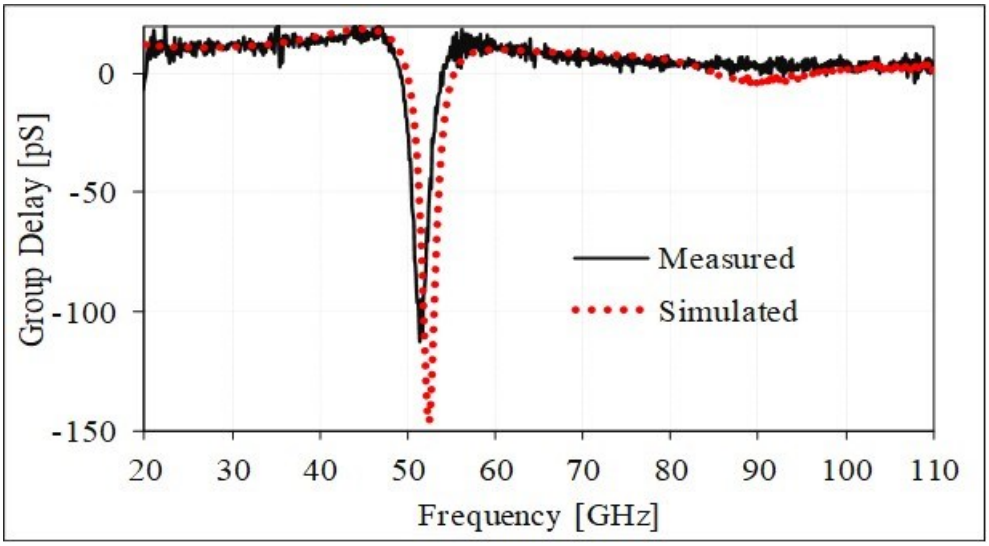


Fig. 2. 19: Simulated and the measured negative group delays results of the proposed asymmetric DGS-based BSF.

Table 2. 5: Performance comparison of the proposed DGS-based BSF with other state-of-arts

Ref.	[34]	**This Work Symmetric**	**This Work Asymmetric**
f_o [GHz]	30/85; 30/80	**53.2**	**52**
CMOS Technology	0.18-µm	**0.18-µm**	**0.18-µm**
Measured Q_l and Q_u	N/A	**4.91 and 26.8**	**4.57 and 20.55**
Return loss [dB] at f_0	4/3; 3/5 *	**1.78**	**2.2**
Max attenuation [dB] at f_0	25/18; 35/25	**14.2**	**11.8**
Max. return loss [dB] at transmission poles [GHz]	23@12, 11@58, 5@90; 20@12, 22@50, 11@70, 22@98*	**23.1@39.8, 25@86**	**17.8@39.2, 17.9@74.4**
Dimension ($\lambda_g \times \lambda_g$)	0.25 × 0.25; 0.48 × 0.10	**0.037 × 0.045**	**0.037 × 0.024**

*estimated from graphs.

2.7.3 Performance Comparison

Table 2.5 presents the state-of-the-art performance comparison results of the proposed BSFs. The proposed BSFs have both a compact circuit size, high Q-factor, and good return losses. Also, the return loss result at the center frequency is better than the other state of arts making them good candidate for both filtering and VCO applications.

2.8 Summary

In this chapter, a novel on-chip BSF design using DGS is introduced and implemented for millimeter-wave applications in CMOS technology. The newly proposed BSFs have transmission poles on both sides of the parallel resonance, and their positions can be independently controlled through the innovative DGS structure. This structure incorporates a capacitively loaded T-shape within the original large loop DGS configuration. Two prototypes (symmetric and asymmetric structures) were fabricated in a 0.18-µm CMOS technology. Experimental measurements demonstrate excellent agreement with the simulated results. Despite reducing the size by nearly 50%, the proposed asymmetric BSF maintains a high Q-factor. Having both compact size and high *Q*-factor, the proposed BSF can be applicable for both on-chip filters application as well as a resonator tank circuit to improve the phase noise of a VCO for millimeter wave and above frequency bands applications.

Chapter 3: Millimeter Wave Band Resonators Design using Substrate Integrate Waveguide Technology

3.1 Introduction

In previous chapter, we developed high Q-filters in the millimeter wave bands. There are some issues for high frequency DGS designs above millimeter wave band as:

- **Imperfect Grounding:** At high frequency above millimeter wave, free space wavelength (λ) becomes smaller like for 100 GHz it is 3 mm. So, any defects around the proximity of the guided wavelength (λ_g) makes the structure radiate. For DGS structures are designed my introducing the defects using slots, or any other shapes. So, inadequate grounding or discontinuities in the ground plane can lead to additional losses from radiation and reduced performance of the DGS structure above millimeter wave bands.
- **Interference with Adjacent Components:** High-frequency circuits are more susceptible to interference from nearby components. The presence of other components around the open structures like DGS can lead to crosstalk and parasitic effects, resulting in additional losses.

Traditional non-planar waveguides, such as rectangular and cylindrical waveguides, have been extensively utilized in wireless systems due to their high unloaded quality factor and efficient transmission of electromagnetic (EM) waves with minimal losses. However, these waveguides suffer from a major drawback: they are bulky and can only operate above the cutoff frequency, limiting their use in miniaturized devices and integration with planar technologies.

To address these limitations, Substrate Integrated Waveguide (SIW) technology has emerged as a promising solution. SIW, is also known by name post-wall waveguide (PWW), is a planar waveguide fabricated on the normal dielectric substrate. It employs metalized vias or posts arranged along the length and width of the substrate, forming a waveguide-like structure. The key advantages of SIW design is its high unloaded Q factor. Also, they offer lower conduction losses in comparison to microstrip and coplanar waveguides. The dielectric substrate facilitates isolation and confinement of the EM waves, leading to improved overall performance.

SIW technology is particularly suitable for integration with planar circuit structures, where high-quality factor components are desired. From last decade, SIW has getting attention and are widely adopted for various fields, including RF and microwave communications, radar systems, biomedical applications, and more. By utilizing SIW technology, it becomes possible

to design and implement various components such as filters, antennas, resonators/cavities, transmission lines, couplers, and duplexers in a compact and cost-effective manner. The advantages of SIW technology, including small size, low cost, and high performance, make it a valuable choice for commercial applications in the wireless communication industry.

3.2 SIW Implementation in PCB Technology

SIW consists of metalized vias/posts that are drilled through dielectric material to make top and bottom metal connection and substitute the metallic walls of non-planar regular metallic waveguides as shown in Fig. 3.1. SIW can be easily fabricated in planer structures with current printed circuit board (PCB) technologies. The summarized conditions based on which the SIW structures have been designed to functioned properly are [36]-[37]:

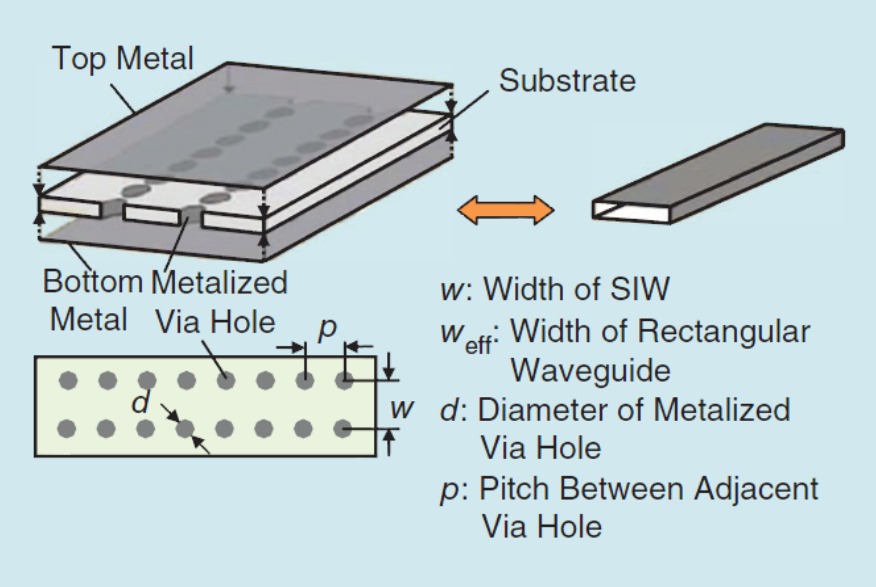


Fig. 3. 1: SIW structure and its equivalent rectangular waveguide (from [36]).

$$\left.\begin{array}{c} p > d \\ \frac{p}{\lambda_c} < 0.25 \\ \frac{a_l}{k_0} < 1x10^{-4} \\ \frac{p}{\lambda_c} > 0.05 \end{array}\right\} \quad (3.1)$$

Where a_l is the total loss and k_0 is the wave number in the free space. These equations ensure that the vias spacing should be larger than the vias diameter to practically make the fabrication

of vias possible. In the fundamental mode of the SIW waveguide, the equivalent width of the SIW is calculated as [37],

$$w_{eff} = w - 1.08 \times \frac{d^2}{p} + 0.1 \times \frac{d^2}{w} \tag{3.2}$$

provided that vias spacing p is sufficiently small. These two equations are found simplified for many SIW derivatives to make the calculations easy. According to [36], there are two important properties of SIW structures: (a) since the truncated sides walls cannot support longitudinal current (i.e. the electrical current are not able to propagate from via to via), SIW structures can only supports the propagation of quasi-transverse electric (TE) modes in waveguide and (b) the substrate thickness is always much smaller than the width of SIW structure (i.e. the thickness is too low that the TM modes cut-off frequency is much higher than the dominant mode), only TE_{m0} modes are dominant and if by any case TM modes are generated they are very weak. Due to this phenomenon, SIW derivatives can be easily fabricated based on only TE modes.

3.3 Wave Propagation Characteristics in SIW

The wave propagation characteristics in SIW are determined by the structure and design parameters of the waveguide. Here are some key characteristics:

1. Guided Mode Propagation: SIW supports guided modes, which are electromagnetic waves that propagate within the waveguide structure. These guided modes can be either transverse electric (TE) or transverse magnetic (TM) modes, depending on the polarization of the electromagnetic field. Most SIW in PCB or CMOS technology has width>>> height. So, fundamental dominant mode is always TE mode. In most cases, unlike in PCB, CMOS vertical height is ~10 μm, TM mode are mostly not possible.
2. Cutoff Frequency: SIW has a cutoff frequency, below which the guided modes cannot propagate. The cutoff frequency depends on dimensions and the geometry of SIW, such as width and height of the waveguide and the spacing between the metalized vias/posts.
3. Dispersion: SIW exhibits dispersive characteristics, which means that the phase velocity of the guided modes depends on their frequency. This can cause frequency-dependent phase delays and group delays in signal propagating through the designed SIW structure.
4. Attenuation: Like microstrip and CPW transmission lines, SIW experiences attenuation due to conduction losses in the metalized vias/posts and dielectric losses in the substrate material.

The amount of attenuation depends on the material properties, dimensions, and fabrication quality of the SIW and are usually lower than conventional microstrip and CPW lines making them suitable for high frequency applications.

Understanding these wave propagation characteristics is crucial for designing and optimizing SIW-based circuits and components, such as filters, resonators, antennas, and transmission lines. It enables RF engineers to control and manipulate the behavior of electromagnetic waves within the SIW structure to get desired performance specifications in terms of power handling, frequency response, and signal integrity.

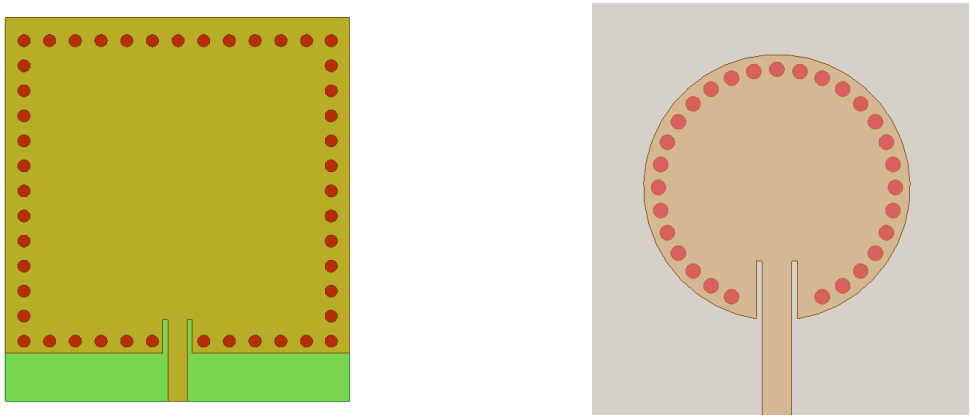
3.4 Millimeter Wave SIW Implementation in CMOS Technology

SIW can be implemented in commercial CMOS technology, similar to PCB technology. Due to its high flexibility and easy planar integration, SIW structures can be utilized to design various components like transmission lines, resonators/cavities, filters, couplers, antennas, duplexers, and more. However, there are certain issues that need to be considered when designing SIW in CMOS technology [38]-[39]:

- **Foundry-wide metal rules for fabrication**: In the CMOS technology used, there are prescribed requirements for the wide metal used, which specify the inclusion of slots at every 35 μm × 35 μm interval. Ideally, the top and bottom metal plates of the SIW should be perfectly closed to avoid additional issues. To address this, smaller-sized slots (less than 5 μm × 5 μm) are created in the CMOS fabrication process where wide metal is used.
- **Available via size**: In the employed CMOS technology, predefined vias of different sizes exist between metal layers, which may not be suitable for SIW design. To achieve solid vias, smaller vias are grouped together. However, it is not possible to realize a design with a single solid via from the top to the bottom layer, which can result in changes in the measured results of the fabricated design.
- **Foundry dummy metal filling rule**: In order to finalize the tapeout of the design, the foundry may require specific metal density filling for each metal layer. This can lead to an increase in the overall size of the design and can also affect its performance. Designers need to be mindful of the metal fillings to avoid excessive additional loss.

3.5 On-chip Miniaturized 60 GHz SIW Resonator Design

Generally, SIW waveguide have two metallic plates top and bottom on the substrate and sideways two parallel metalized vias running along the length of this dielectric substrate. So, like in non-planer waveguide cavity, if we block this SIW structure from two edges with the same vias, SIS cavity is possible. If performs like that non-planer waveguide cavity. Simple structure of SIW resonator is shown in Fig.3.2.



(a) (b)

Fig. 3. 2: SIW Resonators (a) Square, (b) Circular.

Simplified equations for determining the dimension of rectangular waveguide resonators are presented in various research [40]-[50]. For the fundamental mode frequency (TE_{101}), the dimension of square SIW is calculated as,

$$f_{TE_{101}} = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{(\frac{\pi}{W_{eff}})^2 + (\frac{\pi}{L_{eff}})^2} \tag{3.3}$$

$$W_{eff} = W_{SIW} - \frac{d^2}{0.95p} \; and \; L_{eff} = L_{SIW} - \frac{d^2}{0.95p} \tag{3.4}$$

$$p < 4d \;\; and \; p < \lambda_0 (\frac{\varepsilon_r}{2})^{1/2} \tag{3.5}$$

where, $f_{TE_{101}}$ is the fundamental (TE_{101}) resonant frequency, c is free space light speed, μ_r and ε_r are the relative permeability and permittivity of the substrate used, respectively. W_{eff} and L_{eff} are equivalent resonant cavity dimensions. W_{SIW} and L_{SIW} are the actual size of standard SIW resonator whereas d and p are diameter and pitch of metallic posts. λ_0 is the free space

wavelength of light for fundamental resonant frequency. Design equations for circular SIW resonator are presented in [51]-[52].

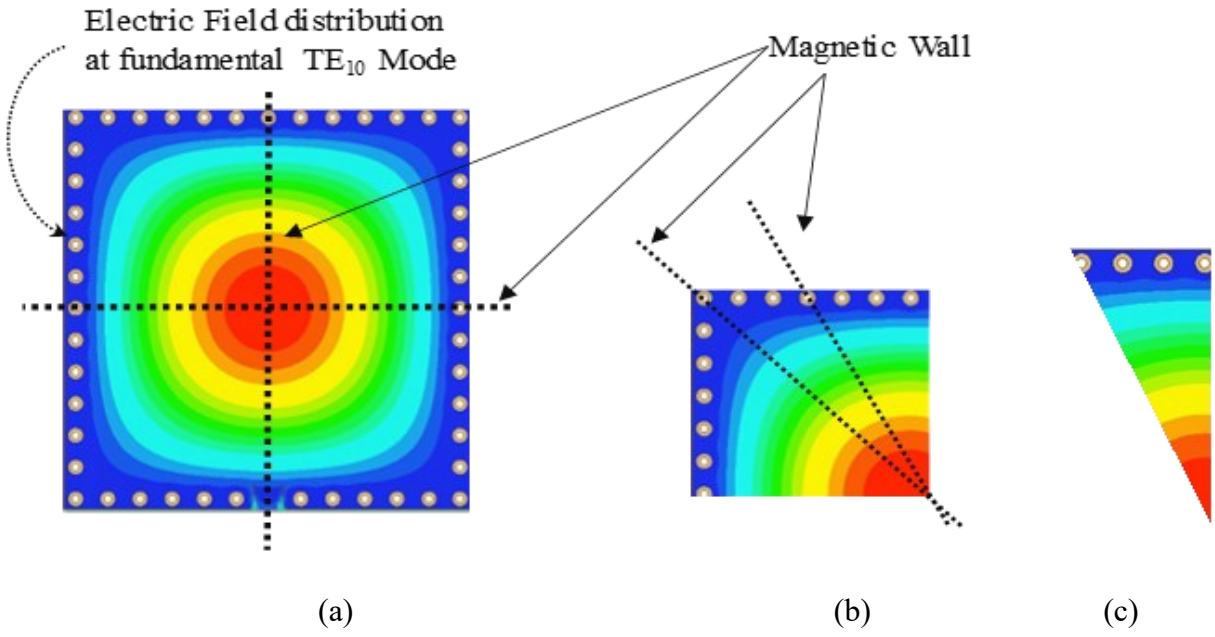


Fig. 3. 3: SIW resonator structures. (a) full-mode. (b) Quarter-mode. (c) Sixteenth-mode.

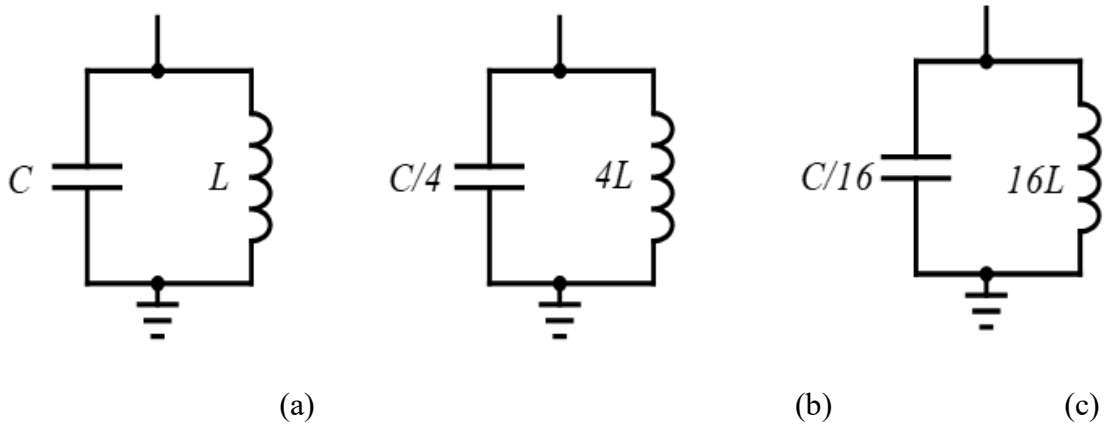


Fig. 3. 4: SIW resonators simplified LC resonance circuit representation of. (a) full-mode. (b) quarter-mode. (c) sixteenth-mode.

Standard SIW resonators can be miniaturized by taking parts of this standard resonator to form half mode, quarter mode, eighth mode, sixteenth mode, and so on still maintaining the same

resonance frequency. These advantages significant lower down the size of resonators and offers higher flexibility to adopt them for miniaturized SIW derivatives like filters, antennas, etc.

3.5.1 n^{th} Mode Standard SIW Resonator

In the fundamental TE10 mode of a SIW resonator, there exist multiple perfect symmetry planes (magnetic walls), represented by broken lines in Fig. 3.3(a). These symmetry planes allow the resonator to be cut without affecting its original resonance. By making a single symmetric cut, the resonator can achieve the half mode of the standard SIW. Further bisecting this cut results in the quarter mode, and continuing this process yields the eighth mode, and so on. Fig. 3.3(c) demonstrates that a 1/16th mode SIW is obtained by making a total of four symmetric plane cuts in the standard SIW. This way, the standard SIW can be miniaturized multiple times. However, in SIW resonators operating in higher modes (nth mode), due to the open sideways in the resonator structure, the return loss becomes worse.

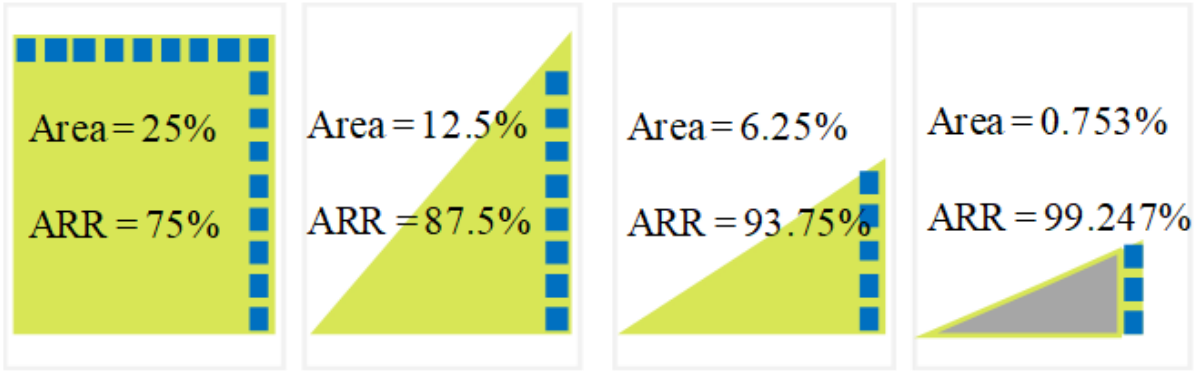
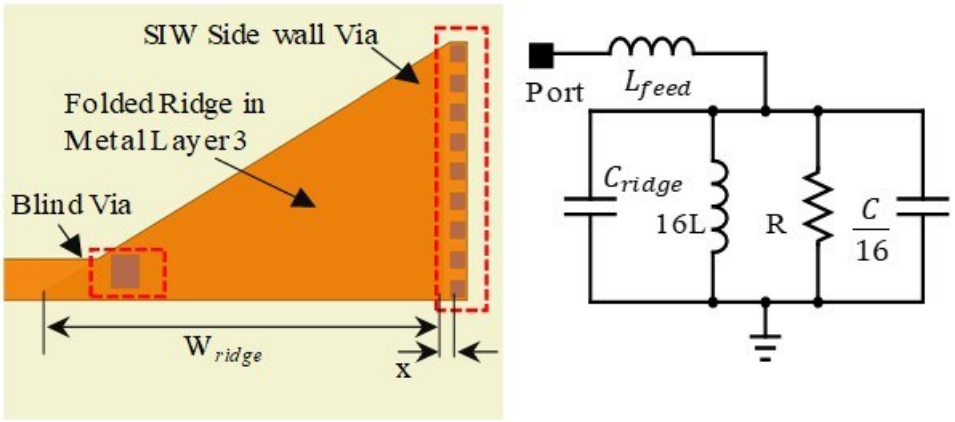


*Fig. 3. 5: Miniaturized SIW resonator. (a) Quarter-mode. (b) Eighth mode. (c) Sixteenth mode. (d) Sixteenth mode SIW with folded ridge. *ARR = Area Reduction Ratio compared to standard SIW at the same resonance.*

3.5.2 Folded Ridge SIW Resonator

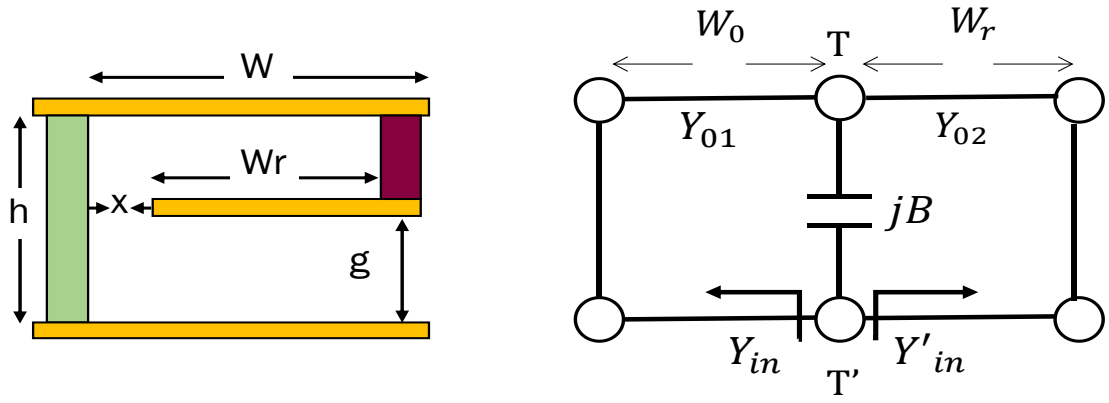
Fig. 3.6 (a) presents a simplified design of sixteenth mode SIW resonator employed with folded ridge structure. The introduction of the folded ridge structure introduces two types of capacitances: (a) from the height between the ridge and main SIW cavity top/bottom walls and (b) the folded ridge closeness with the main sidewall of the SIW vias [53]- [55]. The appearance

of these additional capacitances from folded ridge drops down the resonance frequency, leading to significant miniaturization.



(a) (b)

Fig. 3. 6: (a) Sixteenth mode SIW folded ridge resonator structure and (b) its LC resonance circuit representation.



(a) (b)

Fig. 3. 7: Folded ridge SIW resonator (a) cross- section view. (b) transverse equivalent circuit model.

This equivalent capacitance resulting from the additional capacitances described earlier is combined and denoted as C_{ridge} in Fig. 3.6(b). Due to this C_{ridge} the resonance frequency lowers, enabling significant miniaturization. the resonance frequency lowers, enabling significant miniaturization. The resonance frequency of folded ridge resonator structure is estimated by the expression [53]:

$$-cot\left(\frac{2\pi}{\lambda_c}W_0\right)+\frac{B}{Y_{01}}+\frac{Y_{02}}{Y_{01}}tan\left(\frac{2\pi}{\lambda_c}W_r\right)=0 \tag{3.6}$$

where, the dimensions of waveguide widths and ridges are respectively W and W_r, as shown in Fig. 3.7(a). λc is the wavelength of desired frequency, Y_{01} and Y_{02} the transverse characteristic admittance of the waveguide channel and ridge sections, respectively. Similarly, B is the transverse step capacitance that appears due to the transition of the channel and ridge. The terms B/Y_{01} and Y_{02}/Y_{01} are obtained using the equations presented in references [53] and [56].

In EM simulation, these values can be obtained by optimizing the different parameters like position of the ridge in the used CMOS technology i.e., between metal layers 2 to 5 considering that the bottom layer and the top metal layer are used for the top and bottom plane. Also, the resonance frequency can be altered by changing the width of the ridge as shown in Fig. 3.8. If we want to achieve maximum size reduction using the same structure, the entire region of the resonators can be filled with the ridge structure, and we can achieve the much lower frequency. Also, reflection coefficient of cavity can be improved by increasing the size of the folded ridge.

In this proposed folded ridge design, we use both advantages of size reduction and the reflection coefficient i.e., external quality factor improvement by employing the maximum with folded ridge structure inside the cavity. However, for designing the filter, maximum ridge width may not be effective as requires the strong coupling, making the filter design using the maximum miniaturized cavity difficult to implemented.

Table 3. 1: Comparison of size and Q_u of quarter mode, eighth mode, sixteenth mode, and sixteenth mode folded ridge SIW resonators shown in Fig. 3.5.

Different SIW Design at f_o = 60 GHz	Size mm^2	Area with respect to Standard SIW	Q_u
Quarter Mode	0.785	25 %	15.6
Eighth Mode	0.3925	12.5 %	14.2
Sixteenth Mode	0.1963	6.25 %	12.96
Folded Ridge Sixteenth Mode	0.0236	0.753 %	9.84

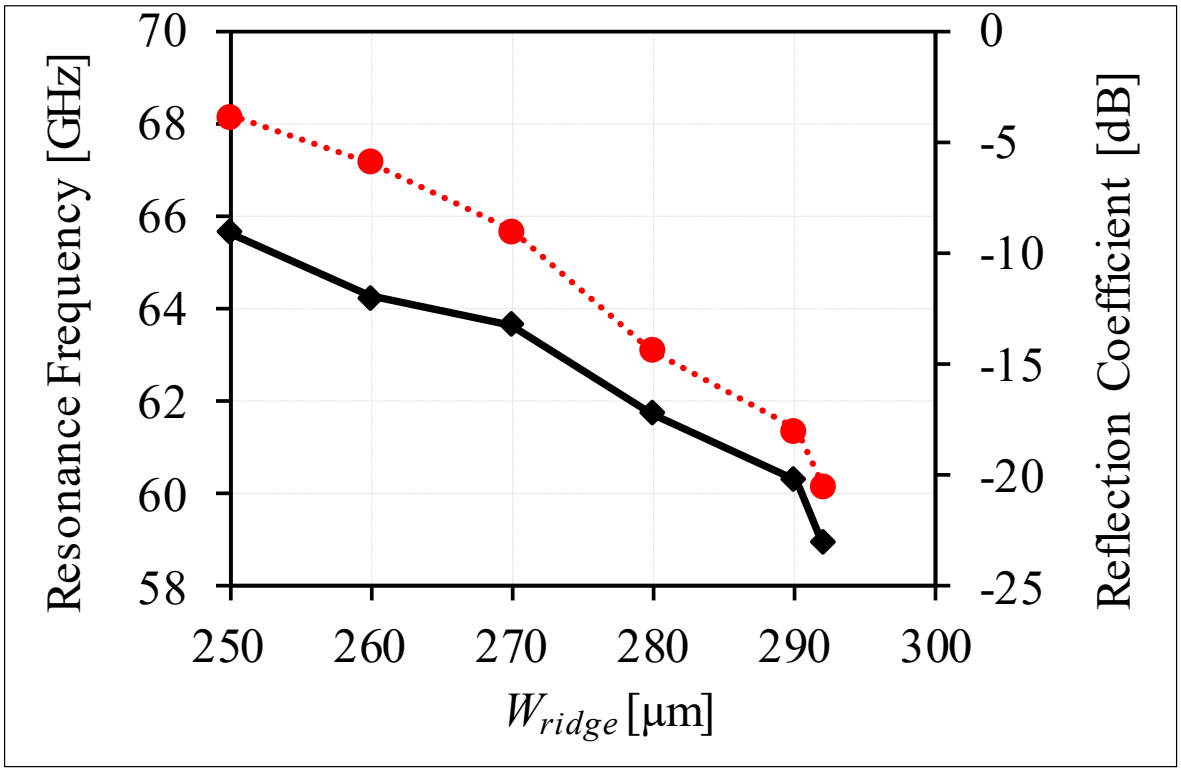
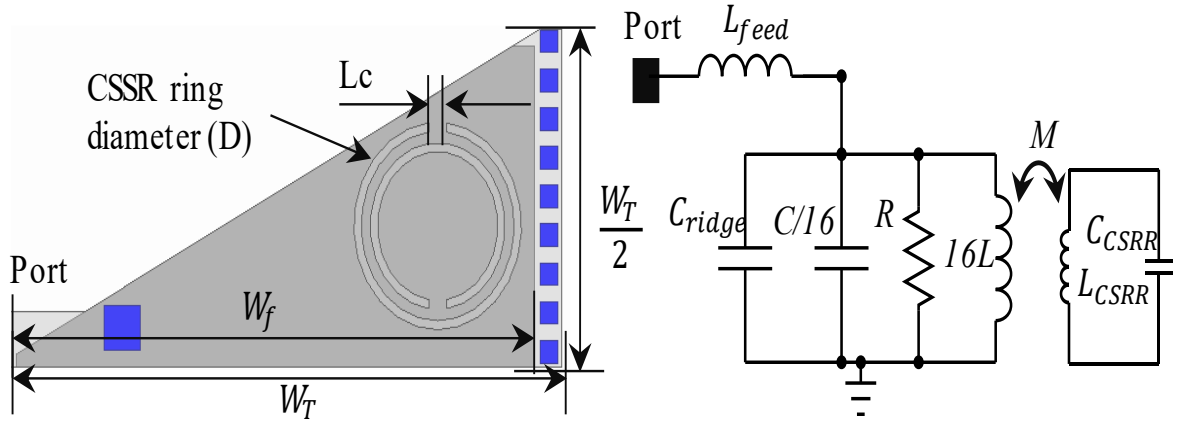


Fig. 3. 8: Frequency and reflection coefficient vs. varying ridge of Fig. 3.6.



(a) (b)

Fig. 3. 9: (a) Proposed inductively loaded sixteenth mode folded ridge resonator with CSRR. (b) its LC equivalent resonance circuit representation.

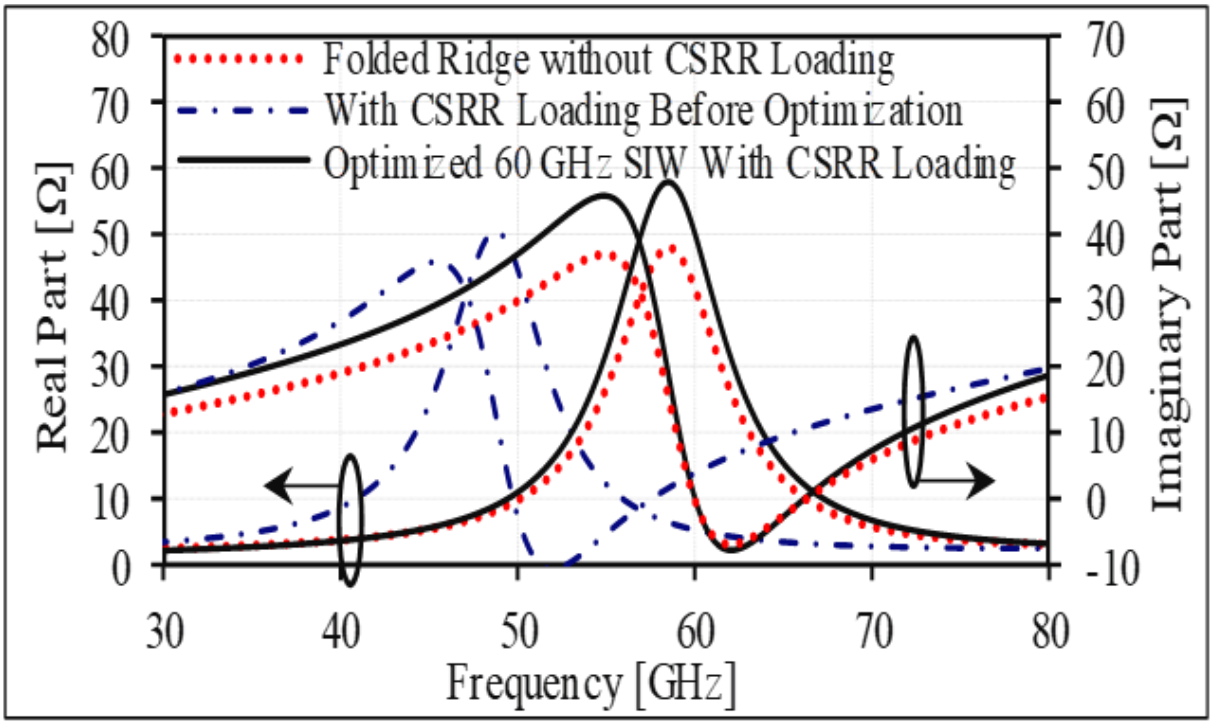


Fig. 3. 10: Proposed sixteenth-mode folded ridge SIW input impedance with and without CSRRs loadings.

3.5.3 SIW Resonator with Folded Ridge Structure and CSRR Loadings

The sixteenth mode folded ridge SIW resonator has maximum miniaturization. However, in this highly miniaturized state, the increased capacitance from the ridge leads to a degradation of reflection coefficient due to mismatch. To address this issue, the proposed design incorporates a CSRR resonators loaded inside the sixteenth mode folded ridge SIW resonator. The CSRR and SIW resonator coupling results in an effective inductance that facilitates for achieving internal matching within the folded ridge structure.

Fig. 3.9(a) shows a design which is loaded with the largest possible CSRR, having its self-resonance at approximately 180 GHz. This loaded CSRR couples with the SIW, as depicted in Fig.3.9(b) [6]. At the frequency of interest, which is 60 GHz in this case, the inductive coupling in-between the CSRR and resonator plays a dominant role. Without considering the impact of feedline, proposed cavity equivalent circuit representation as shown in Fig.3.9(b) can be used to analyzed input impedance expression (3.15) as follows:

$$Z_{in} = \frac{R}{R^2\left(\frac{A}{B}\right)^2 + 1} + j\frac{R^2}{R^2\left(\frac{A}{B}\right) + \left(\frac{B}{A}\right)} \tag{3.15}$$

where, $A = \omega^4 C_1 C_2 (L_1 L_2 - M^2) - \omega^2 (L_1 C_1 + L_2 C_2) + 1$,

$B = L_1 - \omega^2 C_2 (L_1 L_2 - M^2)$,

R is the parallel equivalent resistance appeared due to dielectric and vias conduction losses, $L_1 = 16L$, $L2 = L_{CSSR}$, $C1 = (C/16 + C_{ridge})$, and $C_2 = C_{CSRR}$. Equation (3.15) shows that the loaded CSRR provides a matching of input impedance in both real and the imaginary parts within the resonator. Without CSRR loading, such matching would need to be achieved externally, either through transmission lines or other structures, leading to a larger chip size. However, by incorporating CSRR loading, the matching is achieved internally, resulting in a more compact design. Fig. 3.10 illustrates the input impedance characteristics of this miniaturized resonator without and with CSRR loadings. The graph demonstrates that at the desired 60 GHz resonance frequency, the CSRR loading achieves 50 Ω perfect matching internally, ensuring optimal performance. Table 3.2 shows the resonator dimension that are used for Fig.3.10.

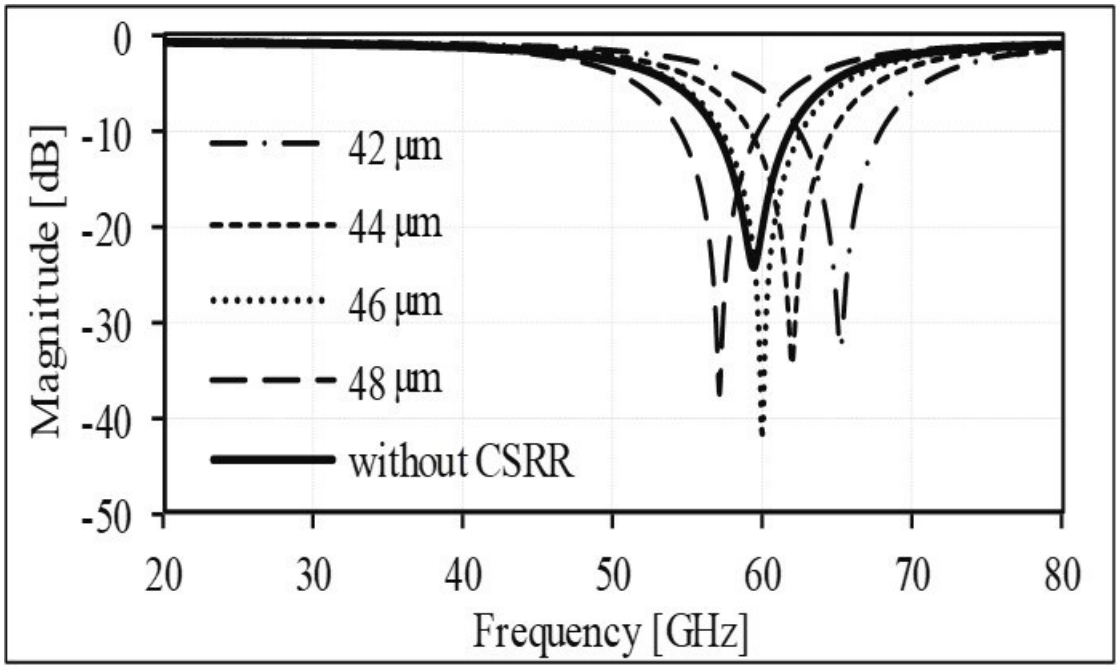


Fig. 3. 11: Investigation of reflection coefficient with different size of CSRRs in proposed folded ridge sixteenth mode SIW resonator.

When the diameter of the CSRR is changed in the cavity resonator design, the effective inductance undergoes variations, leading to corresponding changes in the resonance frequency. This relationship is illustrated in Fig.3.11. Larger the diameter, larger the couplings. Therefore, resonance frequency changes as the CSRR diameter changes. Finally, the resonator size and the CSRR size are optimized to achieve desired resonance frequency at 60 GHz.

Table 3. 2: Analysis of resonators with different dimensions used in Fig. 3.10

Cavity Design	W_T	W_f	D
Folded Ridge without CSRR Loading	310	304	—
With CSRR Loading Before Optimization	310	304	52
Optimized 60 GHz Cavity with CSRR Loading	276	260	46

Table 3.3 presents the computed Q-factors for sixteenth mode folded ridge SIW resonators without and with CSRR loading. The dimensions used for these simulations are presented in Table 3.2. The Q_u was obtained using eigenmode simulation results in HFSS, and the Q_e was calculated from the group delay [57]. The Q_l was calculated as [5], [58],

$$\frac{1}{Q_l} = \frac{1}{Q_e} + \frac{1}{Q_u} \tag{3.16}$$

Table 3.3 illustrates that the incorporation of CSRR loading leads to an improvement in Q_e, resulting in enhanced Q_l of the proposed resonator. This improvement is attributed to the internal matching provided within the resonator by the CSRR loading.

Table 3. 3: Comparisons Q-factors of sixteenth mode folded ridge SIW resonators without and with CSRR loading all designed at the same 60 GHz resonance frequency.

Design	Q_u	Q_e	Q_l
Without CSRR	9.84	64.1	8.53
With CSRR	9.36	146	8.796

3.5.4 SIW Resonator with Folded Ridge Structure and Multiple CSRR Loadings

The effect of multiple CSRR loadings is studied in the proposed design. Multiple CSRR resonators are loaded in sixteenth mode folded ridge SIW resonator. Fig. 3.12 shows the proposed resonator loaded with different numbers of CSRR resonators all optimized to 60 GHz resonance. All the designs are optimized to 60 GHz resonance frequencies. The proposed structure presents better return loss with four CSRR loadings because of the increased inductive couplings.

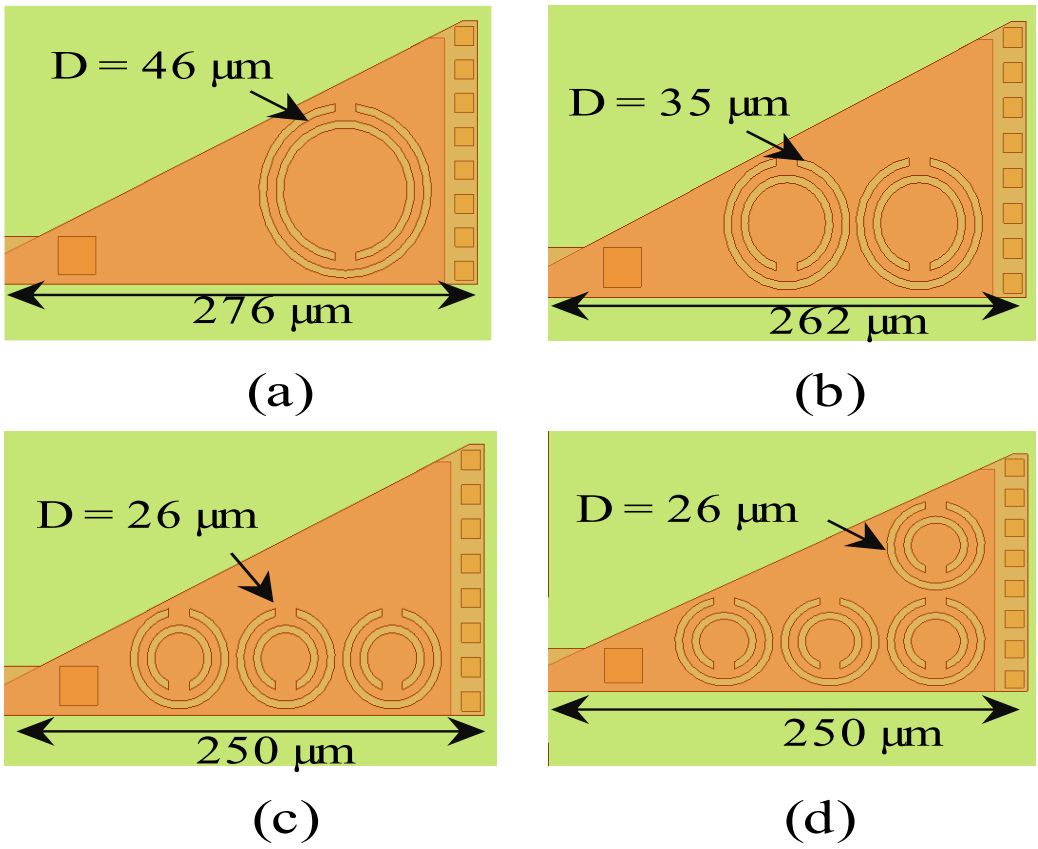


Fig. 3. 12: Inductively loaded CSRR in sixteenth mode SIW resonators with. (a) Single. (b) Two. (c) Three. (d) Four.

The equivalent circuit of the proposed multiple CSRR loadings can be summed up as the added couplings in L_{csrr} and C_{csrr} as presented in Fig.3.9(b). Only difference there will be an additional coupling between the CSRR resonators which is negligible compared to the total couplings of the CSRR resonators with the SIW structure itself. Considering this, multiple CSRR with different dimensions are loaded and simulated as presented in Fig. 3.13. The comparison of Q_l

between all the structures simulated in Fig. 3.13. is presented in Table 3.4, which shows that multiple CSRR loading further reduces the size of the cavity while improving the Q-factor. In conclusion, we achieved both advantages from CSRR loadings (i) low-loss (high Q) design and (ii) size reduction. Such miniaturized cavities have higher potential for the millimeter wave applications.

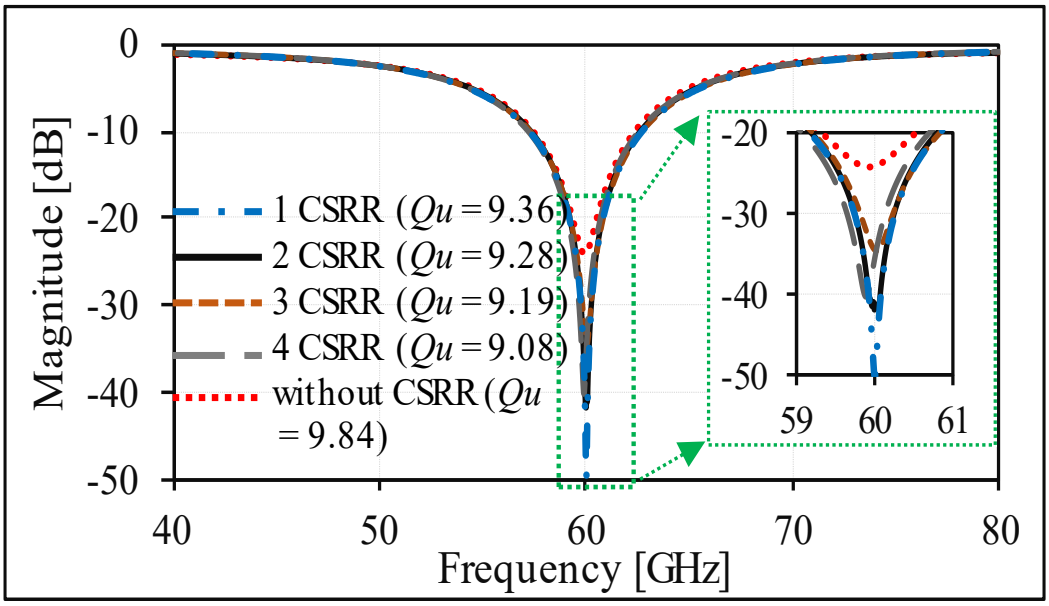


Fig. 3. 13: Reflection coefficient of SIW resonator structures shown in Fig. 3.12 all optimized at the same 60 GHz resonance frequency.

Table 3. 4: Q-factors and size comparison of miniaturized SIW resonators with CSRR loading shown in Fig. 3.12.

Different SIW Design at f_o = 60 GHz	Size reduction compared with folded ridge sixteenth mode SIW	Q_u
Without CSRR	0 %	9.84
With single CSRR	18 %	8.79
With two CSRR	23 %	8.81
With three CSRR	27 %	8.82
With four CSRR	27 %	8.85

3.5.5 Feeding of the Proposed Sixteenth Mode Folded Ridge SIW Resonator

The proposed miniaturized resonators design is investigated using two types of feeding structures: (i) top microstrip line feeding and (ii) transition feeding. The configurations of these feeding structures are depicted in Fig. 3.14. The simulation results of these feeding structures are shown in Fig. 3.15. It is observed that the transition feeding structure exhibits a degradation in the reflection coefficient compared to the top microstrip line feeding. This degradation in the reflection coefficient may be attributed to the signal losses occurring in the transition structures, specifically through two blind vias, which introduce additional impedance mismatches and losses. As a result, the top microstrip line feeding method proves to be more favorable for maintaining a higher return loss and overall performance of the miniaturized resonator design.

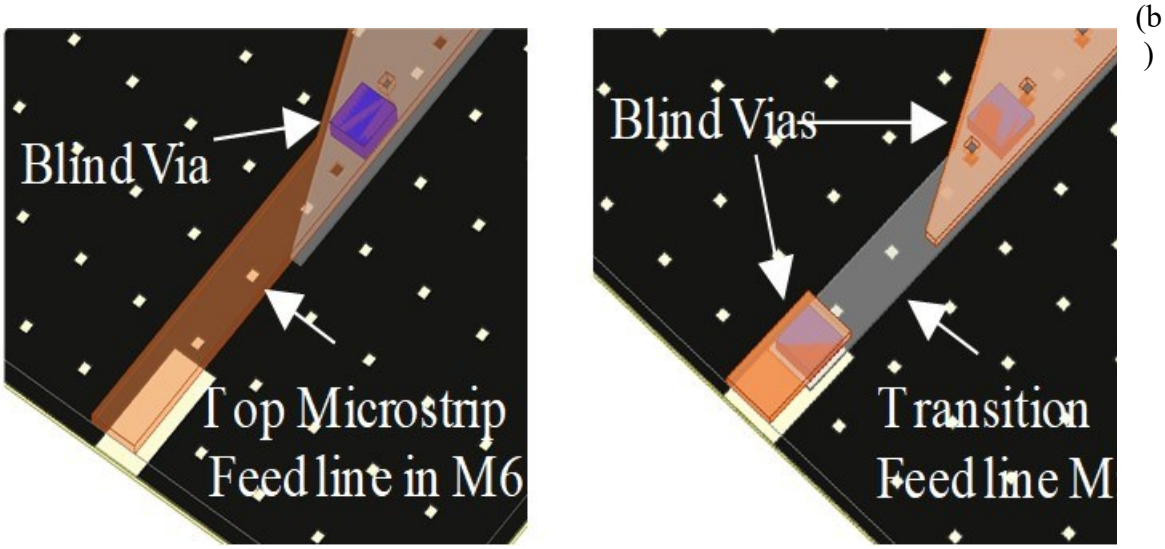


Fig. 3. 14: Proposed sixteenth mode SIW resonators with. (a) top microstrip line feeding. (b) transition feeding.

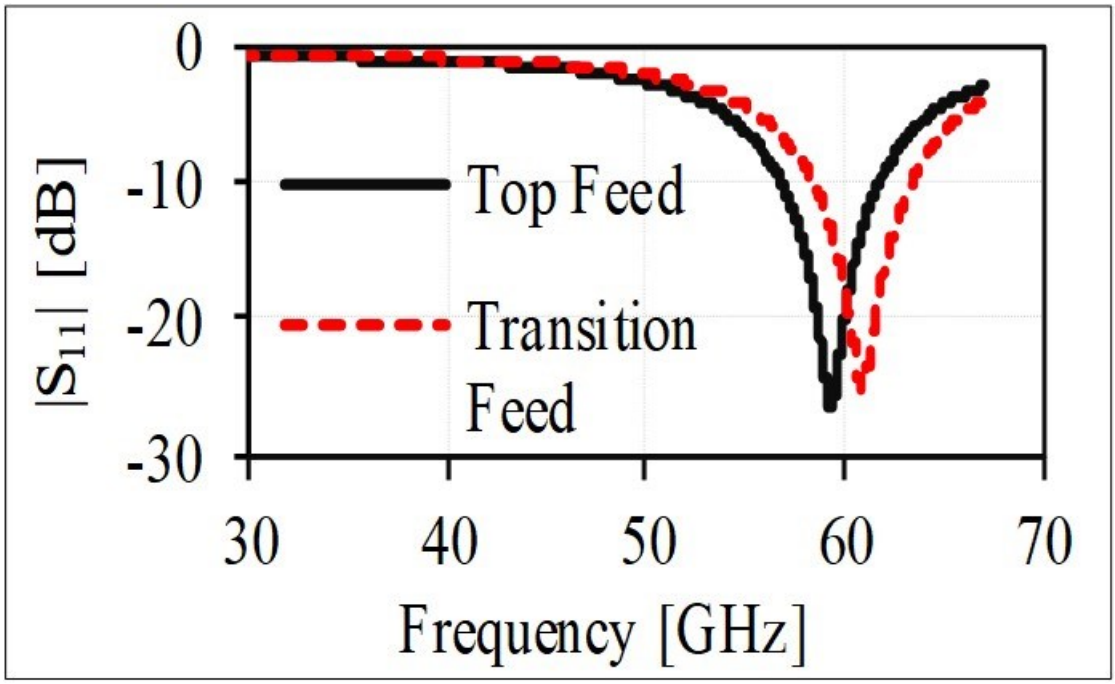


Fig. 3. 15: Different feeding techniques reflection coefficient ($|S_{11}|$) results shown in Fig. 3.14.

3.6 Fabrication and Measurement of the Proposed 60 GHz Miniaturized SIW Resonators Design

All the proposed miniaturized sub-THz band SIW resonators are fabricated using 1P6M CMOS technology, which features six metal layers. The top and bottom planes are constructed using metal layers M6 and M1, respectively, while the ridge is formed in metal layer M3. To establish connections, a blind via (M3 to M6 via) is utilized to link the ridge with the top metal, and an SIW via (M1 to M6 via) connects the top and bottom planes of the resonator. Additionally, slots are etched in the top, ridge, and bottom metals to comply with the wide metal rule of the foundry. To perform all the necessary simulations and optimizations, the ANSYS High-Frequency Structure Simulator (HFSS v2018.01) was used.

3.6.1 Fabricated Designs Layout Preparation

Four prototypes (i) Sixteenth mode folded ridge cavity with top microstrip feeding, (ii) Sixteenth mode folded ridge cavity with transition feeding, (iii) Sixteenth mode folded ridge resonator with single CSRR loadings, and (iv) Sixteenth mode folded ridge resonator with

multiple CSRR loadings, are fabricated for the validation purpose. All the resonators are designed at optimized 60 GHz resonance frequency. Fig.3.16 to Fig.3.19 presents the fabricated layouts of the proposed resonators for final fabrications. Final layouts are shown here after passing all the design rule check for the final fabrication.

Both feeding structures are prepared for sixteenth mode folded ridge SIW structure. The physical layout of both feeding structures is exactly the same as embedded in the EM model in Fig. 3.14. Two blind vias from metal layer 6 to metal layer 3 are used for the transition structures for the input feeding line.

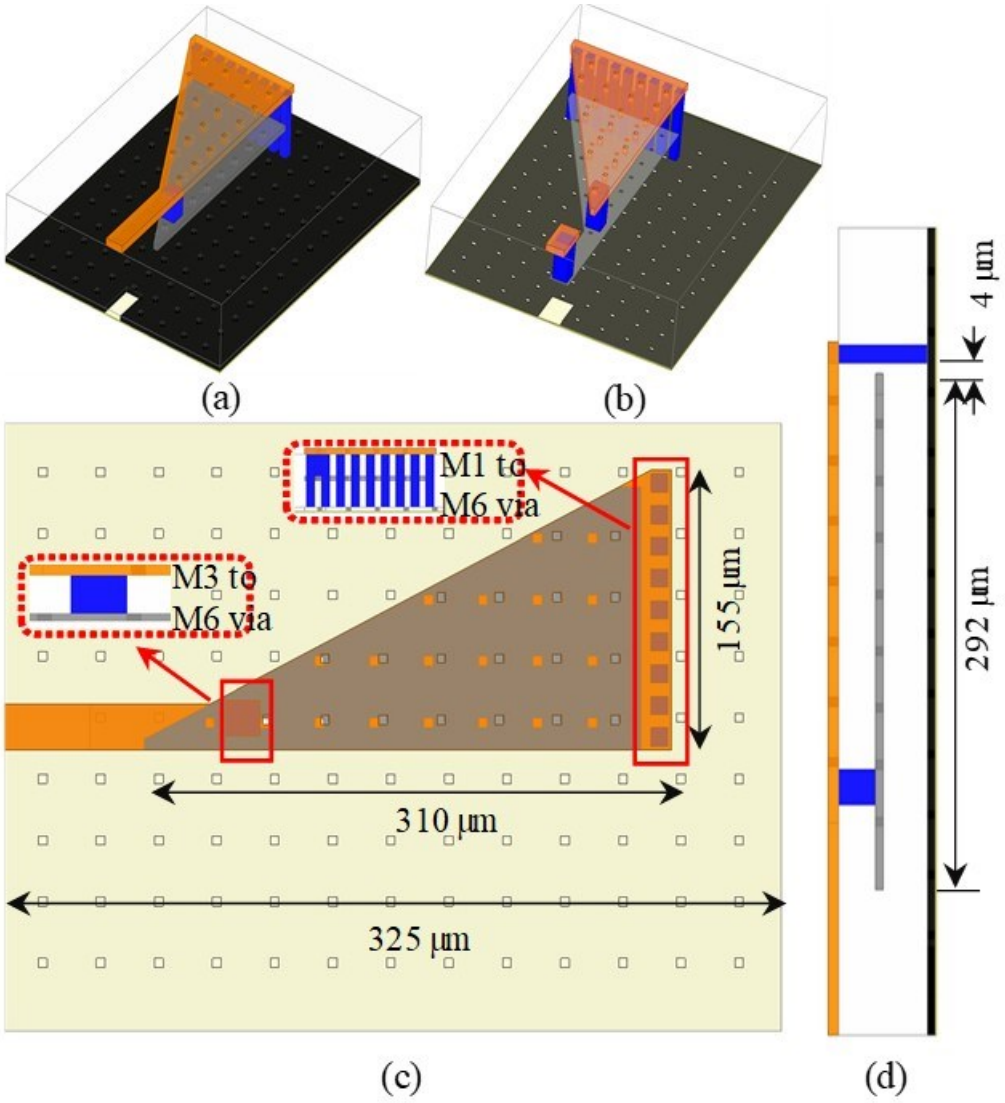


Fig. 3. 16: 3D EM model of the proposed folded ridge sixteenth mode resonators with (a) top microstrip line feeding. (b) transition line feeding. (c) Top view. (d) Side view.

Similarly, Fig. 3.17 shows the 3D EM HFSS model of miniaturized sixteenth mode folded ridge SIW resonator with CSRR loading. Circular CSRR is etched in top metal. The optimized dimensions of this proposed design are presented in the same figure. Without considering the measurement pads, the chip size is only 0.019 mm^2.

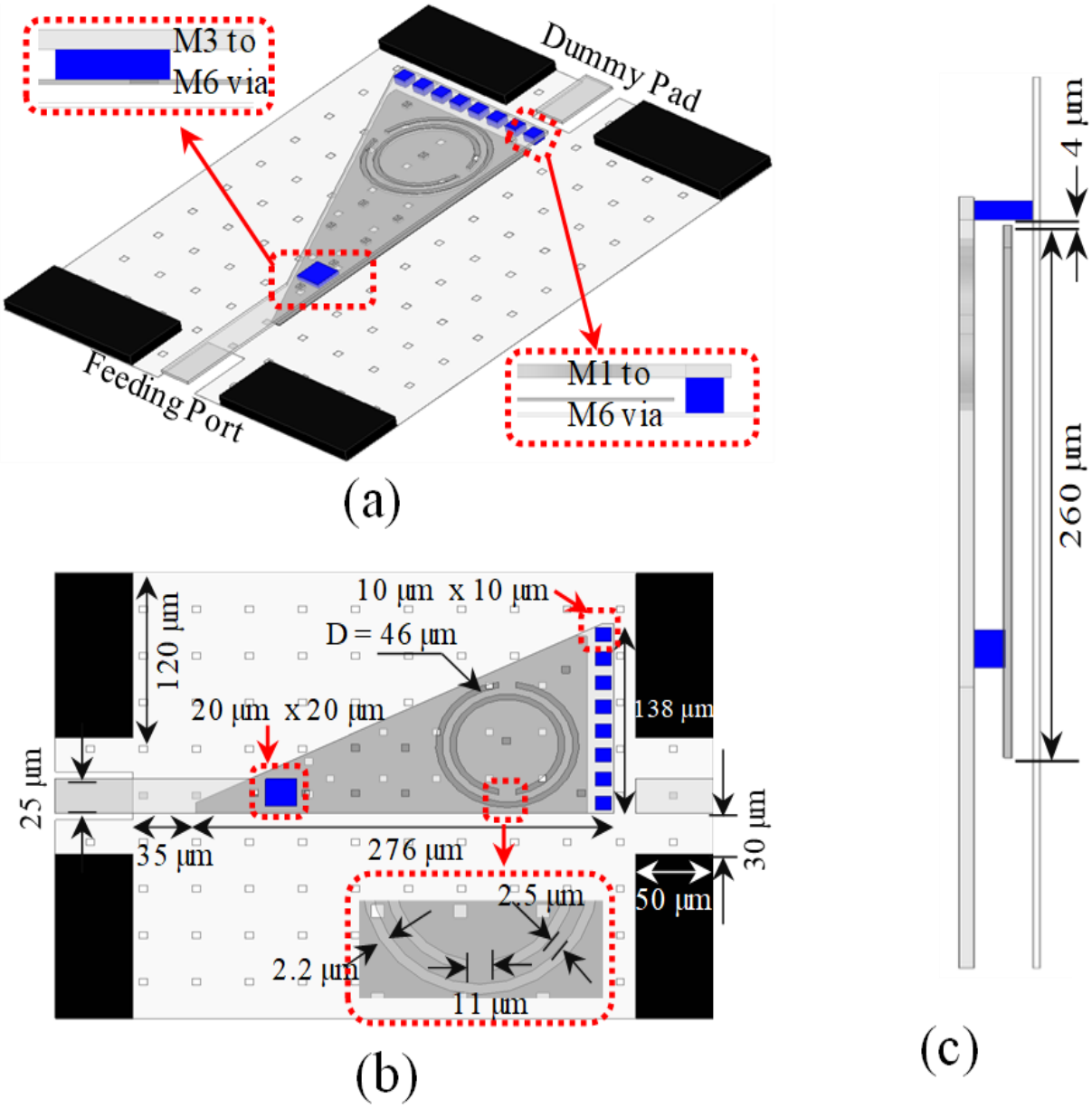
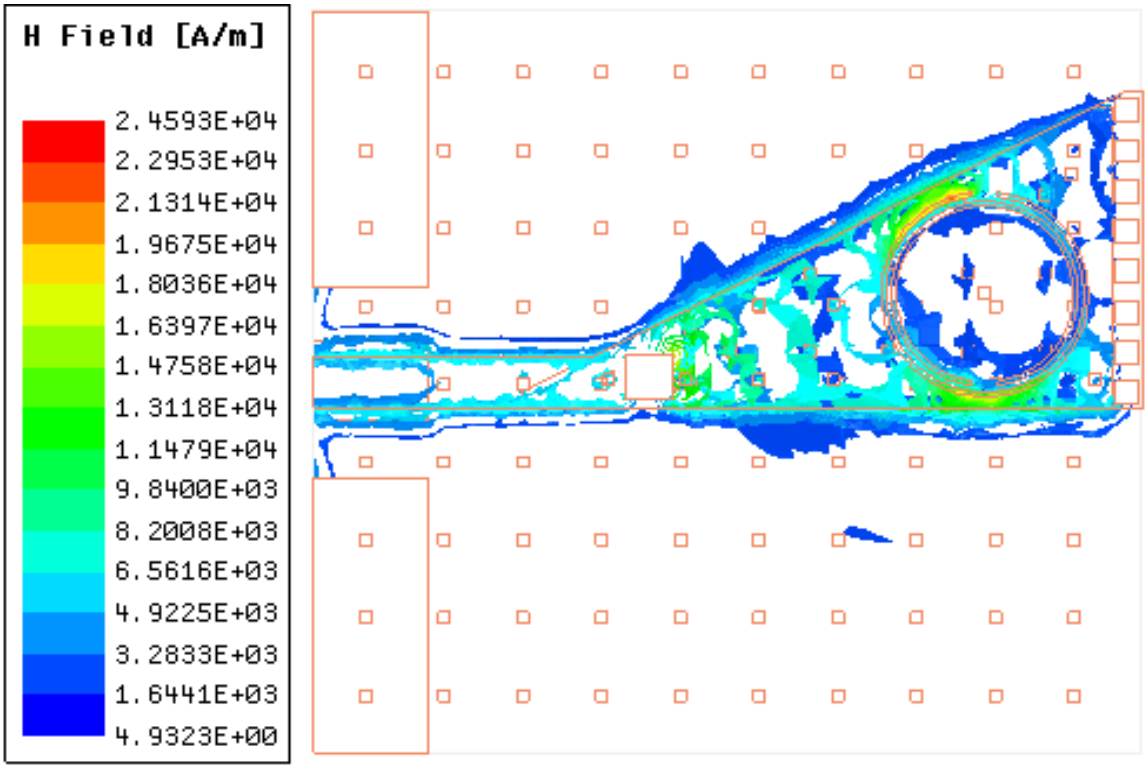
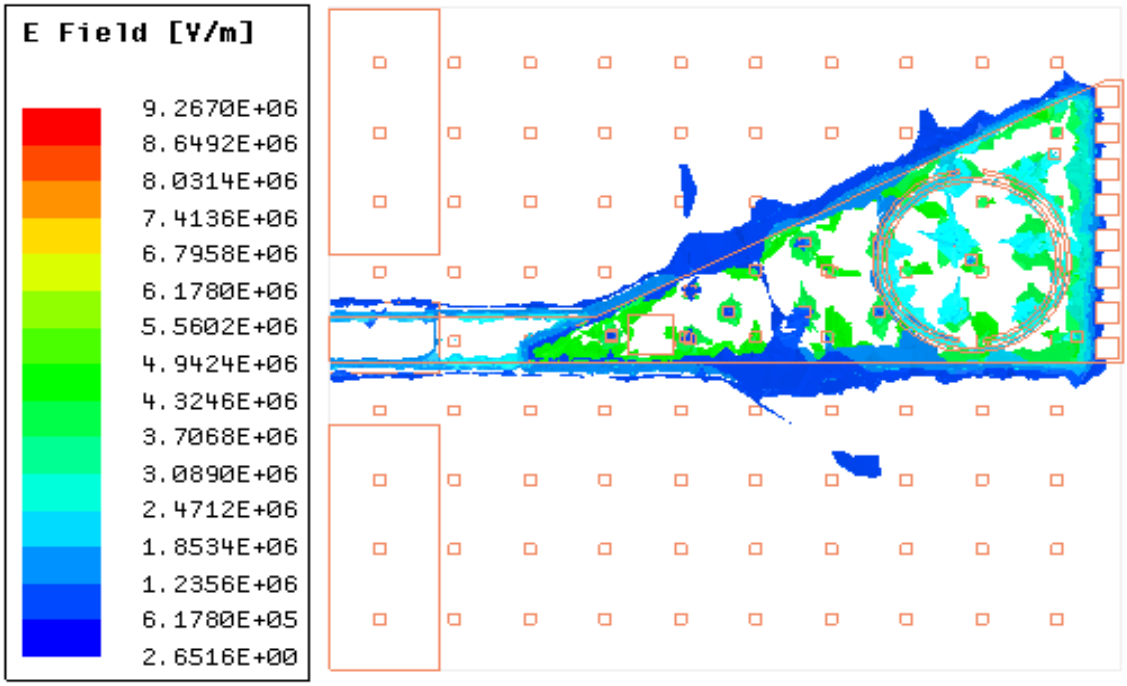


Fig. 3. 17: Proposed resonator sixteenth mode folded ridge CSRR loaded SIW resonator EM model: (a) 3D view; (b) top view; (c) side view.



(a)



(b)

Fig. 3. 18: Field distribution of proposed design with single CSRR loading. (a) Electric field. (b) Magnetic field.

Fig 3.18 presents the electric and the magnetic field distribution in the proposed inductively loaded folded ridge SIW with CSRR resonator. As the CSRR are loaded inductively, at resonance frequency only the magnetic field get enhanced around the CSRR, whereas the electric field is almost the same.

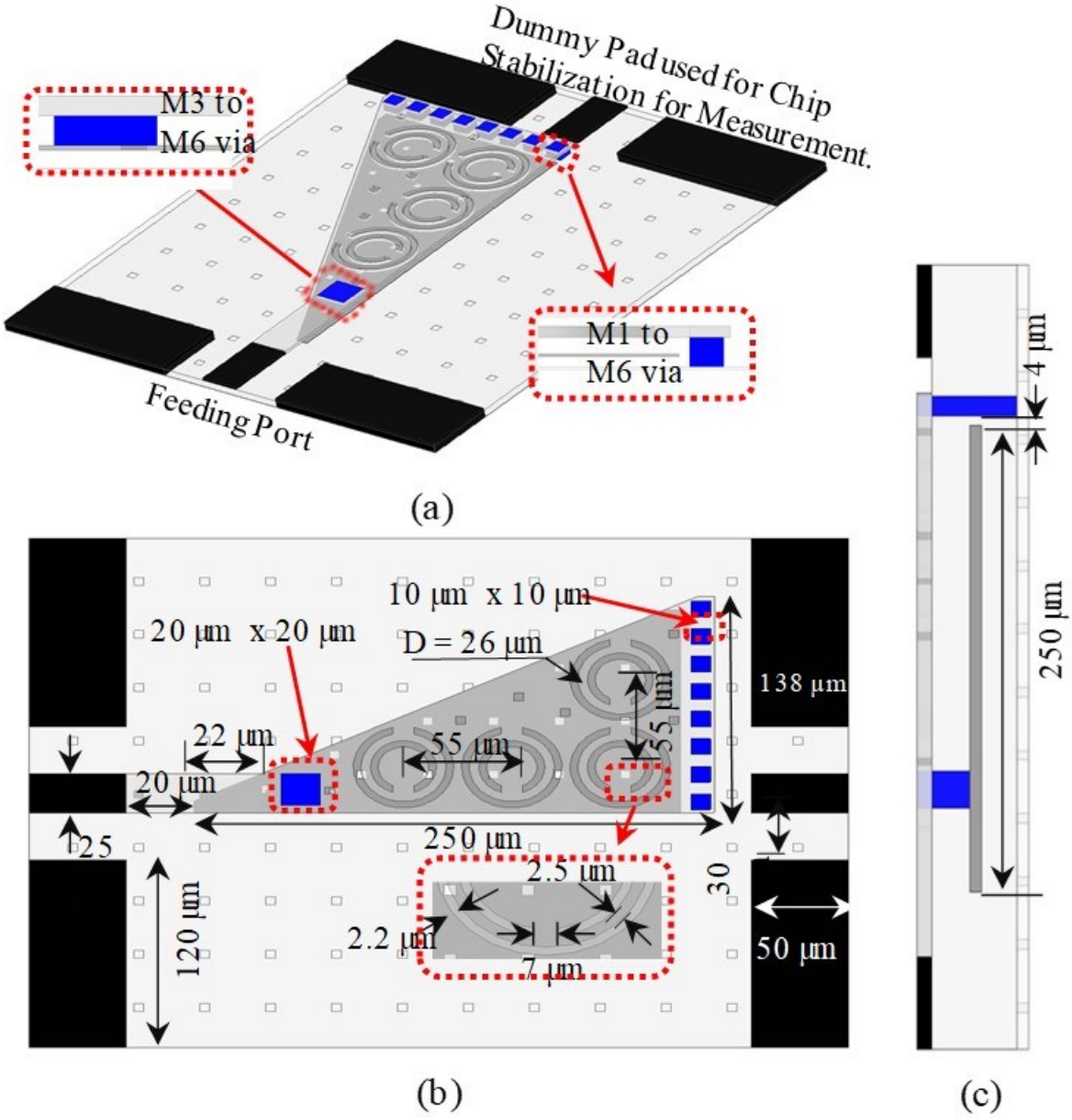
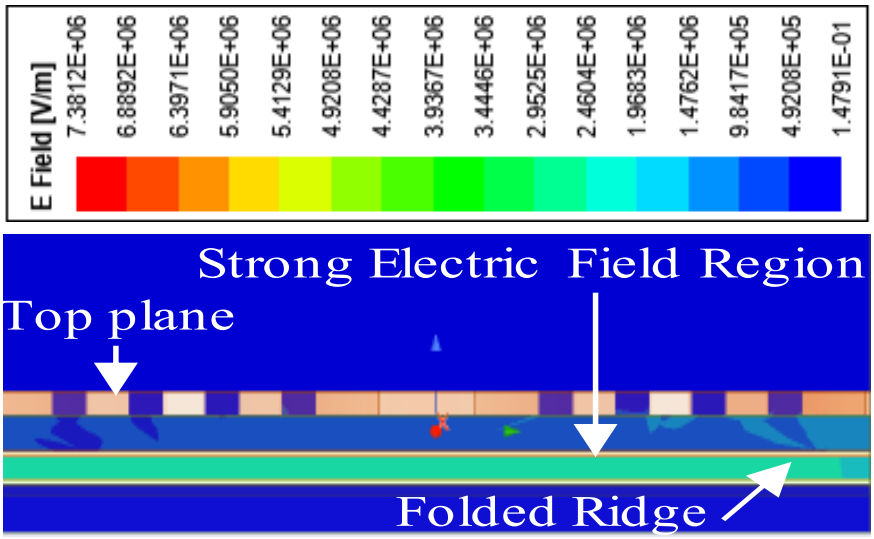
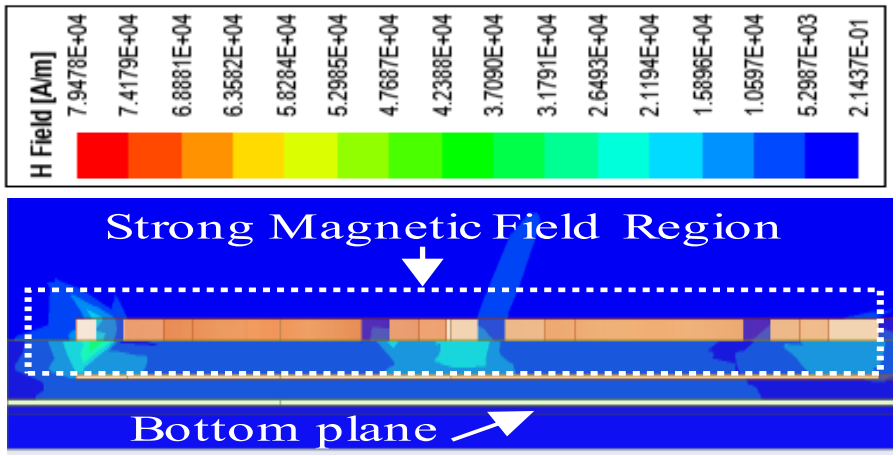


Fig. 3. 19: EM model of the proposed multiple CSRR loaded sixteenth mode SIW: (a) 3D view; (b) top view; (c) side view.

In Fig. 3.19, 3D EM model of four CSRR loaded sixteenth mode SIW resonator is presented. CSRR loaded here are much smaller than the CSRR loaded in Fig. 3.17. Fig. 3.20 shows the magnetic and the electric field intensity in the proposed SIW resonator with multiple CSRRs loading at 60 GHz resonance. The magnetic field is enhanced at the resonance, with no change in the electric field distribution showing improved matching due to inductive couplings.



(a)

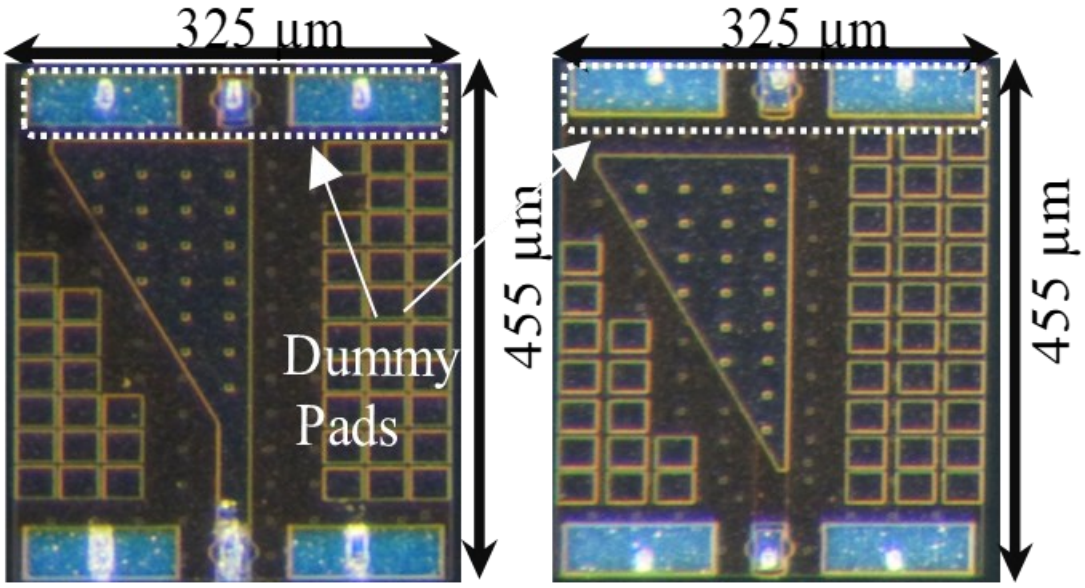


(b)

Fig. 3. 20: Field distribution of proposed design with multiple CSRR loading. (a) Electric field. (b) Magnetic field.

3.6.2 Fabricated Prototypes

The final fabricated chips micrographs are shown in Fig. 3.21 to Fig. 3.23.



(a) (b)

Fig. 3. 21: Prototype sixteenth mode folded ridge SIW resonators with (a) top microstrip line feeding. (b) transition line feeding.

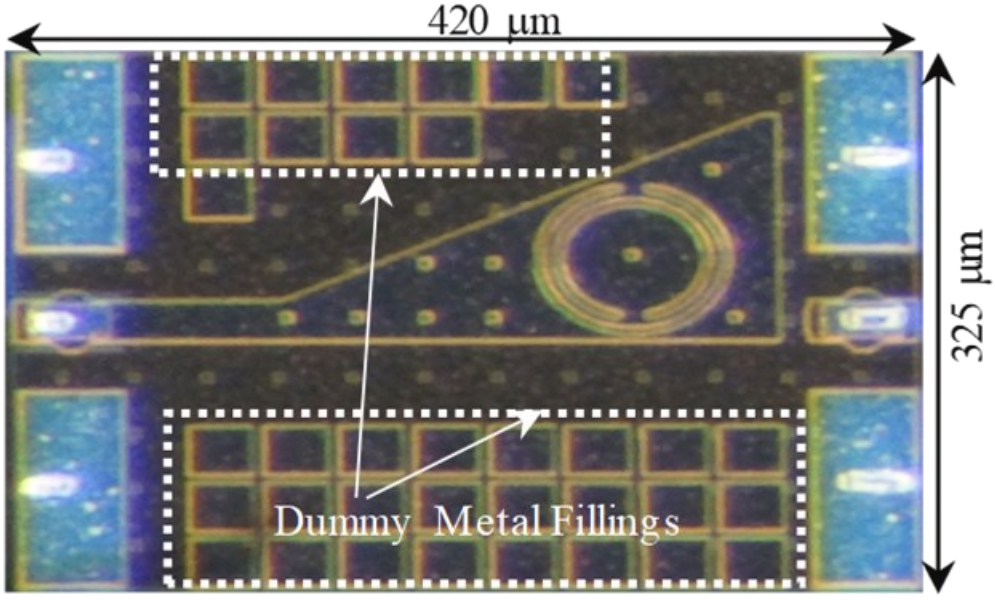


Fig. 3. 22: Micrograph of fabricated prototype of proposed sixteenth mode folded ridge SIW resonator with single CSRR loading.

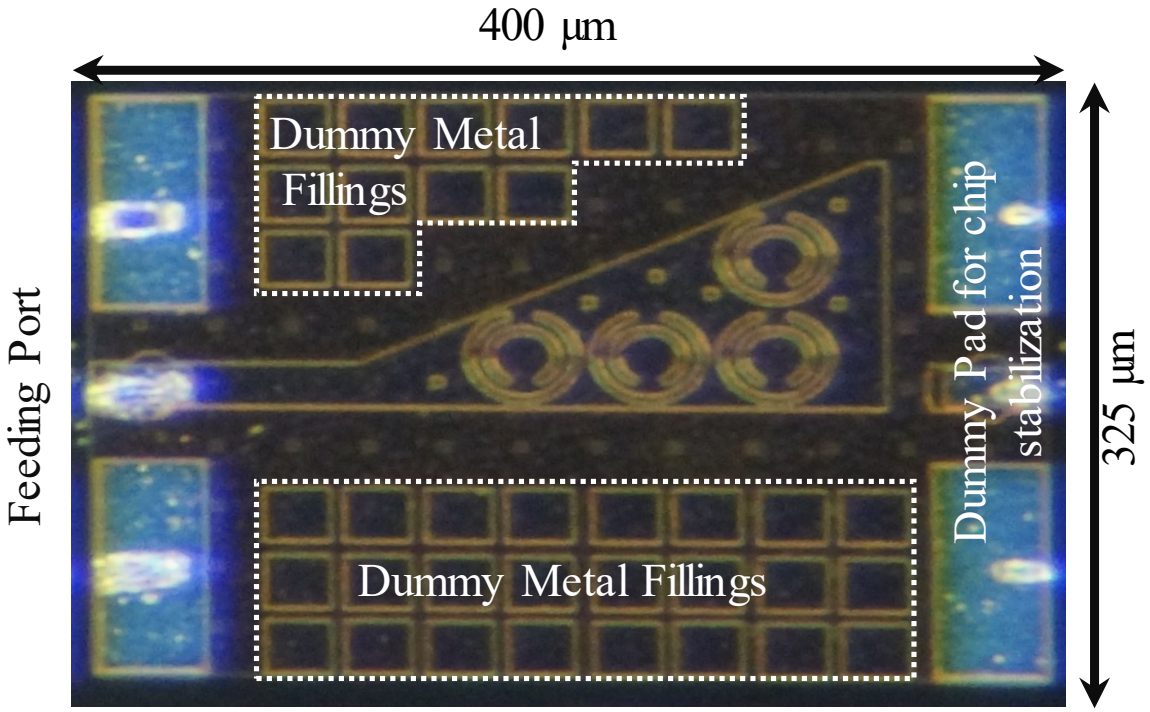


Fig. 3. 23: Micrograph of fabricated prototype of proposed sixteenth mode folded ridge SIW resonator with multiple CSRR loading.

3.6.3 Simulation and Measurement Results

Fig. 3.24 to Fig. 3.27 show the measured $|S_{11}|$ results with simulated results. The prototyped chips were measured in the measurement environment consisting of Keysight E8361C PNA microwave network analyzer and two 150 µm GSG infinity probes.

Measurement results are displayed after conducting de-embedding, employing de-embedding structures. Separate L-2L De-embedding structures are fabricated and are used to performed for the 60 GHz application. Throughout the measurement results both the simulated and the measurement results are accurately aligned. Nevertheless, in all the obtained results, a minor frequency shift is observed, primarily attributable to fabrication tolerances. These tolerances include variations in the effective active area of the fabricated prototypes, as well as the aftereffects of dummy metal fillings and vias that are challenging to fully incorporate in the simulation. Despite these discrepancies, it is worth noting that the simulated and measured reflection coefficient results exhibit satisfactory agreement.

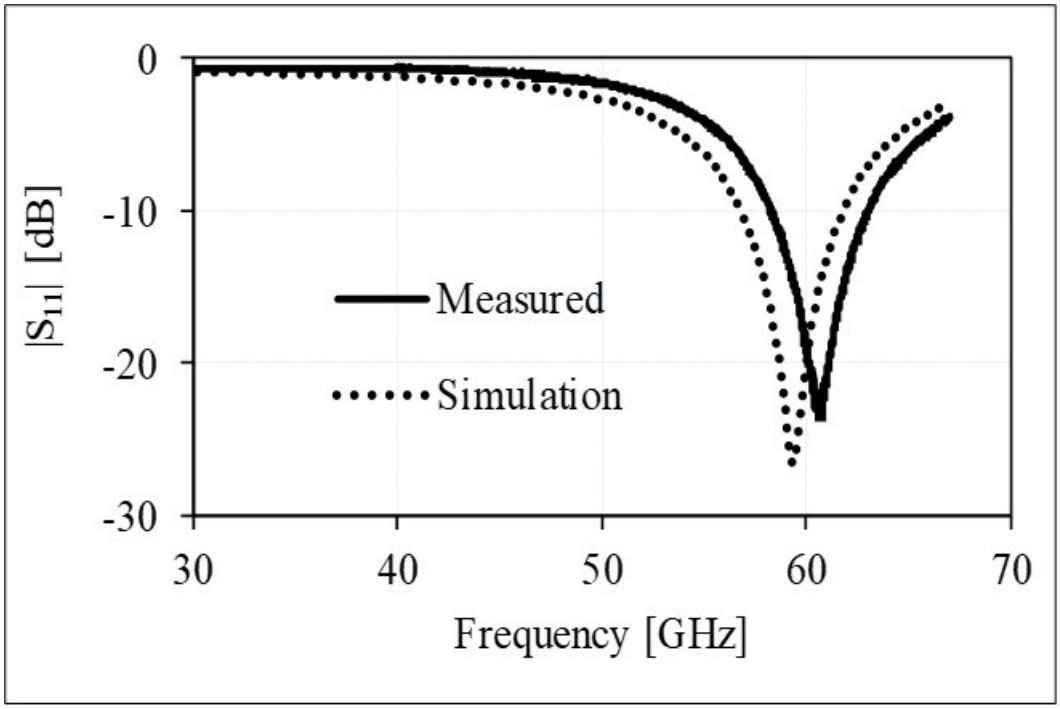


Fig. 3. 24: Simulation and measurement $|S_{11}|$ results of proposed SIW design with top microstrip line feeding.

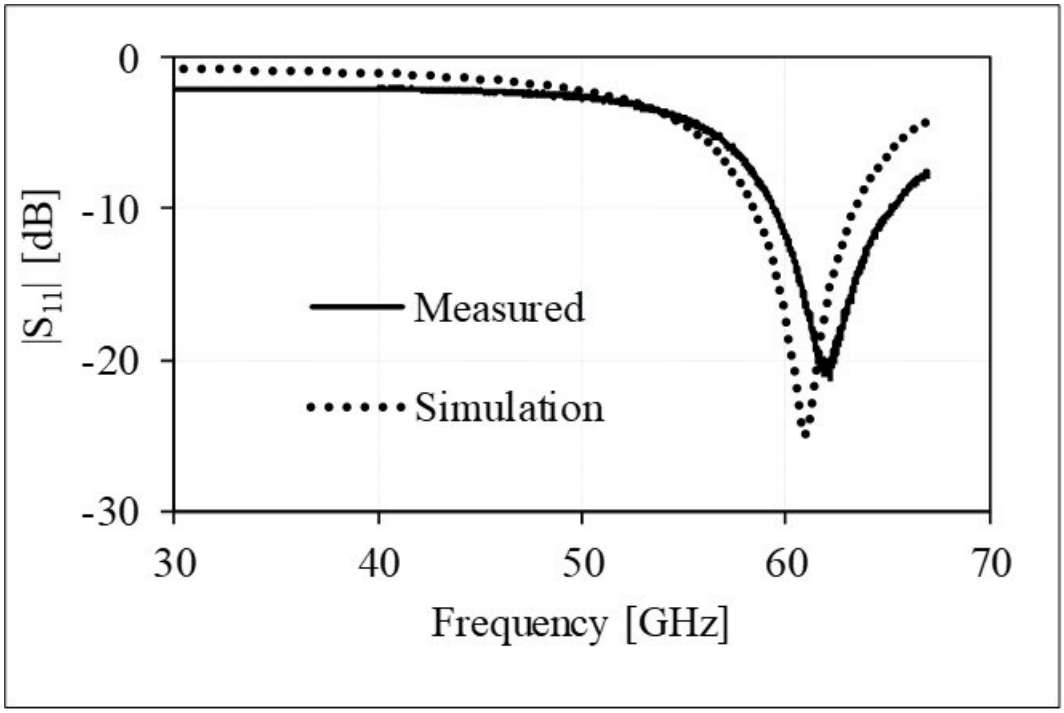


Fig. 3. 25: Simulation and measurement $|S_{11}|$ results of proposed SIW design with transition line feeding.

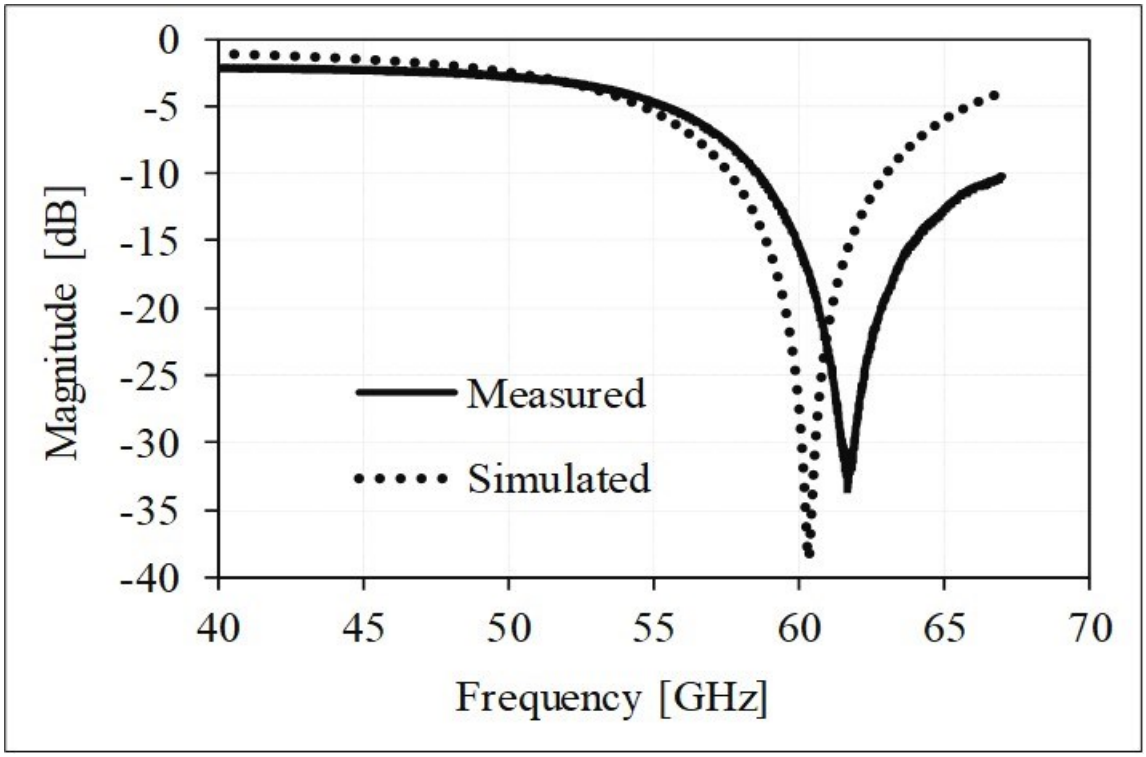


Fig. 3. 26: Simulated and measured reflection coefficient of the proposed sixteenth mode folded ridge SIW resonator design with a single CSRR loadings.

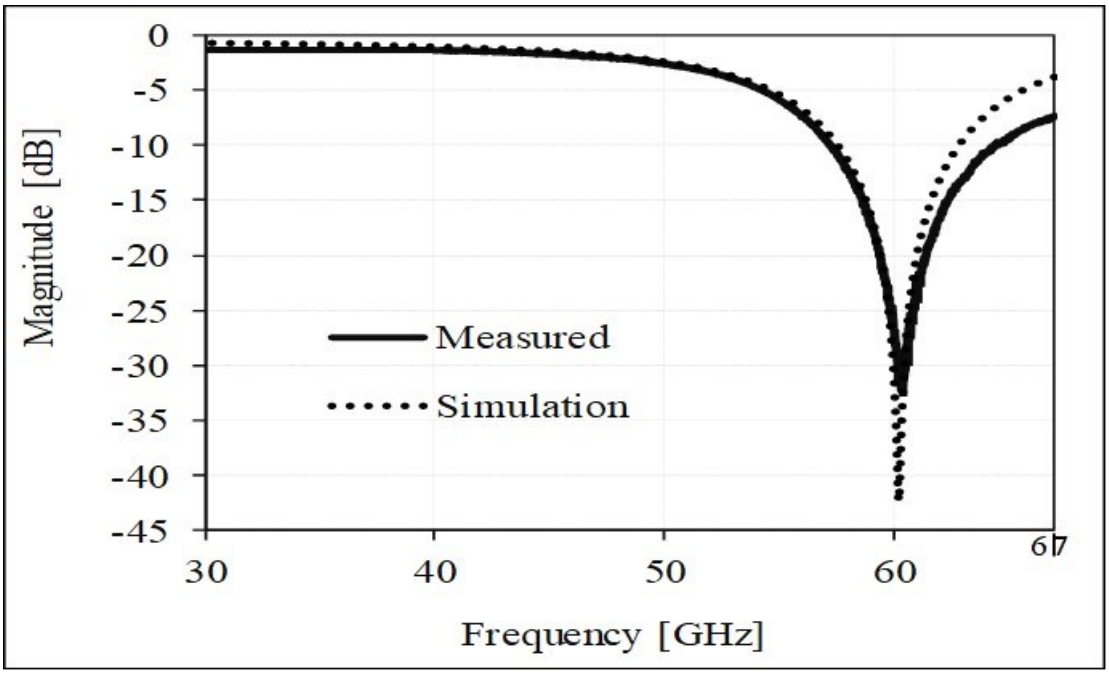


Fig. 3. 27: Simulated and measured reflection coefficient of the proposed sixteenth mode folded ridge SIW resonator design with multiple CSRR loadings.

3.6.4 Performance Comparison

For the proposed resonator's performance comparison, SIW size and the quality factors are considered. Table 3.5 shows the performance comparison of the proposed resonators with the state-of-the-art, which shows that the proposed resonators presented higher Q_l and compact size.

Table 3. 5: Performance comparison with state-of-the-art.

References	**[53]**	**This Work Folded Ridge with top Microstrip Feeding**	**This Work Folded Ridge with transition feeding**	**This Work Folded Ridge with single CSRR Loading**	**This Work Folded Ridge with multiple CSRR Loading**
Technology	In-built Si-Monolithic Fabrication Process	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
SIW Mode	Quarter Mode	Sixteenth Mode	Sixteenth Mode	Sixteenth Mode	Sixteenth Mode
Frequency [GHz]	87.3	60.4	60.9	60	60
Simulated (Measured) *Qe*	111 (101)	64 (58)	56 (49)	146 (108)	312(292)
Active Area (mm^2)	0.566	0.024	0.024	0.019	0.01725
Size Reduction Ratio compared with standard SIW	91 %	98.127 %	98.127 %	99.554 %	99.598 %

3.7 Summary

In this chapter, we discuss the design of low-profile SIW technology in CMOS for millimeter-wave applications. Commercial CMOS technology poses challenges for implementing standard SIWs due to their bulky nature. Therefore, we focus on achieving miniaturization of the standard sixteenth mode SIW resonator by employing a folded ridge design at the 60 GHz frequency band.

Through optimization of the proposed folded ridge width, we improve both the $|S_{11}|$ and the Q-factor of the proposed SIW resonators while achieving significant circuit miniaturization. We

implement four different prototypes of miniaturized sixteenth mode folded ridge SIW resonators in the 0.18-μm CMOS technology. The measured $|S_{11}|$ of all the resonators at the 60 GHz resonance frequency are found to be excellent. Additionally, we conduct an experimental analysis of different feeding structures in the resonators.

The results show that the top feed structure outperforms the transition feed structure due to lower transition losses, as verified through experimentation. Furthermore, we investigate the effect of loading single and multiple CSRRs for the on-chip SIW resonators. By incorporating multiple CSRRs in the miniaturized folded ridge SIW resonators, we observe improvements in the return loss while maintaining the Q-factor, thanks to the introduced inductive couplings. Moreover, the size of the cavity is further reduced through multiple CSRR loading. Moreover, all the proposed structure is fabricated with an active area comprising less than 1% of the standard SIW design. This study provides valuable insights for the design of on-chip miniaturized high Q-factor SIW-based components, including filters, antennas, oscillators, and more, for high-performance millimeter-wave applications.

Chapter 4: Sub-THz band SIW Interconnects and Resonators Design in CMOS Technology

4.1 Introduction

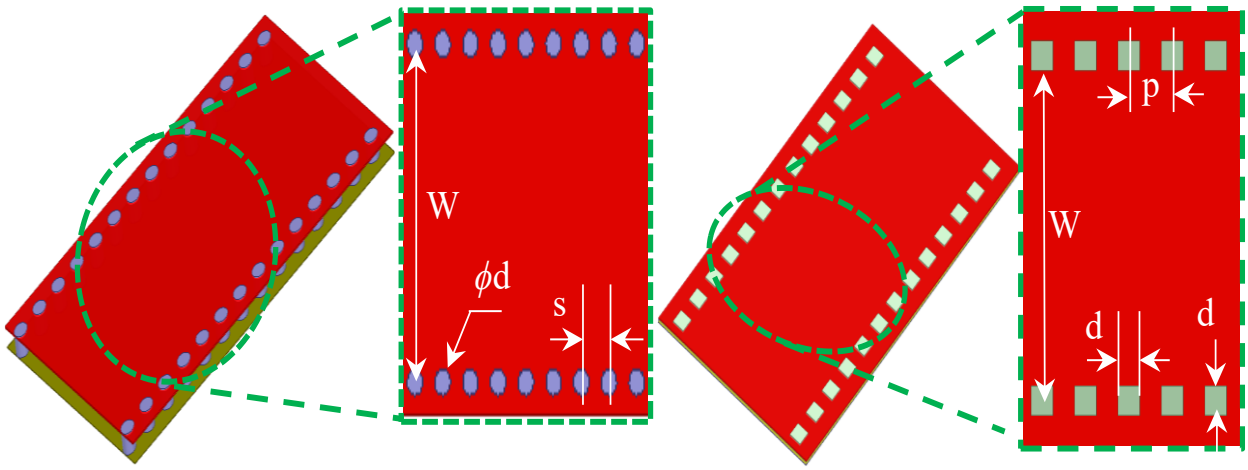
With the successful implementation of 5G, researchers already started thinking for beyond 5G as a future wireless communication. Correspondingly, terahertz (THz) has been appearing as a new interested band for next generation wireless communication system because of the wide swaths of unused and unexplored spectrum and expecting to achieve terabit per second (Tbps) link [1]. The sub-terahertz (sub-THz) band, spanning from 100 GHz to 1 THz, has emerged as a frontier in wireless communication and sensing systems, offering unprecedented possibilities in terms of bandwidth, resolution, and penetration depth. The applications of sub-THz band span across diverse fields. In wireless communication, sub-THz band enable high-capacity data transmission, offering the potential for multi-gigabit-per-second wireless links and alleviating bandwidth constraints. Moreover, such systems can enable ultrafast wireless connections for emerging technologies like 5G and beyond, millimeter-wave backhaul, and wireless virtual reality applications.

In imaging and sensing applications, sub-THz band revolutionize the resolution and depth capabilities. Medical imaging benefits from improved resolution and the ability to penetrate non-conductive materials, facilitating early disease detection and non-invasive imaging techniques. Security screening systems can leverage sub-THz band to enhance detection accuracy, particularly for concealed objects hidden under clothing or within containers. Additionally, sub-THz spectroscopy finds application in material characterization, allowing precise identification of substances and molecular structures in fields such as pharmaceuticals, agriculture, and environmental monitoring.

To cope with the high frequencies like sub-THz, conventional technologies like microstrip, coplanar waveguides, have very limited applications. Waveguides are commonly preferred for such applications. Still the size of the waveguides is questionable to have integration ability with the smaller process that are used for such frequency band applications. Among the various waveguide technologies, Substrate Integrated Waveguide (SIW) has gained significant attention for its ability to seamlessly integrate waveguides into planar substrates. This integration not only enables compact and cost-effective solutions but also facilitates the

realization of integrated advanced sub-THz applications. However, there are very few works that have been reported till dates for such frequency band applications.

In this part we are proposed the design guides for the sub-THz band SIW structure in commercial CMOS technology. Also, various resonators and transmission lines are designed, simulated, fabricated, and validated with the proposed design guides.



(a) (b)

Fig. 4. 1: Conventional SIW model (a) PCB technology and (b) CMOS technology.

4.2 Sub-THz band SIW Design Guides

4.2.1 Region of Interest for SIW Design in PCB Technology

Fig. 4.1 shows conventional SIW model in PCB technology and the CMOS technology. In conventional PCB technology, cylindrical solid vias can be punched from top to bottom metal plane. The region of interest for the generalized SIW periodic vias dimension size (d) and spacing (s) in relation to the cutoff frequency (f_c) and cutoff wavelength (λ_c) which are given by [36]:

$$s > \mathrm{d}, \tag{4.1}$$

$$\frac{s}{d} < 3, \tag{4.2}$$

$$s < \frac{\lambda_c}{4}, \tag{4.3}$$

$$s > \frac{\lambda_c}{20}, \tag{4.4}$$

Equation (4.1) suggests that vias spacing should be greater than via size to make SIW structure practically designable by avoiding overlapping adjacent vias. Equation (4.2) is required to avoid the higher radiation loss for operating in the desired frequency band. Usually, SIW are desired to use in a single-mode operating band is typically from $1.25f_c$ to $1.9f_c$ which has relatively constant transmission coefficient in this range. Equation (4.3) is required to avoid any bandgap within the single-mode band of SIW design. Finally, equation (4.4) suggested for the over-perforated structures, which help to realize the feasible Vias with close enough that is possible to fabricated. It depends on the used technology.

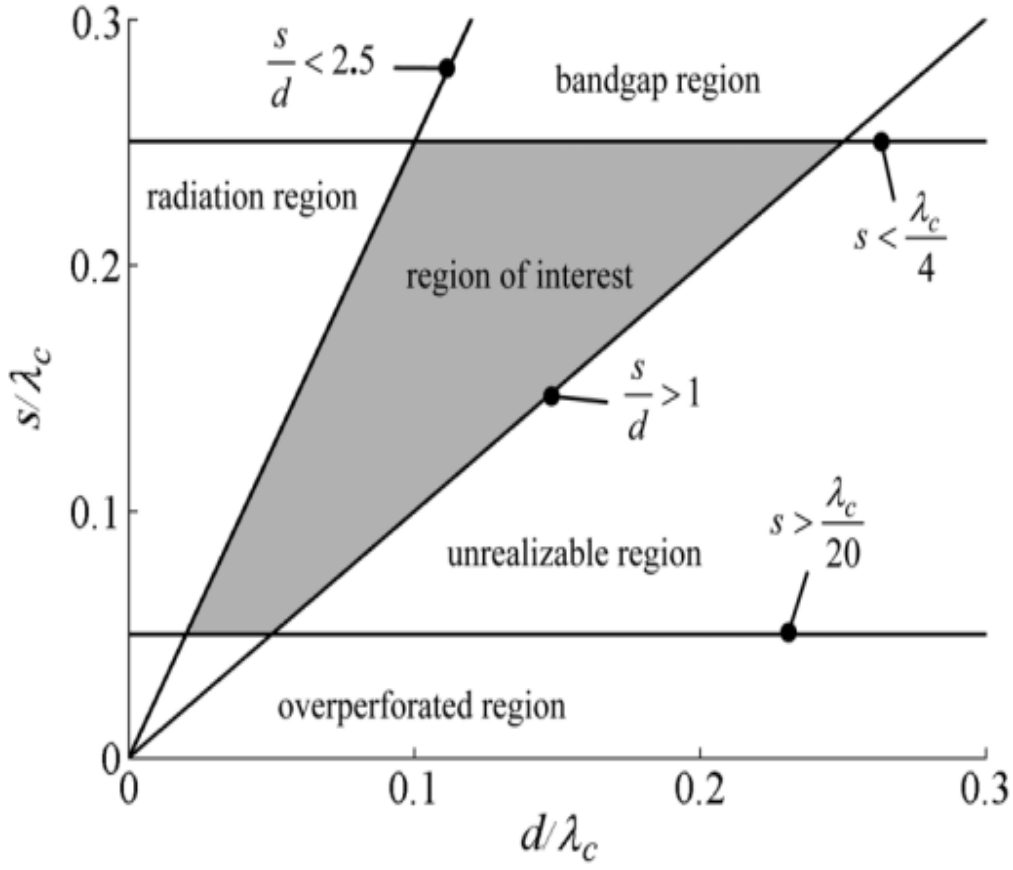


Fig. 4. 2: Region of interest for the SIW structures as a function of d/λ_c and p/λ_c [36].

4.2.2 Proposed Modified Region of Interest for SIW Design in CMOS Technology

The design model of SIW in CMOS technology is shown in Fig. 4.1(b). The commercial CMOS technology has predefined vias size. The foundry only allowed via size is 0.26 µm × 0.26 µm for vias between metal layers M1 and M5. Similarly, the minimal via size is 0.36 µm × 0.36 µm for M5-M6 vias, as shown in Fig. 4.3. These minimal via sizes can also be utilized to design the side via walls, but it becomes the over-perforated structure as suggested by expression (4.4). So, to make the simulated via bigger, a number of small vias are grouped together. But in CMOS technology, the via sizes are non-uniform as shown in Fig.4.3.

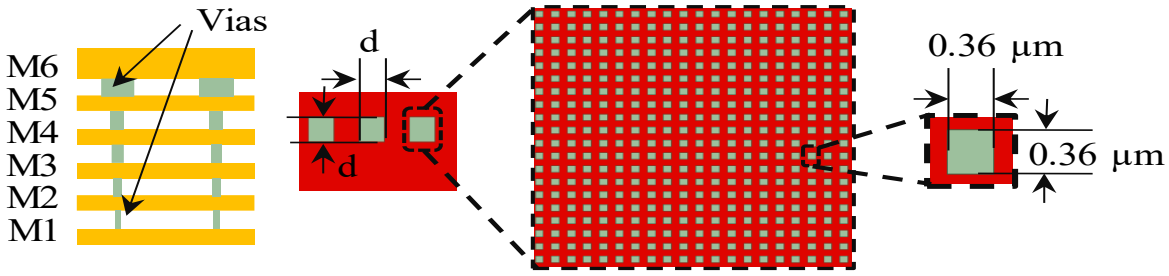


Fig. 4. 3: Predefined vias arrangement for on-chip SIW design in CMOS technology.

Considering these, the region of interest [36] for designing effective on-chip SIW in CMOS technology needs to be redefined. For the used CMOS technology in this work, as illustrated in Fig. 4.4, a new set of generalized equations for via designs is:

$$p > d, \tag{4.5}$$

$$\frac{p}{d} < 2.5, \tag{4.6}$$

$$p < \frac{\lambda_c}{8}, \tag{4.7}$$

$$d > 0.36\ \mu\text{m} \tag{4.8}$$

As (4.5) is required to avoid overlapping between adjacent vias, (4.6) is required to avoid the higher radiation loss for operating in the desired frequency band, (4.7) is required to avoid any bandgap within the single-mode band of SIW, and (4.8) is suggested for the over-perforated structures. Equations (4.7) and (4.8) are modified to be applicable for vias designs in CMOS technology.

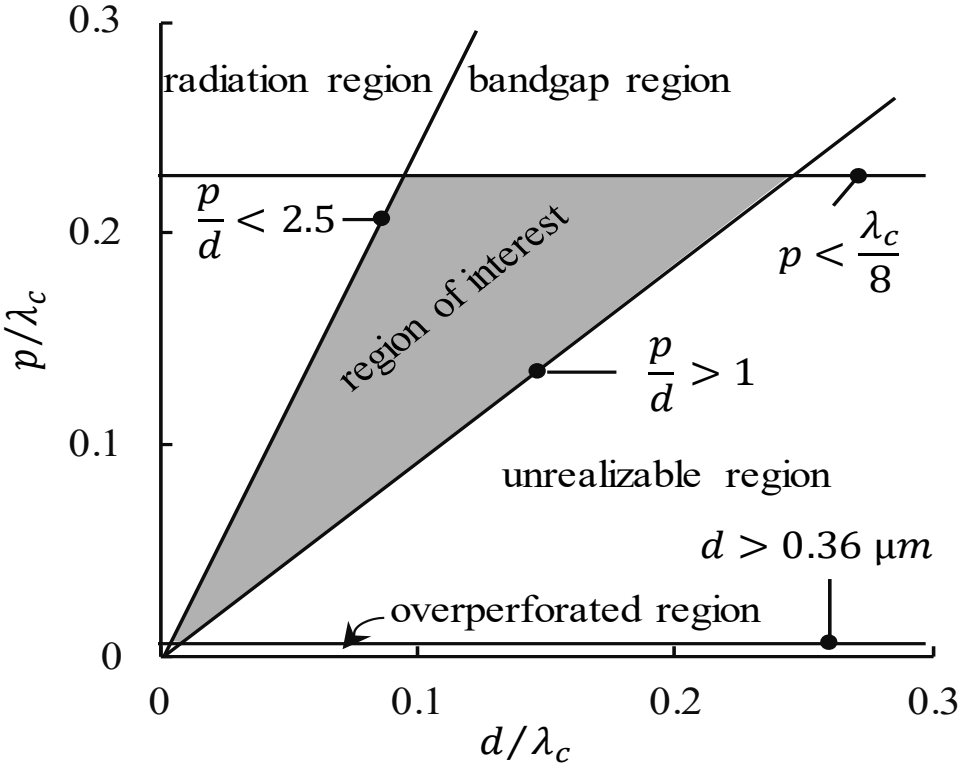


Fig. 4. 4: Region of interest for the SIW design in CMOS technology for a single-mode operating band above 100 GHz.

4.2.3 SIW Via Size Effects in Commercial CMOS Technology

Firstly, using equations (4.5) and (4.6), simulations were performed to obtain the transmission coefficient $|T|$ of Fig.4.1(b). The vias used for the simulations are the rectangular vias with the size d µm × d µm and the spacing size p µm for f_c = 120 GHz. The magnitude of the transmission coefficient with frequency for different vias sizes is plotted in Fig. 4.5. The simulation was performed for the same effective width of the SIW and the same p/dratio. This figure shows that the transmission coefficient fluctuates (degrades) more in higher frequencies for larger vias.

Similarly, in Fig.4.6(a) and (b), the |T| for different p/d ratios were observed throughout the single-mode operation bandwidth of the SIW waveguide for different via sizes. For higher p/d ratio, the transmission coefficient is worse at higher frequencies due to the signal's leakage (radiation loss). In Fig. 4.7, the effect of larger vias in SIW is investigated for the different modes of the SIW. Keeping the same effective width of SIW, for larger d, there is a slight

change in the dominant mode propagation, but the higher order modes shift to the lower frequency rapidly. Due to this effect, the transmission coefficient degrades more in the higher frequencies, as seen in Fig. 4.6. Therefore, to ensure SIW single-mode band operation, i.e., from $1.25f_c$ to $1.9f_c$, the bigger vias size $d > \frac{\lambda_c}{20}$. Thus, condition (4.7) should ensure this operation.

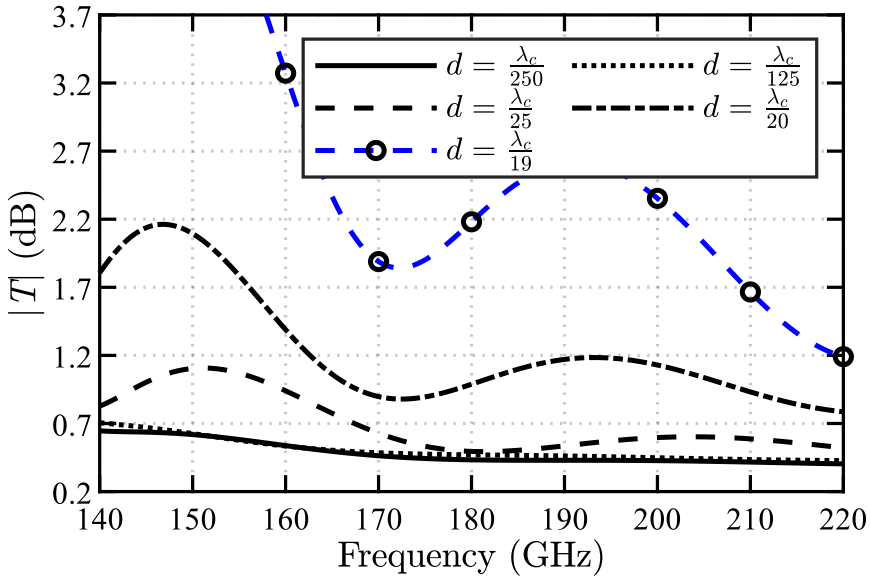
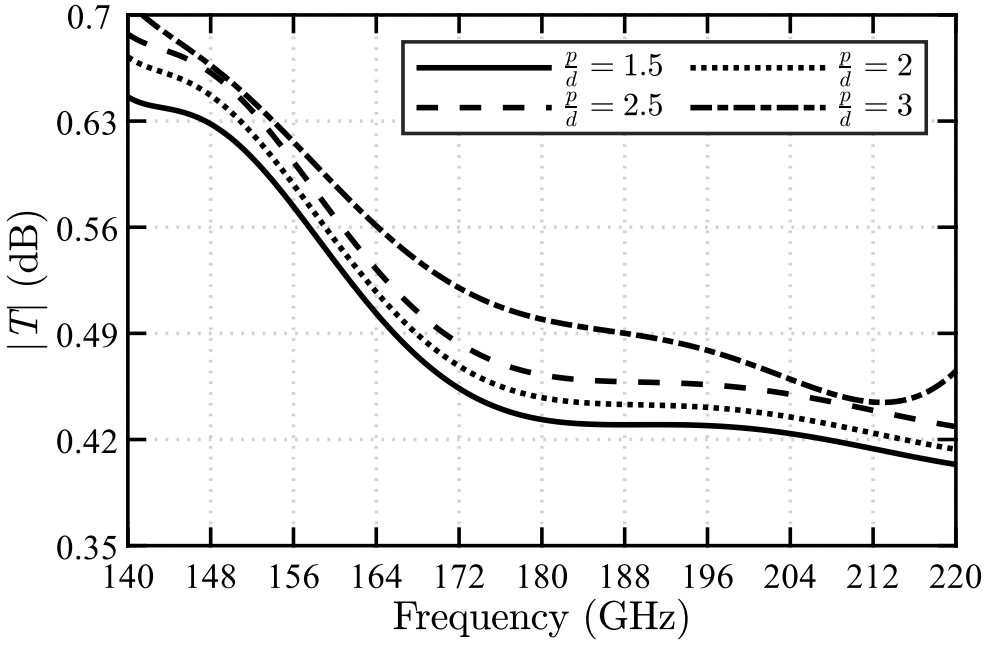


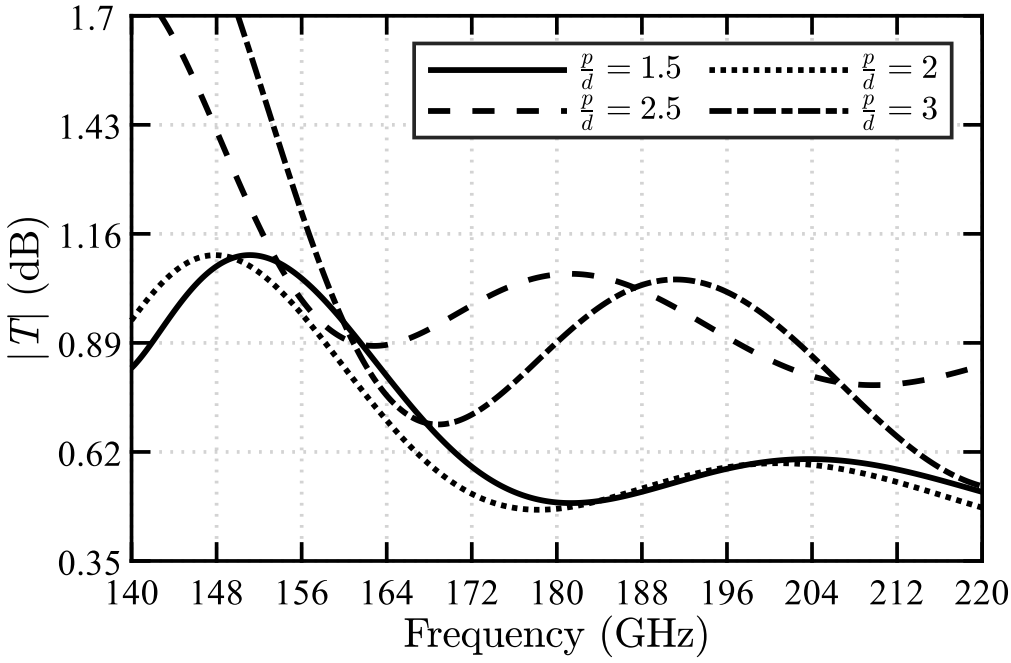
Fig. 4. 5: Transmission coefficient (|T|) vs. frequency for different d/λ_c ratio for p/d = 1.2 and f_c = 120 GHz.

4.2.4 Proposed region of interest more validation for higher frequency bands

Now, to validate the proposed region of interest for higher frequency bands, SIW waveguide in Fig. 4.1(b) is simulated for f_c = 150 GHz. The desired single-mode band of SIW for f_c = 150 GHz is 187.5 GHz to 285 GHz. The full-wave simulations of transmission coefficient (|T|) and the phase constant of the SIW are shown in 4.8 and 4.9, respectively. As suggested by the expression (4.7), the second order mode of SIW is substantially changed and bring back to the region of interest for single mode operation which is undesirable. To avoid this scenario, if the via size is sufficiently bigger and satisfies the condition (4.7), there is a issue of higher-order modes falling into the region of interest. The main reason of this is due to the radiation loss that appears due to vias size and spacing.



(a)



(b)

Fig. 4. 6: Transmission coefficient (|T|) vs. frequency for different p/d ratios for different d/λ_c at fc = 120 GHz. (a) (d=λc)/125 (b) (d=λc)/20.

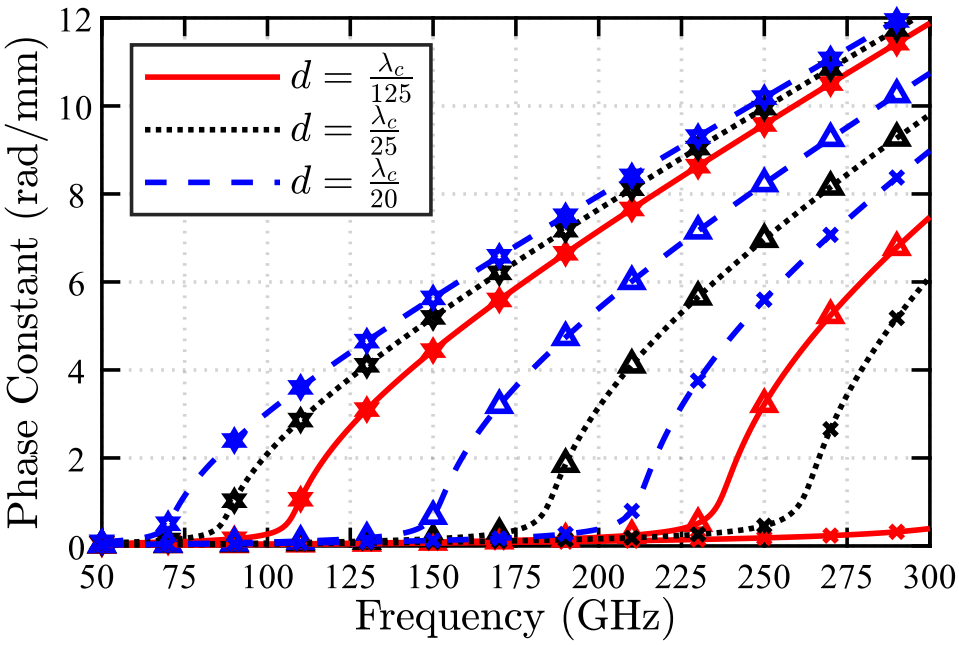
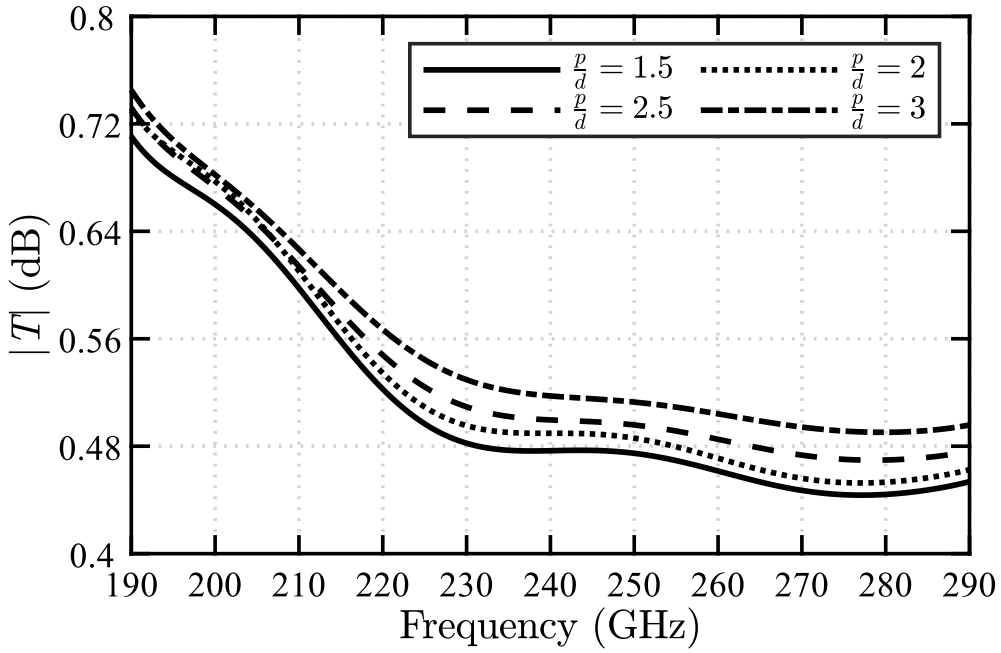
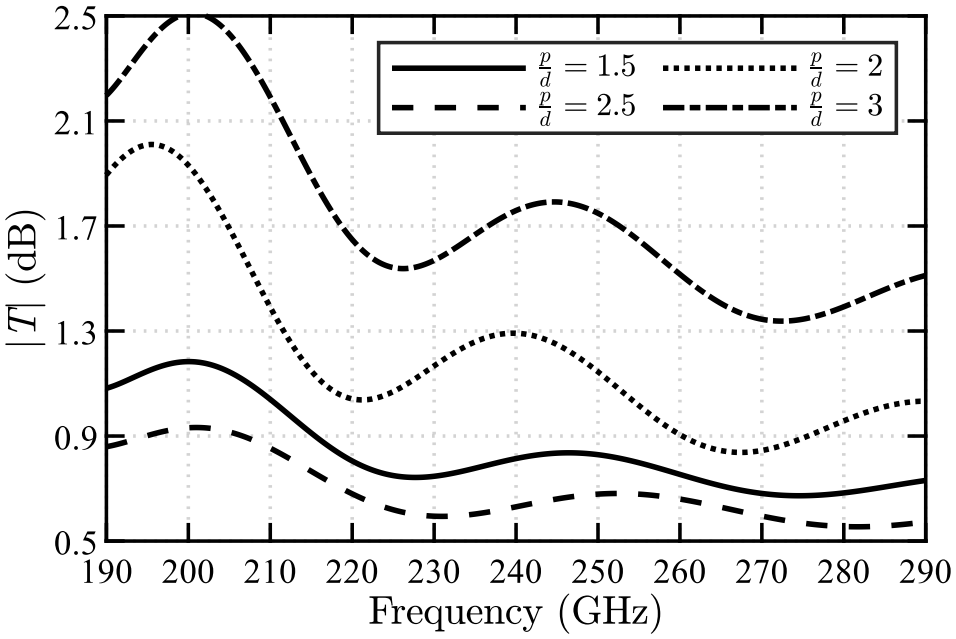


Fig. 4. 7: Phase constant vs. frequency for different d/λc ratios for same p/d = 1.5 ratio and same effective width (W) at fc = 120 GHz. Solid line, long broken lines, and broken lines represent propagation mode 1, mode 2, and mode 3, respectively.



(a)



(b)

Fig. 4. 8: Transmission coefficient (|T|) vs. frequency for different p/d ratios for different d/λ_c at fc = 150 GHz. (a) (d=λc)/125 (b) (d=λc)/20.

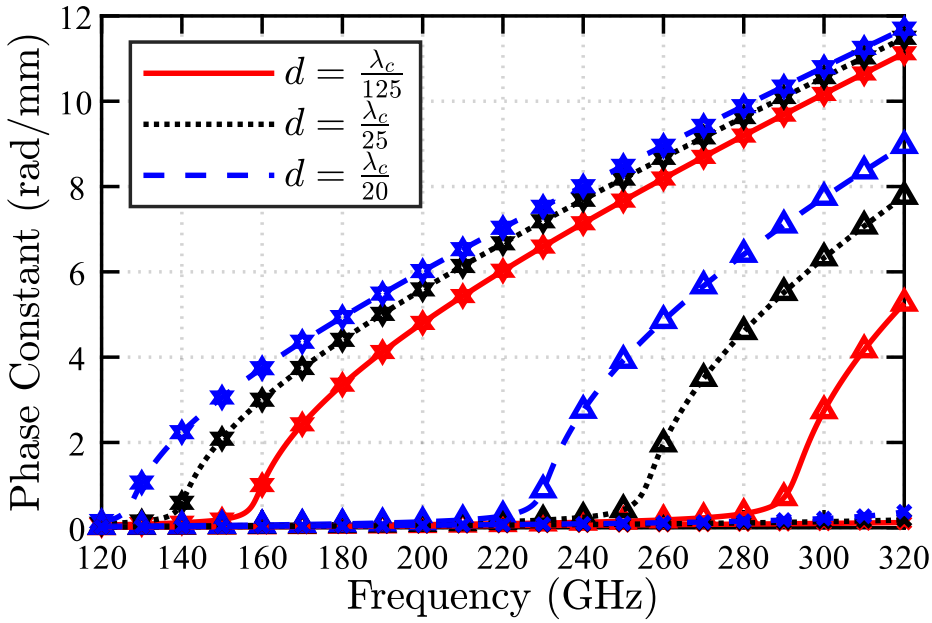


Fig. 4. 9: Phase constant vs. frequency for different d/λ_c ratios for same p/d = 1.5 ratio and same effective width (W) at fc = 150 GHz. Solid line, long broken lines, and broken lines represent propagation mode 1, mode 2, and mode 3, respectively.

4.2.5 Loss Analysis of the standard SIW design in CMOS Technology

In CMOS technology, the maximum available dielectric height between the topmost and bottommost metal layers is very small (typically < 10 µm). So, for on-chip SIW design, via height is restricted to the height of the dielectric thickness of the used technology. Due to this, the width-to-height ratio (W/h) of the SIW is very small, and the SIW behaves more like a rectangular waveguide with the TE_{10} mode as the dominant mode. Also, compared to the SIW with larger W/h ratio, the fields are more concentrated near the top and bottom walls of the waveguide, leading to increased losses which become very high at higher frequency bands.

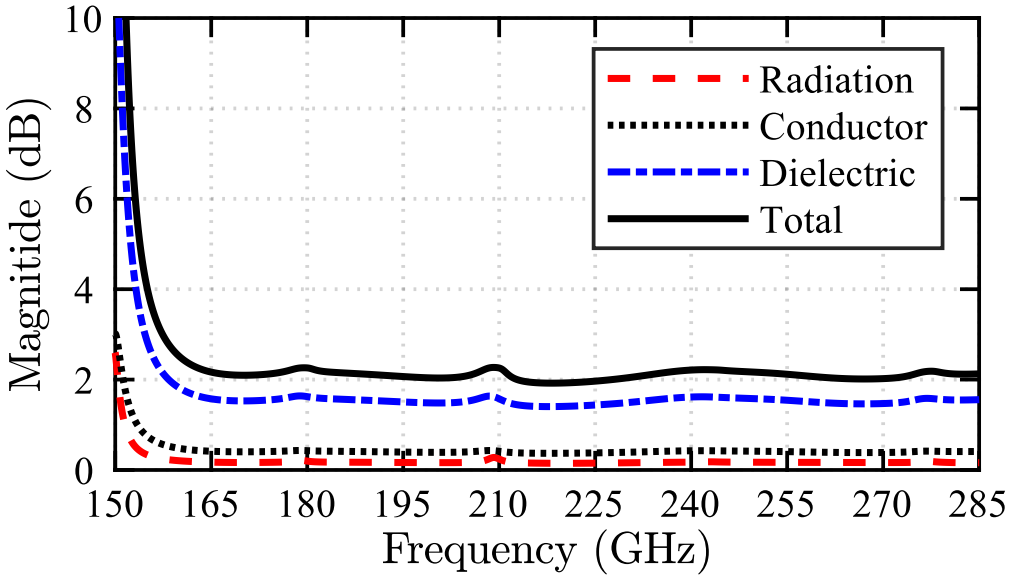


Fig. 4. 10: Attenuation vs. frequency plot of SIW shown in Fig. 1(b) for fc = 150 GHz

Various types of losses that are possible in the SIW structures are conductor, dielectric, and radiation loss. The total losses for SIW calculated from attenuation constant (α) is ,

$$\alpha_T = \alpha_c + \alpha_d + \alpha_r \tag{4.9}$$

$$\alpha = -\frac{1}{d} 10Log_{10}\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) \text{[dB/mm]} \tag{4.10}$$

where, α_c is the attenuation constant due to the finite conductivity of the metals, α_d is the attenuation constant due to dielectric, α_r is the attenuation constant due to radiation. The

method to calculate each attenuation constant is presented in [59]-[60]. Firstly, assuming a top-bottom metal plates perfect conductor and ideal dielectric, α computed represents α_r only. Secondly, considering the finite conductivity of metals and ideal dielectric, α computed represents $\alpha_c + \alpha_r$. So α_c extracted using α_r computed in the first step. Lastly, considering perfect conductor and lossy dielectric, α computed represents $\alpha_d + \alpha_r$. So, α_d is extracted using α_r computed in the first step.

Fig. 4.10 shows the simulated attenuation constants of SIW in Fig.4.1(b) at f_c = 150 GHz, W = 560 µm, d = 8 µm, and p = 12 µm, which shows that even at high frequencies SIW has potentially low radiation loss. Compared to the SIW-based transmission lines reported in [61], [62], the total attenuation constant of the design in Fig. 4.1(b) is lower than 2 dB/mm. In this work, this same SIW structure is implemented to design SIW-based cavities in 200 GHz band applications, which is discussed in the next section.

4.3 Sub-THz band SIW Interconnects Design

Fig. 4.11 shows a general SIW interconnect structure implemented in CMOS technology for Sub-THz band. These top-bottom metal plates (M6 and M1) and the periodic vias serve to confine the EM fields vertically and laterally inside the structure itself. W_{SIW} represents inside edge-to-edge distance between the vias rows. d and p represents square via size and center to center distance between the vias, respectively. h represents available maximum available dielectric thickness between top and bottom metal layers. W and L represents cross section width including some metal after vias size and length of the SIW structure, respectively, which depends on design constraints.

Due to smaller h available in the used CMOS technology (see Fig.4.11(a)), the dominant mode of an electromagnetic (EM) wave inside the SIW TE_{10}, which is the same as the SIW structure in PCB technology. To estimate the SIW equivalent width in relation to vias size (d) and vias spacing (p) for the cutoff frequency (f_c), the effective SIW width can be estimated as [63, eq. (9)]:

$$W_{eff,SIW} = W_a - 1.08\frac{d^2}{s} + 0.1\frac{d^2}{W_a} \tag{4.11}$$

where, W_a is the equivalent width of the conventional rectangular waveguide which has the same height and filled with the same dielectric material.

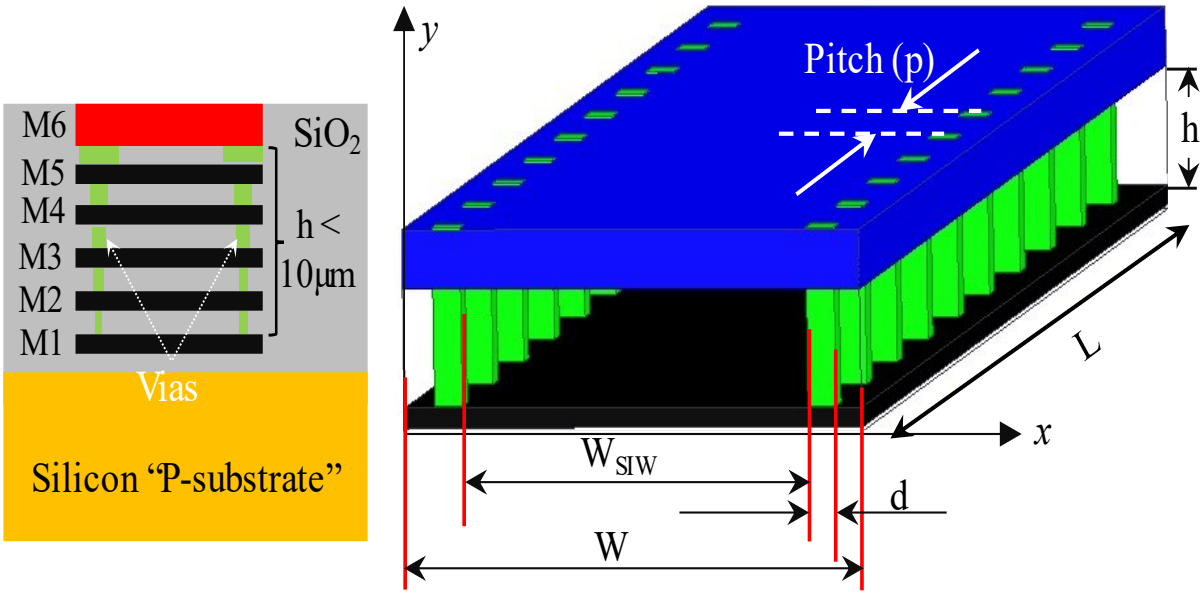


Fig. 4. 11: (a) Side view of 1P6M CMOS technology. (b) SIW structure designed in CMOS technology.

The dominant mode (TE_{10}) electric field distribution of the SIW structure is shown in Fig. 4.12(a). As seen in this field distribution, along the transmission direction (z-direction) it is symmetric from the centre of the SIW structure. If a symmetric plane is cut in the centre of the standard along this transmission direction, the half field direction of the SIW in is unchanged, as seen in Fig. 4.12(b). This is due to the equivalent magnetic wall that is appearing at the cut side open edge appearing due to the high ratio of the width to height. Therefore, the HMSIW structure with the same performance as of standard SIW structure can be achieved but by using only the half area of the standard SIW structure.

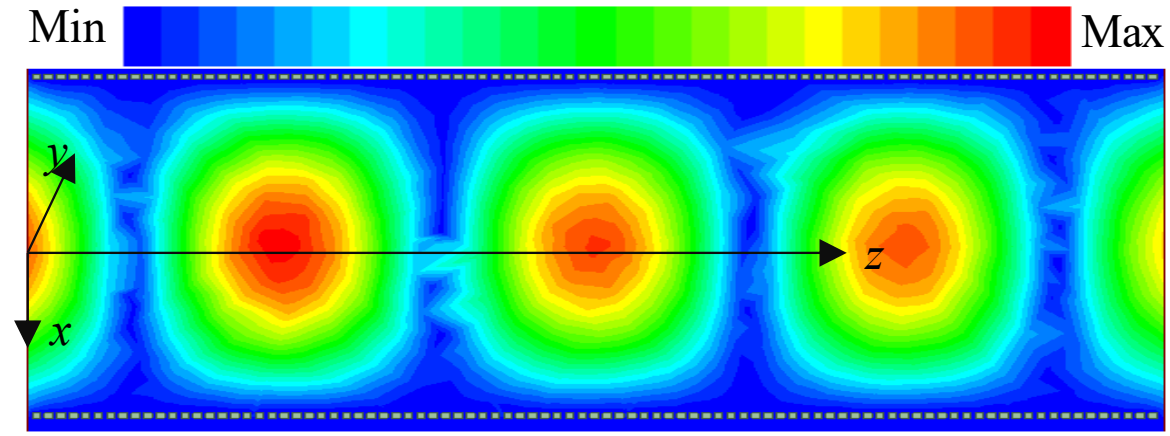
However, if we check the dominant mode field distribution in the Fig. 4.12(b), there are fringing effects of these fields on the open-end edge. To accommodate the fringing fields in the HMSIW structure, an approximate closed-form expression was deduced in [64, eq. (10)] as:

$$W_{eff,HMSIW} = \frac{W_{eff,SIW}}{2} + \Delta w \tag{4.12}$$

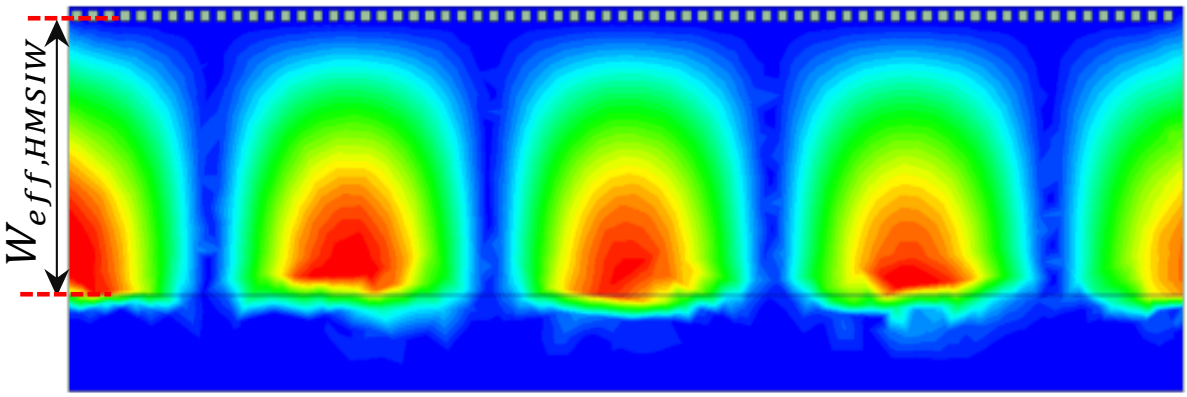
where, Δw is the additional width that takes account those fringing fields which can be estimated by the expression in [64, eq. (13)] as:

$$\frac{\Delta w}{h} = \left(0.05 + \frac{0.30}{\varepsilon_r}\right) \times \ln\left(0.79\frac{W_{eff,SIW}{}^2}{4h^3} + \frac{104W_{eff,SIW} - 261}{2h^2} + \frac{38}{h} + 2.77\right), \quad (4.13)$$

which was obtained by fitting curves for the simulation results obtained for variation of HMSIW dimensions and the dielectric permittivity. (3) holds good approximation for $\varepsilon_r \in (2.2, 15)$, $h \in (0.254mm, 2.54\,mm)$, and $w \in (2.5\,mm, 10\,mm)$, with a range of frequency from 2 to 60 GHz. Utilizing (4.11)-(4.13), low-loss HMSIW can be easily designed.



(a)



(b)

Fig. 4. 12: Dominant mode electric field distribution along the propagation z-direction in SIW-based transmission lines. (a) Standard mode. (b) Half-mode. $W_{SIW} = 660\,\mu m$, $d = 8\,\mu m$, *and* $d = 20\,\mu m$.

Also, to check the attenuation constant of the standard SIW and HMSIW waveguides, we go back to the conductor loss of the traditional rectangular waveguides that is presented in [5, eq. (3.96)] as:

$$\alpha_c = \frac{R_s}{a^3 b\beta k\eta}(2b\pi^2 + a^3k^2)\ N_p/m \tag{4.14}$$

where, R_s is the surface resistance of the metallic walls, a and b are the waveguide width and height, $\eta = \sqrt{\mu/\epsilon}$ is the intrinsic impedance of the dielectric filled waveguide, μ and ϵ are the permeability and permittivity of the dielectric material, $k = \omega\sqrt{\mu/\epsilon}$ is the wavenumber of the waveguide region, and $\beta = \sqrt{k^2 - {k_c}^2}$ is the phase constant. For dominant TE_{10} mode, this phase constant becomes:

$$\beta = \sqrt{k^2 - \left(\frac{\pi}{W_{SIW}}\right)^2}. \tag{4.15}$$

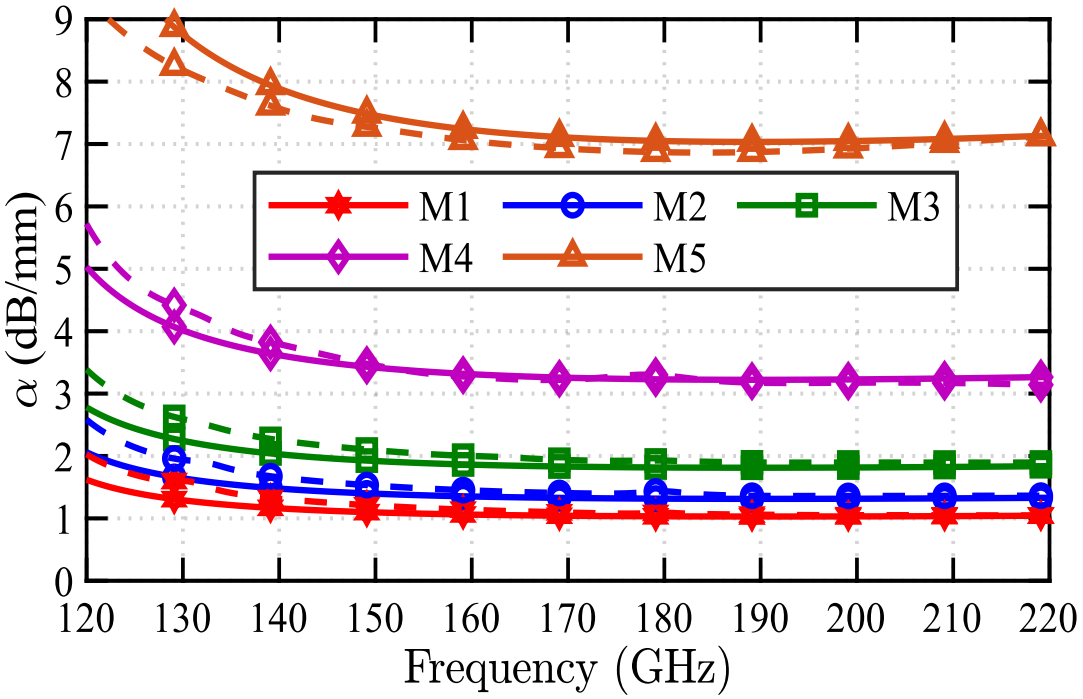
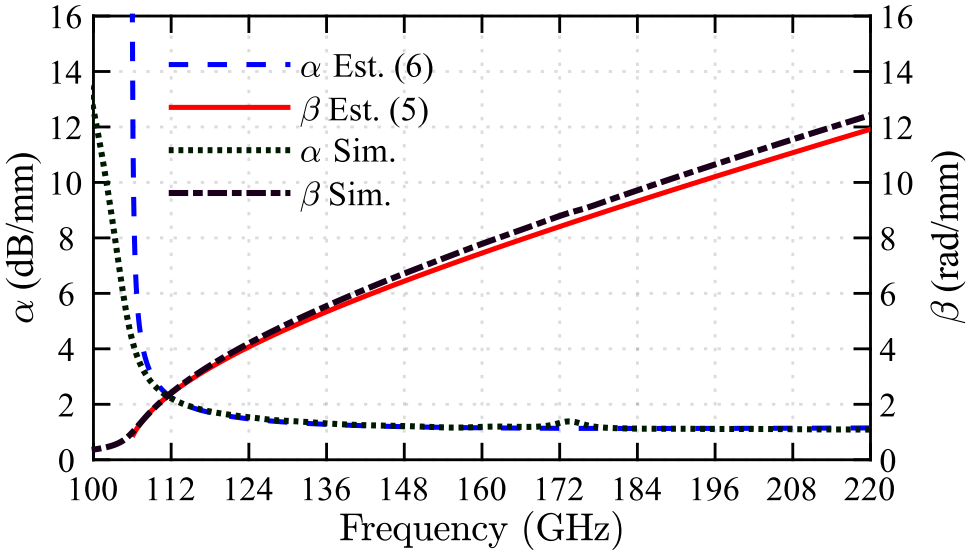
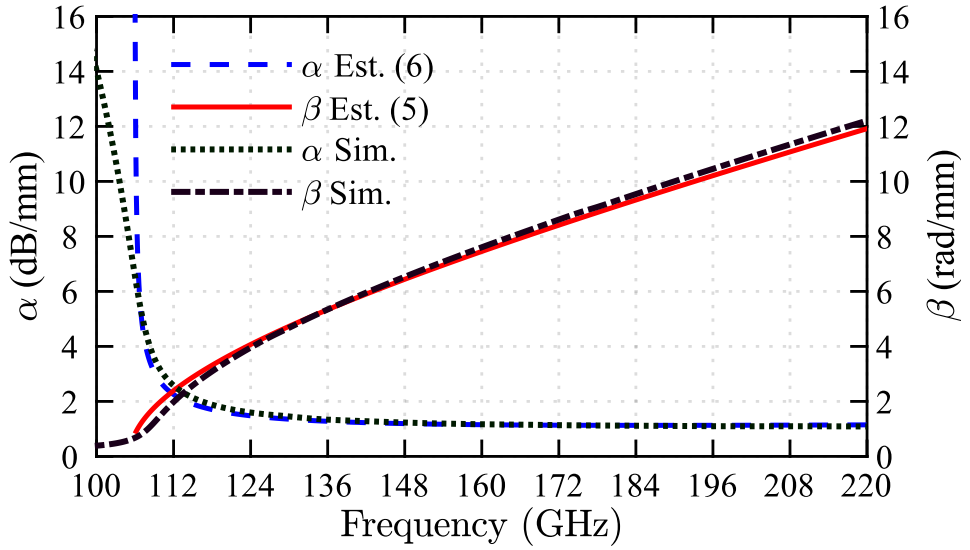


Fig. 4. 13: Computation of α for standard SIW with various metal layer heights, keeping metal layer M6 as top metal and varying the dielectric height with ground layer selections. The dashed lines represent the estimated from the (4.18) and the continuous lines results from an EM simulation.



(a)



(b)

Fig. 4. 14: Propagation constant SIW-based transmission lines; (a) Standard SIW. (b) HMSIW. The line lengths of both structures are keeping constant as L = 1000 µm.

Taking this analogy for the on-chip SIW in Fig. 4.11, the h is much smaller than the working wavelength. The rectangular waveguide attenuation formula (4) still holds true for the SIW structure. But due to smaller broadside height, (4) must be modified to accurately predict the attenuation. A simplified expression of α is presented in [61, eq. (4)] as:

$$\alpha_c \cong \frac{R_s}{h\eta} \cdot \frac{1}{\sqrt{1-(f_c/f)^2}} \tag{4.16}$$

Also, the α due to the dielectric with is presented as [5, eq. (3.29)] as:

$$\alpha_d = \frac{k^2 tan\delta}{2\beta}\ N_p/m \tag{4.17}$$

where, $tan\delta$ is the dielectric loss which depends on the dielectric material used and its operating frequency. Usually most dielectric materials are lossy in higher frequencies resulting higher losses. Now, overall α due to the conductor and dielectric is given obtained from (4.16) and (4.17) as:

$$\alpha\ =\ \alpha_c + \alpha_d = \frac{R_s}{h\eta} \cdot \frac{1}{\sqrt{1-(f_c/f)^2}} + \frac{k^2 tan\delta}{2\beta}\,. \tag{4.18}$$

For on-chip SIW designs, the via height is restricted to the thickness of the dielectric used in the technology. As shown in Fig. 4.11(a), there are six metal layers that are available for creating the top and bottom metal plates. We fix the top metal layer (M6) as top metal. Fig. 4.13 shows the total α due to conductor and dielectric for different ground metal layers computed using (4.18). Due to this limitation of the available h, the W_{SIW}/h of the SIW is large resulting higher α. Also, utilizing (4.15) and (4.18), α for the SIW structures in Fig. 4.12(a), and Fig. 4.12(b) are computed and compared with the full wave EM simulation results as shown in Fig. 4.14, which shows that the estimation values exactly traced by simulated results. Interestingly the attenuation of HMSIW without considering radiation is better than the SIW structure due to the reduced conductor width.

If we check transmission coefficient of the standard SIW transmission line design, it is same as Fig. 4.5, 4.6, and 4.8. But when the magnitude of transmission coefficient of standard and half mode SIW interconnects are checked together as shown in Fig. 4.15, there is mismatch modes in HMSIW designs. This occurs due to the opening on the side of cutting edge, which contributes to some loss compared to the standard SIW design. Such mode mismatching is undesirable and should be eliminated for the good use of the SIW interconnect lines throughout the desired single-mode operating band.

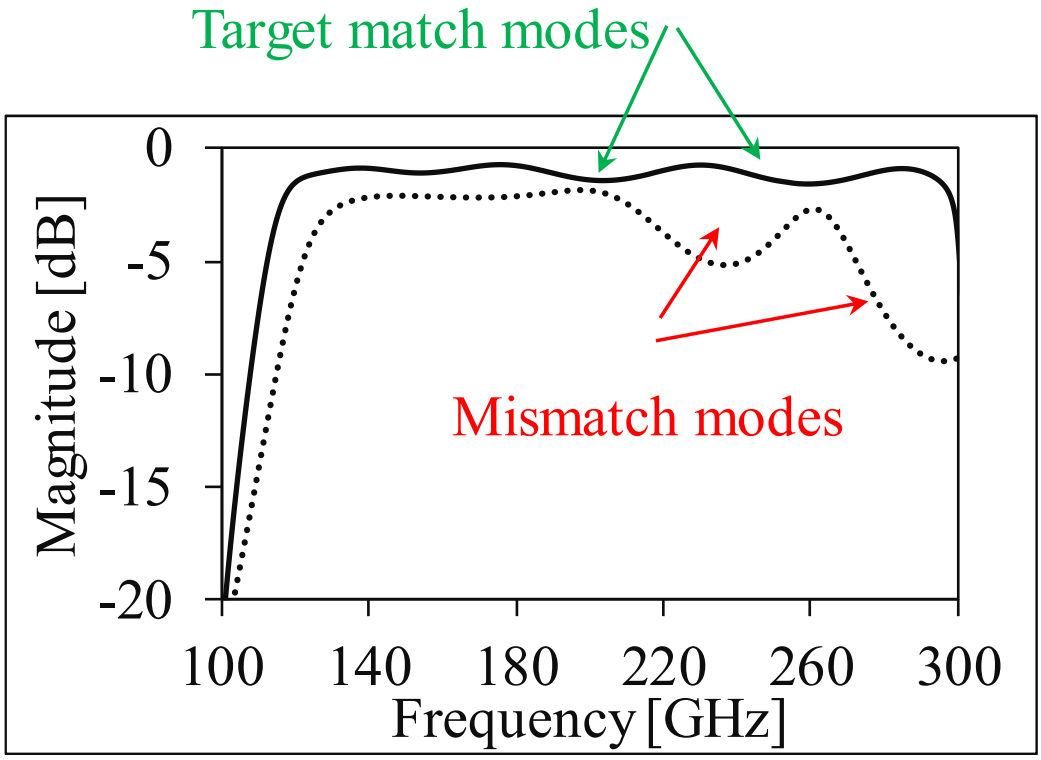


Fig. 4. 15: Transmission coefficient of the matched and mismatched transmission lines.

4.4 CSRR Loaded HMSIW Interconnects Design

A complementary split ring resonators (CSRRs) [65] have been utilized in various applications in SIW structures like filter design by exploiting its metamaterial properties [66]. By loading CSRR as metamaterial, the SIW can be operated below its cutoff frequency and can achieve the bandpass response in that region. To the authors best knowledge, these CSRRs structures are not investigated as metamaterial properties in the CMOS technology for on-chip SIW-based designs. In this work, we investigated on the corresponding behaviour of CSRR on SIW structure and later utilized the potential of CSRR resonators to design HMSIW-based transmission line with lower transition losses.

CSRR Loadings as Metamaterial for Filter Design

Fig. 4.6 shows the layout of the CSRR unit cell in standard SIW and HMSIW structures. For standard SIW, side-by side configuration is used. A full wave EM simulation was performed in Ansys Electronics Desktop 2023R1 of these structures. In general, by changing the orientation

and configurations of CSRR resonators like in [66], various passbands can be observed in the SIW structures below the cutoff frequency commonly termed as metamaterial effect. This passband fractional bandwidth, insertion losses, return loss can be altered by utilizing various configurations [66]. In this manuscript this studied is left untouched.

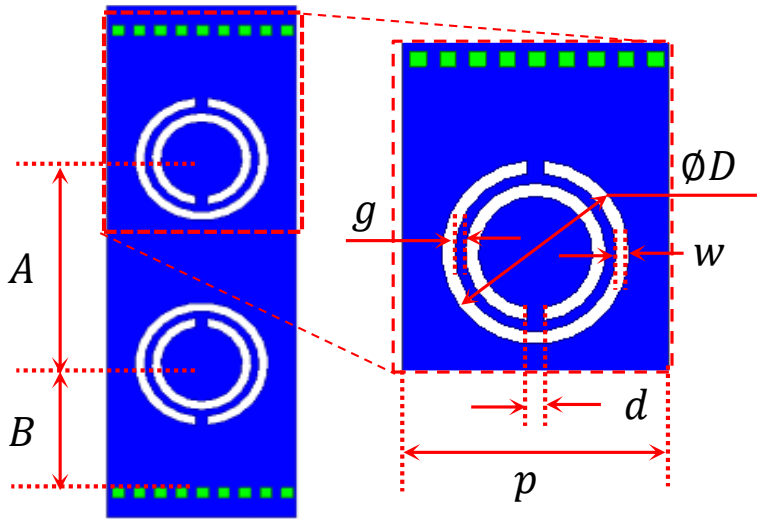


Fig. 4. 16: Configuration of CSRR resonators inside the (a) SIW structure. (b) HMSIW structure. $p = 200\ um$ *is the unit cell length.* $\emptyset D = 65\ um$, $w = 5\ um$, $g = 5\ um$, $d = 12\ um$, $A = 240\ um$, $B = 150\ um$.

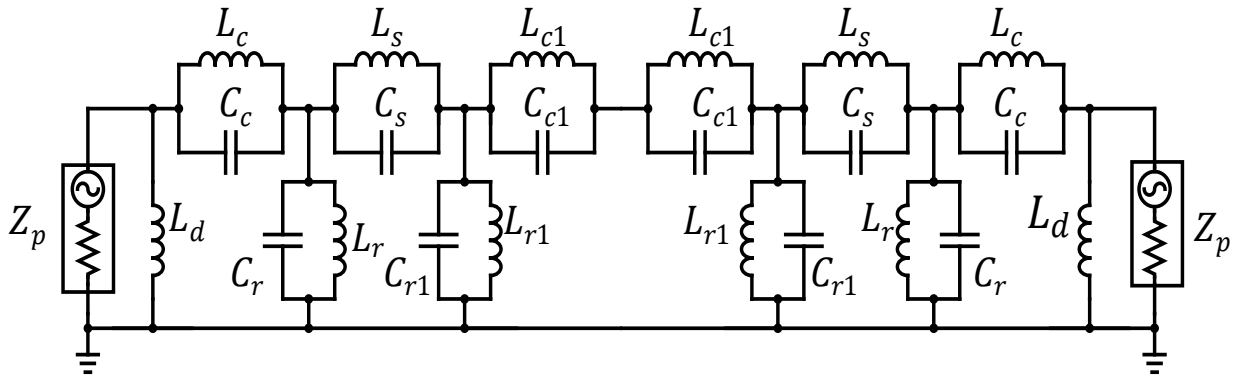


Fig. 4. 17: Equivalent circuit model of Fig. 4.16.

An equivalent circuit of the unit cell metamaterial is shown in Fig. 4.17. The used parameters in the equivalent model are: $L_d = 160\ nH$, $L_c = 36.3\ nH$, $C_c = 79.1\ fF$, $L_{c1} = 9\ nH$, $C_{c1} = 31\ fF$, $L_r = 104\ nH$, $C_r = 21\ fF$, $L_{r1} = 69\ nH$, $C_{r1} = 34\ fF$, $L_s = 34\ nH$, $C_s = 5\ fF$. The EM simulated propagation constant is shown in Fig. 4.18. A clear passband

is observed below f_c i.e., 95 GHz to 103 GHz in this case. Similarly, transmission coefficient of unit cell with and without CSRR loadings and its equivalent circuit in Fig. 4.16 is shown in Fig. 4.19.

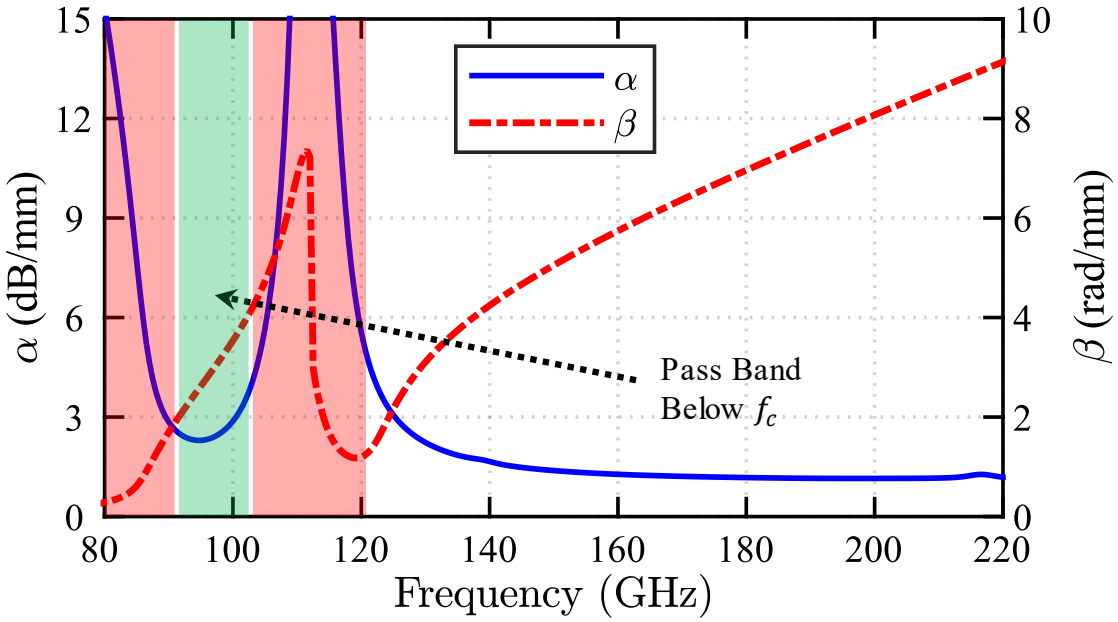


Fig. 4. 18: Propagation constant of the unit cell CSRR metamaterial structure.

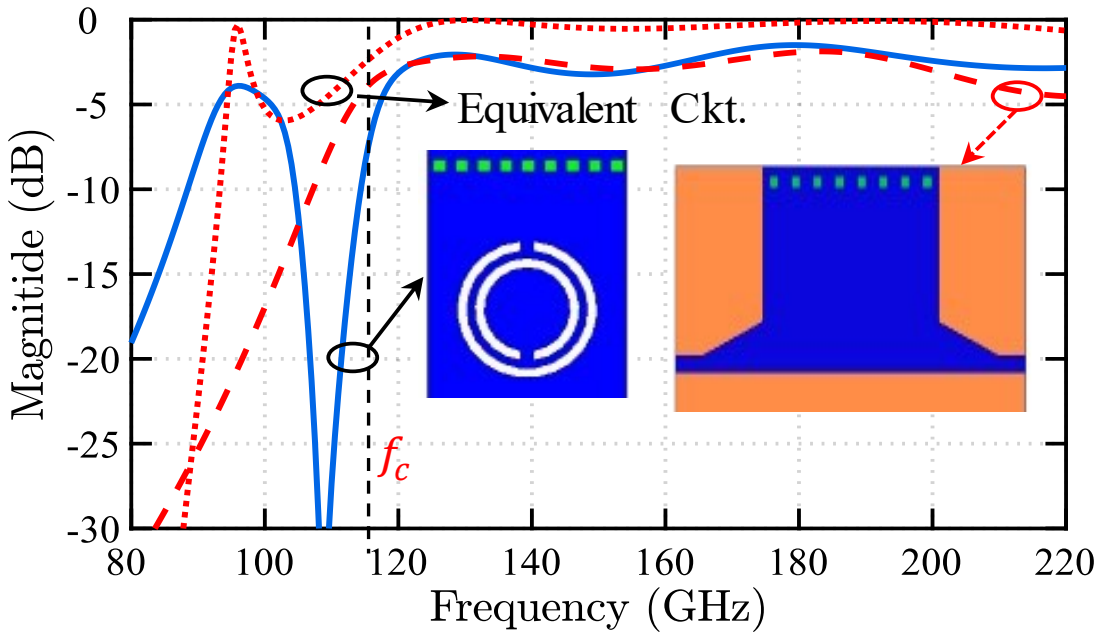


Fig. 4. 19: Comparison of S-parameters results HMSIW-based transmission lines with and without CSRRs.

In order to use as a bandpass filter this CSRR resonator can be optimized to get the better filter response as shown in Fig. 4.20. The used CSRR diameter is $\emptyset D = 65\ um$, and the structure that is optimized is also embedded in Fig. 4. 20.

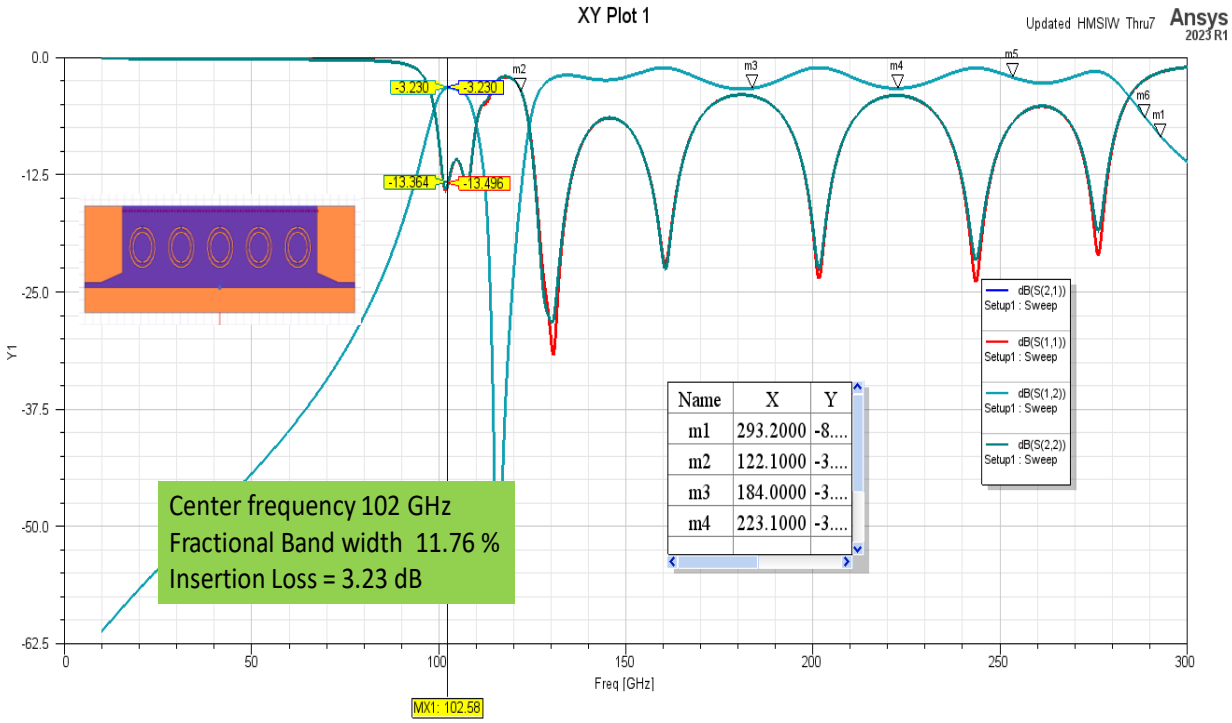
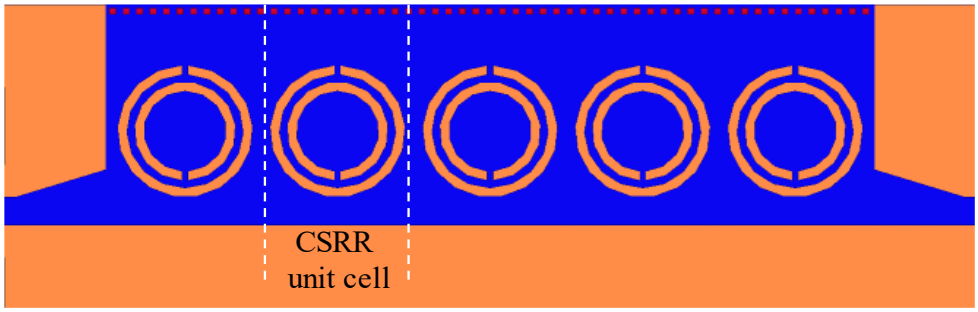


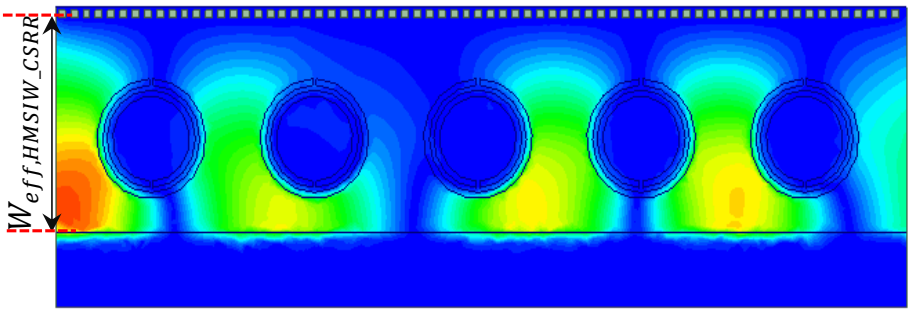
Fig. 4. 20: 100 GHz Bandpass filter design using CSRR metamaterial loading.

CSRR Loadings for Improving Mismatch in HMSIW Single-Mode Operating Band

Besides the metamaterial properties, by changing the size of the loaded CSRR HMSIW transmission lines can be further miniaturized to reduce the broadside width. As shown in Fig. 4.15, HMSIW has issue of fluctuating the transmission coefficient at the higher frequencies in the single mode operating band of the SIW transmission line. This happens due to fringing effects (loss from the sideways opening). When CSRR are designed at much lower than f_c, due to the appearance of the higher order modes inside the single mode operating band of the SIW transmission lines, the fluctuation that appears in the SIW mode can be mitigated. In this work, the resonators are optimized to match with the fluctuation point, the mismatch that occurs in the transmission coefficient can be eliminated without affecting the propagation modes. As shown in Fig. 4.21(b), TE_{10} mode is still a dominant.



(a)



(b)

Fig. 4. 21: Proposed CSRR loaded HMSIW-based transmission line. (a) HFSS design (b) dominant mode field distribution. $W_{eff,HMSIW\_CSRR} = 285\ \mu m$.

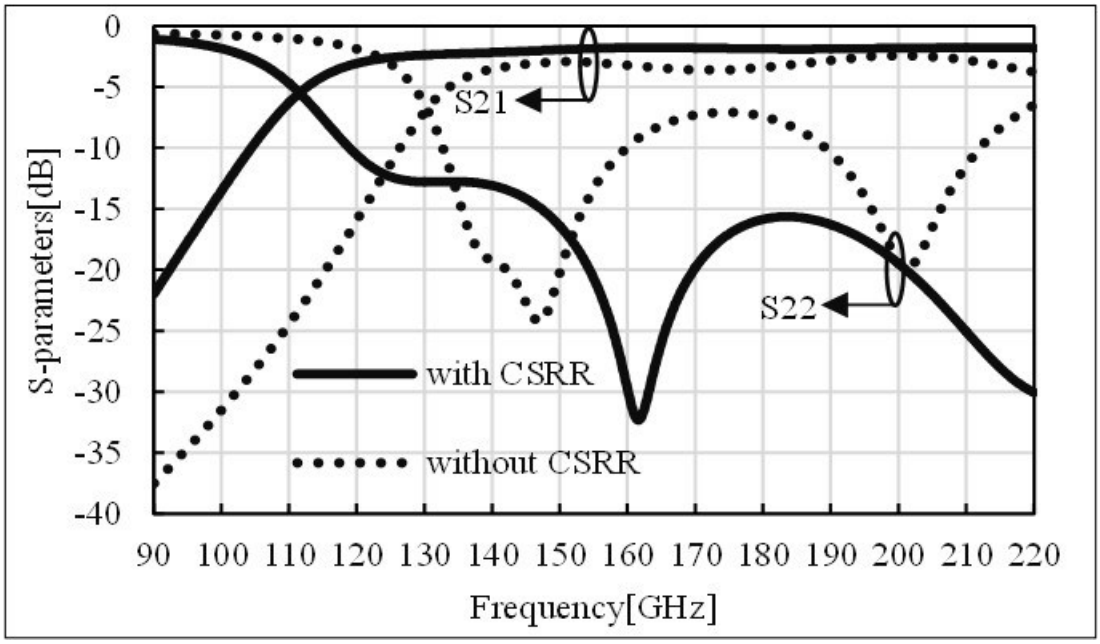
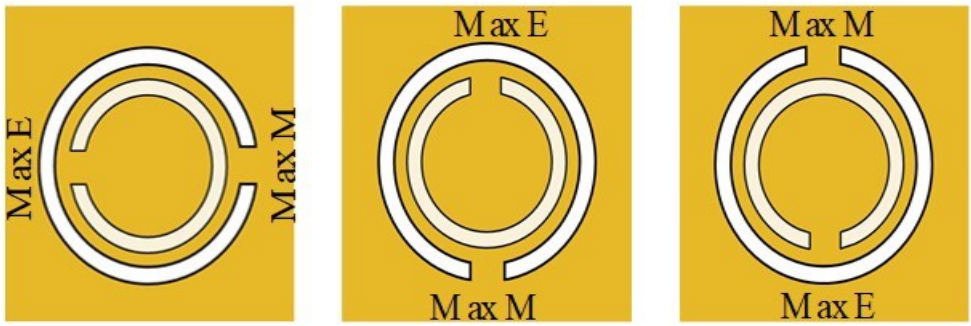


Fig. 4. 22: S-parameter simulation result of Fig. 4.12(b) and Fig. 4.21.

To understand the effect of the different shapes of the CSRR resonators in the proposed design of sub-THz SIW interconnect design different orientation of the resonators as shown in Fig. 4.23 are studied. CSRR resonators has maximum electric field in outer ring closed area and the maximum magnetic field in outer ring opening area. Similarly, HMSIW structure has maximum magnetic field towards vias sides and maximum electric field towards center i.e., opening ends. The design III exactly aligns with the HMSIW structure thus offering more advantage of miniaturization and matching as shown in Fig. 4.24.



(a) (b) (c)

Fig. 4. 23: HMSIW resonator with different CSRRs: (a) Design I; (b) Design II; (c) Design III.

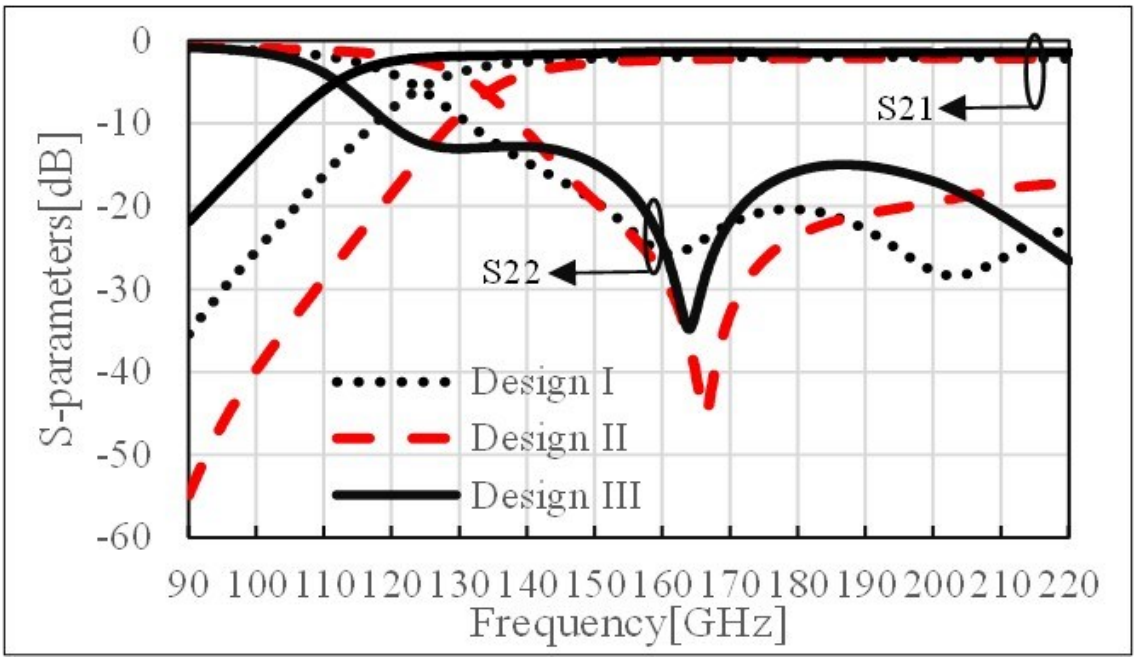


Fig. 4. 24: Simulation result of these different CSRR orientation shown in Fig. 4.23.

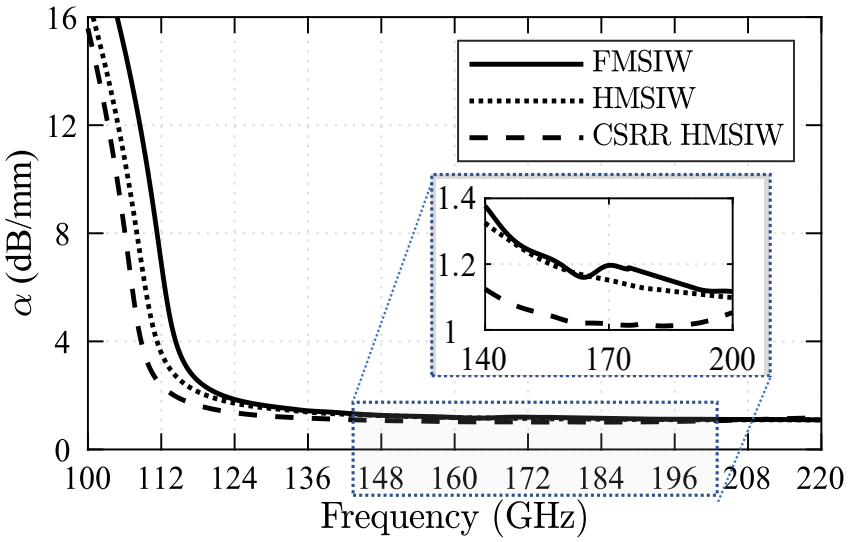


Fig. 4. 25: Comparison of simulated \alpha computed for standard SIW, HMSIW, and HMSIW with CSRR loadings.

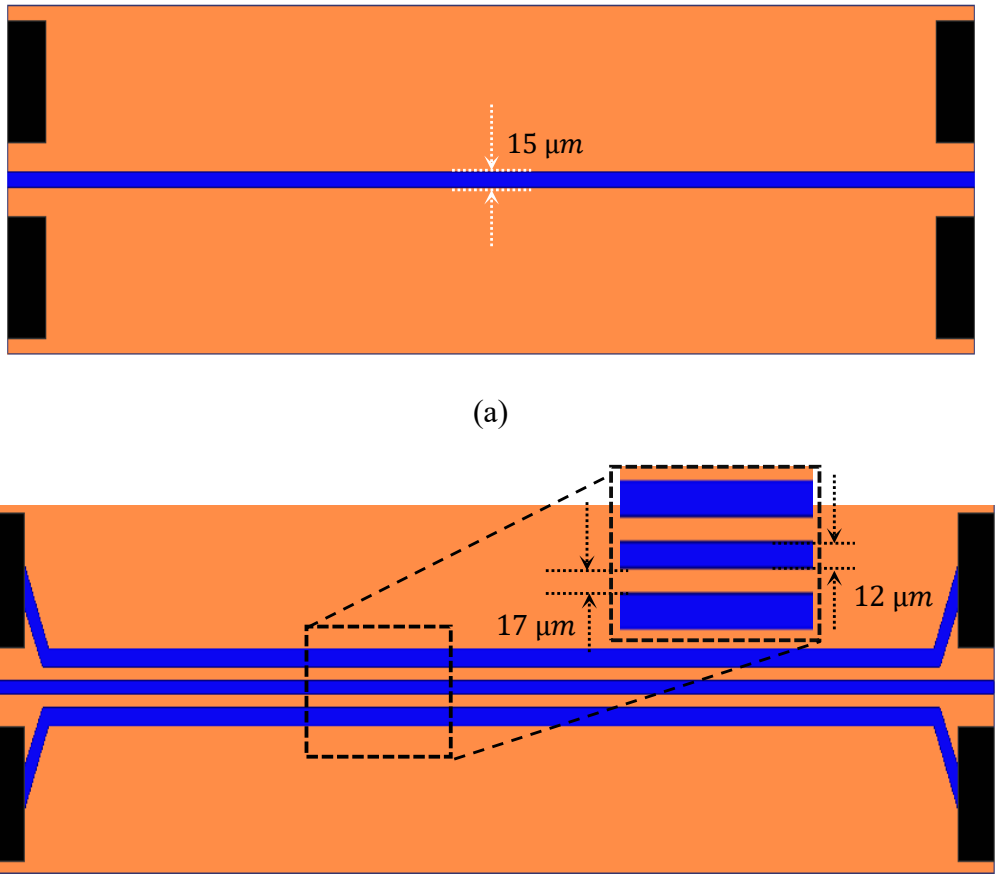


Fig. 4. 26: Transmission lines in CMOS technology. (a) Microstrip Line (MSL). (b) Conductor-backed coplanar waveguide (CB-CPW) Line.

The scattering (S-) parameters of CSRR-loaded HMSIW are simulated and investigated. As shown in Fig. 4.24, the transmission response is improved, and the f_c is changed compared to without CSRR loading, thus reducing the size of the HMSIW for miniaturization. The f_c drops from 120 GHz to 110 GHz. Similarly, the insertion loss has been improved from 2.5 dB to 1.4 dB, and the return loss from less than 7 dB to more than 15 dB.

Also, the comparison of α computed for SIW transmission lines in Fig. 4.12 and CSRR loaded HMSIW as shown in Fig. 4.21, shows that due to the reduced W_{SIW}/h in CSRR loaded HMSIW, it is lower than the standard SIW structure. To compare the on-chip SIW-based transmission lines with the various transmission lines that are designed in the same CMOS technology, we simulated the structures for microstrip line and the conductor-backed coplanar waveguide (CB-CPW) as shown in Fig. 4.26(a) and 4.27(b), respectively. The α of these structures is shown in Fig. 4.26. Similarly, Table I shows the size, α, and Q-factor comparison of these various on-chip interconnects. Relatively proposed CSRR Loaded HMSIW design has lower loss compared to the conventional transmission lines designs. The Q-factor is computed as [64];

$$\mathrm{Q} = \frac{\beta}{2\alpha}. \tag{4.19}$$

Table 4. 1: Comparison between the different commonly used transmission lines with SIW-based designs

	α [dB/mm] at f = 150 GHz	α [dB/mm] at f = 200 GHz	Q at f = 150 GHz	Q at f = 200 GHz
MSL	2.1	2.38	21	24
CB-CPW	1.72	1.9	22	26
FMSIW	1.18	1.15	14.6	31
HMSIW	1.182	1.1	14.7	27.8
CSRR loaded HMSIW	1.05	1.09	12.9	21.2

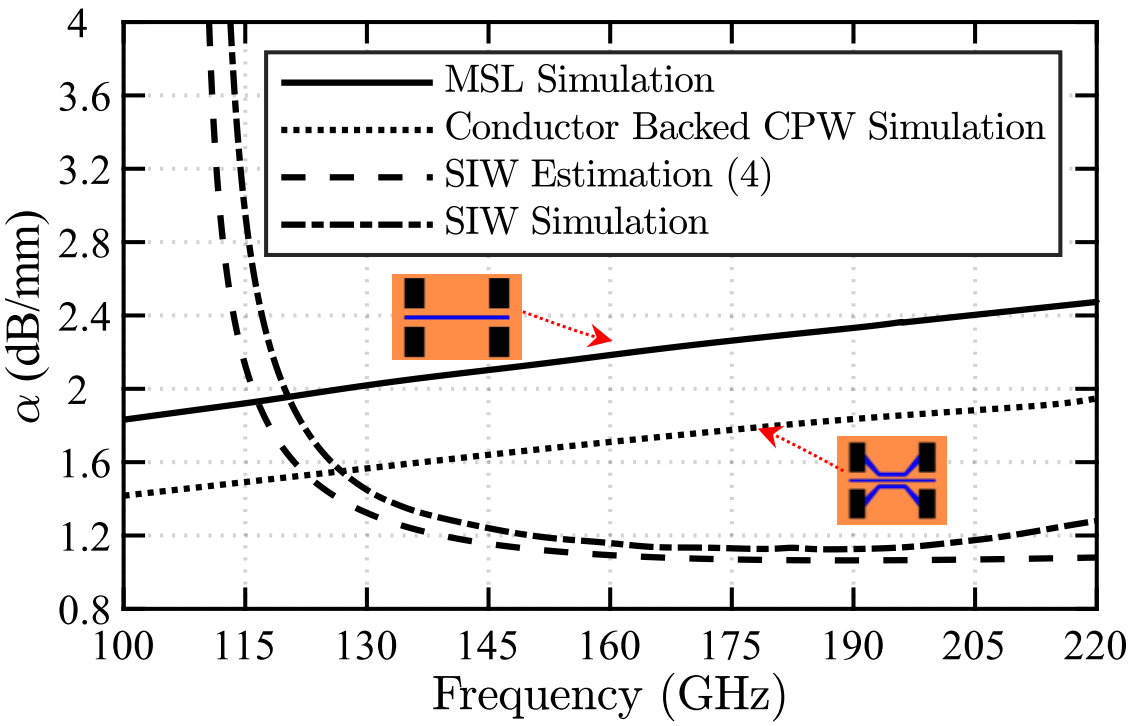


Fig. 4. 27: α computed for different on-chip transmission lines for the same transmission line lengths.

4.5 Sub-THz band m-TRL de-embedding

To use the structures in high frequency bands, we need the intrinsic results of any structures for getting the exact performance. In all the RF and microwave structures, measuring pads and feeding structures plays important role in the performance. It is desired to check the result of the device under test (DUT) only. Here comes handy de-embedding structures which are employed to extract the exact performance removing the unwanted structures. There are various de-embedding structures proposed for millimeter and THz band applications like Short only de-embedding, Thru only, de-embedding, Short-Open-Thru de-embedding, L-2L de-embedding, Line-Reflect-Match de-embedding, multi-line Thru-Reflect-Line (m-TRL) de-embedding. Among them, m-TRL de-embedding seems promising for the frequency particularly above 100 GHz bands [69]. Here we use m-TRL de-embedding method as presented in [67]-[69] for de-embedding of our proposed structures which are working all above the 100 GHz frequency bands.

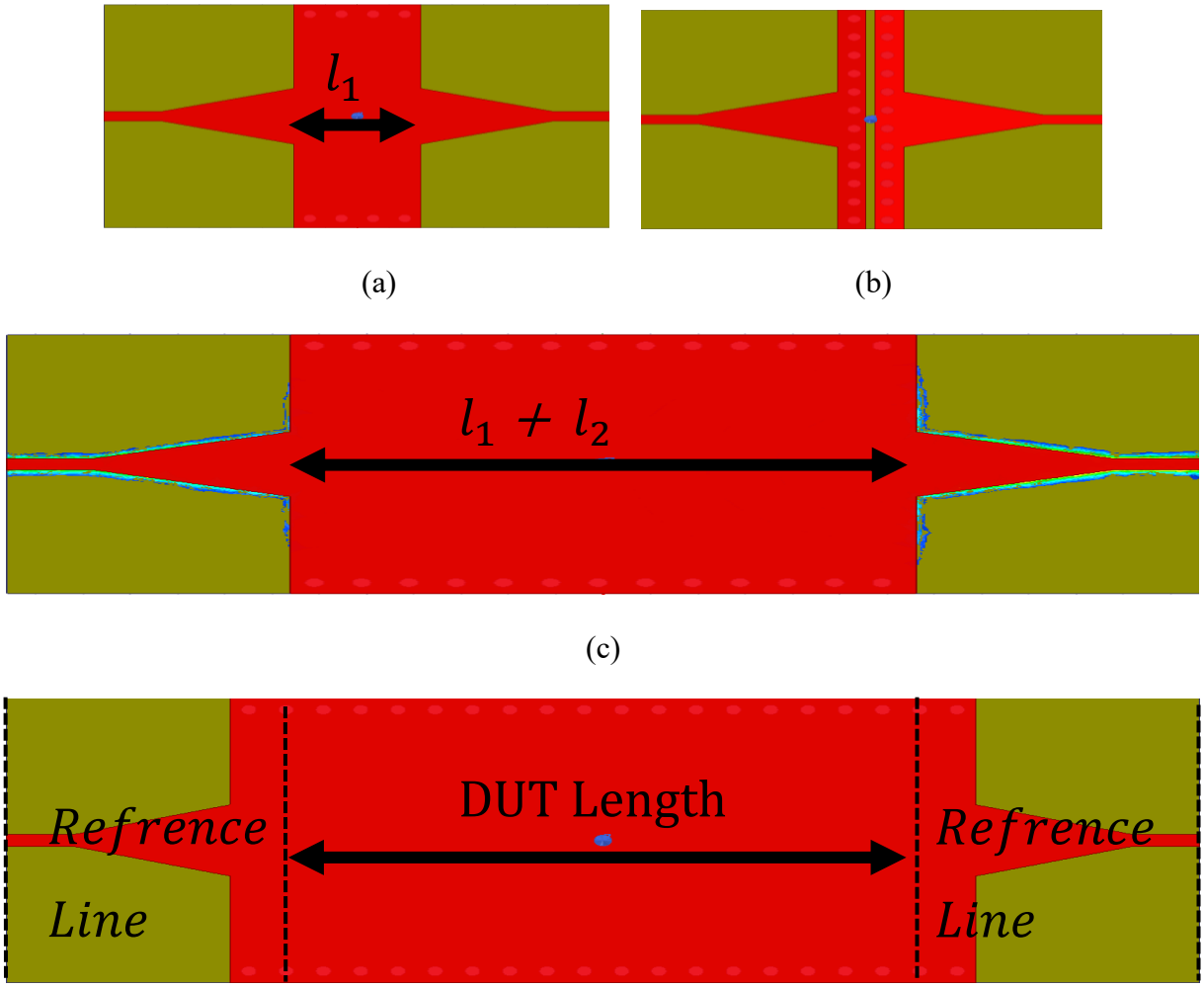
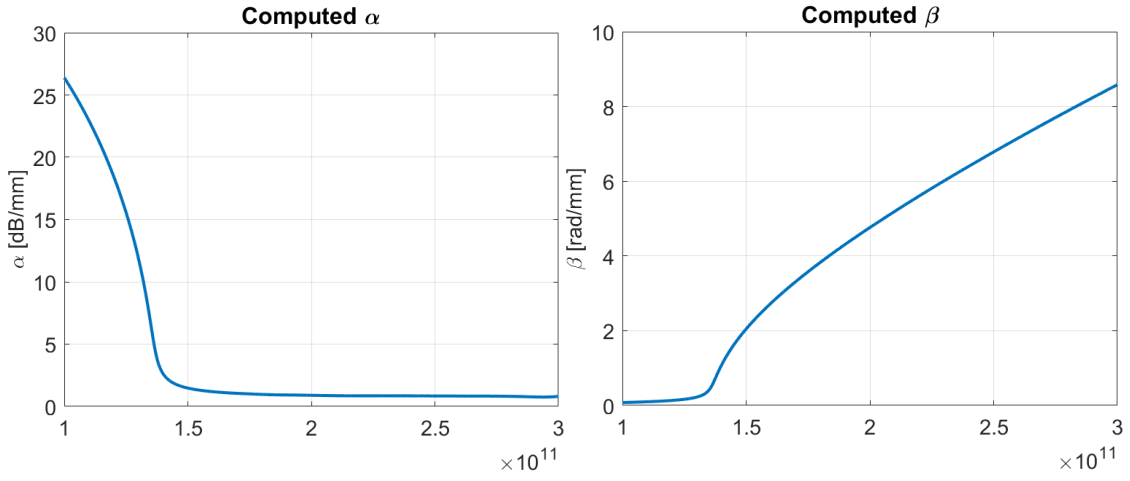


Fig. 4. 28: m-TRL De-embedding of the sub-THz band SIW transmission line. (a) Thru structure. (b) Reflect structure. (c) Line structure. (d) DUT transmission line under test.

To get the intrinsic result of the SIW interconnect itself for the use in other circuit designs, multi-line Thru-Reflect-Line (m-TRL) was performed in the proposed structure. For de-embedding upto maximum 300 GHz, three separate de-embedding structures are used for de-embedding which are as:

- Thru length $l_1 = \frac{\lambda g}{10} = 63.09\ um\ @\ 300GHz$
- Line length $l_1 + l_2$ *where* $l_2 = 0.89\lambda g = 561\ um$

whereas reflect length is exactly half of the thru length having a gap and the shorting vias as in illustrated in Fig.4.28 (b).



(a) (b)

Fig. 4. 29: Computed propagation constant of de-embedding structures. (a) Attenuation constant. (b) Phase constant.

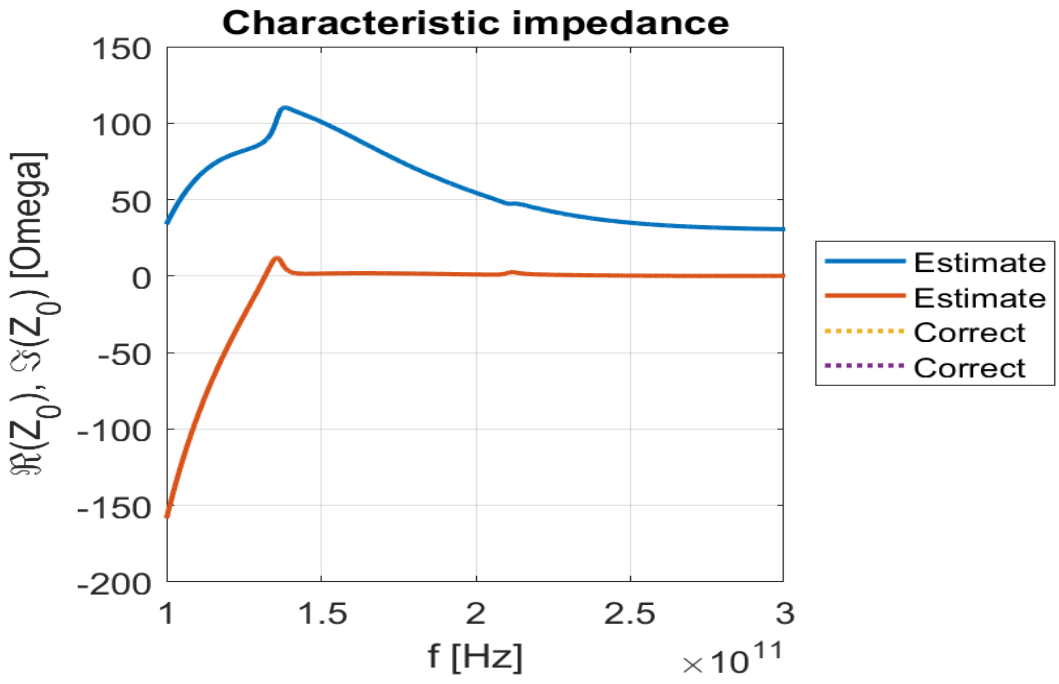


Fig. 4. 30: Characteristic impedance of the de-embedding structure in Fig.4.28.

Fig. 4.29(a) and (b) shows the computed propagation constant (attenuation constant and phase constant) of the de-embedding structures. The computed characteristic impedance for the de-

embedding structures is shown in Fig. 4.30. Finally, these information's are used to de-embed the S-parameters of the DUT structure Fig. 4.28 (d). The initial S-parameters simulated for the DUT including pads is shown in Fig. 4.31 which is not good. The de-embedded result of the S-parameters is shown in Fig. 4.32, which is a desired result of the proposed structure for higher frequency applications.

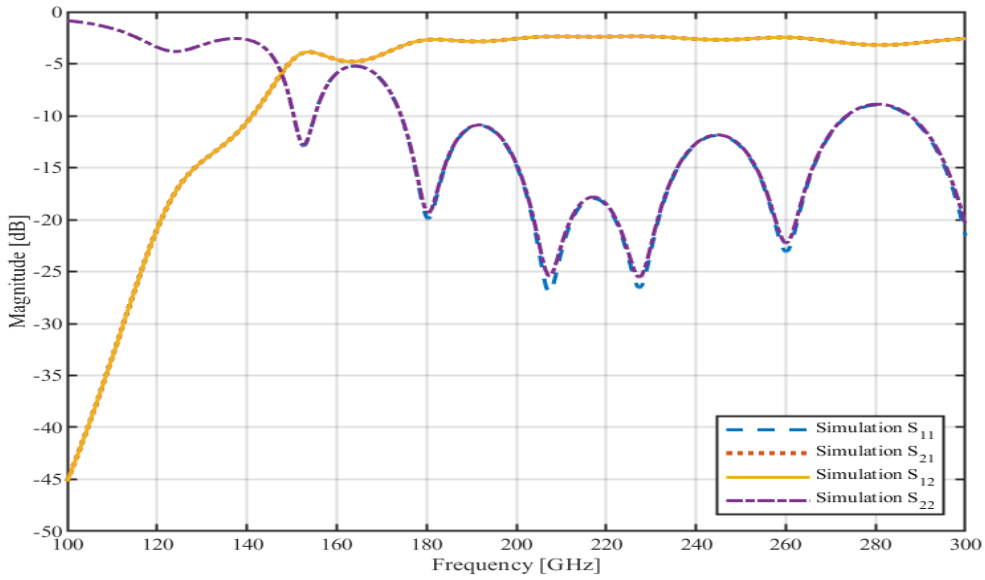


Fig. 4. 31: S-parameter simulation result of DUT in Fig. 4.28(d) including measurement pads.

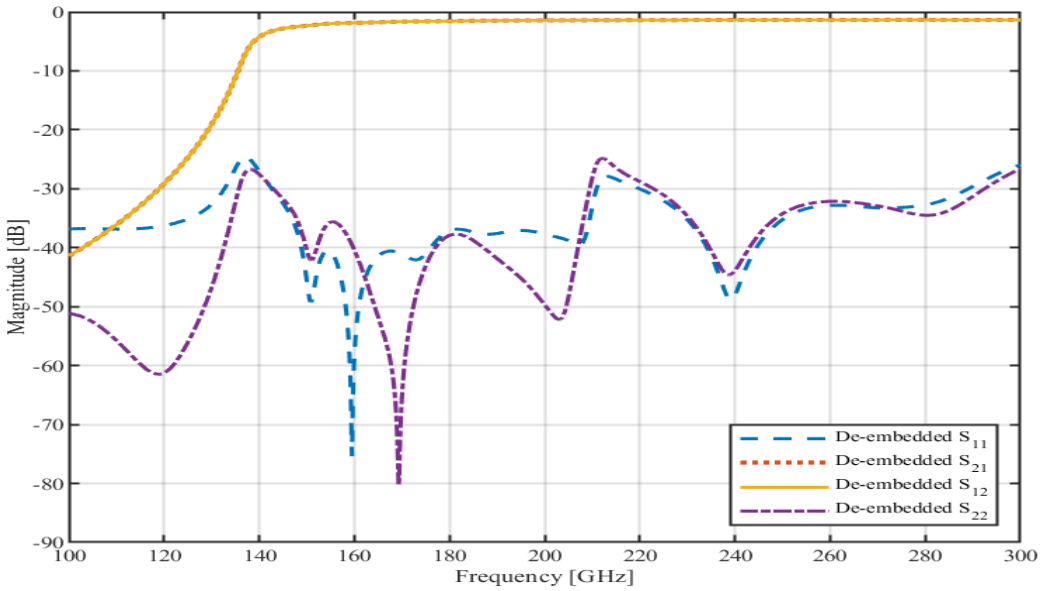


Fig. 4. 32: De-embedded S-parameters result of DUT shown in Fig. 4.21 (d).

Similar de-embeddings are performed with the following two sets of the proposed HMSIW interconnect lines as shown in Fig. 4.33 and 4.36. We get the perfect desired results from the de-embedding in both the designs in Fig. 4.35 and 4.38.

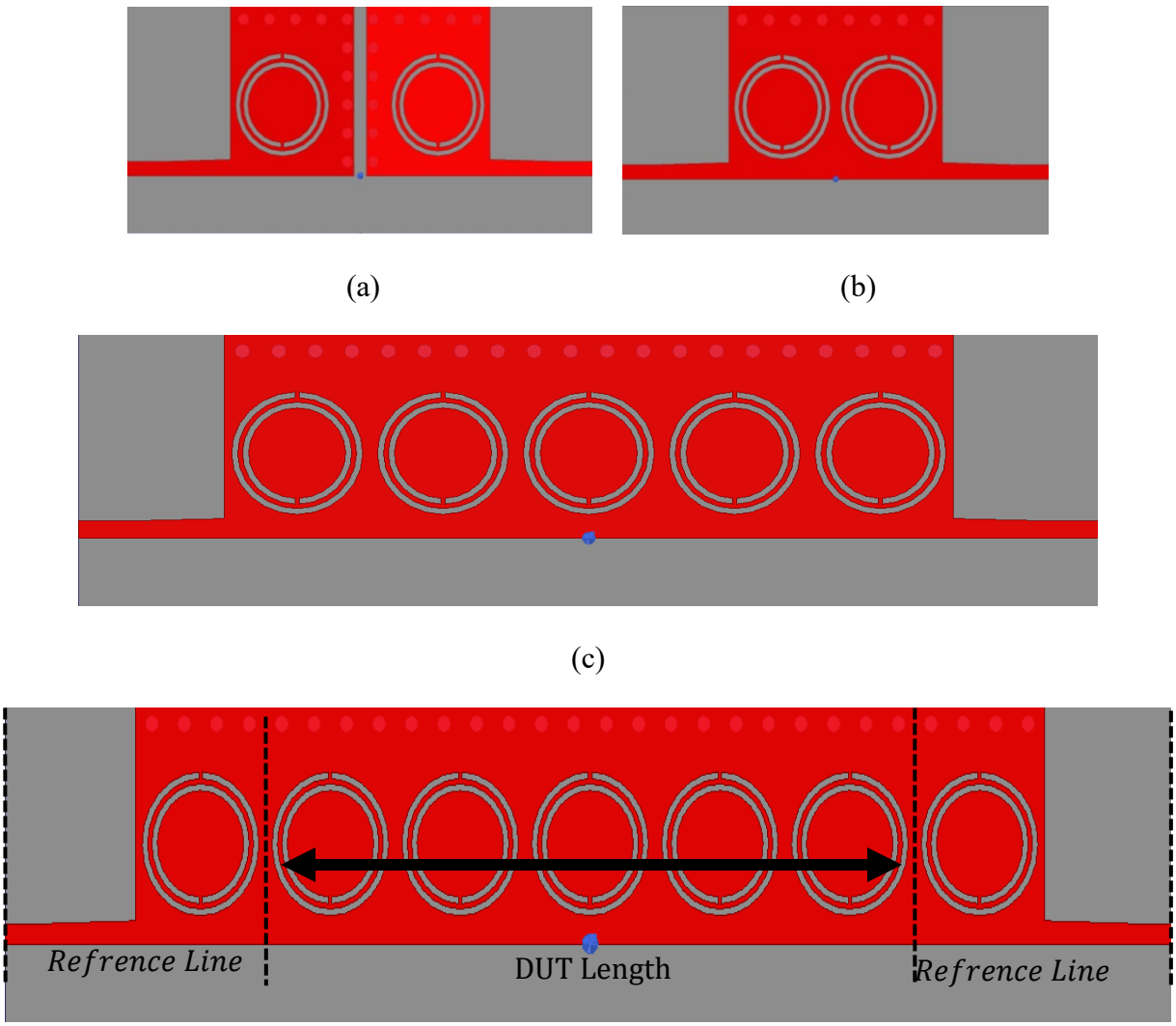


Fig. 4. 33: De-embedding of the proposed sub-THz band HMSIW interconnect. (a) Reflect structure. (b) Thru structure. (c) Line structure. (d) DUT line.

The de-embedded result of the HMSIW interconnect shown in Fig. 33 (d) shows a good result with the insertion loss less than 1.6 dB throughout the operating band of the single-mode operating band of SIW as shown in Fig, 35.

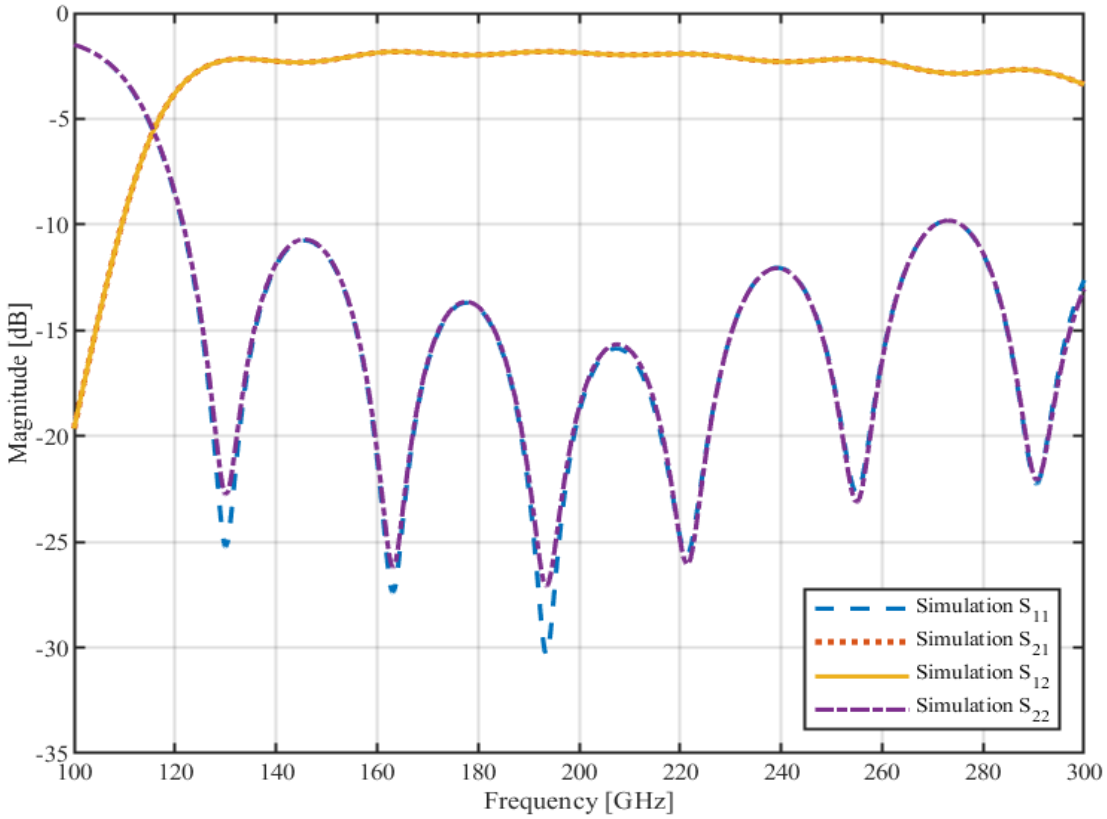


Fig. 4. 34: S-parameter simulation result of the DUT shown in Fig. 4.33 (d) including measurement pads.

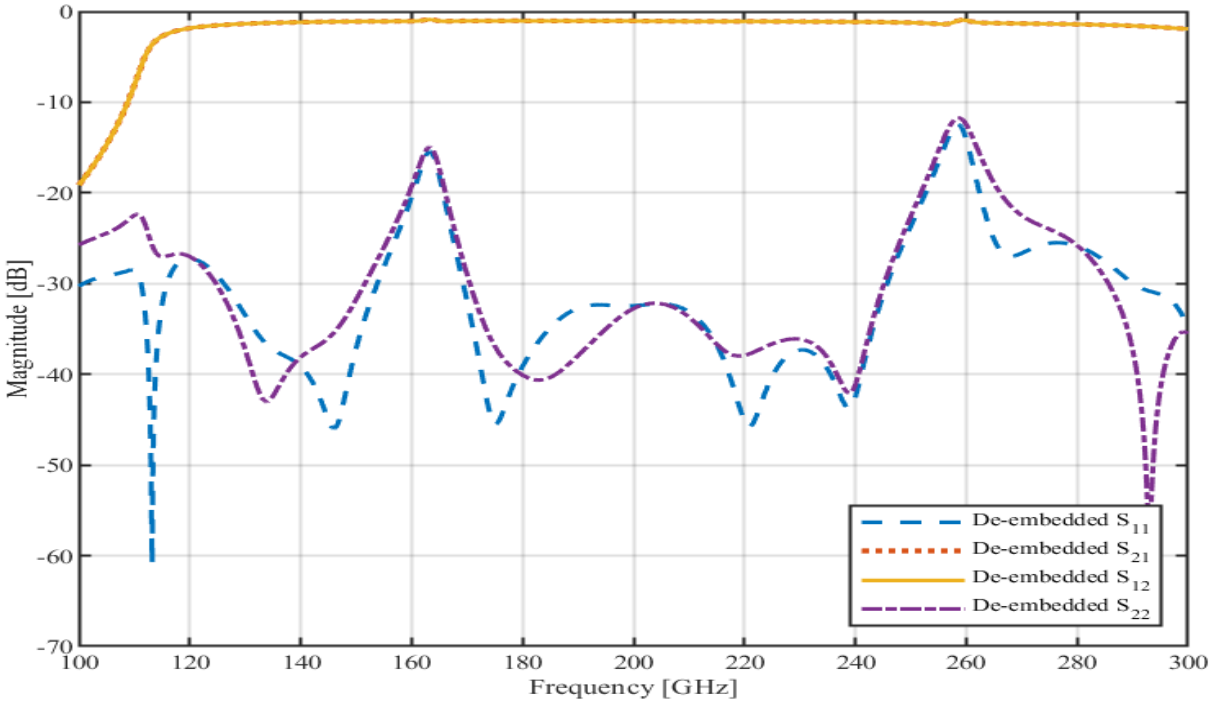


Fig. 4. 35: De-embedded S-parameters result of DUT shown in Fig. 4.33 (d).

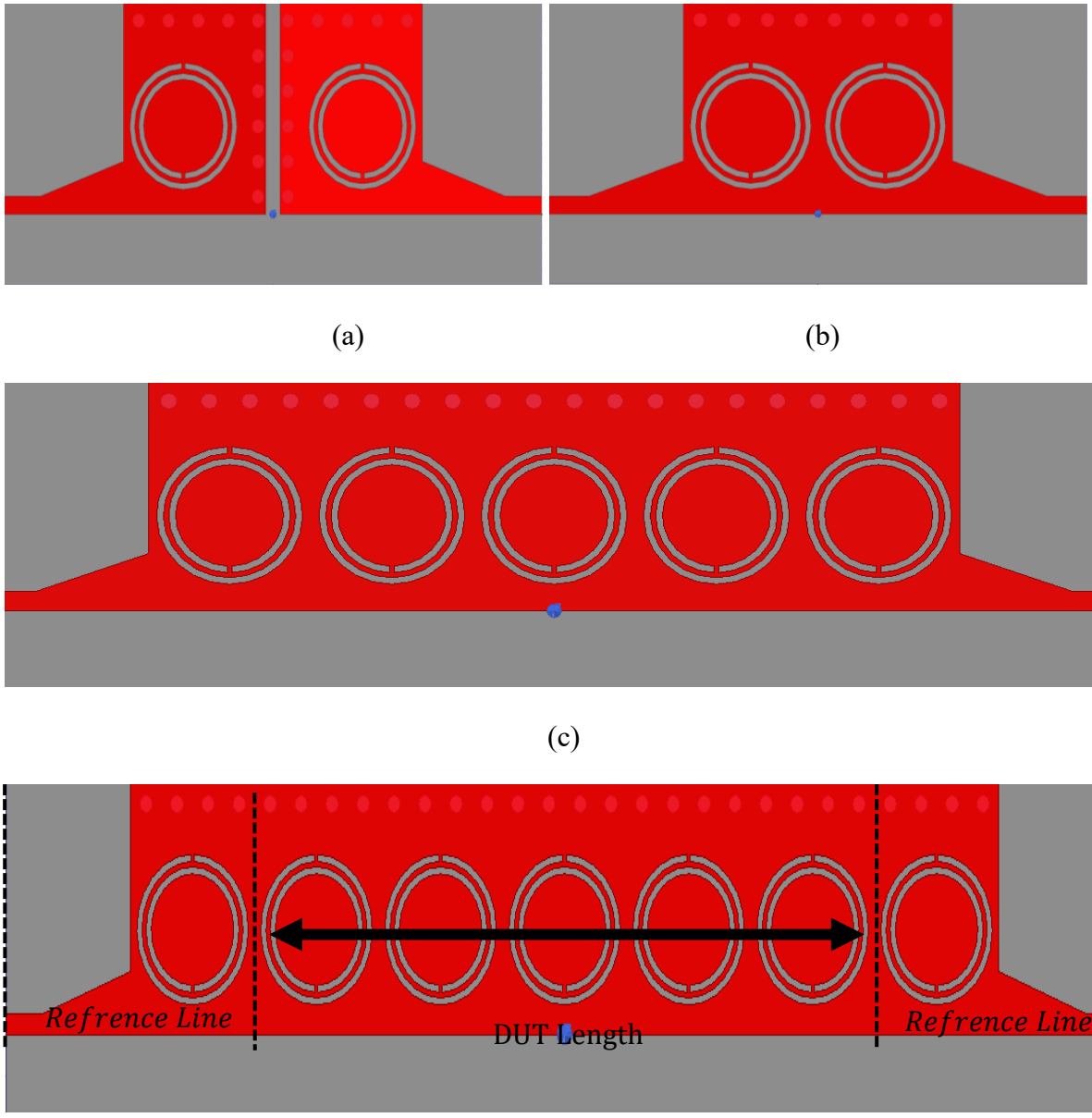


Fig. 4. 36: De-embedding of the proposed sub-THz band HMSIW interconnect with wider taper feeding line. (a) Reflect structure. (b) Thru structure. (c) Line structure. (d) DUT line.

The simulated result of the proposed sub-THz band HMSIW interconnect with wider taper feeding line seems unwanted. After de-embedding in Fig. 4.38, the result is too good to be used as the transmission line in the sub-THz band applications for various designs like filters, transmission lines, couplers, etc.

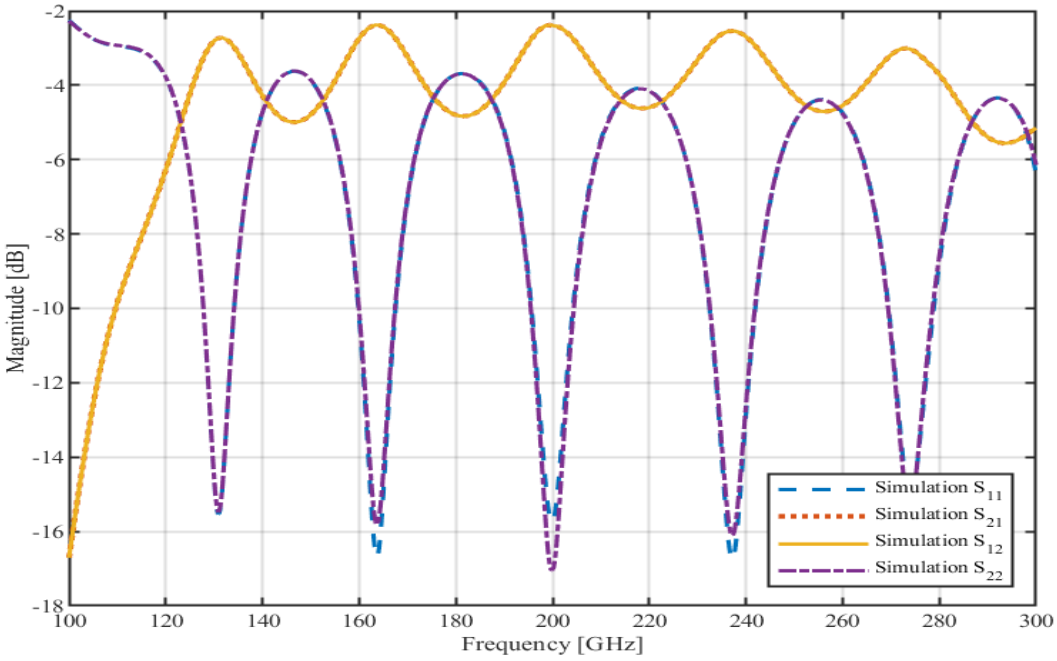


Fig. 4. 37: Fig. 4. 24: S-parameter simulation result of the DUT shown in Fig. 4.26 (d) including measurement pads.

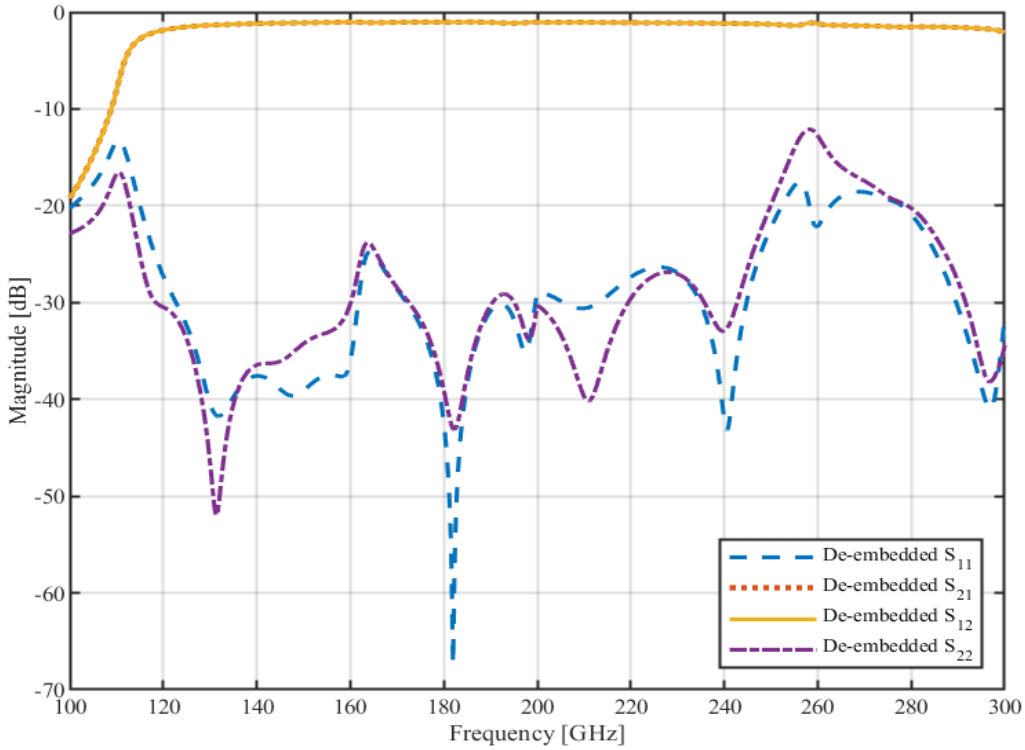


Fig. 4. 38: De-embedded S-parameters result of DUT shown in Fig. 4.26 (d).

4.6 Sub-THz band SIW Interconnects Fabrication and Measurement

The micrographs of the fabricated prototypes of the proposed resonators are shown in Fig. 4.39. In each design, dummy pads are positioned opposite the feeding port to provide stability for the chips during the measurements and to aid in the de-embedding of the results. The measurement setup consists of MPI TS200-THZ probe station, Anritsu MS4647B 70 GHz Anritsu vector network analyzer, Anritsu MA25400A mmWave module 70 KHz to 220 GHz, two MPI T220 ground-signal-ground (GSG) probes with a 75 μm pitch. The calibration was performed using MPI QAlibria software, employing a two-step process: (i) from 100 MHz to 50 GHz using the thru-reflect-reflect-match (TRRM) method at 100 MHz step size, and (ii) from 50.2 GHz to 220 GHz using the multiple thru-reflect-line (mTRL) method with four transmission lines, at 200 MHz. The photograph of the measurement setup is shown in Fig. 4.40.

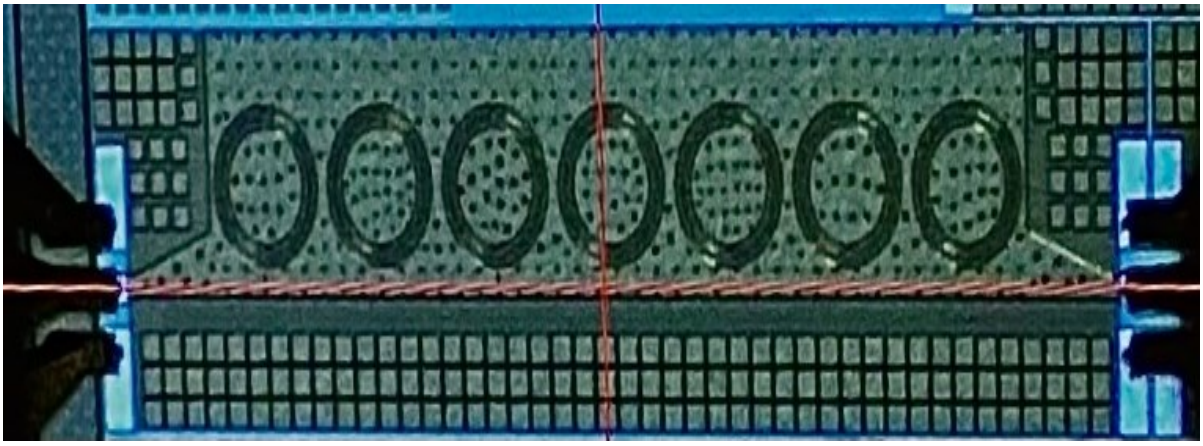


Fig. 4. 39: Micrographs of the fabricated CSRR loaded HMSIW transmission line chip.

The simulated and measured S-parameters results are shown in Fig. 4.41. Limited by our experiment environment, we can only measure data up to 220 GHz. The cutoff frequency is 109 GHz which agrees well with the simulation. Simulations results are presented without including the measurement pads and the measurement results are presented after de-embedding to remove the effects of measurement pads. The measurement result shows a good agreement with the simulation results which is presented without pads. m-TRL de-embedding were employed to remove the effect of the pads.

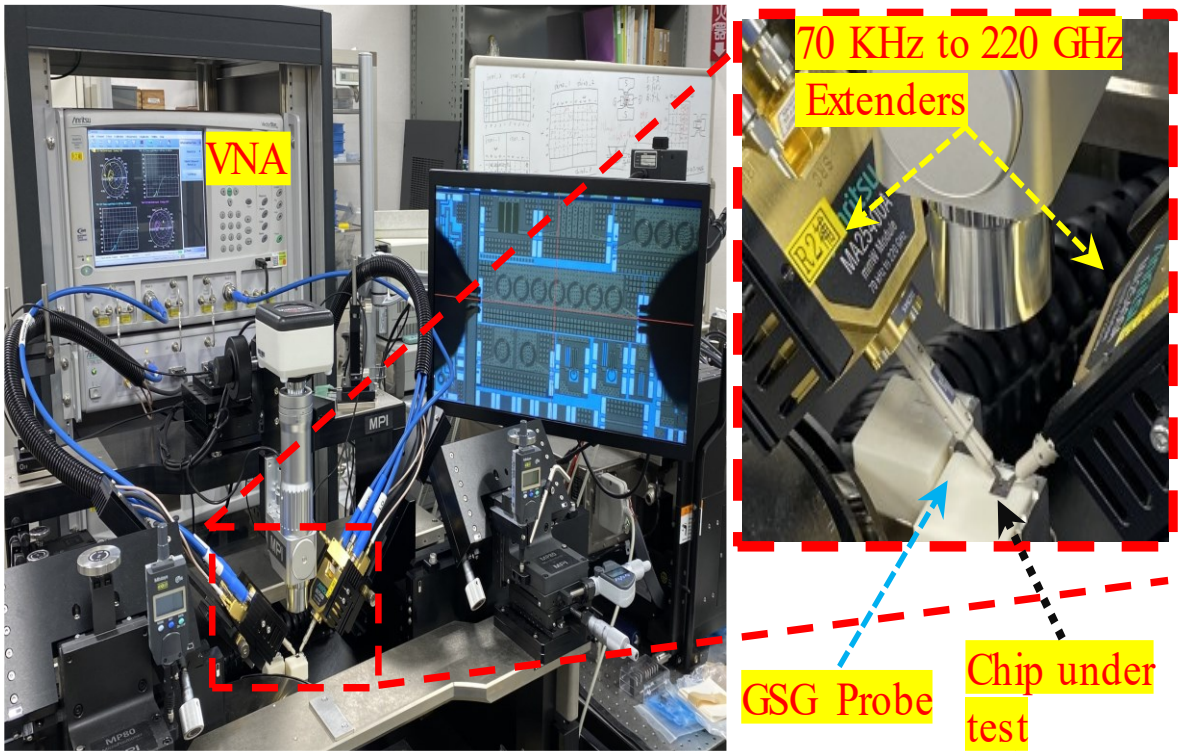


Fig. 4. 40: Chip measurement setup.

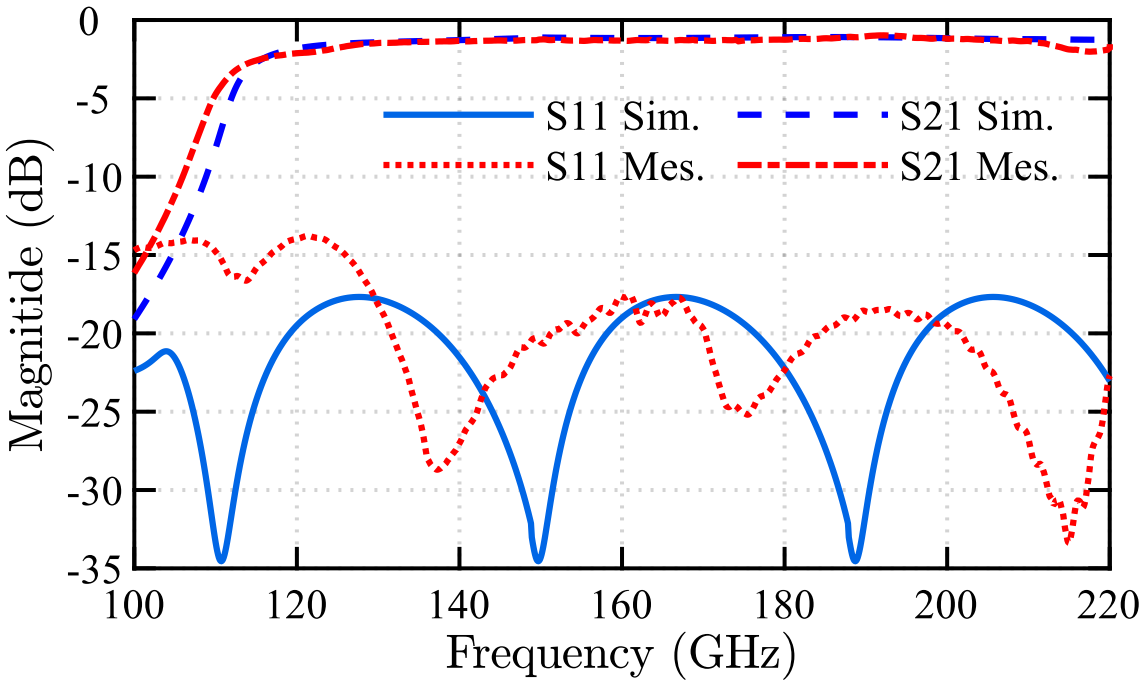


Fig. 4. 41: Simulation and de-embedded S-parameters of CSRR loaded HMSIW transmission line.

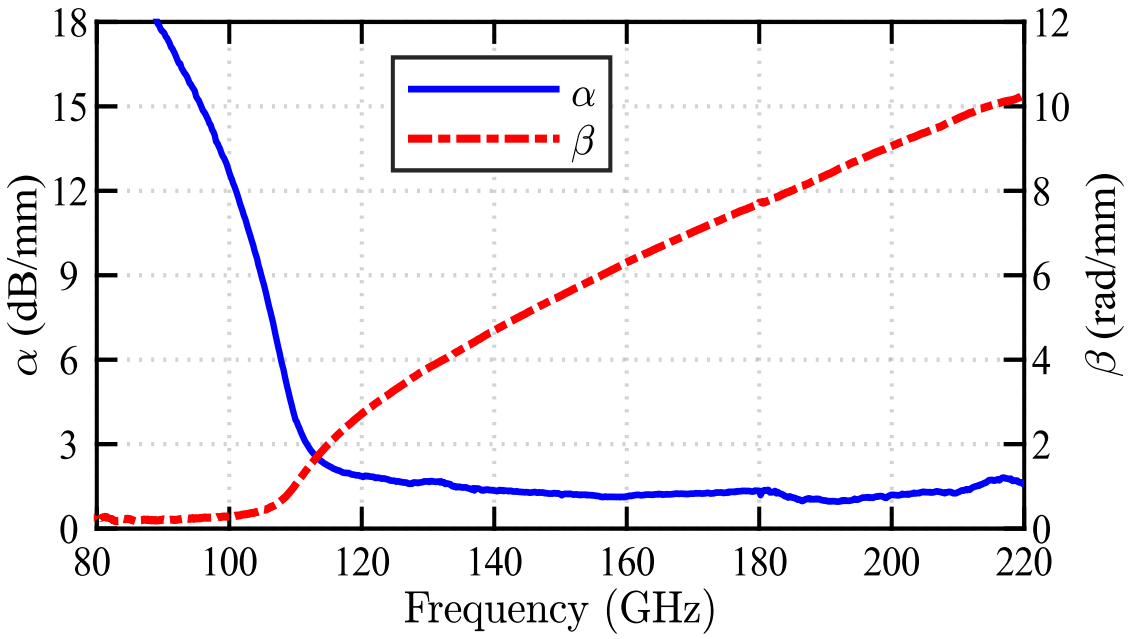


Fig. 4. 42: Measured propagation constant of proposed transmission line.

Table 4. 2: Summary of the measurement results and the performance comparision of the different SIW-based on-chip transmission lines with the other state-of-the-arts

	[61]	[62]	[70]	[71]	[69]	**This Work**
Transmission Line	SIW	SIW	SIW	SIW	Shielded MSL	**SIW**
Frequency range [GHz]	140-220*	180-220	200-330	110-220	N/A	**110-220**
Insertion loss [dB]	<5*	5	<7	< 2	N/A	**<1.8**
SIW Attenuation @ *f* = 220 GHz [dB/mm]	2.35#	2.4#	1.8#	1.5	1.5*	**1.2**
Transition loss @ *f* = 220 GHz [dB]	3.2#	2#	1.2#	0.8#	N/A	**0.335**

N/A: Not Available. *estimated from the graphs. #simulation results.

The measured attenuation (α) and phase constants (β) are shown in Fig. 4.42. The α from 135 GHz to 220 GHz is maintained below 2 dB/mm, and from 175 GHz to 220 GHz is around 1.4 dB/mm. Also, the computed Q-factor at 220 GHz is 35. This works outperforms other state-of-art in terms of insertion loss, attenuation, and the Q-factor, as shown in the performance comparison Table. 4.2.

4.7 Sub-THz band SIW Resonators Design in CMOS Technology

4.7.1 Miniaturization of Sub-THz band SIW Resonators Design and Implementation

4.7.1.1 Standard SIW and Half Mode SIW Resonator Implementation

The SIW cavity is implemented by closing one side of the structure in Fig. 4.1. Considering plane of symmetry at the fundamental TE_{10} mode, as shown in Fig. 4.43, the resonators with sub modes with same resonance can be obtained as in Fig. 4.44. This structure can be pushed to extreme miniaturization, but after multiple cuts it is difficult to preserve the fundamental resonance frequency of such miniaturized designs and leads to low quality factor.

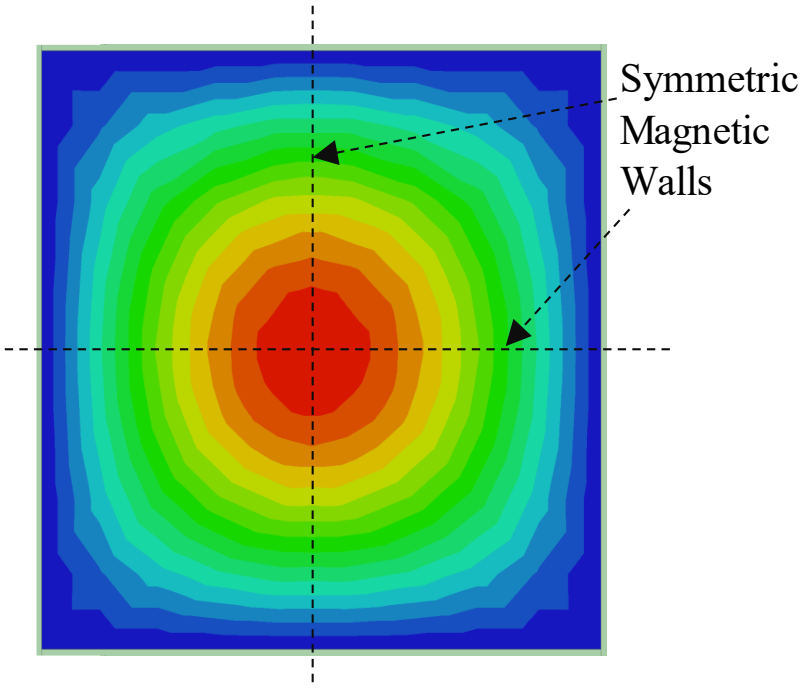
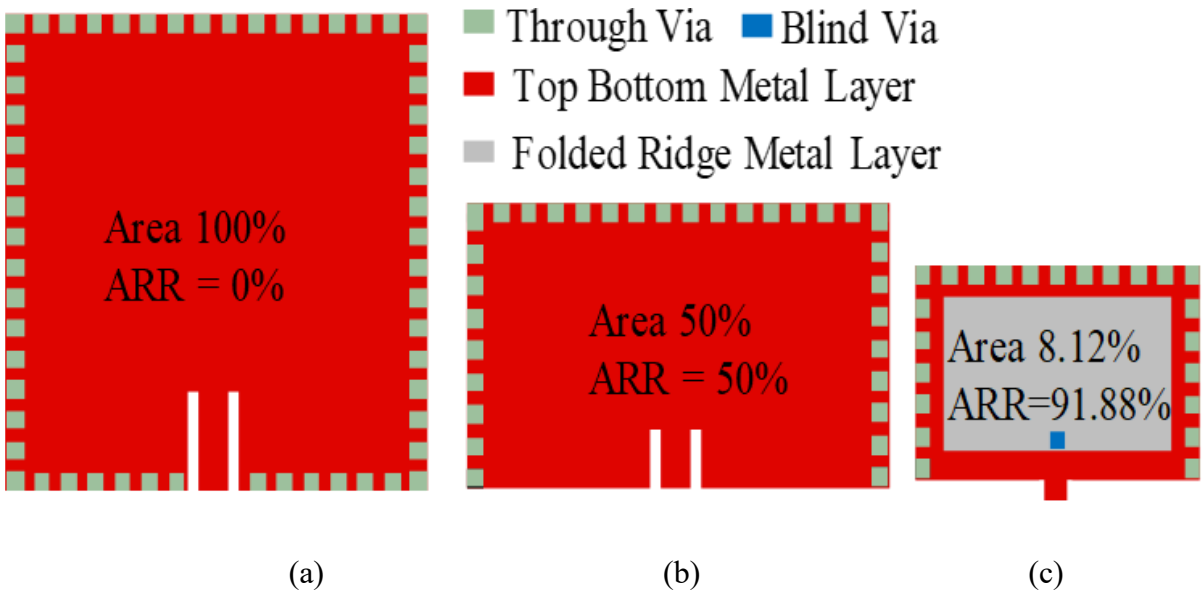


Fig. 4. 43: Standard SIW resonator with electric field distribution.



(a) (b) (c)

*Fig. 4. 44: SIW resonators. (a) Standard mode. (b) Half mode. (c) Half mode with folded ridge. *ARR = Area Reduction Ratio compared to standard SIW at the same resonance.*

Fig. 4.44 (a) and 4.44 (b) show the standard mode SIW and HMSIW resonators. Designing standard mode SIW structures requires a larger area, even at very high frequencies. The HMSIW structure is exact half the size of standard SIW and still preserves the resonance of standard SIW structure. To provide input to the SIW-based structures, various feeding structures have been adopted [72], [73]. Microstrip feeding with slot feeding is utilized in this work to achieve the compact size of the overall cavity structure. The impedance of the HMSIW ($Z_{initial}$) and HMSIW with slot (Z_{with_slot}) as shown in Fig 4.44 (a) is shown in Fig. 4.45. To match the input impedance of HMSIW $Z_{initial}$, we need a matching network consisting of two elements. By introducing the slot in the HMSIW, as shown in Fig. 4.44(a), the initial impedance is changed to Z_{with_slot} and now with the single series inductor, the input impedance can be matched. So, simple impedance matching of HMSIW is achieved with a series inductor implemented with the transmission line.

Still, the size of HMSIW is bigger for on-chip implementation. To further miniaturize HMSIW, folded ridge structure can be loaded, as shown in Fig. 4.44(c). The use of the folded ridge structure introduces additional capacitance as a result of the close proximity of the folded ridge to the sidewall and the height difference between the ridge and the top/bottom walls of the main SIW cavity. This phenomenon was discussed in chapter 3.

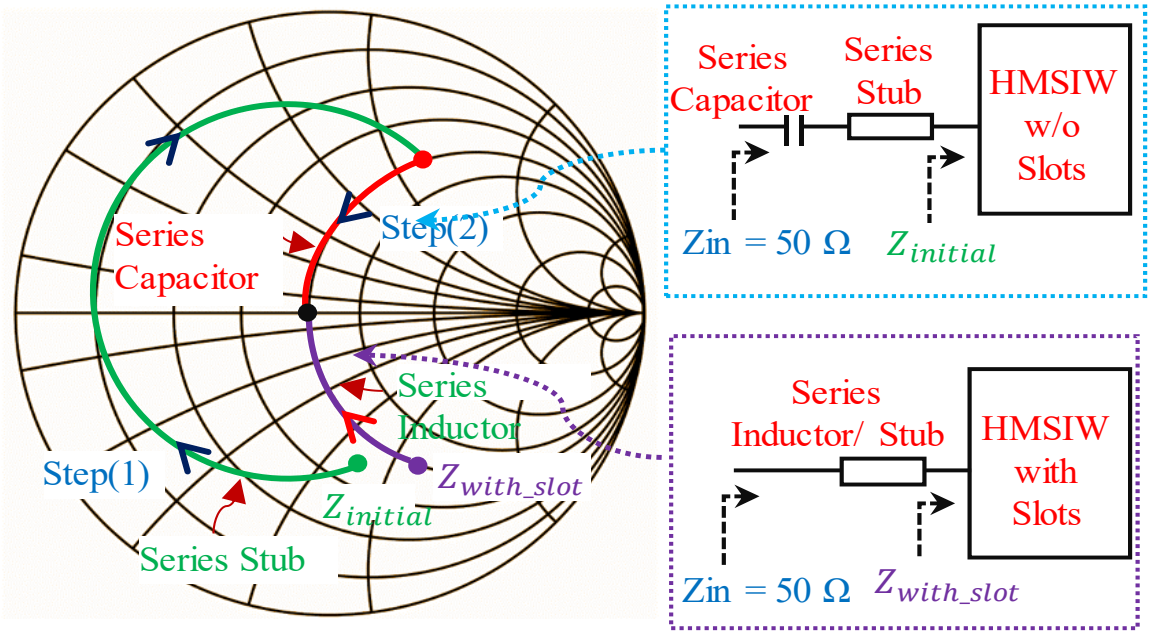


Fig. 4. 45: Matching steps for HMSIW resonator in Fig. 4.44(b) to 50 Ω input impedance. Without slots in HMSIW, it needs two matching elements: series stub and series capacitor. After placing slots in HMSIW, it can be matched using a single series inductor element.

Due to the inclusion of the folded ridge structure, there is an increase in capacitance, leading to a reduction in the resonance frequency. Consequently, the input impedance gets closer to the desired 50 Ω, as illustrated in Figure 4.45. With a simple transmission line and removing some ground from this transmission line, desired impedance matching is achieved. The extent of added capacitance in the folded ridge relies on factors such as the width of the ridge, the position of the blind via, and the height of the ridge. By appropriately selecting these parameters, it becomes possible to achieve significant size reduction in folded ridge SIW resonators.

Table 4. 3: Size and ARR of standard mode, HMSIW, and folded ridge HMSIR SIW resonators in Fig. 4.44.

Cavities Designed at f_o = 200 GHz	**Size (mm^2)**	**Area with respect to Standard SIW**	**ARR**
Standard Mode	0.287	100 %	100 %
HMSIW	0.144	50 %	50 %
Folded Ridge HM SIW	0.0212	8.12 %	91.88 %

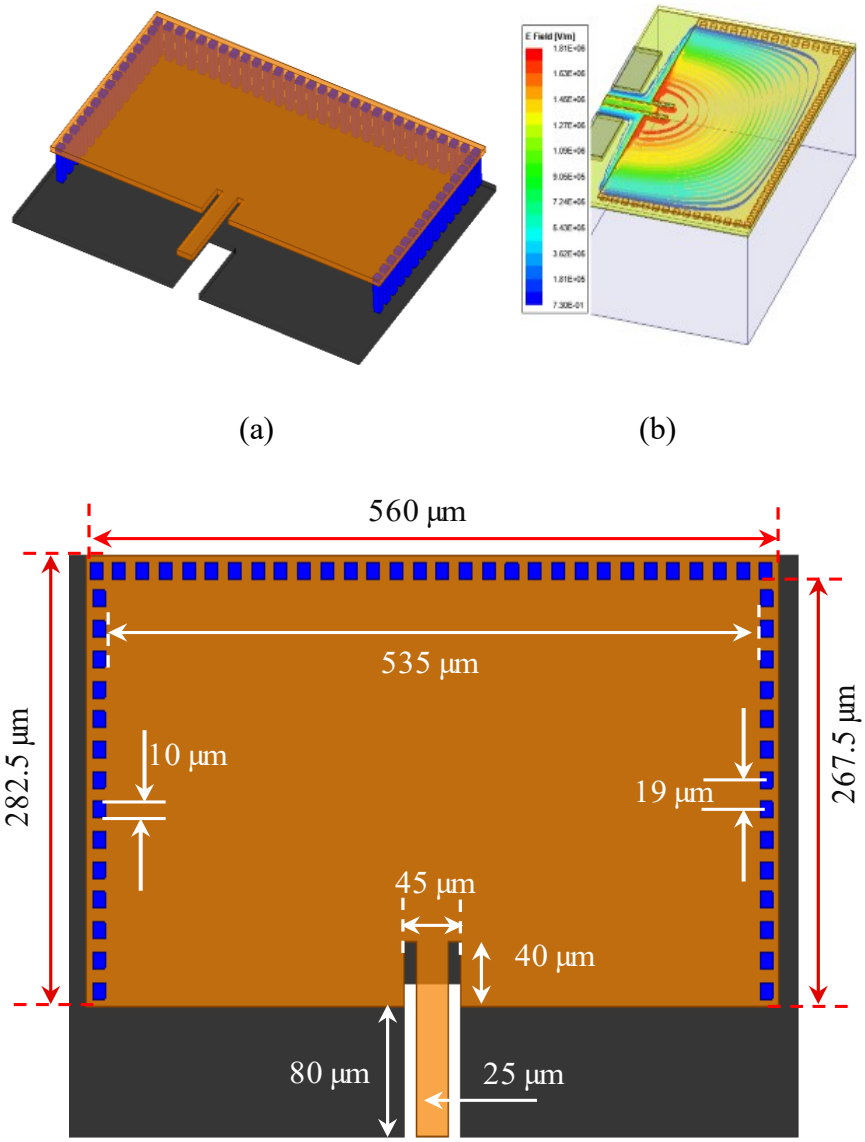


Fig. 4. 46: HMSIW resonator EM model. (a) 3D view. (b) Electric field distribution. (c) Top View.

The standard HMSIW cavity 3D view is shown in Fig. 4.46. The HMSIW cavity resonator is created by taking half portion of standard SIW resonator. The dimensions this resonator is placed in the figure itself. The overall dimension of the half-mode cavity resonator for getting the resonance of 200 GHz is 536 µm x 267.5 µm. The feed line is varied along the HMSIW cavity's sides to select the best feeding point. The variation of the matching and frequencies while varying the feed line is shown in Fig. 4.47. Best response is achieved when the feed line

is placed in the centre of the half-mode opening edge. The electric field distribution of the HMSIW at resonance frequency is shown in Fig. 4.46(b). The dominant mode is still TE_{10}.

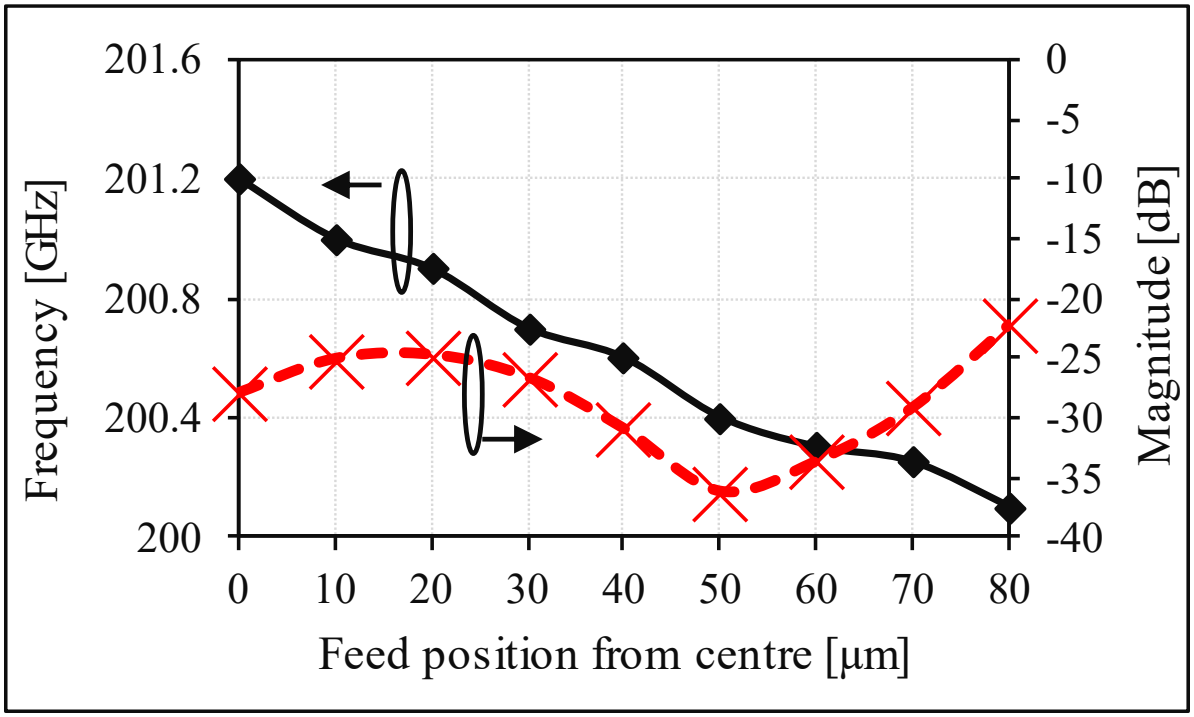
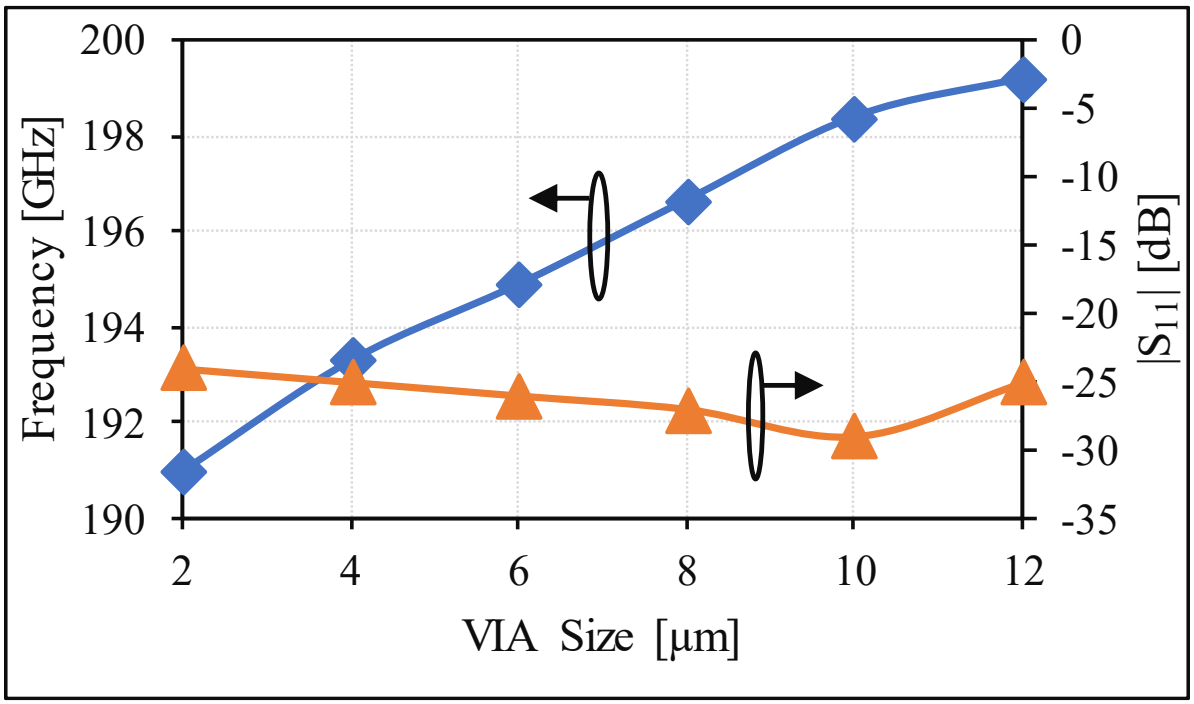
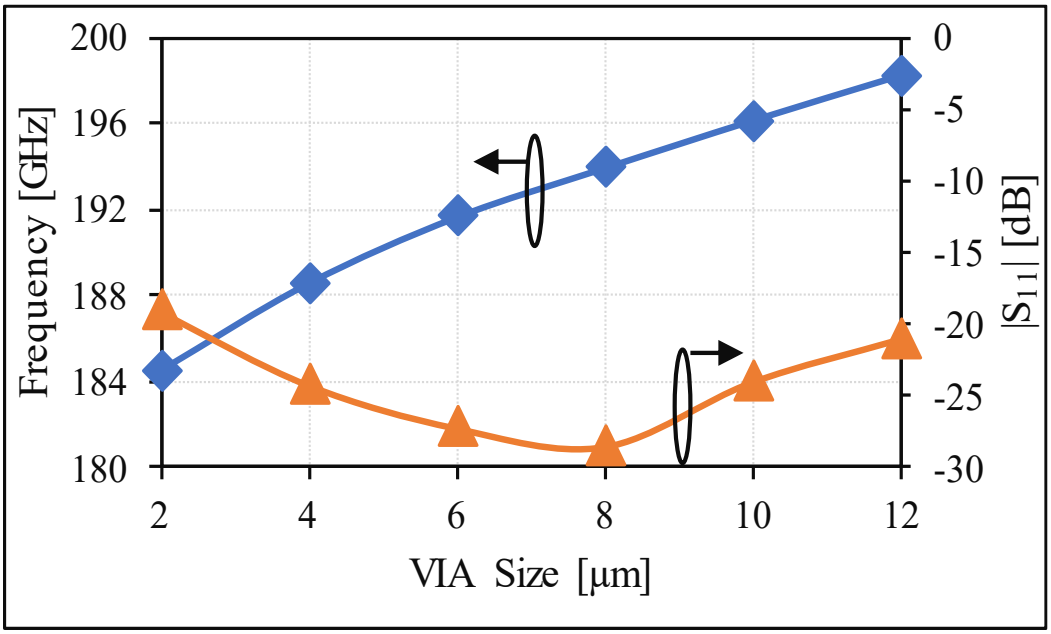


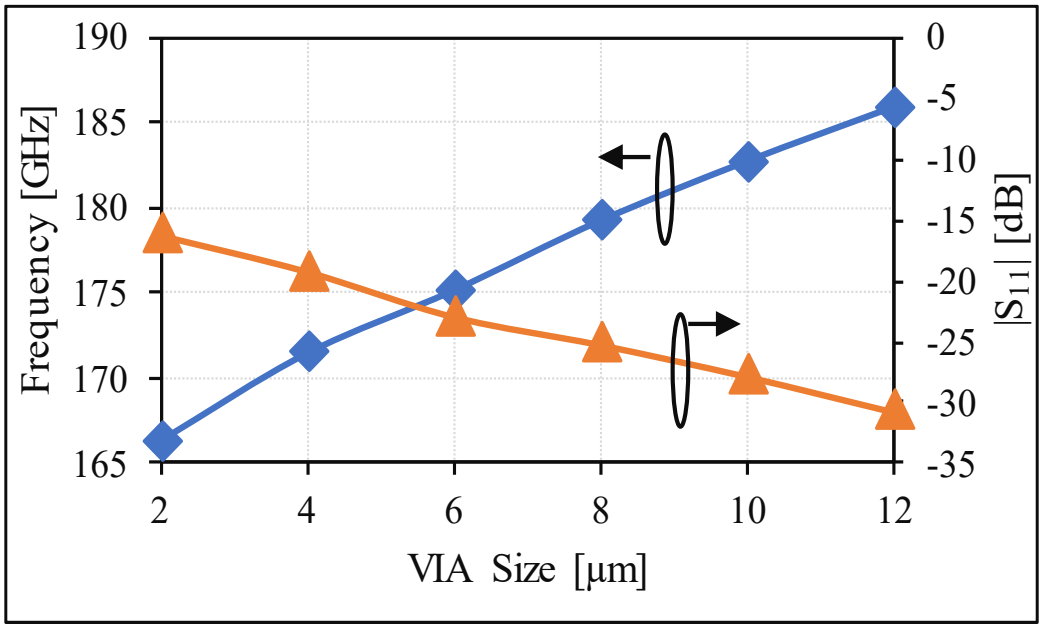
Fig. 4. 47: A 200 GHz HMSIW resonator with frequency and reflection coefficient magnitude by varying feed position.



(a)



(b)

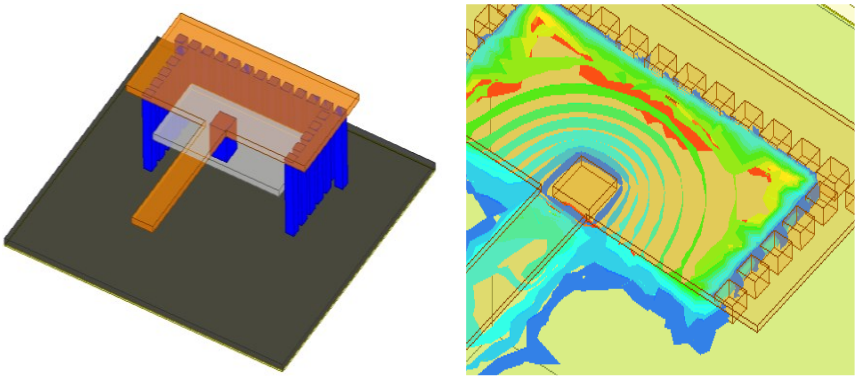


(c)

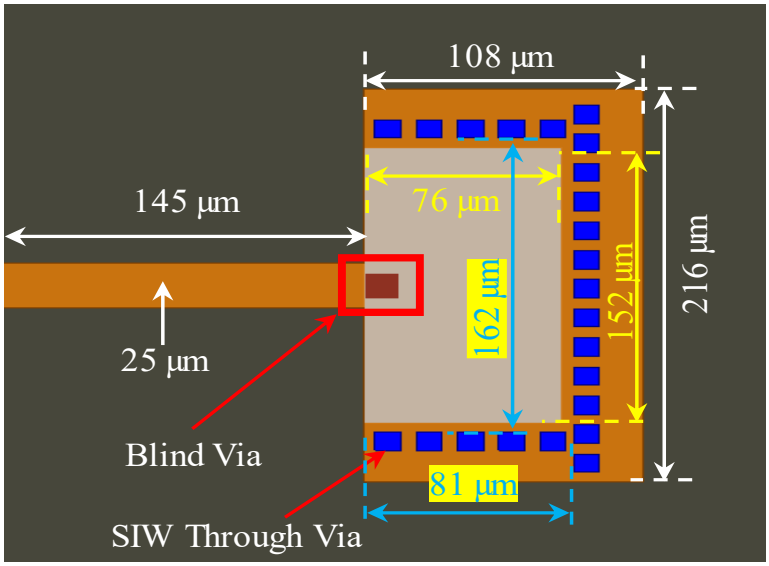
Fig. 4. 48: Resonance frequency and reflection coefficient magnitude with varying via size and spacing for200 GHz folded ridge HMSIW resonators. (a) 30 µm, (b) 50 µm, and (c) 100 µm.

The dimensions of the vias and their spacing play a crucial role in the resonance and reflection coefficient of on-chip substrate integrated waveguide (SIW) design, especially at very high

frequencies. This is due to the significant variation in the total effective inductance caused by the via wall in on-chip designs compared to their counterparts on printed circuit boards (PCBs). The effect of different vias size and vias spacing for folded ridge HMSIW cavity resonator in Fig. 4.46 are presented in the Fig. 4.48. It was found that the most suitable VIA dimensions are 10 µm for via size and 24 µm for via spacing for this specific design.



(a) (b)



(c)

Fig. 4. 49: Folded ridge HMSIW resonator EM model. (a) 3D view. (b) Electric field distribution. (c) Top View.

4.7.1.2 Proposed HMSIW with folded ridge

A 3D model of folded ridge HMSIW resonator is presented in Fig. 4.49(a). Similarly, the electric field distribution of the HMSIW cavity with folded ridge is shown in Fig.49(b), which shows still TE_{10} is the dominant mode. The dimension for the resonance frequency of the SIW resonators with folded ridge are estimated from [53] – [56]. The resonance frequency can be varied by varying the width, height, and position of the blind via position. The variation of the resonance frequency and the return loss at the point of resonance with varying the width of the folded ridge is shown in Fig. 4.50. Maximum miniaturization is achieved by making the larger size of the folded ridge structure. This is because of added capacitance that appeared from the closeness of the ridge structure with the via walls [55].

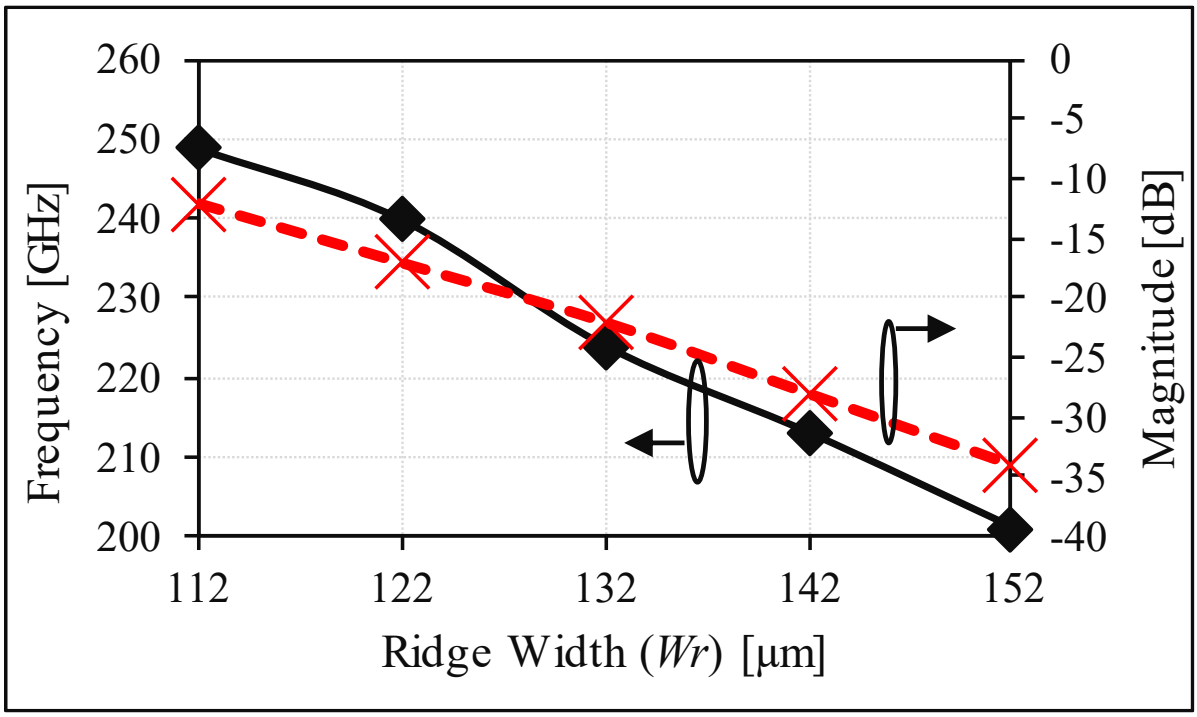


Fig. 4. 50: Sub-THz band folded ridge HMSIW frequency and $|S_{11}|$ magnitude vs. varying ridge width.

4.7.1.3Proposed HMSIW with folded ridge and CSRR Implementation

After loading the HMSIW structure with folded ridge, the size of folded ridge HMSIW is only 14.72 % of the standard HMSIW. There is still room for miniaturization by loadings like slots, CSRR structures, defected ground structures, etc. Microwave designs is subjected to such

loadings, it experiences additional losses specially in high frequency, leading to increased radiation from the structures. External matching should be employed to minimize transition losses. Here rectangular CSRRs are loaded in Fig. 4.51(a), to achieve internal matching. The rectangular CSRR are selected to fit with the smaller available size in the miniaturized HMSIW with folded ridge structure. The simplified equivalent circuit of CSRR loading HMSIW with folded ridge is shown in Fig. 4.51(b) [74].

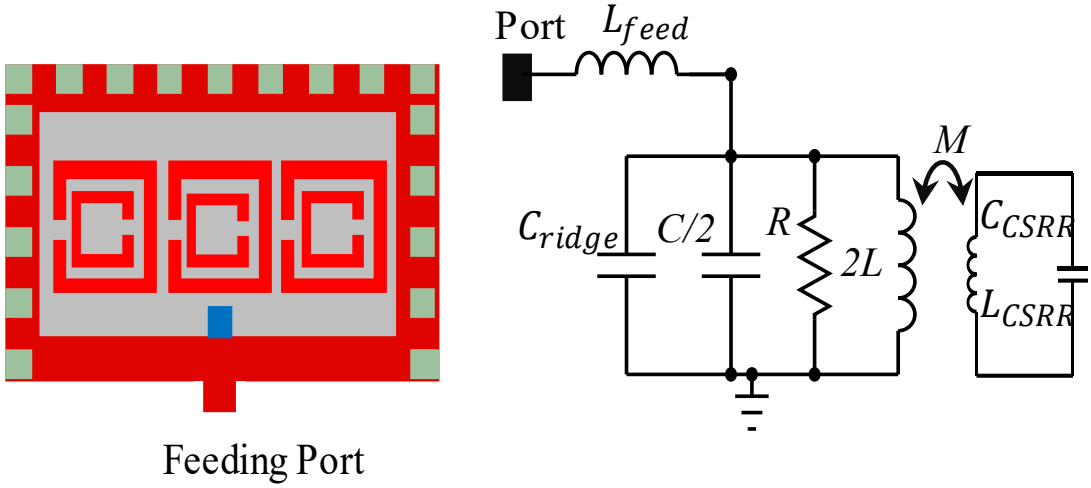


Fig. 4. 51: HMSIW with folded ridge and CSRR structures. (a) Model. (b) Equivalent circuit.

Besides internal matching, the CSRR loading results in the miniaturized resonator realization i.e., resonance frequency lowers. Since the target resonance frequency of the proposed resonator is 200 GHz, the dimensions of the folded ridge CSRR-loaded HMSIW resonator are adjusted to bring back to the desired resonance. Upon changing the CSRR, $Z_{CSRR + folded\_ridge}$ can be altered, thus removing the external matching elements, as shown in Fig. 4.52. Besides this impedance matching, the CSRR loading results in the miniaturized resonator realization.

In Fig. 4.53 (a), a 3D EM model of the folded ridge HMSIW resonator with CSRR loading is presented. The optimized design dimensions of this design are presented in Fig. 4.53(c) and 4.52(d). Fig. 4.53(b) shows the electric field distribution of folded ridge HMSIW resonator with CSRR loading. As shown in the electric field distribution, TE_{10} is the dominant mode.

To confirm this structure is not radiating, the total radiation efficiency was calculated as shown in Fig. 4.54. The total radiation efficiency is computed from antenna structure simulation as:

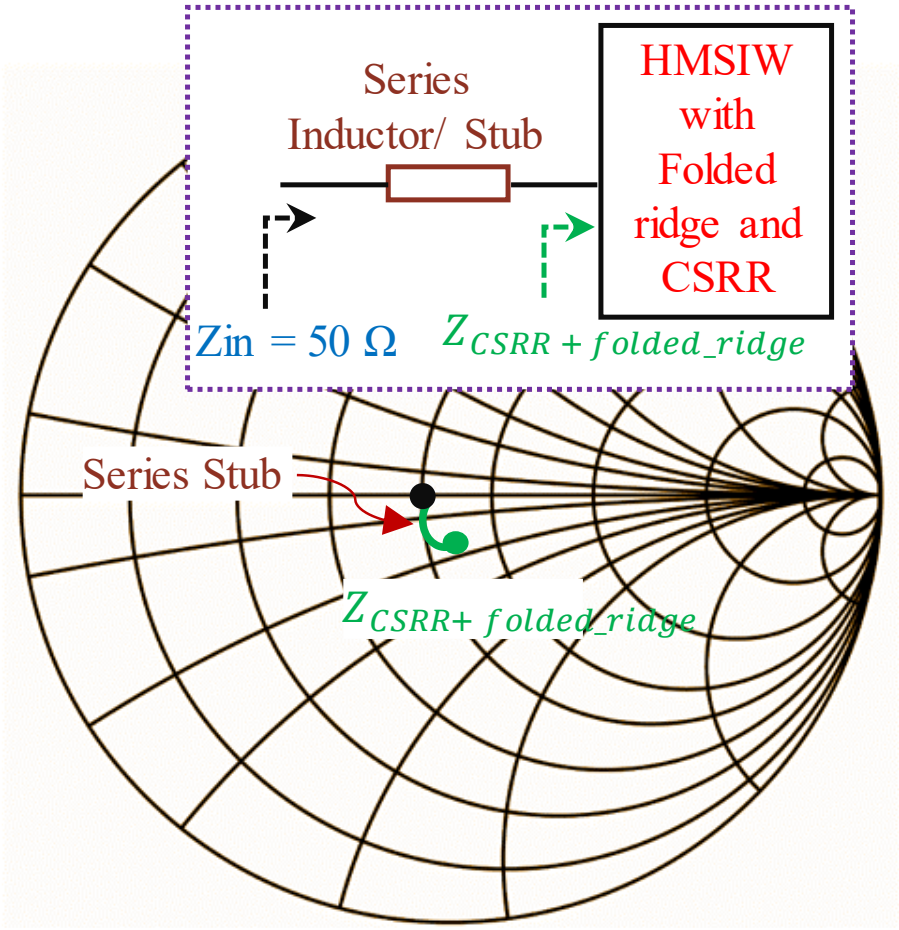


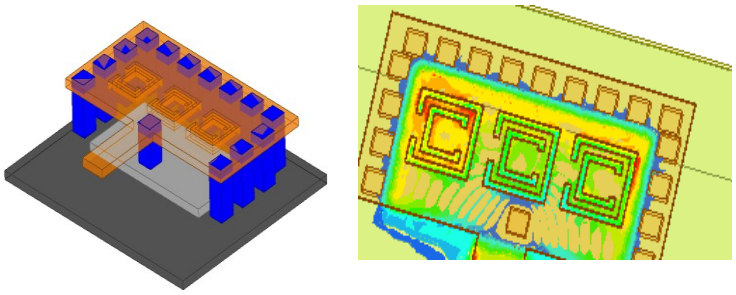
Fig. 4. 52: Matching steps for HMSIW resonator with folded ridge structure with CSRR loadings in Fig. 4.51(a) to 50 Ω input impedance using small series stub. $Z_{CSRR + folded\_ridge}$ *can be adjusted by adjusting CSRRs.*

$$R_{eff.} = \frac{P_r}{P_a + P_r} \tag{4.20}$$

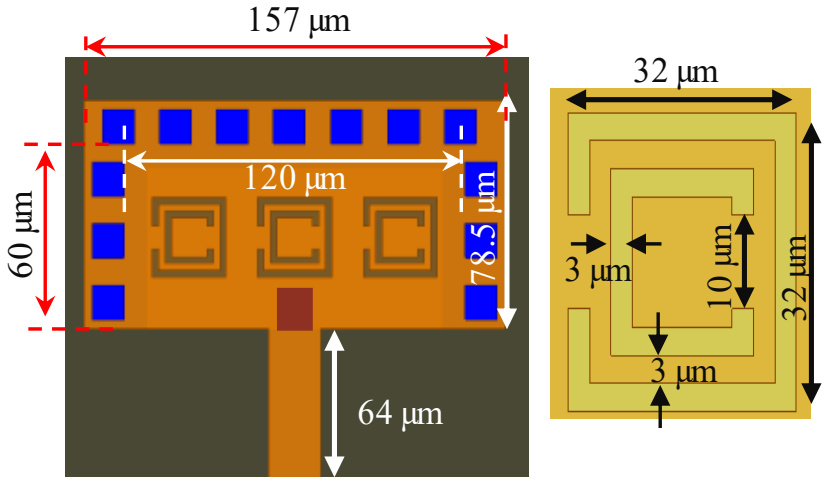
$$M_{eff.} = \frac{P_a + P_r}{P_{re} + P_a + P_r} \tag{4.21}$$

$$Total\ Efficiency = R_{eff.} \times M_{eff.} \tag{4.22}$$

where P_r is radiated power, P_a is absorved power, P_{re} is reflected power, $R_{eff.}$ is radiation efficiency, and $M_{eff.}$ is mismatch efficiency. The total radiation efficiency value is too low, confirming that the structure is not radiating.



(a) (b)



(c)

Fig. 4. 53: Folded ridge HMSIW resonator EM model. (a) 3D view. (b) Electric field distribution. (c) Top View. (d) Rectangular CSRR dimension.

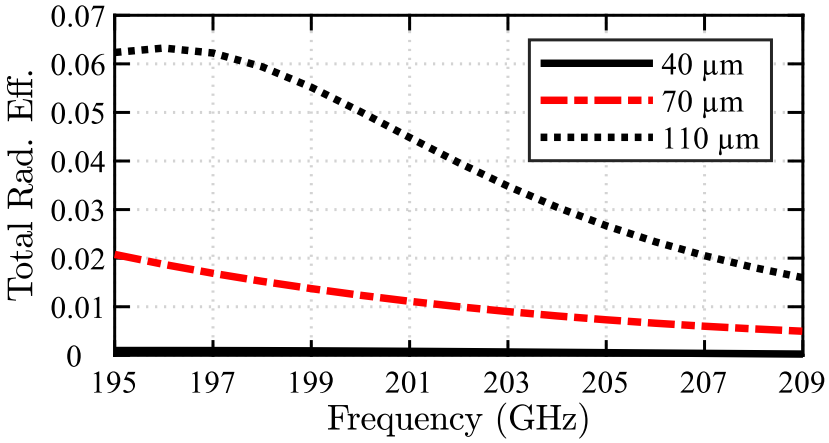


Fig. 4. 54: Radiation efficiency calculation of the HMSIW resonator with folded ridge and CSRR loading.

In the sub-THz design, proper feeding transition for SIW structure is essential for low loss design. Any circuits can easily radiate in very high frequencies, if there is impedance mismatch occurs. We examined two types of feeding structure. One is simple microstrip feeding with some slots. Another is blind feeding as in [76]. The blind via feeding introduces more loss in this design So, microstrip feeding is utilized in this design. Besides, the position of the microstrip line is varied around the cavity resonator. A good matching is achieved when feeding is provided in the center of the opening side of the HMSIW cavity. Also, the blind via position in the ridge SIW structure changes the frequency. Blind via is placed in various locations inside the cavity. The better return loss is achieved with via position is fixed at $\pm$5µm from the centre of the feed line. The simulated reflection coefficient ($|S_{11}|$) after optimization is presented in Fig. 4.55. At the resonance of 201 GHz, the magnitude of $|S_{11}|$ is less than -28 dB from all three designs of cavity resonators.

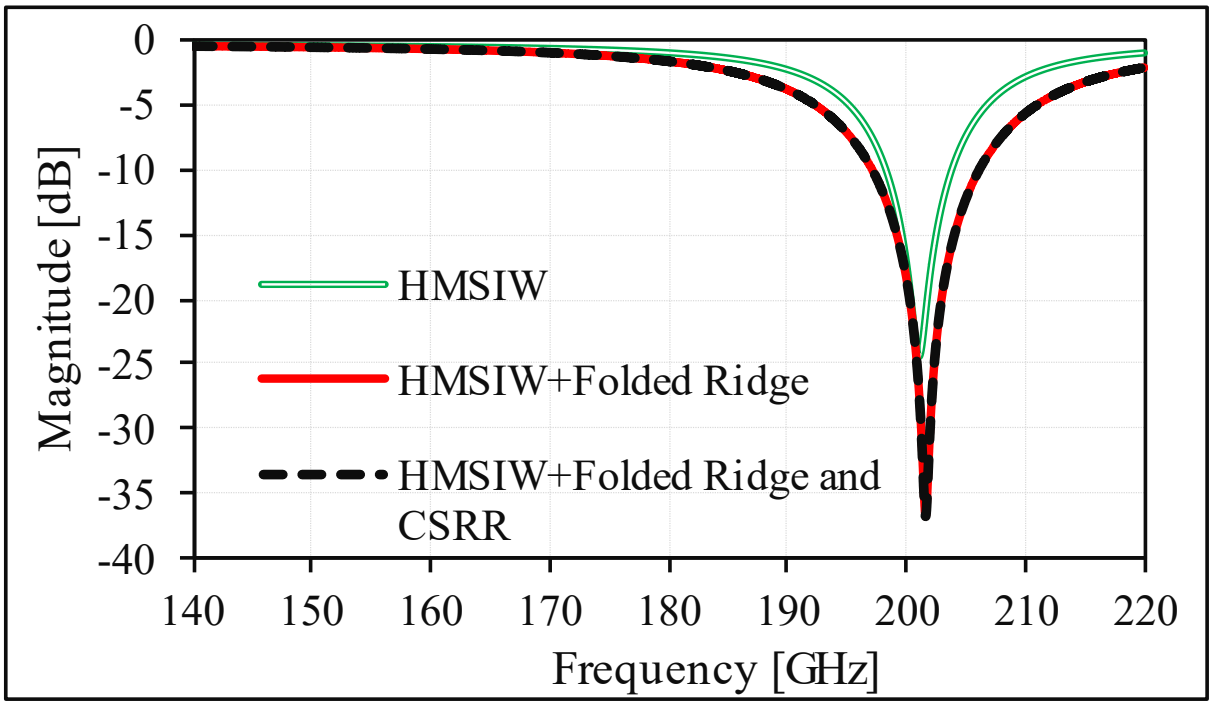


Fig. 4. 55: Reflection coefficient results of the SIW resonators that all design at the 200 GHz.

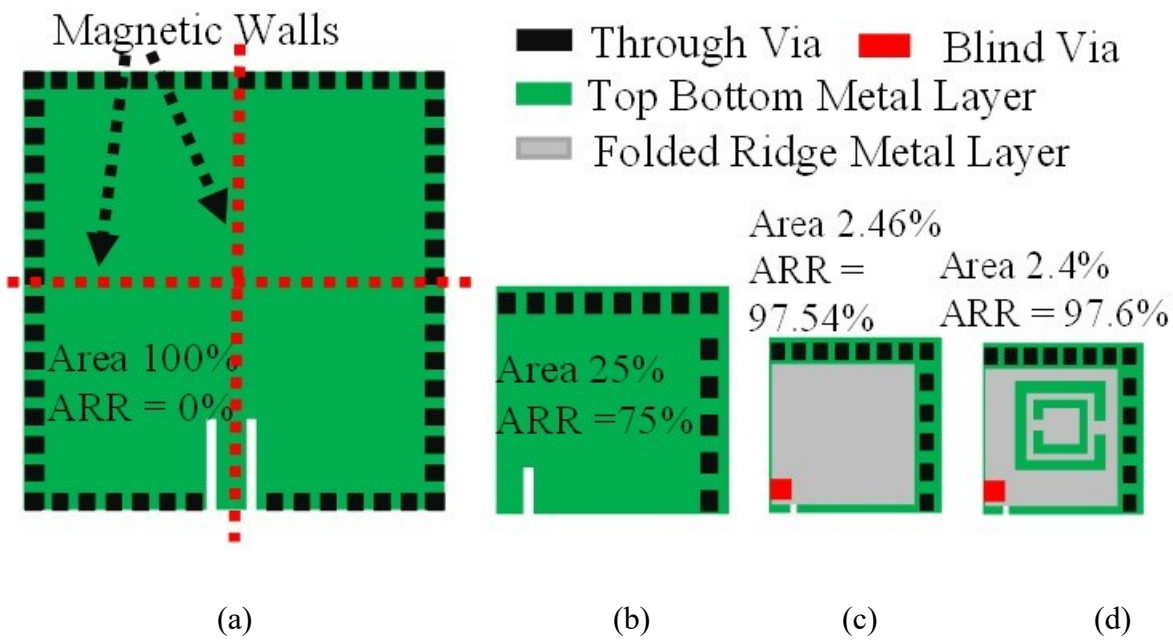


*Fig. 4. 56: SIW resonators: (a) standard; (b) Quarter mode; (c) Quarter mode with folded ridge; (d) Quarter mode with folded ridge and CSRR loadings. *ARR = Area Reduction Ratio compared to standard SIW at the same resonance.*

4.7.1.4Proposed QMSIW with folded ridge and CSRR Implementation

The design of the QMSIW cavity is achieved by dividing a standard SIW cavity into quarters using two symmetric cuts, as depicted in Fig. 4.56(a). This division results in a 75% area reduction compared to the original SIW resonators. However, this modification introduces sideways openings, leading to different losses that impact the return loss and degrade the quality factor. Nevertheless, by incorporating the folded ridge structure in the QMSIW design and loading it with CSRR, improvements in S-parameters can be achieved.

Fig. 4.57 shows the simulated results of the S-parameters for the structures depicted in Fig. 4.56(b), (c), and (d). All the designs have been optimized to resonate at 204 GHz. As a consequence of adding capacitance from the folded ridge and loading from the CSRR, the folded ridge CSRR loaded QMSIW resonator exhibits better return loss compared to the regular QMSIW design. Fig. 4.58 shows that for bigger vias sizes there will be higher radiation which totally agrees with our proposed guidelines.

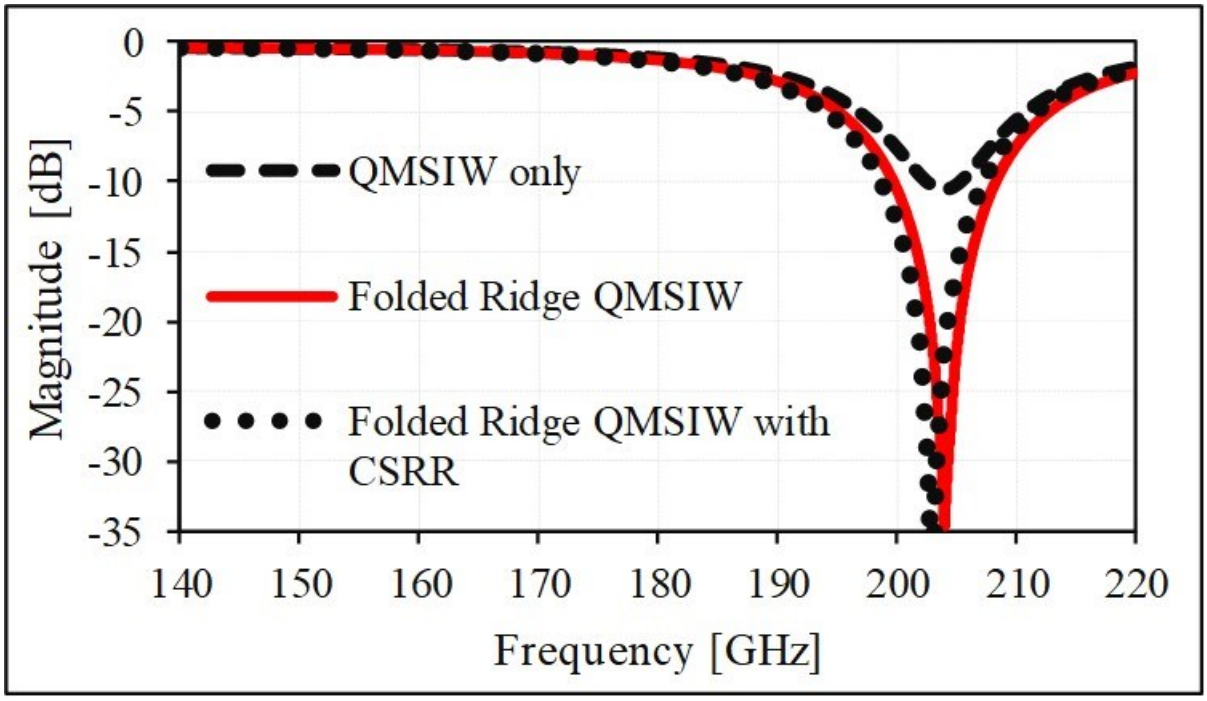


Fig. 4. 57: Reflection coefficient results of the SIW resonators that all design at the 200 GHz.

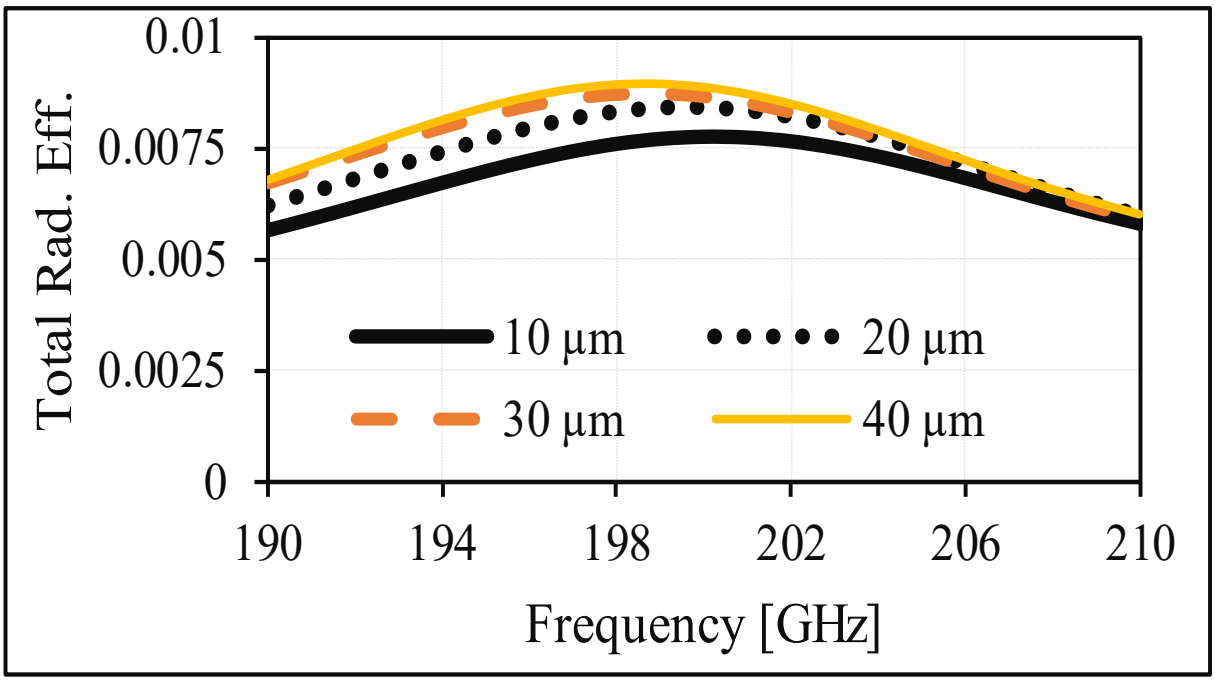


Fig. 4. 58: Total radiation efficiency calculation for QMSIW resonator with folded ridge and loading for varying spacing of vias.

The 3D EM model of the folded ridge QMSIW and folded ridge QMSIW with CSRR loadings are shown in Fig. 4.59 and 4.60. The optimal dimensions of the designs are embedded within the designs. The intrinsic area of these two structures are less than 100 µm compared to 536 µm for standard SIW cavity for same resonance frequency.

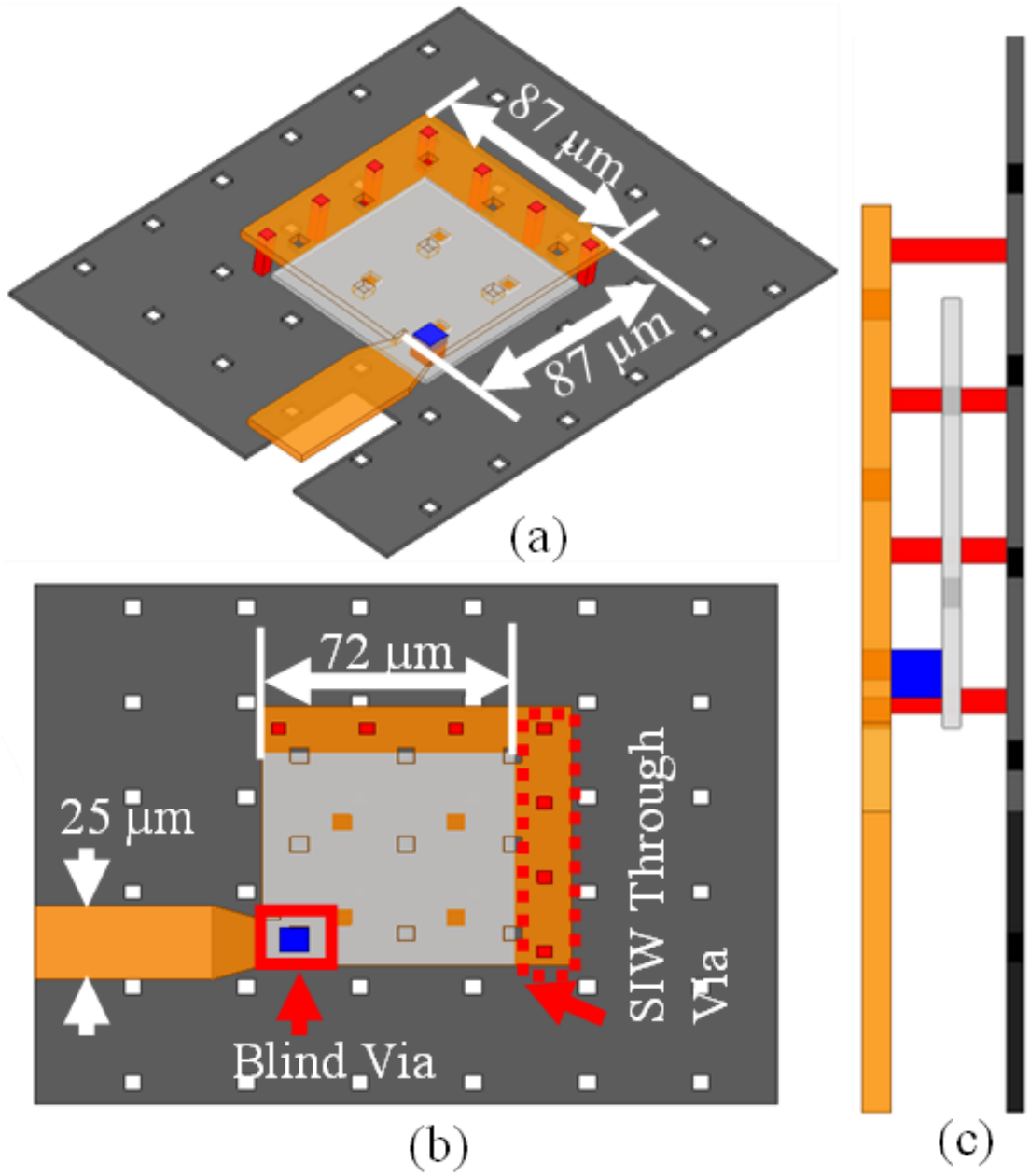


Fig. 4. 59: Proposed 200 GHz band folded ridge QMSIW resonators EM model. (a) 3D view; (b) top view; (c) side view.

4.8 Fabrication and Measurements

All the proposed miniaturized sub-THz band SIW resonators are fabricated using 1P6M CMOS technology, which features six metal layers. The top and bottom planes are constructed using metal layers M6 and M1, respectively, while the ridge is formed in metal layer M3. To establish connections, a blind via (M3 to M6 via) is utilized to link the ridge with the top metal, and an SIW via (M1 to M6 via) connects the top and bottom planes of the resonator. Additionally, slots are etched in the top, ridge, and bottom metals to comply with the wide metal rule of the foundry. To perform all the necessary simulations and optimizations, the ANSYS High-Frequency Structure Simulator (HFSS v2018.01) was used.

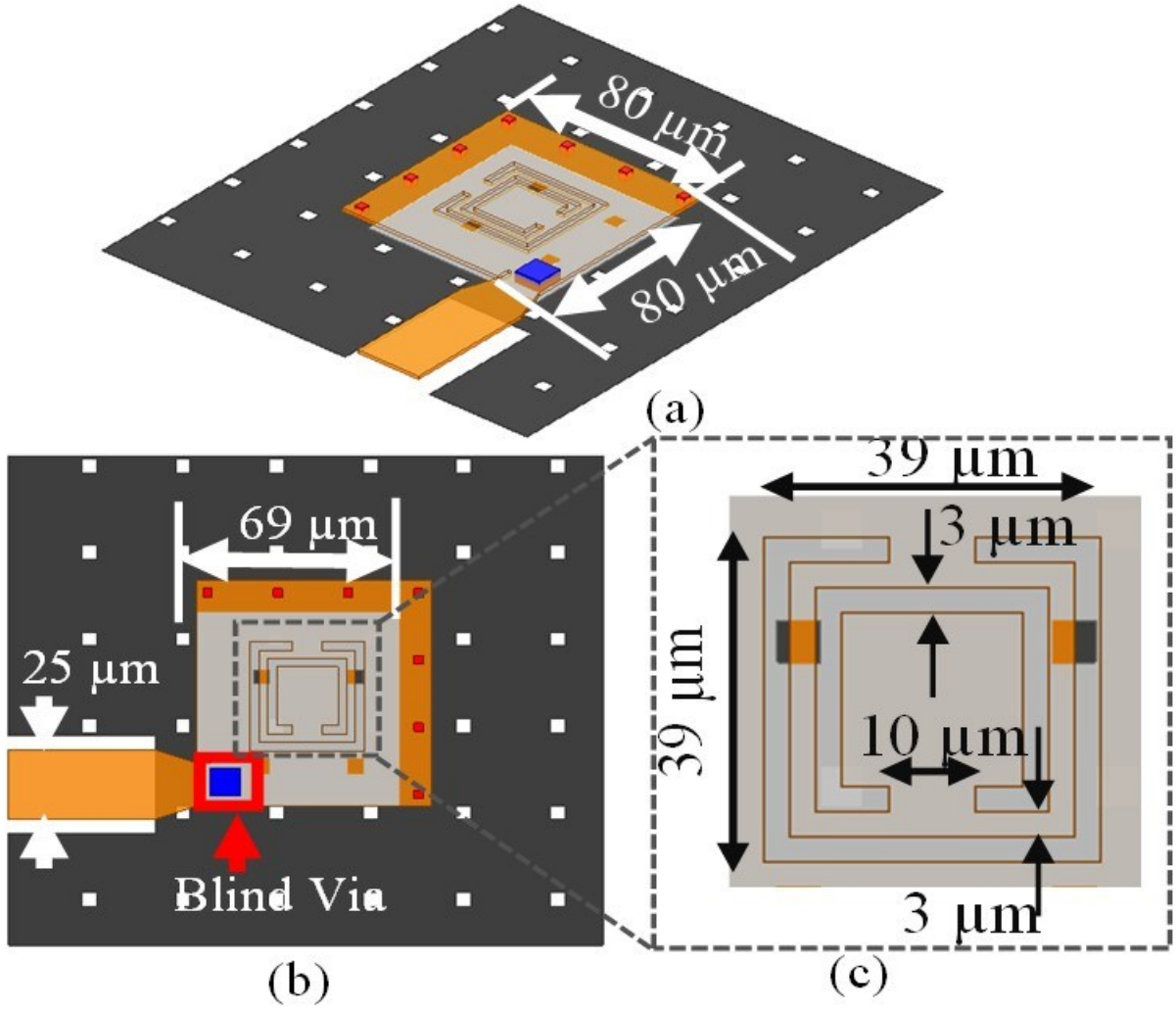


Fig. 4. 60: Proposed 200 GHz band folded ridge QMSIW resonators with CSRR loadings EM model. (a) 3D view; (b) top view; (c) loaded CSRR dimensions.

4.8.1 Fabricated Prototypes

The fabricated chips micrographs are presented in Fig. 4.61 (a)-(f). The micrograph of the folded ridge QMSIW in Fig. 4.61 (f) is just 2.22 % of the standard SIW resonator Fig. 4.61(a), while still maintaining the performance. Therefore, this works demonstrates the extreme miniaturization of the sub-THz band SIW resonators. Similarly, the m-TRL de-embedding structures for these resonators are shown in Fig. 4.62.

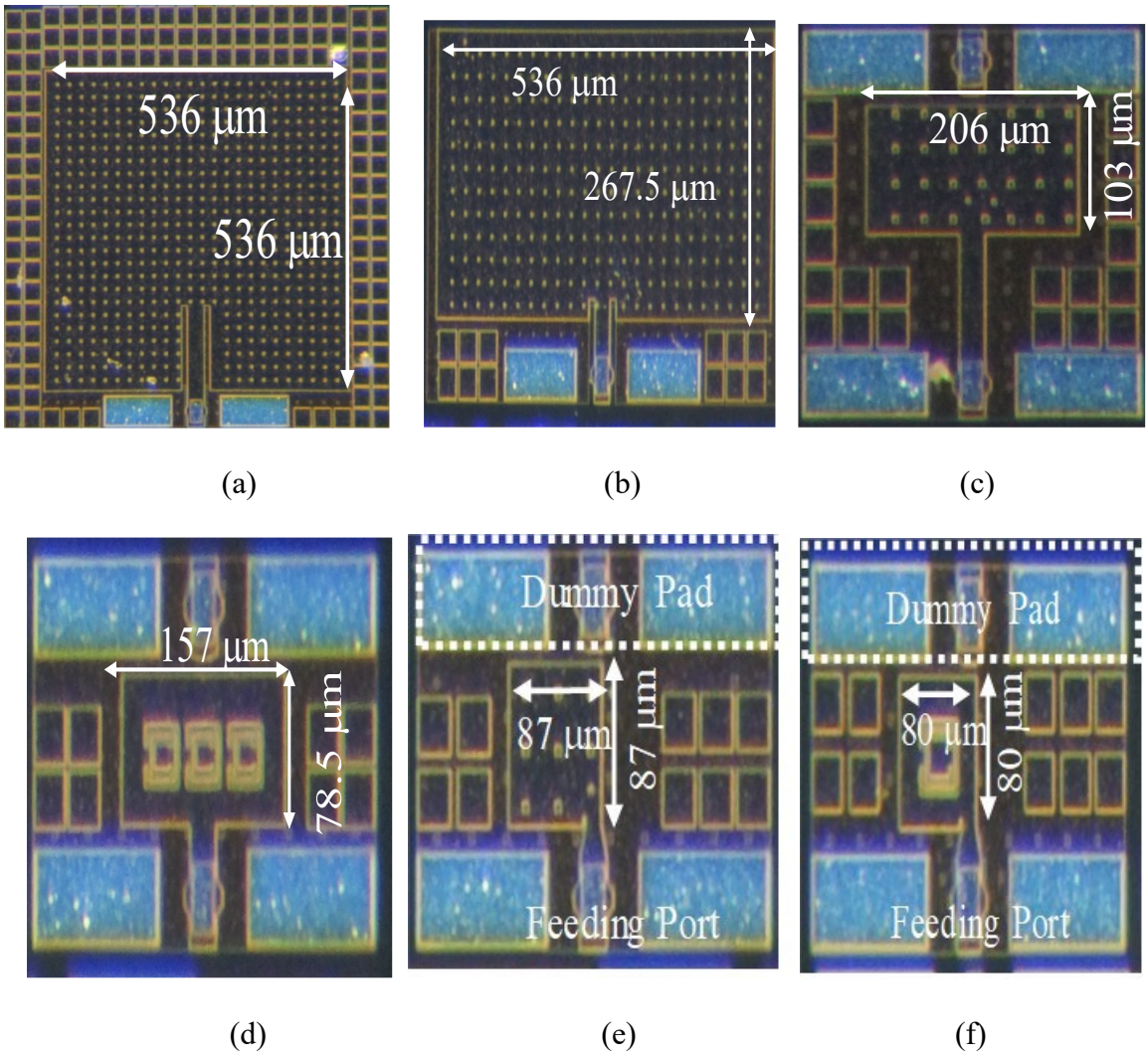


Fig. 4. 61: Micrograph of the fabricated sub-THz band SIW resonators. (a) Standard mode. (b) HMSIW mode. (c) HMSIW with Folded ridge. (d) HMSIW with Folded ridge and CSRR loadings. (e) QMSIW with Folded ridge. (f) QMSIW with Folded ridge and CSRR loadings.

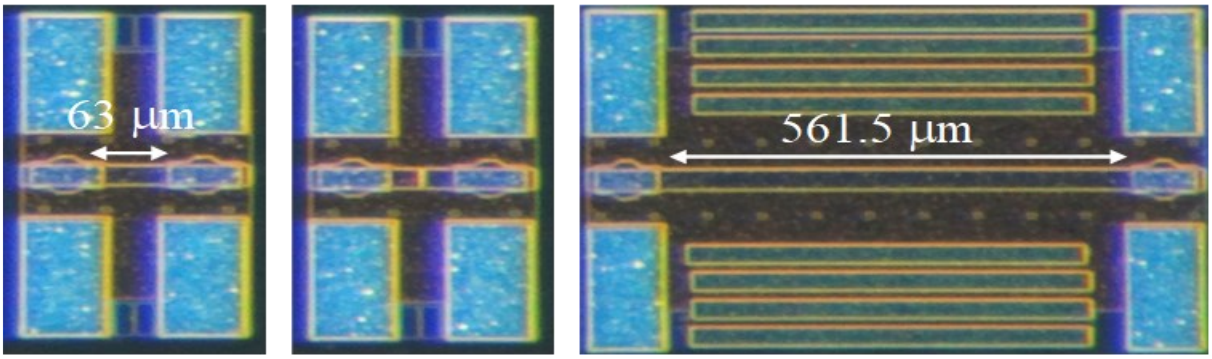


Fig. 4. 62: m-TRL structures used for de-embedding SIW resonators in Fig. 4.61.

To perform the m-TRL de-embedding each resonator in Fig. 4.61 are fabricated along with the additional dummy port that are placed in the opposite side of feeding structure. This also advantages for the chip stabilization during the measurement of the one port cavity.

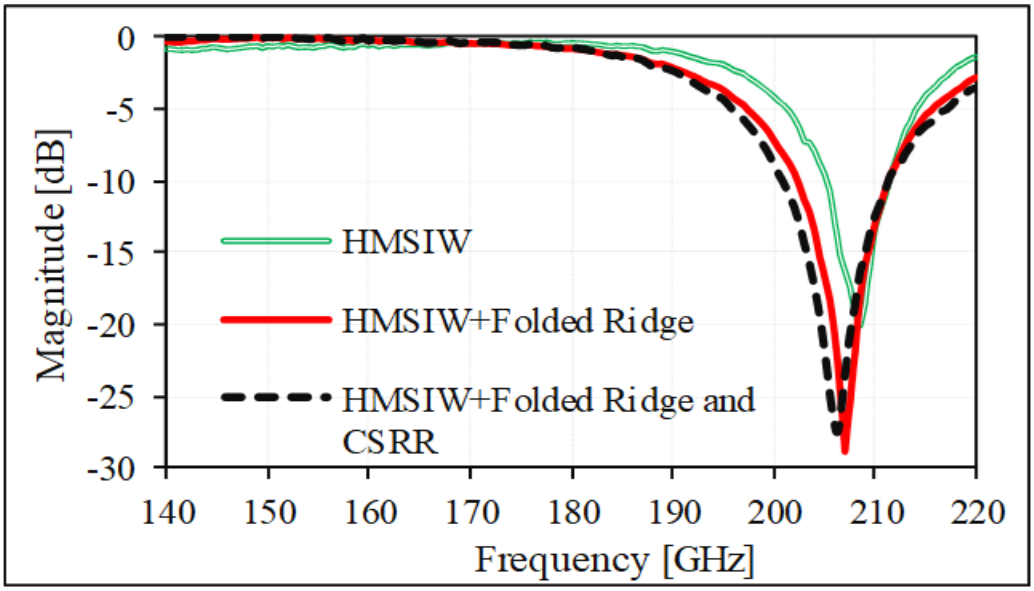
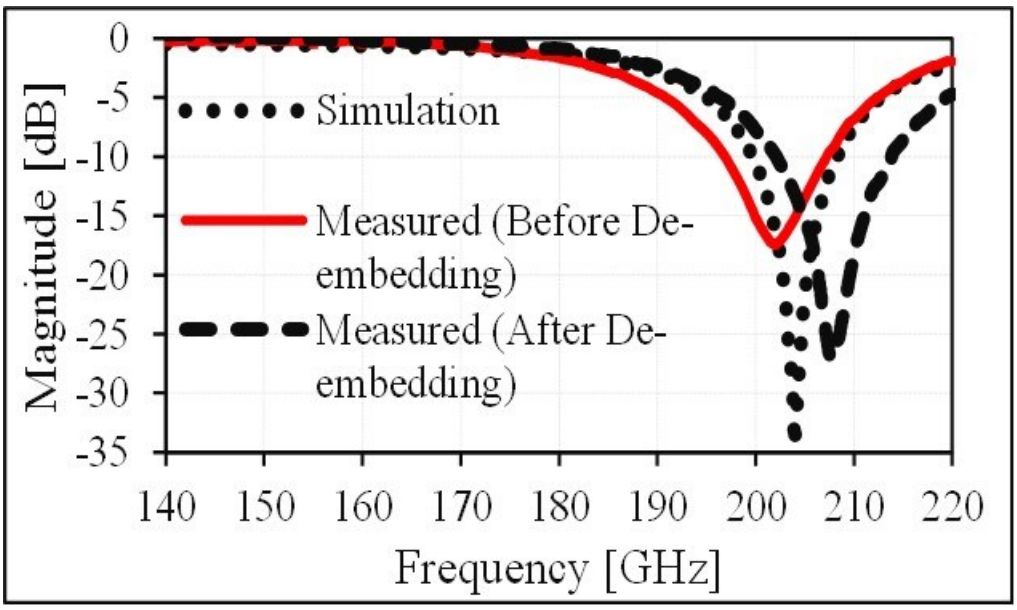


Fig. 4. 63: Reflection coefficient measurement of the fabricated chips in Fig. 4.61(b), (c) and (d).

4.8.2 Simulation and Measurement Results

Fig. 4.63 and Fig. 4.64 shows the measured $|S_{11}|$ parameter results with the simulated. Measurement results are first de-embedded using m-TRL de-embedding structures and

presented. After de-embedding, measurements results are almost like the simulation. Throughout the range of the measurement results both the simulated and the measurement results are accurately aligned.



(a)

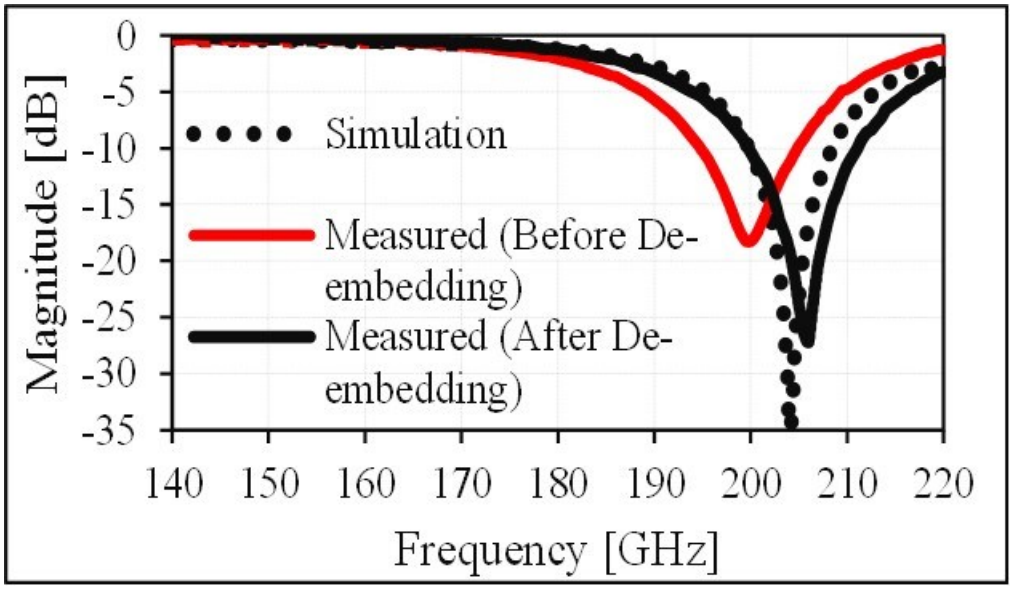


Fig. 4. 64: Measurement $|S_{11}|$ of the proposed 200 GHz band QMSIW with folded ridge resonators: (a) without CSRR in Fig. 4.61(e); (b) with CSRR loading in Fig. 4.61(f).

But in all the outcomes indicate a slight deviation in the measured frequency, which can be primarily ascribed to fabrication tolerances. These tolerances include variations in the effective active area of the fabricated prototypes and the effects of dummy metals fillings and vias that cannot be entirely accounted for in the simulation. However, the resonance shift is only less than 3% which is quite acceptable in high frequency measurements as the measurement set-up environment also greatly affects the performance in such high frequencies. Considering all these effects, all the measurement results after de-embedding are almost perfectly traced throughout the measurement range of 140 GHz to 220 GHz band.

4.8.3 Performance Comparison

For the fabricated resonator's performance comparison, SIW size and the quality factors are considered. Table 4.4 shows the comparison of the proposed resonators with the state-of-the-art, which shows that the proposed cavity resonator presented higher Q_l and compact size.

Table 4. 4: Performance comparison

Ref.	**Standard Mode**	**HM-SIW**	**HMSIW with folded ridge**	**Folded Ridge HMSIW with CSRR Loading**	**QMSIW with folded ridge**	**Folded Ridge QMSIW with CSRR Loading**
Frequency [GHz]	209	208	207	206.1	207.2	206.3
$\|S_{11}\|$ dB	-19	-20.2	-28.8	-27.2	-27.2	-28.9
Meas. *Qe*	142	148	258	189	207	158
Active Area (mm^2)	0.287296	0.1434	0.021218	0.0123245	0.00757	0.0064
Size Reduction Ratio compared with standard SIW	0 %	50 %	92.61 %	95.71 %	97.36%	97.77%

4.9 Summary

In this chapter, we present the very first implementation of SIW interconnects and resonators in the sub-THz band using commercial CMOS technology. We also discuss the design

challenges associated with on-chip SIW designs for frequencies above 100 GHz. To address these challenges, we propose a novel set of design equations specifically tailored for on-chip SIW designs above 100 GHz band, which we validate through various simulations. Also, we perform the first-ever loss analysis of on-chip SIW structures operating above 100 GHz. The results reveal that the major contribution to loss at such high frequencies is due to dielectric and conductor losses. To accurately measure these high-frequency structures, de-embedding becomes crucial. Hence, we briefly discuss sub-THz band de-embedding of the proposed structures, and we provide a few de-embedding examples and results.

Furthermore, we design sub-THz band SIW resonators and interconnects based on the proposed region of interest. These structures demonstrate excellent measurement results with high Q values and good return losses. In conclusion, such on-chip low loss sub-THz band SIW based structures are good candidates for the future high frequency applications like filters, interconnects, antennas, coupler, sensors, etc. design for applications ranging from wireless communication to the medical imaging.

Chapter 5: Conclusion and Future Prospect

The thesis has outlined the on-chip design of the passive circuits like filters, resonators, transmission lines ranging from millimeter wave to the sub-terahertz band applications meeting the stringent requirements of low-loss, high Q designs for such applications. All these works carried in this thesis have been implemented in 0.18 μm CMOS technology and meet the requirements of the size as well as low loss in the working frequencies 52 GHz, 60 GHz, and 200 GHz which are the potential frequency ranges for millimeter wave 5G applications and beyond 5G applications.

5.1 Conclusion

The main contributions in this thesis are summarized as follows:

- Two transmission poles DGS-based band-stop filters for the millimeter wave band are proposed and validated. These filters are designed with a T-shaped capacitively loaded resonator embedded within the original DGS, that results in two high-Q factor smaller loop resonators. The TPs position in the proposed DGS-based BSF can be independently controlled by changing this structure with the feedline structure and capacitor in series with this feedline. Interestingly, the active area remains the same while achieving a sharp S- parameter response. As a consequence, the loaded Q-factor is significantly enhanced making them highly suitable for oscillator and filter designs.
- On-chip SIW cavity resonators for the millimeter wave band at 60 GHz resonance frequency are designed and fabricated. One of the major issues for implementing SIW-based cavities in CMOS technology, is the bulky size. To address these challenges, sub-modes SIW structure (Sixteenth mode SIW) with folded ridge structures inside the proposed cavities are utilized, resulting in a significant reduction in size. Additionally, Complementary Split Ring Resonators (CSRRs) are incorporated into the design to achieve internal matching within the SIW cavities, eliminating the need for external matching circuits. The designed ultraminiaturized cavities have a compact size and are less than 1% the area of the standard SIW resonators designed at the same resonance frequency while still maintaining the high Q-factor.
- Prior to this research, there were few sub-THz band SIW designs. None of these works have clearly presented the design aspects of sub-THz band SIW in their work. Also, the

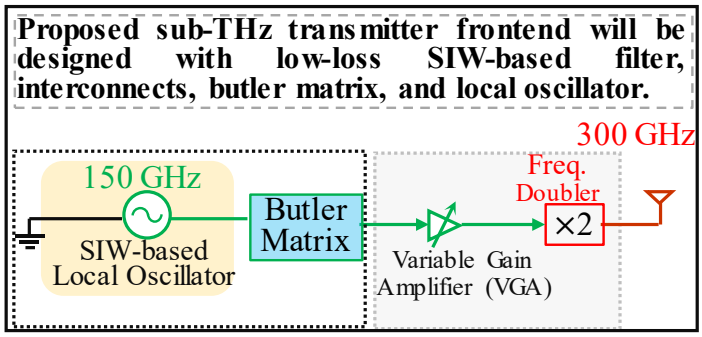
SIW structures proposed in the literature have design equations that are valid for PCB CMOS technology in low-frequency bands. However, these design equations need to be redefined for frequencies above the millimeter wave range. For the first time, in this work, a new set of design equations for SIW in sub-terahertz designs is first proposed and verified through simulation. Sub-THz band HMSIW interconnect with low attenuation loss is verified with the experiment as well.

- Various sub-THz band designs of compact and miniaturized SIW cavities, ranging from standard to sub-modes, are then fabricated using half mode and quarter mode designs based on the updated equations. Six prototypes of sub-terahertz band SIW cavity resonators are fabricated: standard SIW, half mode SIW, half mode with folded ridge SIW, half mode with folded ridge and CSRR loading, quarter mode with folded ridge, and quarter mode with folded ridge and CSRR loadings. All of these designs exhibit lower return loss, high Q-factor, and small chip area overhead. The measurement results are obtained by performing multi-line thru-reflect-line (m-TRL) de-embedding to remove the effect of the pads in such high-frequency designs. Additionally, using the same design equations, a 200 GHz band half mode SIW transmission line is designed and fabricated. The simulation results of this design demonstrate a promising insertion loss of 1.1 dB in the frequency band ranging from 150 GHz to 280 GHz, making it suitable for various sub-terahertz band applications.

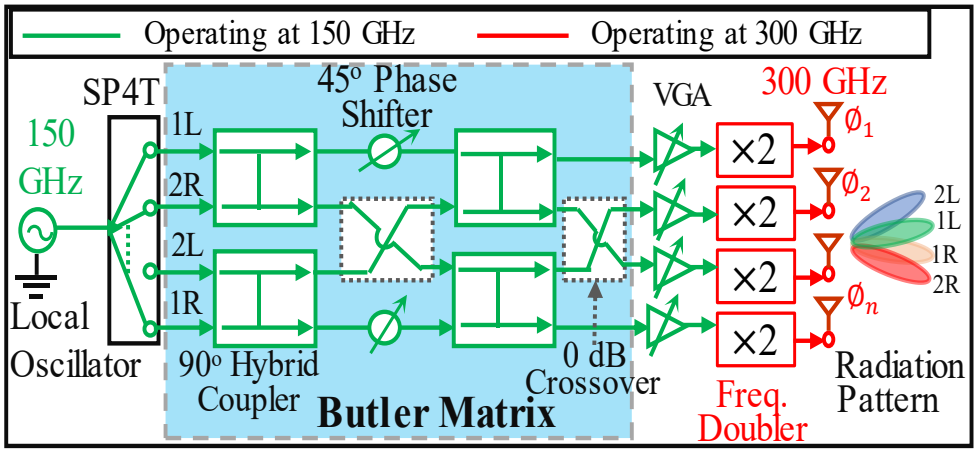
5.2 Future Prospects

The future prospects of this thesis outcomes can be pointed as:

- DGS resonators provide all way freedom to be optimized for the different range of filter applications. To improve the filter performance further for millimeter wave filtering applications, higher order modes of the filter can be implemented. This will be more applicable for the VCOs design with low phase noise for millimeter wave applications.
- SIW result presented in this thesis if the very early result of on-chip SIW realization in millimeter and sub terahertz bands. In the used technology, we are getting higher dielectric loss. I want to employ the findings of this thesis to design high performance SIW-based designs in more optimized process like GaN or 45 nm SOI to get full advantage of this design.
-



(a)



(b)

Fig. 5. 1: Proof-of-concept of the sub-THz band SIW Bulter matriz-based beamforming IC. (b) Working of proposed sub-THz band beamforming IW with SIW-based oscillator and 4 x 4 bulter matrix.

- Beamforming technology is indispensable to achieve high-data-rate and low-latency capabilities for future sub-terahertz (sub-THz) wireless systems. Many conventional beamforming integrated circuits (ICs) were designed directly for sub-THz frequencies using upconversion mixers and power amplifiers (PAs). However, at frequencies like 300 GHz, PAs or RF frontends can't produce sufficient gain due to limitations such as transistor's unity-power-gain frequency (f_{max}), significant parasitic effects, and high losses in semiconductor fabrication. PA-less beamforming IC was reported using harmonic mixer, requires further improvements for output power and spurious frequencies. To address these issues, I am considering 300 GHz band beamforming IC using Butler matrix and frequency multiplier (see Fig. 5.1). This advantage low-loss system design as: ❶ high gain on-chip PA is feasible at 150 GHz and ❷ system operation near f_{max} is limited to the last stage after frequency multiplier only, reducing

overall losses. Also, butler matrix provides benefits beyond energy efficiency, including compact design, precise beam steering, lower signal interference, and adaptability to various frequencies.

- Recent research shows the 100 GHz to 300 GHz band could be a possible solution for the future medical imaging technology to detect cancers and object detections for security things [76]-[77]. I am planning to implement the 200 GHz band SIW designs to early-stage cancer detection application as shown in Fig. 5.2, where SIW acts as sensor to measure the relative change in the dielectric permittivity which is read to imaging by contour plot for tumor region detection.

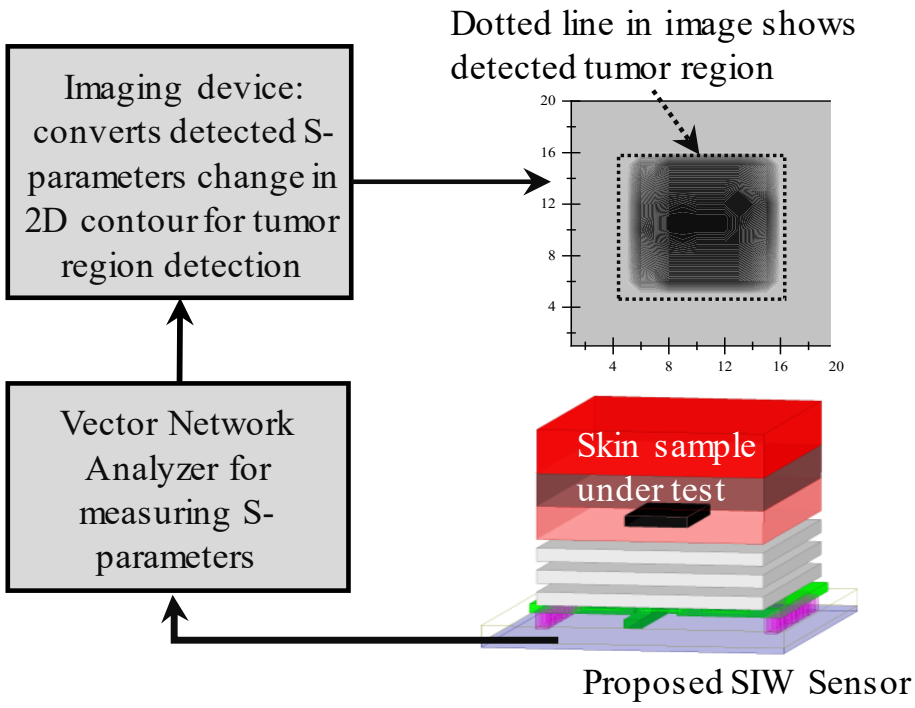


Fig. 5. 1: Sub-THz SIW sensor for medical imaging for early-stage cancer detection.

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List of Publications

Journal Publications

[1] **S. K. Thapa**, B. Chen, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "X-Band Feedback Type Miniaturized Oscillator Design with Low Phase Noise Based on Eighth Mode SIW Bandpass Filter," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 5, pp. 485-488, May 2021, doi: https://doi.org/10.1109/LMWC.2021.3064602.

[2] B. Gyawali, **S. K. Thapa**, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Analysis and design of diode physical limit bandwidth efficient rectification circuit for maximum flat efficiency, wide impedance, and efficiency bandwidths", *Nature Scientific Reports* 11, 19941 (2021), doi: https://doi.org/10.1038/s41598-021-99405-7.

[3] B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "A W-band Compact Substrate Integrated Waveguide Bandpass Filter With Defected Ground Structure in CMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 889–893, March 2022, doi: https://doi.org/10.1109/TCSII.2021.3123655.

[4] B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "A W-band 0.01 mm^2 Cavity Resonator Employing Slot-loaded Shielded Folded Ridged Quarter-Mode in CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 2, pp. 113–116, Feb. 2022, doi: https://doi.org/10.1109/LMWC.2021.3122149.

[5] **S. K. Thapa**, R. K. Pokharel, B. Chen, and A. Barakat, "On-chip Millimeter-Wave DGS based Bandstop Filter in 0.18-µm CMOS Process," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 889–893, March 2022, doi: https://doi.org/10.1109/TCSII.2022.3158995.

Conference Publications

[1] **S. K. Thapa**, B. Chen, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Miniaturized Slot-Loaded SIW Resonator and Its Application to C-band Low Phase Noise Oscillator," in *Proc. The 50th European Microwave Conference 2020*, Netherlands, 10-15 January 2021, DOI: https://doi.org/10.23919/EuMC48046.2021.9338129.

[2] T. Fukuda, B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "Design of Compact W-Band Cavity in 0.18-µm CMOS Technology," in *IEICE Technical Report*, vol.121, no.254, MW2021-68, pp. 11-12, Nov. 2021.

[3] B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "A 100GHz Bandpass Filter Employing Shielded Folded Ridged Quarter-Mode SIW Resonator in CMOS Technology," in *Proc. 2021 51st European Microwave Conference (EuMC)*, London, UK, 2022 pp. 853-856. DOI: https://doi.org/10.23919/EuMC50147.2022.9784336

[4] B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "Design Methodology of Wide Tuning Range DGS-based VCO for K-band Applications in 0.18-µm CMOS Technology," in *Proc. 2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, London, UK, 2022 pp. 26-29. DOI: https://doi.org/10.23919/EuMIC50153.2022.9783689

[5] T. Fukuda, B. Chen, **S. K. Thapa**, A. Barakat, and R. K. Pokharel, "Design of Compact and High Q-factor W-Band Cavity in 0.18µm CMOS Technology," in *Proc. 2021 51st European Microwave Conference (EuMC)*, London, UK, 2022 pp. 221-224. DOI: https://doi.org/10.23919/EuMC50147.2022.9784193

[6] B. Gyawali, R. K. Pokharel, **S. K. Thapa**, M. Aboualalaa, A. Barakat, and K. Yoshitomi, "Broadband and Compact 3-Bit Digitally-Controlled Reconfigurable Rectification Circuit," in *Proc. 2022 IEEE Wireless Power Week (WPW 2022),* Bordeaux, France, 2022, pp. 780-783. DOI: https://doi.org/10.1109/WPW54272.2022.9901332

[7] **S. K. Thapa**, R. K. Pokharel, B. Chen, T. Fukuda, and A. Barakat, "Millimeter-Wave High Q-factor Sixteenth Mode SIW Cavity Resonator Implemented in 0.18-µm CMOS Technology," in *Dig. 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, Denver, USA, 2022, pp. 560-563, doi: https://doi.org/10.1109/IMS37962.2022.9865522

[8] **S. K. Thapa**, B. Chen, A. Barakat, and R. K. Pokharel, "A Compact Millimeter-Wave DGS-based Bandstop Filter with Two Transmission Poles in CMOS Technology," in *Proc. 2022 52nd European Microwave Conference (EuMC)*, Milan, Italy, 2022, pp. 564-567, doi: https://doi.org/10.23919/EuMC54642.2022.9924382

[9] **S. K. Thapa**, B. Chen, A. Barakat, and R. K. Pokharel, "Experimental Study on the Effect of Feeding Topology of 60 GHZ Sixteenth Mode SIW Cavity Resonator in CMOS Technology," in *2022 Asia-Pacific Microwave Conference (APMC2022)*, Yokohama, Japan, 2022, pp. 384-386, DOI: https://doi.org/10.23919/APMC55665.2022.9999830

[10]B. Gyawali, **S. K. Thapa**, M. Aboualalaa, A. Barakat, K. Yoshitomi, and R. K. Pokharel, "Design of Self-Impedance Matching Ultra-Wideband Rectification Circuit," in *2022 Asia-Pacific Microwave Conference (APMC2022)*, Yokohama, Japan, 2022, pp. 671-673. DOI: https://doi.org/10.23919/APMC55665.2022.9999810

[11]**S. K. Thapa**, R. K. Pokharel, et al., "Implementation of SIW Cavity in Commercial CMOS Technology for Sub-Terahertz Band Applications," in *2023 IEEE/MTT-S International Microwave Symposium (IMS2023)*, San Diego, CA, USA, pp. 493-496. DOI: https://doi.org/10.1109/IMS37964.2023.10188161

[12]R. K. Pokharel, T. Fukuda, **S. K. Thapa**, et al., "200 GHz-band Low-loss Half-Mode SIW CMOS Interconnects and Transmission Lines for Sub-Terahertz Frequency Band Applications," in *2023 IEEE/MTT-S International Microwave Symposium (IMS2023)*, San Diego, CA, USA, pp. 497-500. DOI: https://doi.org/10.1109/IMS37964.2023.10188034

[13]B. Gyawali, **S. K. Thapa**, M. Aboualalaa, A. Barakat, and R. K. Pokharel, "Frequency Switching Dual Power Band Rectifier with Load-Modulation Technique," in *2023 IEEE Wireless Power Technology Conference and Expo (WPTCE 2023),* San Diego, CA, USA. DOI: https://doi.org/10.1109/WPTCE56855.2023.10216256

[14]**S. K. Thapa**, R. K. Pokharel, et al., "Implementation of Low-Loss Sub-Terahertz Band Substrate Integrated Waveguide-based Interconnects and Cavities in CMOS Technology," in *XXXVth URSI General Assembly and Scientific Symposium (URSI GASS 2023)*, Sapparo, Japan, Aug. 2023. DOI: https://doi.org/10.23919/URSIGASS57860.2023.10265470

Appendix - A

De-embedding

De-embedding is a technique used in electrical engineering and signal processing to separate the effects of unwanted components or structures like measurements pads from the measured response of a device or system. It is commonly employed in high-frequency and microwave engineering to characterize the intrinsic behavior of individual components. The main goal of de-embedding is to eliminate the parasitic effects of interconnects, test fixtures, and other elements in the measurement setup, allowing accurate characterization of the DUT or the system being analyzed.

The de-embedding process involves two main steps: calibration and de-embedding. Calibration is performed using known calibration standards to establish a reference plane, while de-embedding is used to extract the device-under-test characteristics from the measured data. A simplified explanation of the de-embedding process:

1. Calibration:
    - Connect the calibration standards (such as known impedance or transmission line sections) to the measurement system.
    - Measure the response of the calibration standards using appropriate test equipment (such as vector network analyzers). For IC measurements may be done in measurement probe stations.
    - Store the measured calibration data for subsequent calculations.
2. De-embedding:
    - Connect the DUT to the measurement system, along with the same calibration standards used in the calibration step.
    - Measure the combined response of the DUT and the calibration standards.
    - Use the previously measured calibration data to mathematically remove the effects of the calibration standards from the combined response.
    - The resulting data represents the de-embedded response of the DUT alone, eliminating the unwanted effects of the calibration standards.

The de-embedding process involves various mathematical techniques, such as inverse scattering parameters (S-parameters) or de-embedding matrix algorithms, to separate the DUT response from the calibration standards. The equations used for de-embedding depend on the specific technique employed, application frequencies, and the characteristics of the calibration standards and the DUT. These equations are often complex and involve matrix operations. Here in this appendix three different de-embedding methods are discussed:

1. Short-Open-Thru De-embedding
2. L-2L De-embedding
3. m-TRL De-embedding

1. Short-Open-Thru De-embedding

Short-Open-Thru de-embedding is one of the oldest de-embedding methods proposed for GHz band application by T. E. Kolding in 2000 [A.1]. This is very effective calculations for the various RF and microwave components and successfully verified for measuring and extraction components parameters like inductors, filters, amplifiers, etc., working for few GHz frequencies band. The detailed information of short-open-thru de-embedding is explained below:

At first the DUT along with the other fabricated short-open-thru standards are measured in the measurement setup after the device calibration using the measurement standards. Fig. A.1(a) represents the full circuit and the equivalent measurement pads effects in the measurement full circuit. Various pads effects involve the capacitance from pad to ground plane, contact impedance between measurement RF-probes and the measurement pads, transmission impedance of pads, coupling between two measurement pads, coupling impedance between DUT and pads, etc.

Such measurement effects should be removed to extract the intrinsic performance of the DUT as because they have significant effect on the measured results. In GHz band measurement these effects are much higher because size of the pads and other couplings sometimes comes to the dimensions of wavelength. All these measurement effects during measurement are presented in Fig. A.1(b) which will be used for de-embedding in this method.

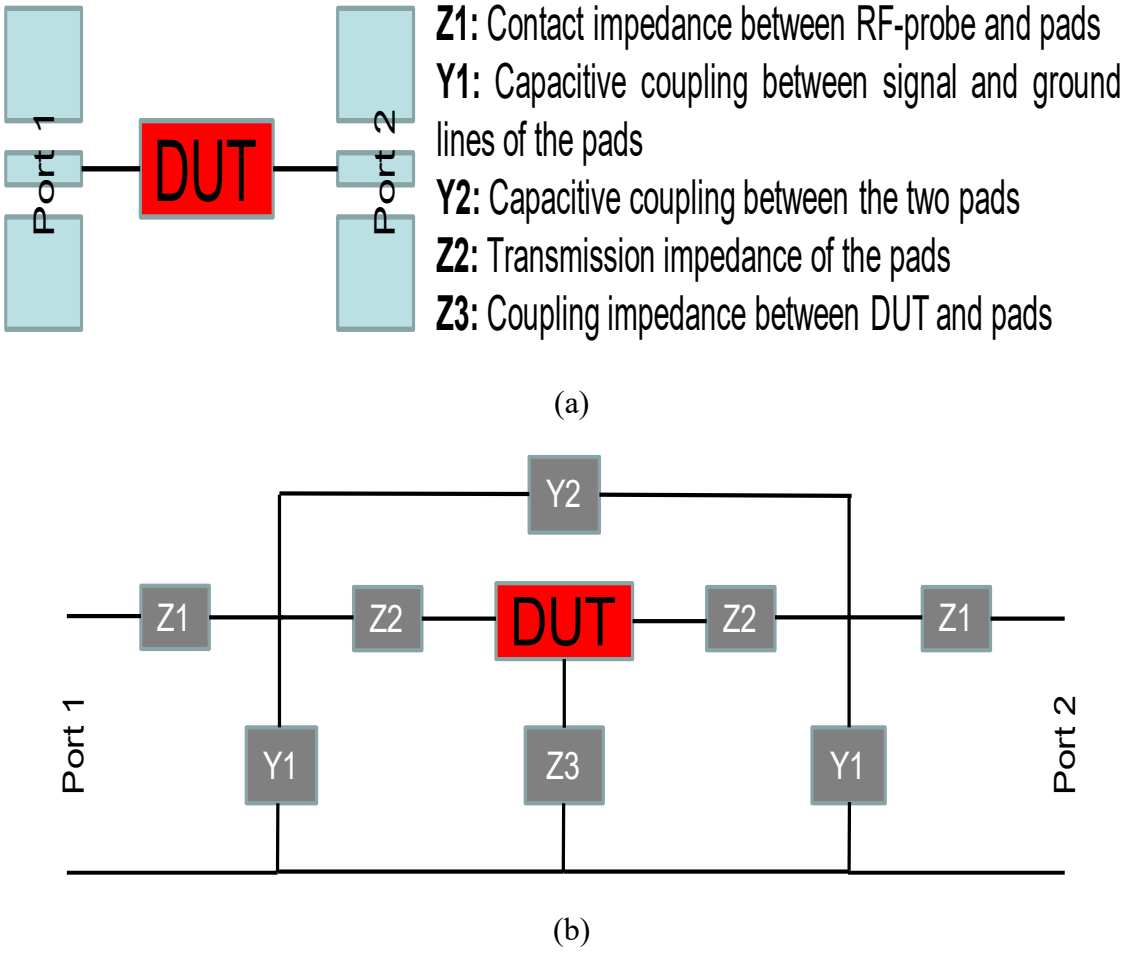

Fig. A. 1: (a) Full circuit measurement overview with DUT and pads. (b) Various coupling component representation of the full measurement circuit.

Some representations used for the short-open-thru de-embedding in this method are:

S_F: represents the S-parameters of the full circuit.

Z_F: represents the Z-parameters of the full circuit.

S_{short}: represents the S-parameters of the short structure.

Z_{short}: represents the Z-parameters of the short structure.

S_{open}: represents the S-parameters of the open structure.

Z_{open}: represents the Z-parameters of the open structure.

Y_{open}: represents the Y-parameters of the open structure.

$S_{through}$: represents the S-parameters of the thru structure.

$Z_{through}$: represents the Z-parameters of the thru structure.

$Y_{through}$: represents the Y-parameters of the thru structure.

Z_{DUT}: represents the Z-parameters of the DUT structure. Later, Z_{DUT} is converted to S_{DUT} for the extraction of the exact DUT parameters. Sometimes in case of inductors, conversion to S-parameters of DUT may not be required.

Step 1: Now, to remove the series effect of Z1, short structures are utilized. First as shown in Fig. A.2(a) and (b). Short structures represent only the contact impedance between measurement pads and RF probes. To subtract this effect at first, both the full circuit and the short structure S-parameters are converted to Z-parameters and then subtracted. Fig. A.2 (c) represents the results of full circuit after de-embedding with short structure only.

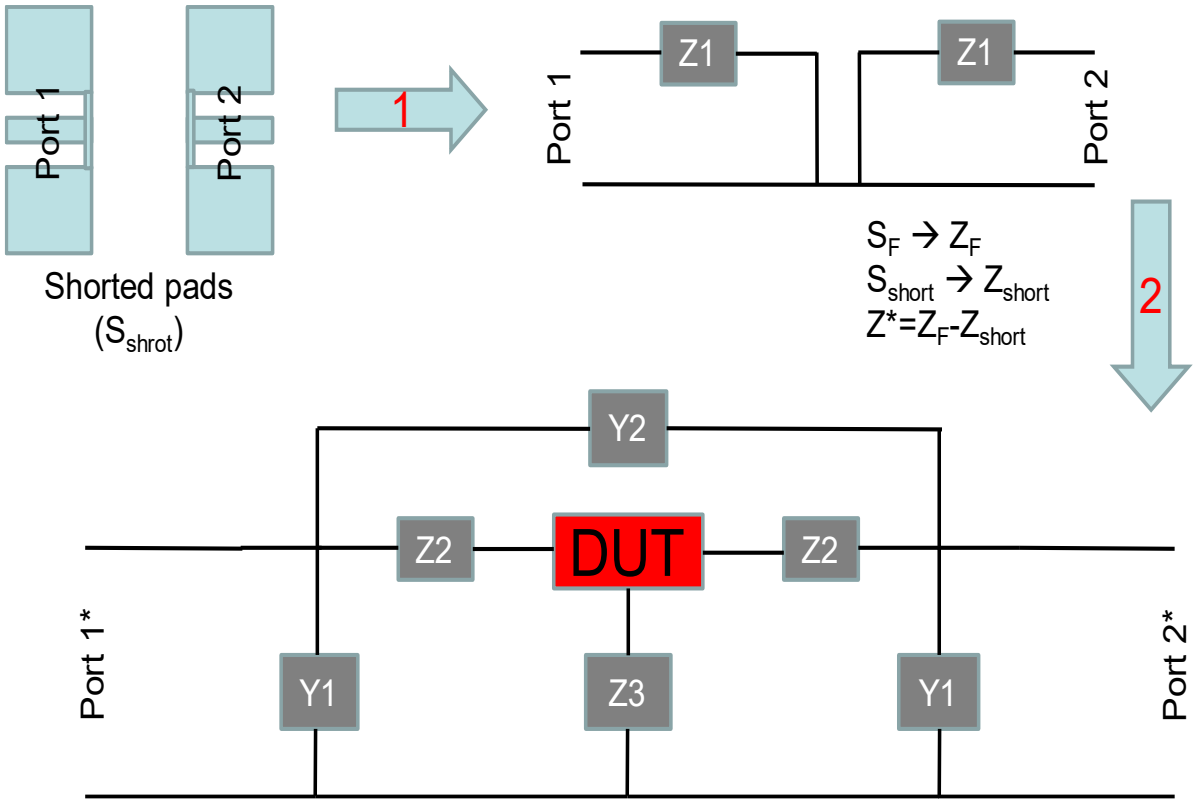

Fig. A. 2: Short De-embedding of full circuit. (a) Short S-parameter representation. (b) Short S-parameter to Z-parameter conversion and subtracted from Z-parameter of full circuit. (c) Full circuit after short de-embedding.

Step 2: Similarly, to remove the series effect of Y1 and Y2, open structures are utilized. First as shown in Fig. A.3, first the Z1 effect of the open structure are removed using short structure. Then using the Z1 removed open structure full circuit effect of Y1 and Y2 are removed. The calculations carried out in this step are shown in Fig. A.3 going from step 1 to 3.

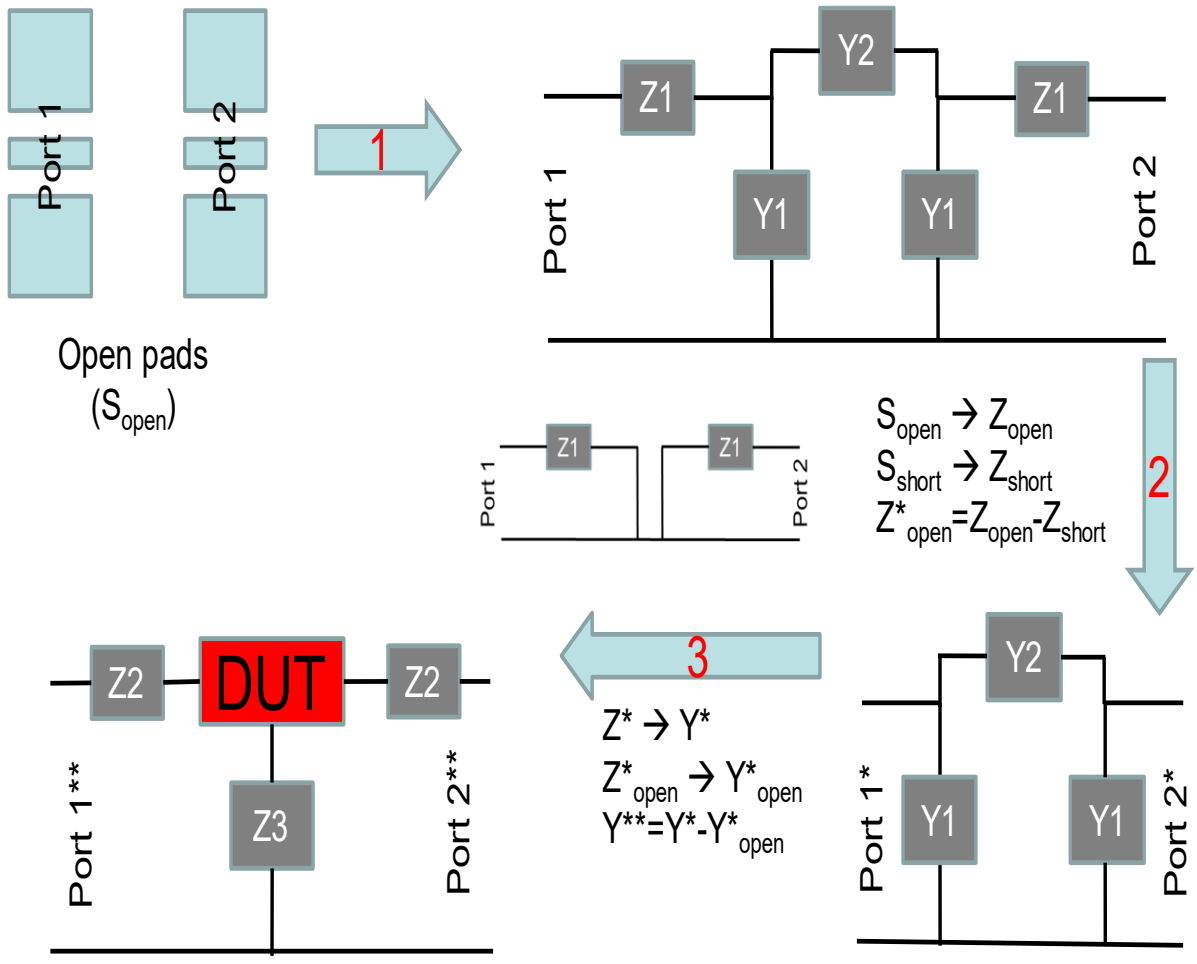

Fig. A. 3: Short-open De-embedding steps in the full circuit. First open is de-embedded using short structure and using the step 1 and step 2 results short-open de-embedding is done.

Step 3: Now the thru structure is used. In thru structure also, there are effect of Z1, Y1 and Y2 as shown in Fig. A.4. At first, these effects are removed using the short and open structure similar to step 1 and step 2 for full circuit. Final circuit represents the short open de-embedded thru structure which will be used to remove the thru effect of done in step 2 for the full circuit.

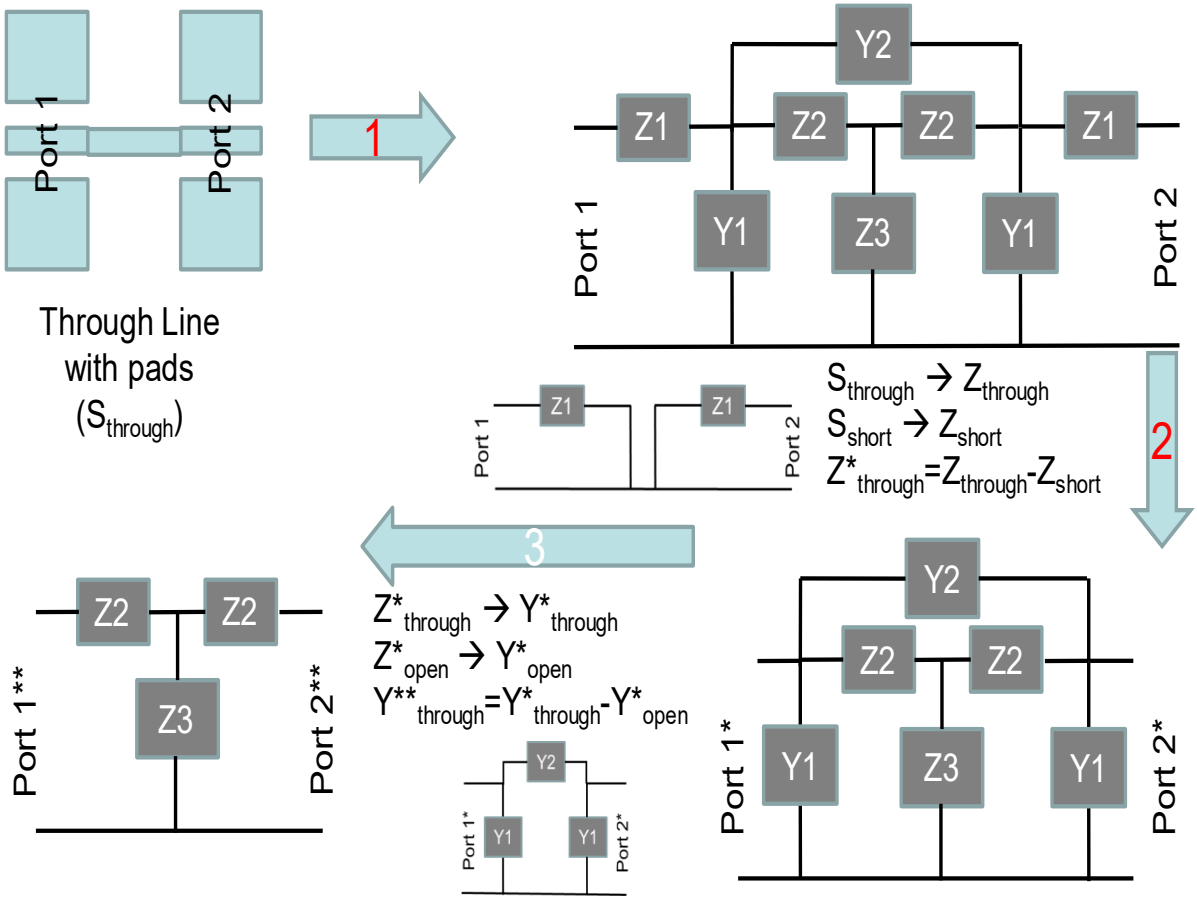

Fig. A. 4: Short-open De-embedding steps in the thru structure. First open is de-embedded using short structure and using the step 1 and step 2 results short-open de-embedding is done.

Step 3: Now the after short open de-embedding of both full circuit and the thru structure, we have both having effect of Z2 and Z3 whereas full circuit has DUT too.

Using this short-open de-embedded thru structure, the short-open de-embedded full circuit is de-embedded as shown in Fig. A.5. Both structure Y parameters are now converted to z-parameters and thru impedance is deducted from the full structure.

The final results contain the Z_{DUT}. This represents the is the de-embedded result of short-open-thru de-embedding. In case of inductors, information's like inductance and quality factors can be extracted from Z_{DUT}. This can also be converted to S_{DUT} for S-parameters study and representations.

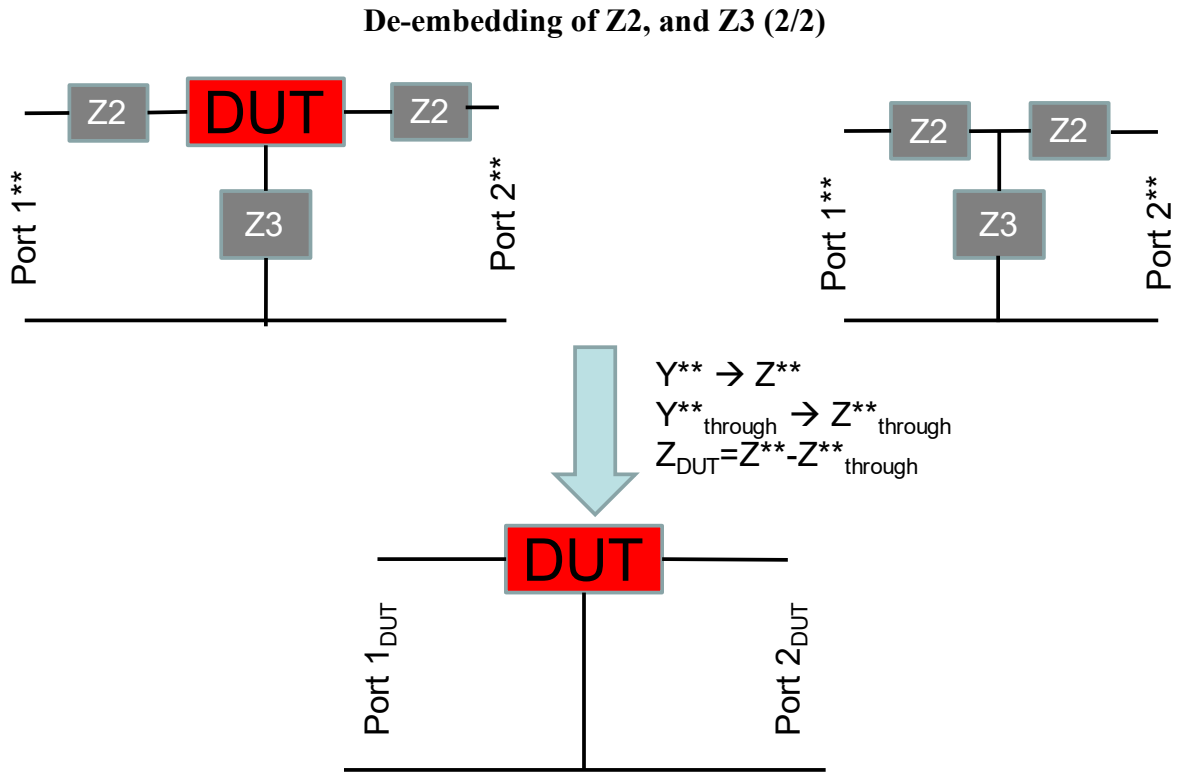

Fig. A. 5: Final short-open-thru de-embedded result.

Example: De-embedding of the DGS inductor and its verification.

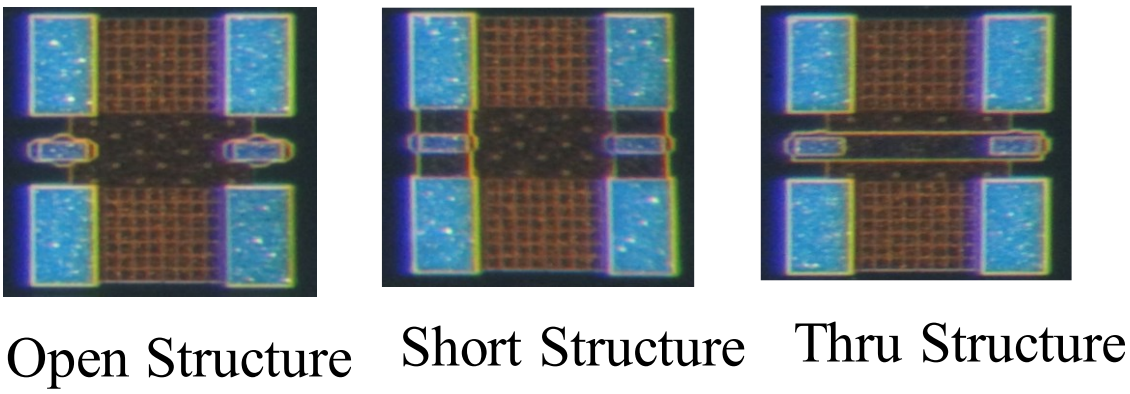

Fig. A. 6: Open-short-thru structures for DGS inductor de-embedding.

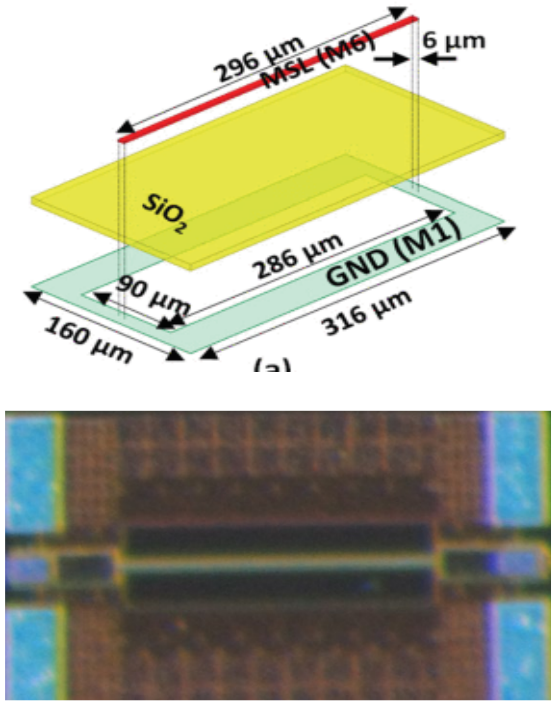

Fig. A. 7: EM model and fabricated prototype of DGS inductor [A.2].

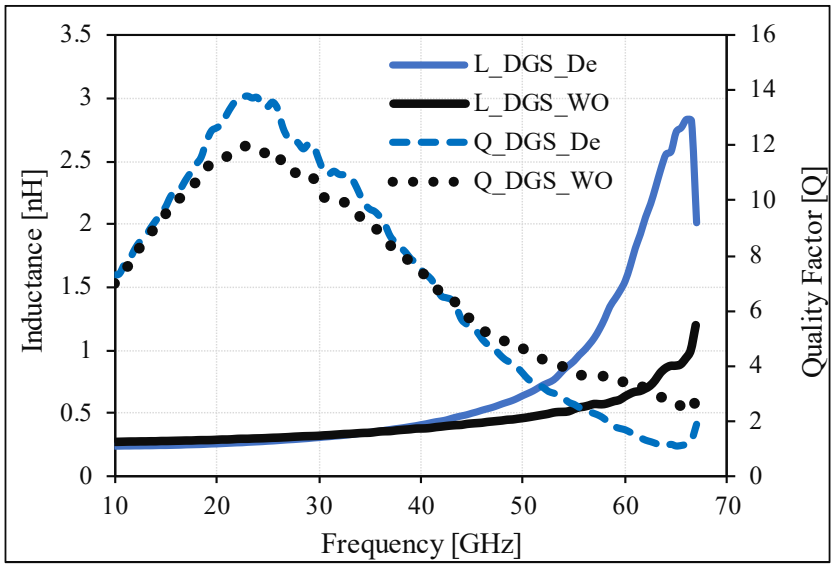

Fig. A. 8: short-open-thru before and after de-embedding results of DGS inductor [A.2]

2. L-2L De-embedding

L-2L de-embedding also involves compensating for the effects of the launch structures or interconnects in high-frequency signal analysis and characterization. The process is similar to slightly different than short-open-thru de-embedding, and also specific considerations must be taken into account due to the higher frequency range. Here is an overview of the theory involved:

- Measurement: Measurements are performed using a vector network analyzer (VNA) or other suitable instruments capable of operating at frequencies range of interest. The measurements capture the complete test setup, including the launch structures and the DUT.
- Reference Measurement: Additional measurements are taken with a reference standard that represents the launch structures (L and 2L structures). This reference standard can be a known impedance, or a calibration substrate specifically designed for high-frequency applications.
- De-embedding Algorithm: A de-embedding algorithm is applied using the measurements from steps 1 and 2 to calculate the inverse of the transfer function of the launch structures at operating frequency range. This algorithm determines the compensation needed to remove the launch structures' effects from the measured data accurately which will be explained below.
- De-embedding Process: The de-embedding algorithm is then used to mathematically remove the launch structures' influence from the measured data obtained in step 1. This process yields the de-embedded response of the DUT.
- Analysis: With the de-embedded response, we can analyze and characterize the intrinsic behavior of the DUT. This analysis may involve assessing the DUT's impedance, S-parameters, eye diagrams, or other relevant metrics specific to high-frequency applications.

By performing L-2L de-embedding, we can obtain a more accurate characterization of the DUT, isolate its intrinsic behavior from the launch structures' effects, and make informed design decisions to optimize the performance of high-frequency systems. In this thesis L-2L de-embedding discussed in the reference [A.3] and [A.4] are followed.

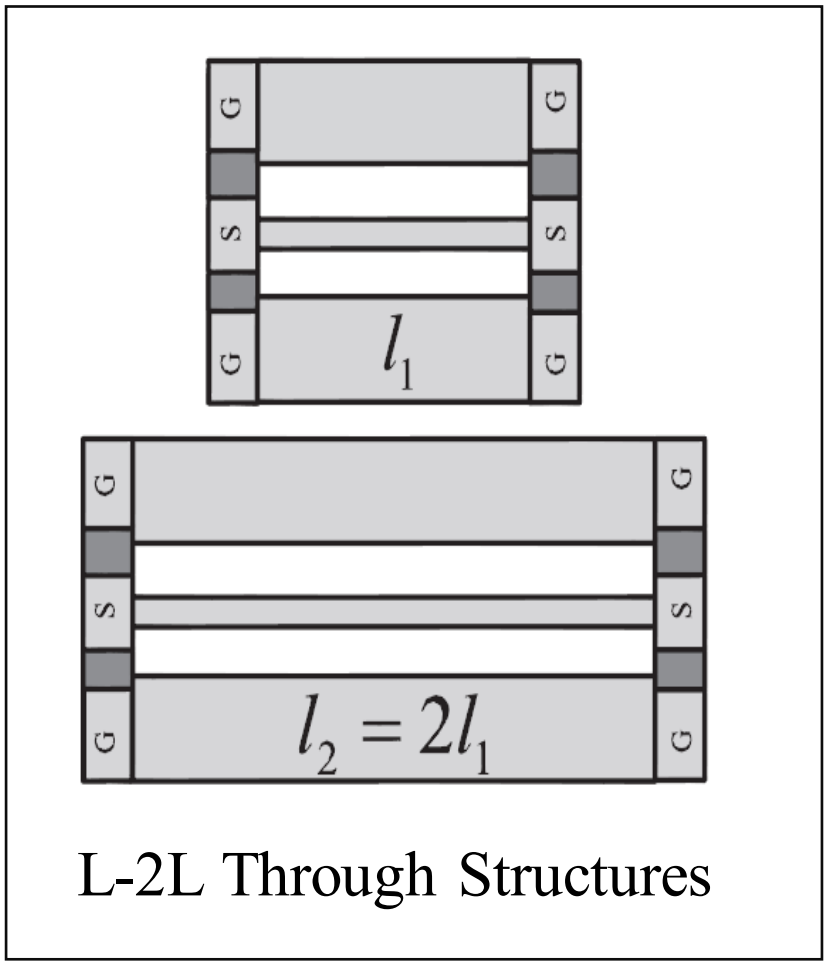

Fig. A. 9: L-2L de-embedding structures. Note 2L is double of L in size.

Represent L and 2L in T-parameters as:

$$\boldsymbol{T_1} = \boldsymbol{T_{lpad} T_{l_1} T_{rpad}} \quad \text{(A. 1)}$$

$$\boldsymbol{T_2} = \boldsymbol{T_{lpad} T_{l_1} T_{l_1} T_{rpad}} \quad \text{(A. 2)}$$

$$\text{So, } \boldsymbol{T_{lpad} T_{rpad}} = \boldsymbol{T_1 \, T_2^{-1} T_1} = \boldsymbol{T_{thru}} \quad \text{(A. 3)}$$

Use $\boldsymbol{T_{thru}}$ to calculate $\boldsymbol{Y_{shunt}}$ and $\boldsymbol{Z_{series}}$ as,

$$\boldsymbol{Y_{shunt}} = \boldsymbol{Y_{thru11}} + \boldsymbol{Y_{thru12}} \quad \text{(A. 4)}$$

$$Y_{shunt} = \frac{-1}{2*Y_{thru12}} \qquad \text{(A. 5)}$$

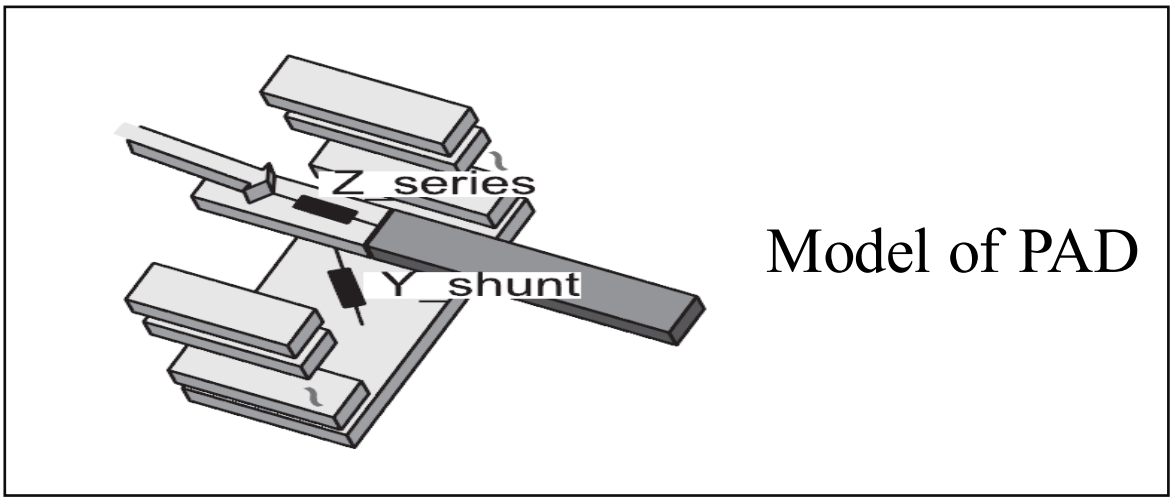

Fig. A. 10: Model of Pad in IC designs.

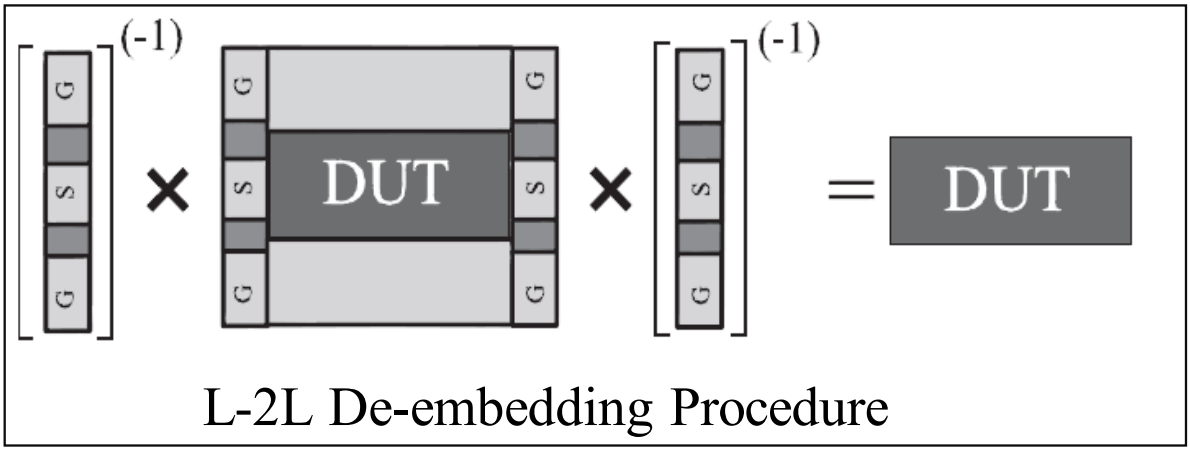

Fig. A. 11: L-2L de-embedding procedure.

Assuming the pads are symmetric then left and right pads are calculated using (A.4) and (A. 5)

$$T_{lpad} = \begin{pmatrix} 1 & Z_{series} \\ Y_{shunt} & Y_{shunt}Z_{series}+1 \end{pmatrix} \qquad \text{(A. 6)}$$

$$T_{rpad} = \begin{pmatrix} Y_{shunt}Z_{series}+1 & Z_{series} \\ Y_{shunt} & 1 \end{pmatrix} \qquad \text{(A. 7)}$$

Finally, to get the DUT, multiply measured data with the inverse of T_{lpad} and T_{rpad} as;

$$T_{DUT} = T_{lpad}^{-1} T_{meas} T_{rpad}^{-1} \qquad \text{(A. 8)}$$

This DUT represents the de-embedded result.

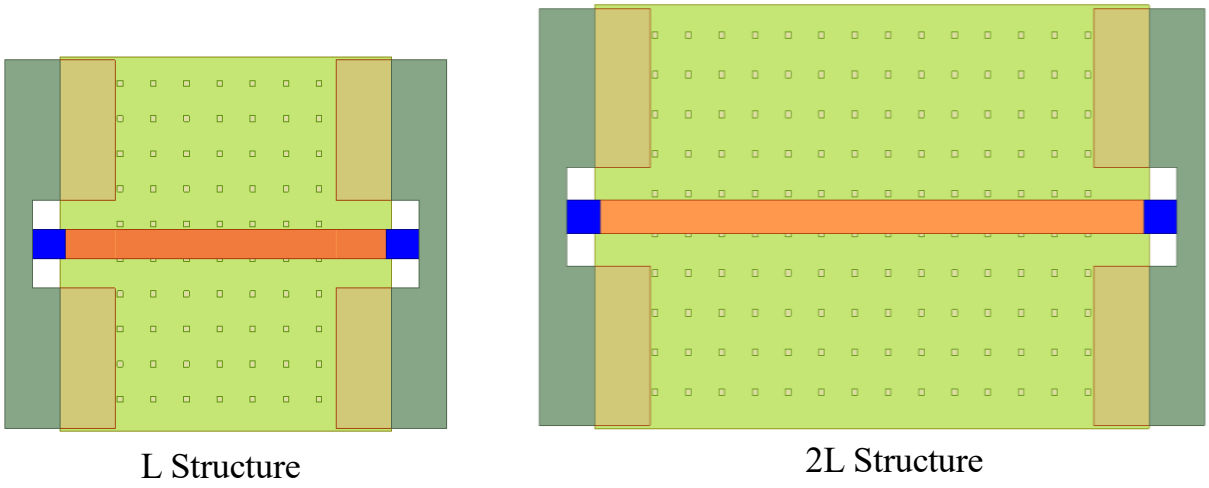

Fig. A. 12: Fabricated L-2L de-embedding structures.

Design Examples of L-2L de-embedding:

In this thesis chapter 2 and chapter 3 all designs are de-embedded by L-2L de-embedding methods. All the measurement and simulation results are in good agreement.

m-TRL De-embedding

The m-TRL is the advanced de-embedding technique used for high frequency applications typically above 100 GHz band. This method deals with extracting the characteristic impedance of the exact thru-reflect-line structures that extract the impedance of the reference plane. After extracting the characteristic impedance this will be employed to do the de-embedding. In this thesis, mTRL de-embedding discussed in [A.5] are used which is explained as follows.

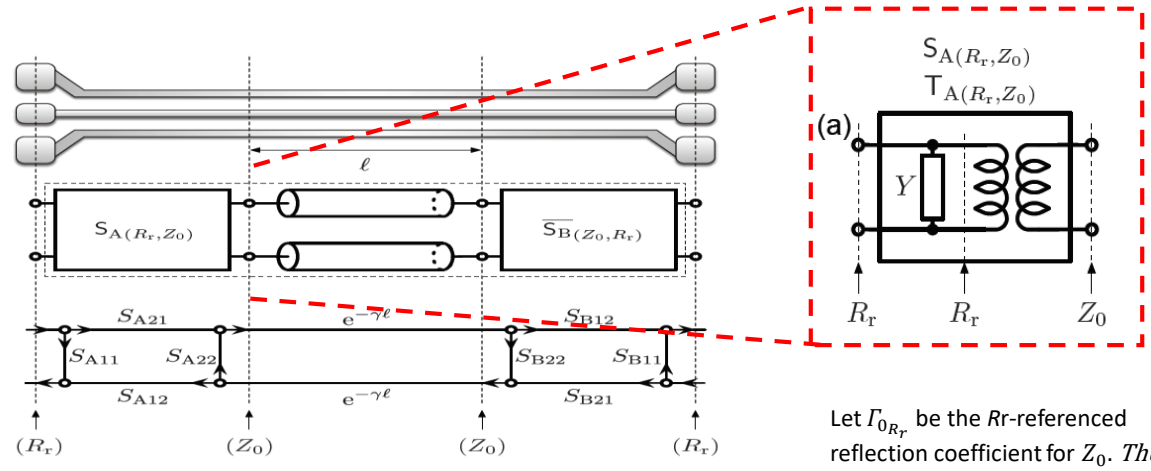

Fig. 2. A TL standard with pads and access lines, its error-box representation, signal-flow graph, and reference impedances in parentheses. R_r is the reference resistance set by a 1st-tier probe-tip calibration. Z_0 is the unknown characteristic impedance of the TL.

Let $\Gamma_{0_{R_r}}$ be the *R*r-referenced reflection coefficient for Z_0. *Then,*

$$\Gamma_{0_{R_r}} = \frac{Z_0 - R_r}{Z_0 + R_r}$$

Fig. A. 13: Transmission line structure with reference plane and DUT.

$$\Gamma_{0(R_r)} = \left\{ \sqrt{\frac{(T_{A12} + T_{A21})^2}{4\left[1 - j\frac{\Im(Z_0)}{\Re(Z_0)}\right] + (T_{A12} + T_{A21})^2}} \right\}_{(R_r, Z_0)}$$

$$T_A = \frac{1}{S_{A21}} \begin{bmatrix} S_{A12}S_{A21} - S_{A11}S_{A22} & S_{A11} \\ -S_{A22} & 1 \end{bmatrix}. \tag{A.9}$$

Upon Simplification as in Ref [A.5], $\Gamma_{0_{(R_r)}}$ becomes;

$$\Gamma_{0(R_r)} = \left\{ \sqrt{\frac{(S_{A11} - S_{A22})^2}{4S_{A12}S_{A21} + (S_{A11} - S_{A22})^2}} \right\}_{(R_r, Z_0)} \quad \text{(A.10)}$$

, Resulting Characteristic Impedance Z_0 as

$$Z_0 = \frac{1 + \Gamma_{0(Rr)}}{1 + \Gamma_{0(Rr)}} R_r \quad \text{(A.11)}$$

The complex-referenced S matrix of a length, *l*, of transmission line is

$$S_{(Z_{ref})} = \frac{1}{Z_0^2 + Z_{ref}^2 + 2Z_0 Z_{ref} \coth(\gamma \ell)} \times \begin{bmatrix} Z_0^2 - Z_{ref}^2 & 2Z_0 Z_{ref} / \sinh(\gamma \ell) \\ 2Z_0 Z_{ref} / \sinh(\gamma \ell) & Z_0^2 - Z_{ref}^2 \end{bmatrix} \quad \text{(A.12)}$$

With $Z_{ref} = Z_0$ becoems

$$S_{(Z_0)} = \begin{bmatrix} 0 & e^{-\gamma \ell} \\ e^{-\gamma \ell} & 0 \end{bmatrix}, \quad \text{(A.13)}$$

It also is the reason for the line's (generally unknown) Z_0 becoming the reference impedance ($Z_{ref} = Z_0$) of the new reference planes after performing TRL calibration.

More generally, a pair of reference impedances $Z_{i1}$and Z_{i2} that makes $S_{11} = S_{22} = 0$ are known as the image impedances of the 2-port. If $S_{(Z_{ref1}, Z_{ref2})} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$, than

$$S_{(Z_{i1},Z_{i2})} = \begin{bmatrix} 0 & e^{-\theta_{i12}} \\ e^{-\theta_{i21}} & 0 \end{bmatrix}, \tag{A.14}$$

where θ_{i21} and θ_{i12} are the image propagation parameters. Obviously, $Z_{i1} = Z_{i2} = Z_0$ and $\theta_{i21} = \theta_{i12} = \gamma$ in the case of transmission lines. The matrix elements of the complex-referenced Scattering parameters (SP) matrix of a length of transmission line are

$$S_{P11(Z_{ref1},Z_{ref2})} = \frac{(Z_0^2 - Z_{ref1}^* Z_{ref2}) \tanh \gamma\ell + Z_0(Z_{ref2} - Z_{ref1}^*)}{(Z_0^2 + Z_{ref1} Z_{ref2}) \tanh \gamma\ell + Z_0(Z_{ref1} + Z_{ref2})}, \tag{A.15}$$

$$S_{P22(Z_{ref1},Z_{ref2})} = \frac{(Z_0^2 - Z_{ref1} Z_{ref2}^*) \tanh \gamma\ell + Z_0(Z_{ref1} - Z_{ref2}^*)}{(Z_0^2 + Z_{ref1} Z_{ref2}) \tanh \gamma\ell + Z_0(Z_{ref1} + Z_{ref2})}, \tag{A.16}$$

$$\begin{aligned} S_{P21(Z_{ref1},Z_{ref2})} &= S_{P12(Z_{ref1},Z_{ref2})} \\ &= \frac{2Z_0 \sqrt{\Re(Z_{ref1})\Re(Z_{ref2})}/\cosh \gamma\ell}{(Z_0^2 + Z_{ref1} Z_{ref2}) \tanh \gamma\ell + Z_0(Z_{ref1} + Z_{ref2})}. \end{aligned} \tag{A.17}$$

Note that $Z_{ref1} = Z_{ref2} = Z_0$ doesn't make $S_{P11} = S_{P22} = 0$

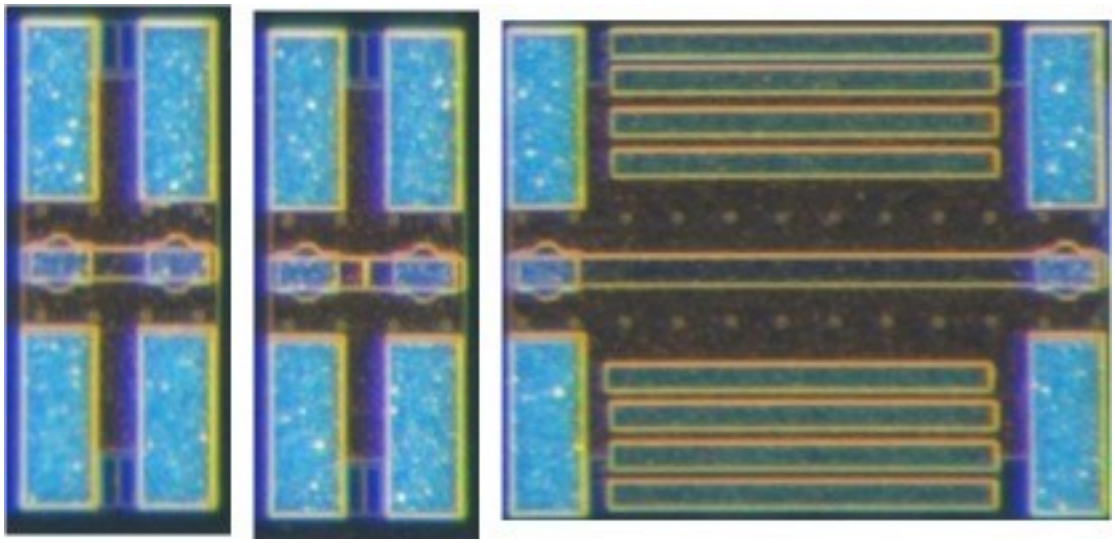

Fig. A. 14: m-TRL Structures. (a) Thru Standard. (b) Reflect Standard. (c) Line Standard.

Requirements taking maximum measurable frequency:

In our case we use measurement results upto 300 GHz band. So, the design og the thru and line length are:

- Thru length $l_1 = \frac{\lambda g}{10} = 63.09\ um\ @\ 300GHz$
- Line length $l_1 + l_2$ *where* $l_2 = 0.89\lambda g = 561\ um$

Example of m-TRL De-embedding:

All the de-embedding performed in chapter 4 are done using m-TRL de-embedding.

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