

Study on Power Module Design for Digital Gate Driver Circuit

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論 文 内 容 の 要 旨

Thesis Summary

In this thesis, the design of power modules for a digital gate driver was studied. IGBT power modules are critical components in various power electronics systems, such as electric vehicles and wind turbines. In IGBT modules, there is a need for low-loss switching operation and minimal switching noise. Therefore, it is essential to consider the trade-off characteristics between switching losses and noise in power semiconductor devices. Digital Gate Drivers DGD offer a technology that significantly improves the trade-off between turn-on loss E_{on} and collector current overshoot $I_{overshoot}$, as well as turn-off loss E_{off} and collector-emitter voltage overshoot $V_{overshoot}$ compared to conventional gate drivers for power transistors (IGBT, MOSFET, etc.). However, despite these advancements, there has been limited exploration of power modules specifically tailored for digital drivers.

In the operation of DGD, the dynamic control of gate drive current during switching leads to a complex and intense variation in gate current I_g , resulting in the occurrence of gate voltage V_g spikes that pose a potential risk of damaging the DGD. The timing of gate voltage spikes V_{g_spike} corresponds to changes in the digital control vector, i.e., when I_g is raised or lowered. It was predicted that the V_{g_spike} is generated due to dI_g/dt and the gate inductance L_g of the IGBT module. Therefore, we manufactured IGBT modules with different L_g values and conducted double-pulse tests. Experimental results showed that the trade-off between switching losses and overshoot was improved with digital gate control, but significant V_{g_spike} occurred during turn-off. It was observed that V_{g_spike} positively correlates with the changes in L_g and the gate drive vector. Achieving a balance between trade-off improvement and suppression of gate voltage spikes requires reducing the L_g of IGBT modules driven by DGD.

To increase the rated current of IGBT modules, a common approach involves parallelizing IGBT devices. However, this method introduces current imbalances due to the uneven parasitic inductances associated with each IGBT device. While there are many power modules with parallel IGBTs designed for traditional gate driving, there is currently a lack of parallel IGBT power modules tailored for digital drivers. Moreover, digital drivers are expected to suppress current overshoot and mitigate current imbalances during switching. We fabricated modules with varying L_g and emitter inductance L_e to correspond to parallel IGBTs and conducted double-pulse tests using digital drivers. Experimental results demonstrated that, during turn-off, the current imbalance caused by uneven L_e could be improved by varying L_g . Additionally, during turn-on, current overshoot and imbalances caused by uneven L_e could be suppressed using a small digital drive vector.

Finally, to suppress V_{g_spike} , it is essential to elucidate the mechanism of V_{g_spike} generation in IGBT switching operations. According to the basic principles of LC resonance circuits, V_{g_spike} is believed to originate from inductance and capacitance. As mentioned earlier, we have established that larger L_g in IGBT modules leads to larger V_{g_spike} , and the change in the gate drive vector Δn reflecting dI_g/dt correlates with the magnitude of V_{g_spike} . However, the origin and impact of capacitance remain unclear. To address this, we focused on the turn-off

waveform and investigated the influence of IGBT input capacitance on V_{g_spike} using IGBT modules with the same L_g and different input capacitances. We also examined the impact of parasitic capacitance and impedance on the DGD side using external capacitance C_{ex} and control vector value adjustments. Experimental results revealed that V_{g_spike} was independent of IGBT input capacitance. On the other hand, when C_{ex} was parallelized with DGD, increasing C_{ex} resulted in a reduction of V_{g_spike} . Additionally, enlarging the gate drive vector led to a decrease in V_{g_spike} . It was demonstrated that V_{g_spike} depends on the output impedance of DGD. Changes in DGD's output impedance cause variations in I_g , generating V_{g_spike} due to induced voltage in L_g .

In this study, we conducted the design verification of IGBT modules applicable to a digital driver through simulations and experiments. It was clearly established that V_{g_spike} has a positive correlation with L_g and vector changes. During IGBT parallel operation, we were able to improve the current imbalance during turn-off by varying L_g . Moreover, during turn-on, both current overshoot and current imbalance could be suppressed with a small digital drive vector. Additionally, the risk of gate voltage spikes that could potentially damage the digital driver was shown to have a positive correlation with the output impedance of the digital driver.