Study on Power Module Design for Digital Gate Driver Circuit

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Doctoral Thesis

Study on Power Module Design for Digital Gate Driver Circuit

デジタルゲートドライバー用パワーモジュールの設計に関する研究

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by

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ABSTRACT

In this thesis, the design of power modules for a digital gate driver was studied. IGBT power modules are critical components in various power electronics systems, such as electric vehicles and wind turbines. In IGBT modules, there is a need for low-loss switching operation and minimal switching noise. Therefore, it is essential to consider the trade-off characteristics between switching losses and noise in power semiconductor devices. Digital Gate Drivers DGD offer a technology that significantly improves the trade-off between turn-on loss E_{on} and collector current overshoot $I_{overshoot}$, as well as turn-off loss E_{off} and collector-emitter voltage overshoot $V_{overshoot}$ compared to conventional gate drivers for power transistors (IGBT, MOSFET, etc.). However, despite these advancements, there has been limited exploration of power modules specifically tailored for digital drivers.

In the operation of DGD, the dynamic control of gate drive current during switching leads to a complex and intense variation in gate current I_g, resulting in the occurrence of gate voltage V_g spikes that pose a potential risk of damaging the DGD. The timing of gate voltage spikes V_{g_spike} corresponds to changes in the digital control vector, i.e., when I_g is raised or lowered. It was predicted that the V_{g_spike} is generated due to dI_g/dt and the gate inductance L_g of the IGBT module. Therefore, IGBT modules with different L_g values were manufactured and double-pulse tests were conducted. Experimental results showed that the trade-off between switching losses and overshoot was improved with digital gate control, but significant V_{g_spike} occurred during turn-off. It was observed that V_{g_spike} positively correlates with the changes in L_g and the gate drive vector. Achieving a balance between trade-off improvement and suppression of gate voltage spikes requires reducing the L_g of IGBT modules driven by DGD.

To increase the rated current of IGBT modules, a common approach involves parallelizing IGBT devices. However, this method introduces current imbalances due to the uneven parasitic inductances associated with each IGBT device. While there are

many power modules with parallel IGBTs designed for traditional gate driving, there is currently a lack of parallel IGBT power modules tailored for digital drivers. Moreover, digital drivers are expected to suppress current overshoot and mitigate current imbalances during switching. Modules with different L_g and emitter inductance L_e were fabricated to conduct double-pulse tests using digital drivers. Experimental results demonstrated that, during turn-off, the current imbalance caused by uneven L_e could be improved by varying L_g. Additionally, during turn-on, current overshoot and imbalances caused by uneven L_e could be suppressed using a small digital drive vector.

Finally, to suppress V_{g_spike}, it is essential to elucidate the mechanism of V_{g_spike} generation in IGBT switching operations. According to the basic principles of LC resonance circuits, V_{g_spike} is believed to originate from inductance and capacitance. As mentioned earlier, it has been clarified that larger L_g in IGBT modules leads to larger V_{g_spike}, and the change in the gate drive vector Δn reflecting dI_g/dt correlates with the magnitude of V_{g_spike}. However, the origin and impact of capacitance remain unclear. To address this, the turn-off characteristics were focused to investigate the influence of IGBT input capacitance on V_{g_spike} using IGBT modules with the same L_g and different input capacitances. The impact of parasitic capacitance, and impedance on the DGD side using external capacitance C_{ex}, and control vector value adjustments were also examined. Experimental results revealed that V_{g_spike} was independent of IGBT input capacitance. On the other hand, when C_{ex} was parallelized with DGD, increasing C_{ex} resulted in a reduction of V_{g_spike}. Additionally, enlarging the gate drive vector led to a decrease in V_{g_spike}. It was demonstrated that V_{g_spike} depends on the output impedance of DGD. Changes in DGD's output impedance cause variations in I_g, generating V_{g_spike} due to induced voltage in L_g.

In this study, the design verification of IGBT modules applicable to a digital driver were conducted through simulations and experiments. It was clearly established that V_{g_spike} has a positive correlation with L_g and vector changes. During IGBT parallel operation, the current imbalance could be impressed during turn-off by varying L_g. Moreover, during turn-on, both current overshoot and current imbalance could be

suppressed with a small digital drive vector. Additionally, the risk of gate voltage spikes that could potentially damage the digital driver was shown to have a positive correlation with the output impedance of the digital driver.

CONTENTS

CHAPTER 1 Introduction

1.1 The introduction and assignments of power modules

In the transition towards a decarbonized society, proactive efforts such as transitioning to high-efficiency systems and increasing the use of renewable energy sources are essential. As depicted in Fig. 1.1, in the year 2050, energy efficiency and renewable energy will play significant roles, constituting 37% and 32% respectively [1]. The sustainable expansion of wind and solar power systems within renewable energy sources is anticipated [2-6], leading to an unprecedented increase in sustainable electricity generation. This surge in generation levels will necessitate the connection to the grid through power converters/invertors [7-9]. Additionally, driven by the global emission reduction targets outlined in the Paris Agreement, electric vehicles and hybrid

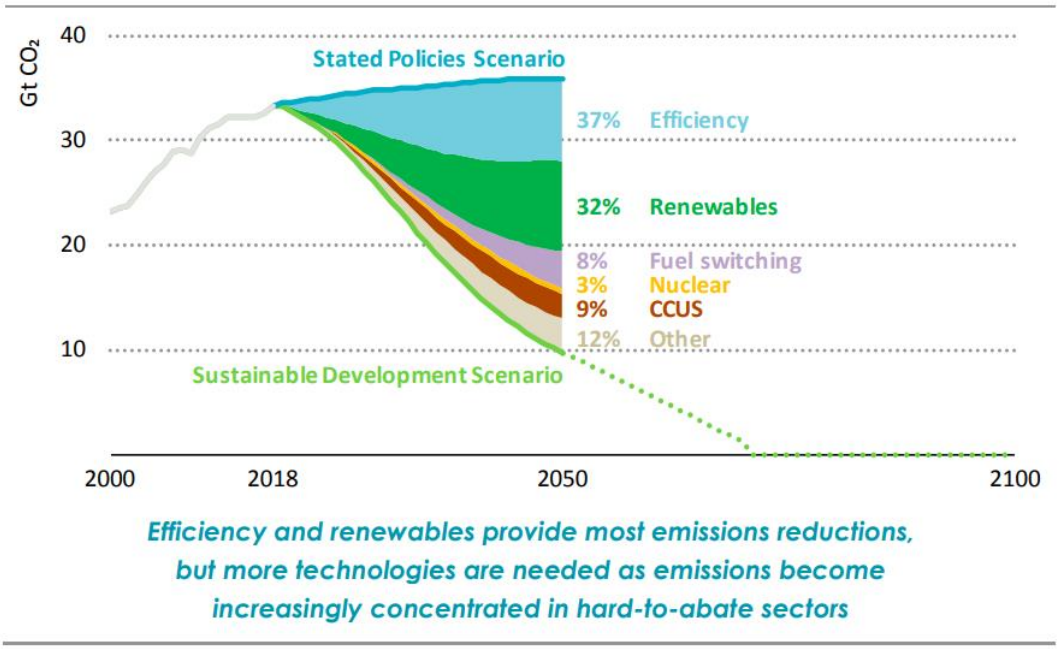


Fig. 1.1 Energy-related CO_2 emissions and reductions by source in the Sustainable Development Scenario [1].

cars have become directions for the automotive industry's development, exhibiting notable advancements in recent years [10-15]. Consequently, converters and inverters

in power conversion systems for motor drives are set to take a crucial role. To pave the way for renewable energy, the utilization of high-efficiency converters and inverters is vital in electricity generation, transmission, distribution, and end-user applications [7-9].

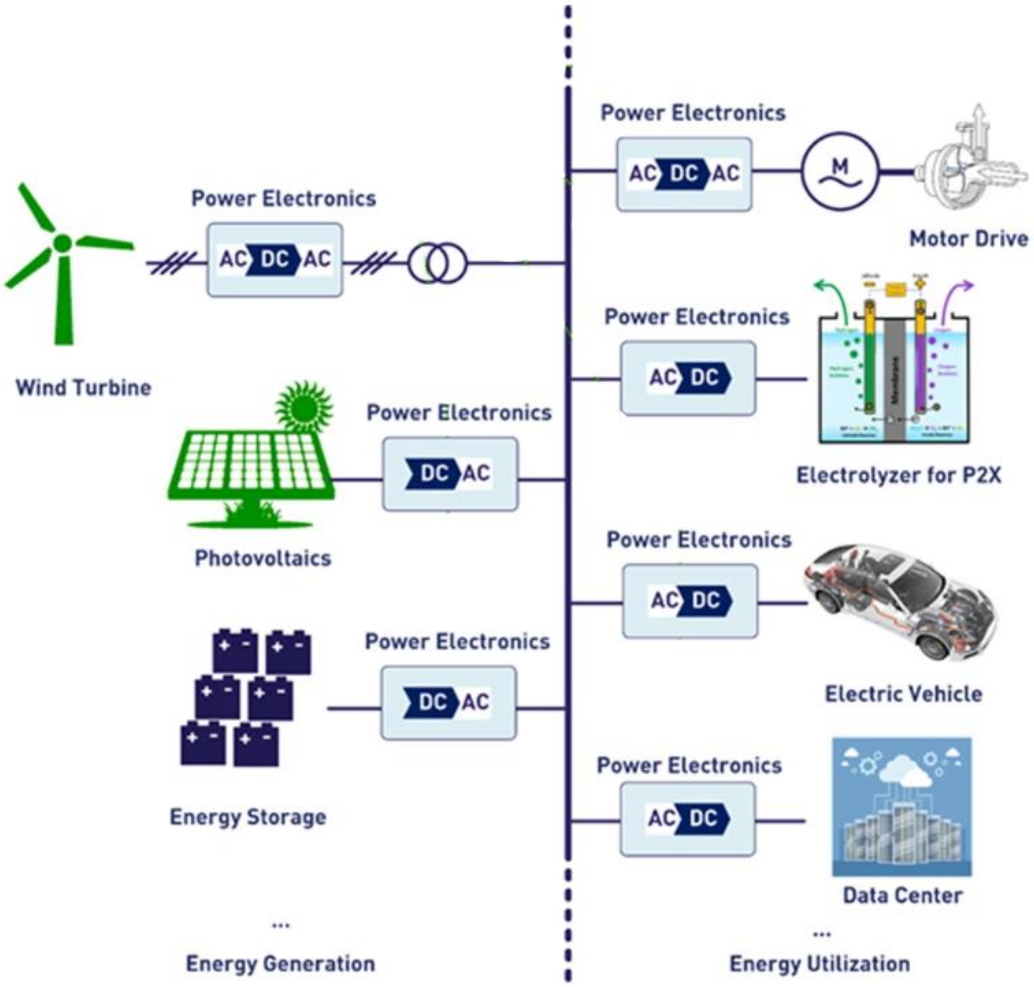


Fig. 1.2 Simplified electricity grid [16].

Figure 1.2 shows the simplified grid of the electricity transmission produced by renewable energy [16]. It can be noted that there are many converters/inverters from energy source to users, because the current or the voltage is necessary to be converted to the same level as the grid before transmitted to users. And there are also a lot of converters and inverters to convert the current and voltage to needed level for different end-user applications. Fig. 1.3 shows the simplified structure of power converters, whose primary components are power modules. And power modules are made by

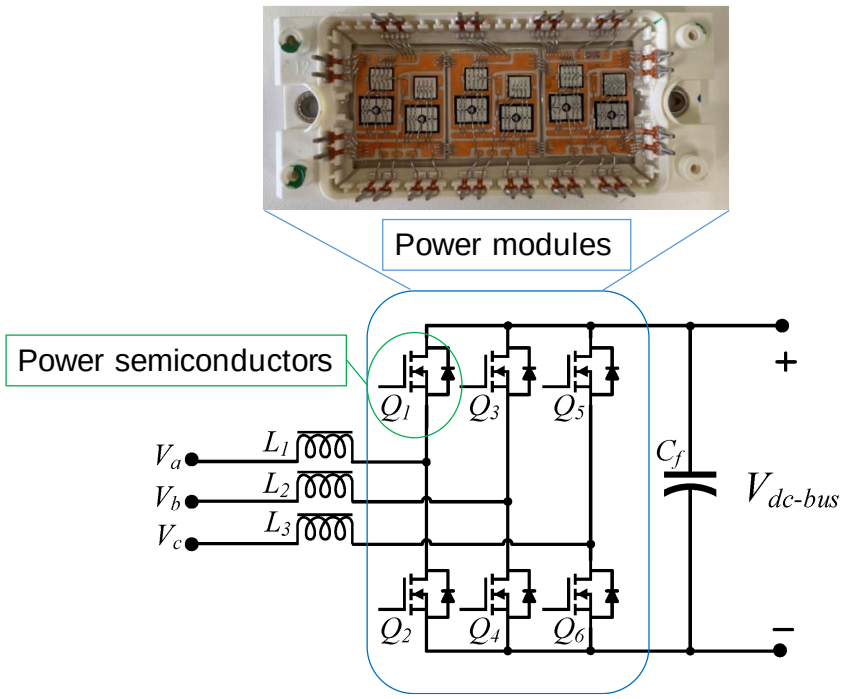


Fig. 1.3 Circuit schematic of power converters [9] and IGBT modules from Infineon.

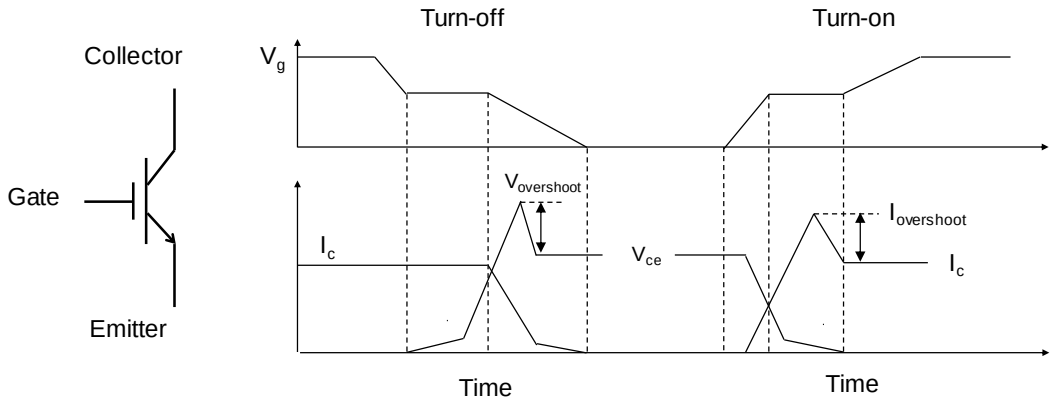
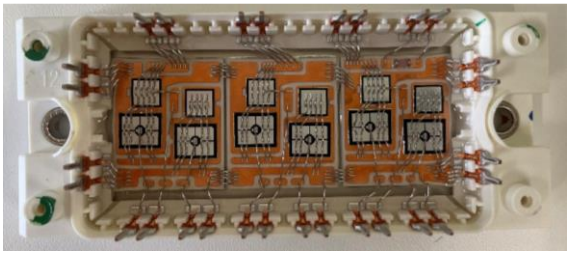


Fig. 1.4 Schematic circuit and primary switching behavior of IGBT.

power semiconductors. Converters/inverters use the switching function of power semiconductor devices (IGBT, MOSFET etc.) to regulate the voltage or the current. Fig. 1.4 shows the schematic circuit and primary switching behavior of IGBT. When the gate is negative biased, the gate voltage will decrease to turn off the IGBT. The collector-emitter voltage of IGBT increases to power supply voltage and collector current decreases to zero. When the gate bias is positive, the IGBT will be turned on. The transient is opposite to that in turn-off.



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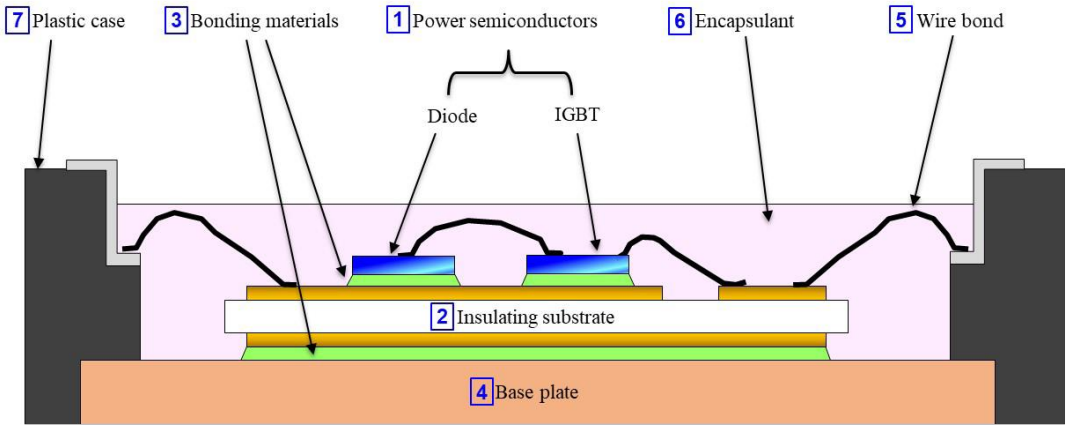

b

Fig. 1.5 The structure of power modules [18].

There are discrete type [17] and multi-chip type power modules mainly. The image of multi-chip type power module cross section diagram is shown in Fig. 1.5 b [18]. Power modules consist of seven basic elements, which is power semiconductor devices, an insulating substrate, base plate, bonding materials, bonding wires, encapsulant, and plastic case. The chips are connected to contact terminals by aluminum wires. These wires are the main cause of stray inductance that will result in voltage/current overshoot threatening the safe operation of power semiconductor devices.

Another type of power modules is called IPM (Intelligent Power Module) [19]. Although there are some sub-categories in the IPM, the wide sense of IPMs are that the power modules or power stacks which have more functions than standard power modules. For example, Fig. 1.6 shows the 6th generation Fuji Electric IPM available in the market [19], the extra features are: 1) Integrated IGBT pre-driver; 2) Three protections: Over temperature, over current and under gate drive voltage; 3) Alarm output when protection activated. More functional and integrated IPM should be the future form of power modules.

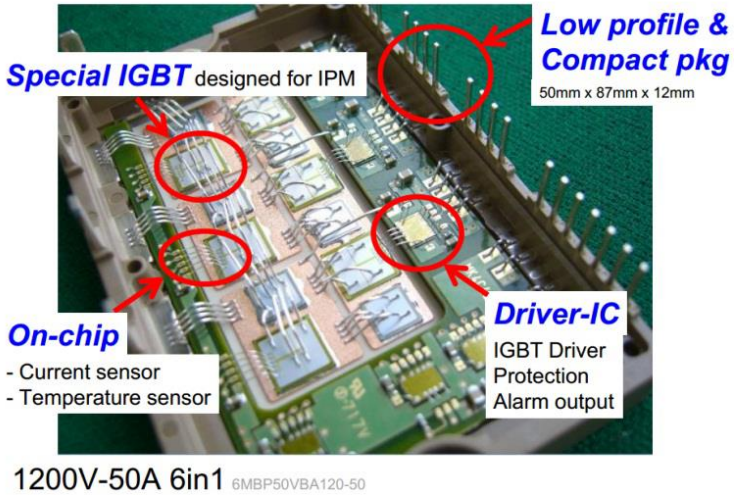

Fig. 1.6 The structure of intelligent power modules [19].

Parasitic inductance exists from the semiconductor chip to their terminal connections. The stray inductance can be introduced by DBC substrate and bonding wires in modules. The substrate inductance is much smaller than that of bonding wires. The above main types of power modules use bonding wires to make electrical linkages between the power semiconductors, conductor traces, and input/output terminals of the module. The most common material used for top-side connection is aluminum wires. The parasitic inductance stores energy whenever the current flows through the interconnections inside the module when the chip is turned on or turned off. As shown in Fig. 1.4, when the IGBT is turned off, the energy is released directly as a voltage overshoot. This overshoot is a function of inductance and collector current I_c gradient, dI_c/dt. The dI_c/dt is affected by the gate resistance R_g, which determines the switching speed of IGBT. Small R_g results in large dI_c/dt leading to large voltage overshoot $V_{overshoot}$, but the turn-off loss E_{off} can be reduced. In the contrast, large R_g can reduce the $V_{overshoot}$, but the E_{off} will be enlarged due to low switching speed. In the turn-on, there is a similar phenomenon of turn-on loss E_{on} and current overshoot $I_{overshoot}$. So, a tradeoff relationship of switching loss and voltage/current overshoot should be improved for IGBT modules. How to deal with the parasitic effect and improve the tradeoff relationship will ultimately affect the EMI, efficiency, and performance of the converters and inverters [20].

1.2 Package schemes of power modules for suppressing loss and noise

To reduce the impact of parasitic inductance in power modules, several packaging schemes, such as planar interconnection, chip embedded package, 3-D interconnection, and innovative layout design have been proposed.

Planar interconnection: Siemens introduced a novel packaging technique for power modules based on a planar interconnect technology (SiPLIT), as shown in Fig. 1.7. The SiPLIT featured thick Cu interconnects on a high-reliable insulating film for top contacts of power chips. Thanks to the conductor structure and contact technology, parasitic inductances of the power module were very low in comparison to state-of-the-art Al wire bonded interconnection. Through electrical characterization, it was found that up to 50% reduction in parasitic inductances of the interconnects was achieved [21].

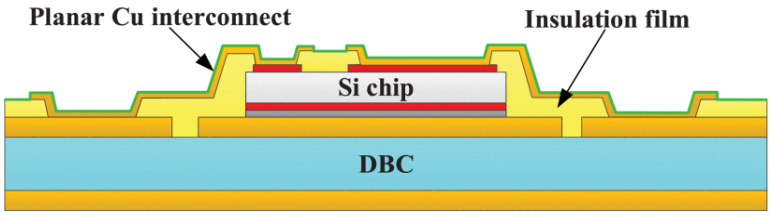

Fig. 1.7 Power modules based on a planar interconnect technology (SiPLIT) [21].

Mitsubishi reported a simple, compact, robust, and high-performance transfer-molded power module with direct lead bonding technology, as shown in Fig. 1.8. Cu lead was directly bonded on the emitter and cathode electrodes by solder, and Al conventional wire was bonded on the gate electrode. And the Cu lead shown in Fig. 1.9 was developed to enlarge bonding area, which is equal to realize the inner connection by a thick wire. The wire diameter is negative corresponding to self-inductance. Compared with conventional wire bonded power module, the transfer-molded power module showed 43% reduction in parasitic inductance [22]. But according to the product lineup in the homepage of Mitsubishi Electric, this kind of power modules are only applied to EV and HEV.

Liang *et al.* [23] proposed a multilayer planar interconnection package structure for a 200 A/1200 V IGBT phase-leg power module, as shown in Fig. 1.10. The IGBT and

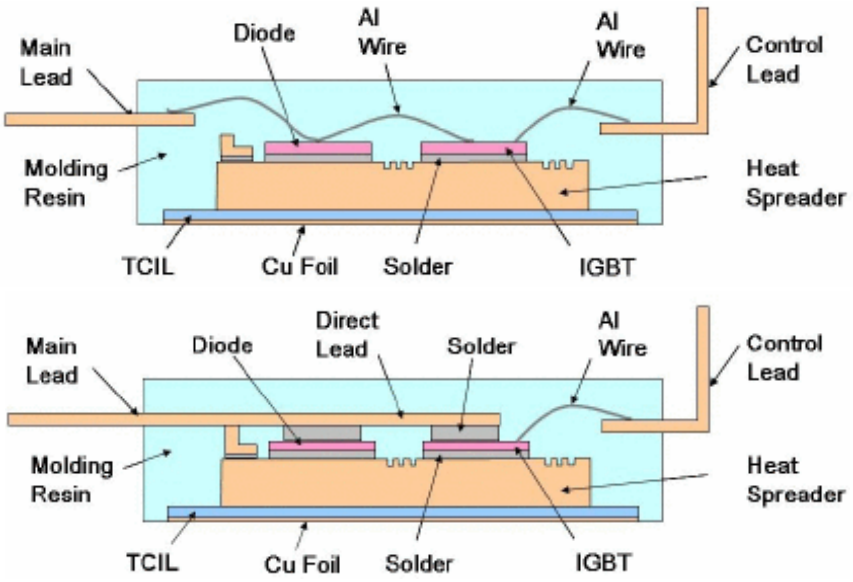

Fig. 1.8 Transfer-molded power module with direct lead bonding technology [22].

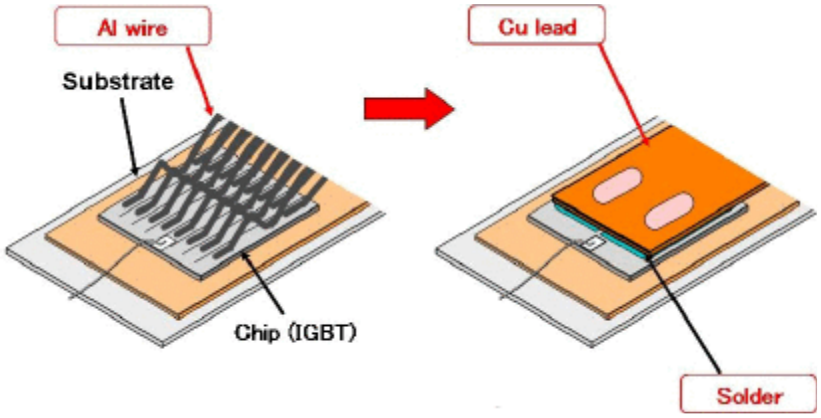

Fig. 1.9 Cu lead of Transfer-molded power module [22].

diode dies were sandwiched between two DBC substrates. The electrical interconnection is achieved by conductively bonding switch dies to the copper layers on the two DBCs, which are used to form circuitry which physically corresponds with the electrode pad layout on the dies. The upper switch pair and lower switch pair in the phase-leg were oriented in a face-up/face-down configuration. Compared to traditional wire bond packaging, where all dies are placed in a face-up orientation on a substrate, the layout shown in Fig. 1.10 makes the main current flow loops in the vertical direction. The thickness of the switch die is typically 0.1 mm, while its length in plane level is in the range of 10 mm. Compared with wire bonded power module, total inductance of the planar bonded power module decreased by 62%. Besides, voltage overshoot reduced by 54% of that of the wire bonded package.

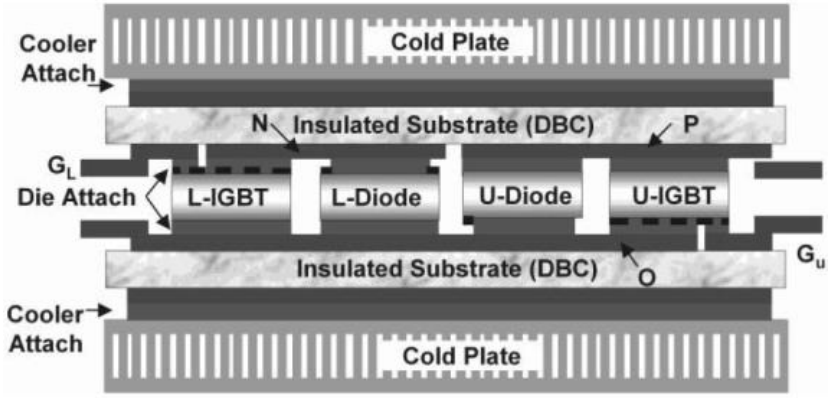

Fig. 1.10 A multilayer planar interconnection package structure for a 200 A/1200 V IGBT phase-leg power module [23].

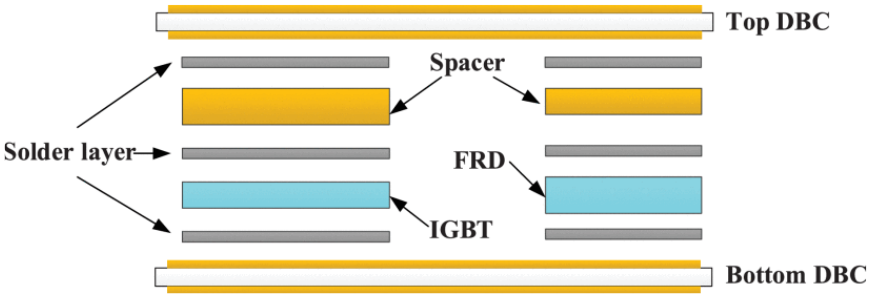

Fig. 1.11 A schematic of spacer-based sandwich structure for power module [24].

Fig. 1.11 shows a schematic of spacer-based sandwich structure for power module. Cu spacers with different thicknesses were used to accommodate height differences between IGBT and diode in a power module [24]. To build solder bump on the IGBT and diode, an additional metallization layer was needed to be sputtered on the front-side source and gate pads to increase the wettability of solder. For this purpose, the original Al metallization of emitter, anode, and gate contact was modified by sputtering of Ti/Ni/Ag (60/500/800 nm) layers [24]. Compared with conventional IGBT module, 55.1% and 13.2% reduction in parasitic inductance and resistance.

Chip embedded package: Fig. 1.12 shows a structure schematic of a ceramic embedded power module [25]. It consists of three layers which are: 1) base substrate; 2) embedded power stage; and 3) components, stacked by solder interconnects. The second layer is built on a ceramic frame, as shown in Fig. 12(b), with the chips buried into it. The dielectric is used as an interlayer to protect the chip and form a flat surface

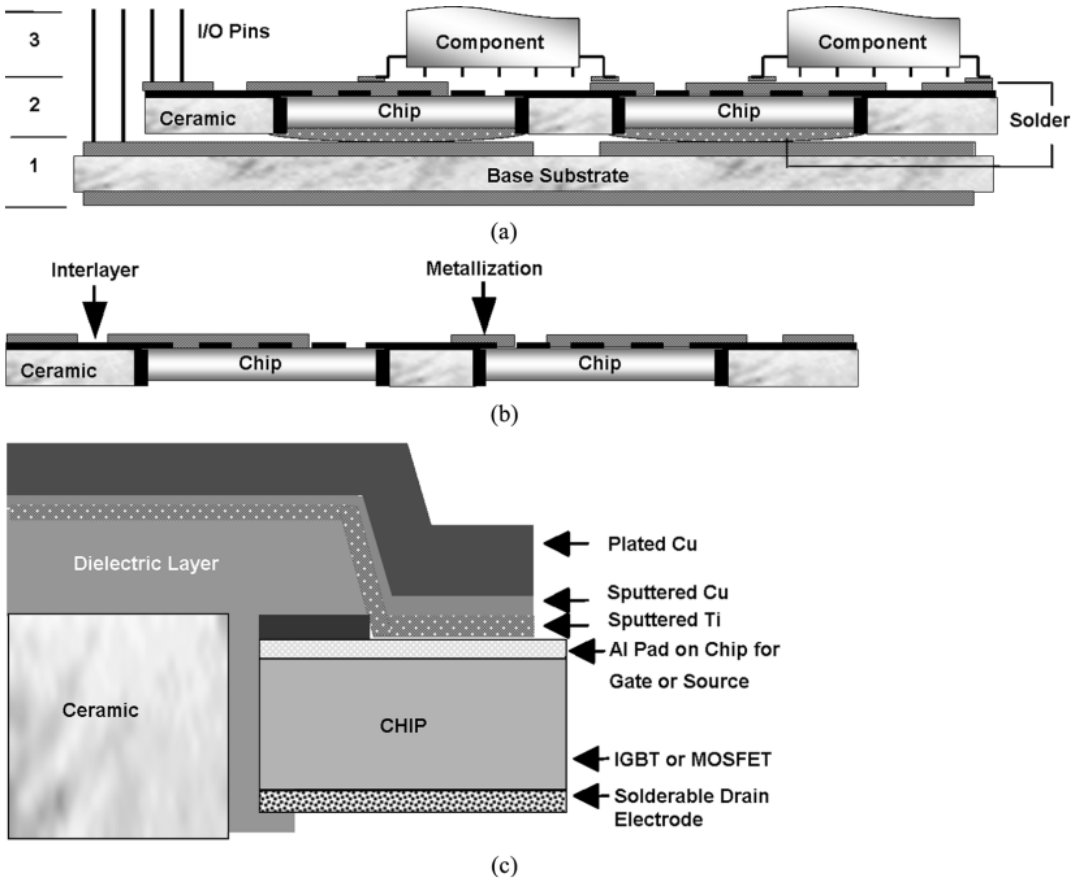

Fig. 1.12 A structure schematic of a ceramic embedded power module [25].

with defined via holes exactly on the top pads of the chips. The metallization is for the interconnection of multiple power chips through metallurgical contact to aluminum pads on the chips through via holes in the dielectric layer; this replaces the bonding wires in the conventional module, and also is used as the interconnection for the attachment of associated components in layer 3. Compared with conventional wire bonded package, a 75% reduction in parasitic inductance were achieved. But the process of this embedded power modules are complicated. Although several other previous works realized this kind of power modules and tried to improve the process [26-31], it is still complicated and costly.

3-D interconnection: Marchesini et al. [32] presented a power chip-on-chip packaging technology for IGBT power module, as shown in Fig. 1.13. Electrical interconnection of the IGBT chips was realized through two DBC substrates and a four-layer PCB. DC link and decoupling capacitors were integrated directly on the PCB to reduce the stray inductance. The experimental results showed that the parasitic

inductance of the power chip-on-chip module was drastically reduced compared to conventional ones.

In [33], a power chip-on-inductor packaging technique with dual sided cooling was

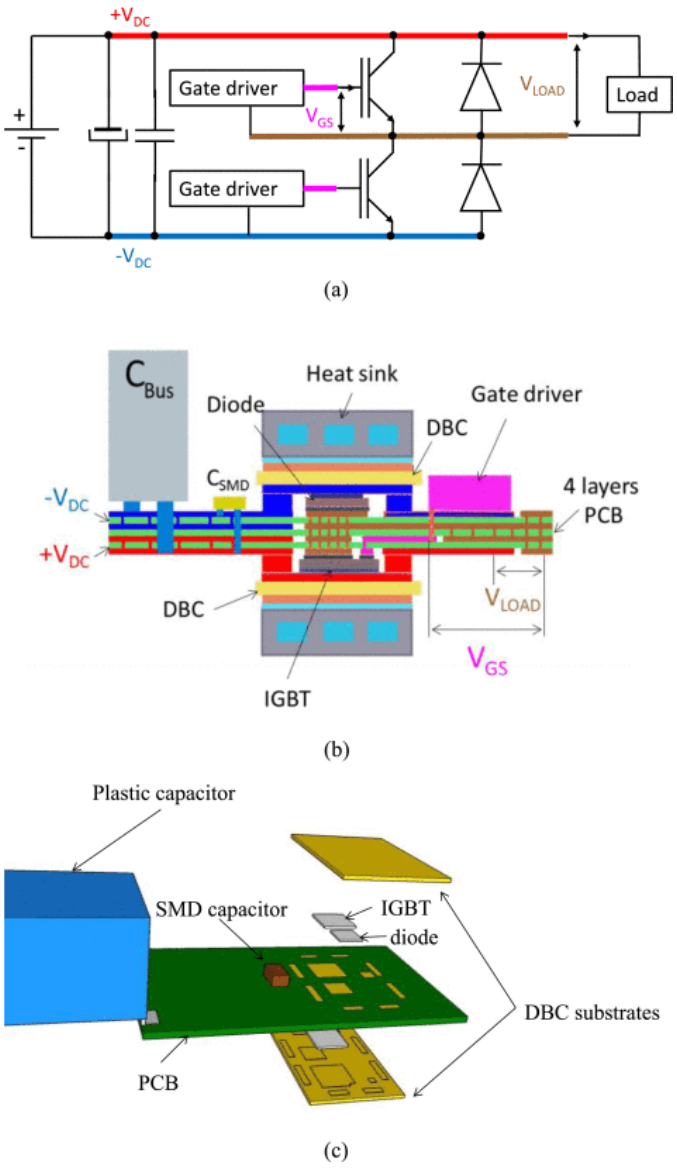

Fig. 1.13 A chip-on-chip packaging technology for IGBT power module [32].

presented. The structure diagram of this package is shown in Fig. 1.14. The power MOSFETs and low-temperature co-fired ceramic (LTCC) inductor were embedded in the top and the bottom PCB, respectively. A stacking of the top PCB and the bottom PCB was implemented to form a 3-D integrated power module. The MOSFETs, gate driver, and passive components were interconnected by the redistribution layer (RDL) and PCB vias. The innovative PCB package technology has advantages such as lighter weight, higher power density, lower parasitic elements, etc.

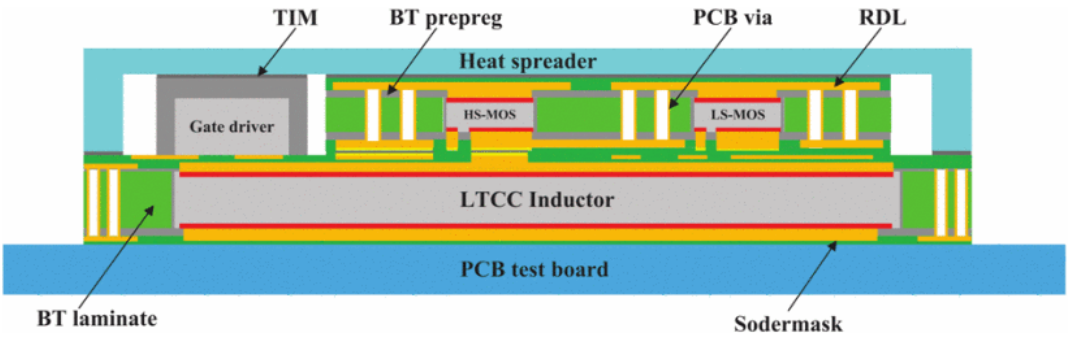

Fig. 1.14 A chip-on-inductor packaging technique with dual sided cooling [33].

Innovative layout design: In [34-35], an innovative layout of traditional wire-bonded IGBT module was proposed. Fig. 1.15 (a) and (b) shows the conventional layout and proposed layout, respectively. Comparing to the conventional module, two devices in the commutation loop of the p-cell and n-cell module were placed at the same side, and thus, the physical length of the commutation loop was reduced. The parasitic inductance

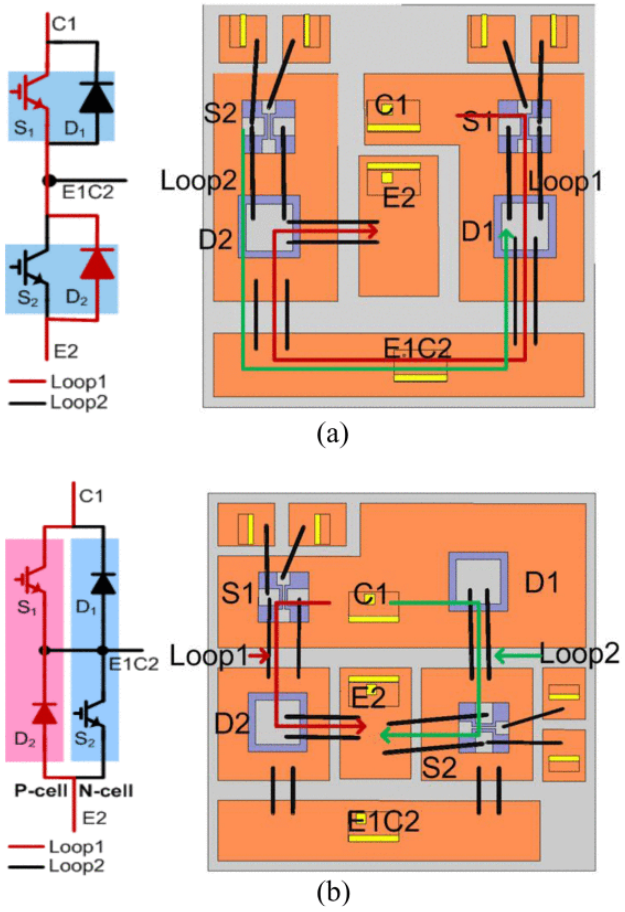

Fig. 1.15 A innovative layout of wire-bonded IGBT module: (a) conventional layout, (b) proposed layout [34].

reduction of the layout design was in the range of 5-10 nH. But the overshoot was decreased only about 10%.

Comparing to the conventional wire-bonded power modules, all of the the above technique can reduce the parasitic inductance to suppress the voltage overshoot. However, the above techniques, such as chip embedded package and 3-D interconnection, are much more complicated than conventional wire-bonded power modules. And the proposed new layout design can only suppress the voltage overshoot a little. Besides, the above methods did not investigate the switching loss and the current overshoot in the turn-on.

1.3 Active gate drivers for suppressing loss and noise

Different ways to suppress the loss, and overshoot generated by dI_c/dt, dV_{ce}/dt, parasitic inductance during switching using active gate drivers have been proposed.

Open-loop methods: these methods add external gate-emitter capacitor, gate-collector capacitor, or use predefined gate currents or voltages to optimize switching waveforms [36-43]. Due to no feedbacks, open-loop AGDs are simple, robust but generally have little flexibility to match IGBT switching operations accurately under various conditions.

In [36], an active clamping circuit for HV-IGBTs was proposed as shown in Fig. 1.16. This active clamping circuit is a combination of the basic Zener diode active clamping scheme and the enlarging Miller capacitor scheme. During the stage when V_{ce} is rising, the active clamping circuit injects current, which is discharged from C_1, into the gate of the HV-IGBT to suppress the falling of gate voltage, and prolong the HV-IGBT's operation time; thus, the decreasing rate of dI_c/dt results in the $V_{overshoot}$ being suppressed. But this method cannot control the turn-on of IGBTs and causes frequent operation of the clamping circuit, thus leading to a large loss is inevitable.

In [39], with a monostable flip-flop adopted in Fig. 1.17, the gate resistance can be changed during the turn-off to suppress the voltage overshoot. In the turn-off of the

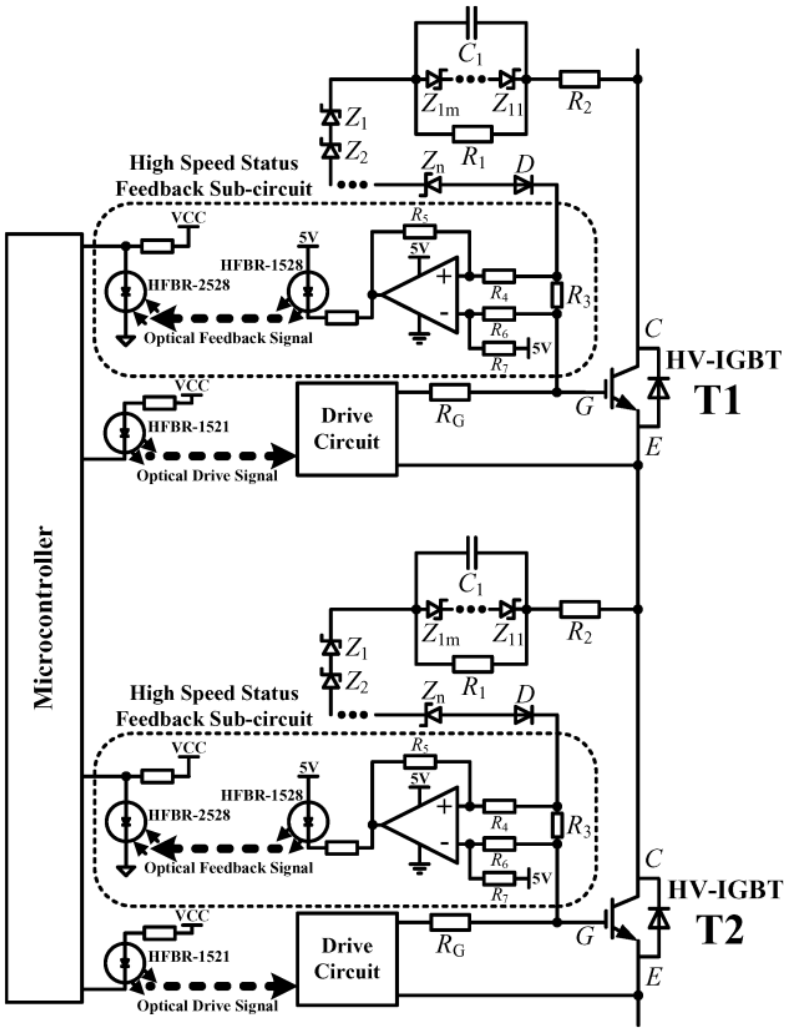

Fig. 1.16 An active clamping circuit, a combination of the basic Zener diode active clamping scheme and the enlarging Miller capacitor scheme [36].

IGBT, the initial gate voltage is high and the turn-off gate resistance is about R_{O2} (R_{O2} is much smaller than R_{O1}) shown in Fig 1.17b and Fig. 1.17c, the turn-off speed of the IGBT is fast and the slope of the V_{ce} is relatively large. However, the large gradient of V_{ce} can be captured by the dV_{ce}/dt sensing circuit to trigger the monostable flip-flop to turn off MN4. The turn-off gate resistor for the IGBT is is changed to R_{O1}. Thanks to the increase of turn-off gate resistance, the turn-off speed of the IGBT is slowed, and the collector current slope dI_c/dt is decreased resulting in small voltage overshoot. After t_3, gate resistance returns to R_{O2}. By using the proposed method, the trade-off between the turn-off loss E_{off} and voltage overshoot can be improved. However, this driver can

only adjust the turn-off operation. And, due to there are only two steps, it cannot control the IGBT more accurately.

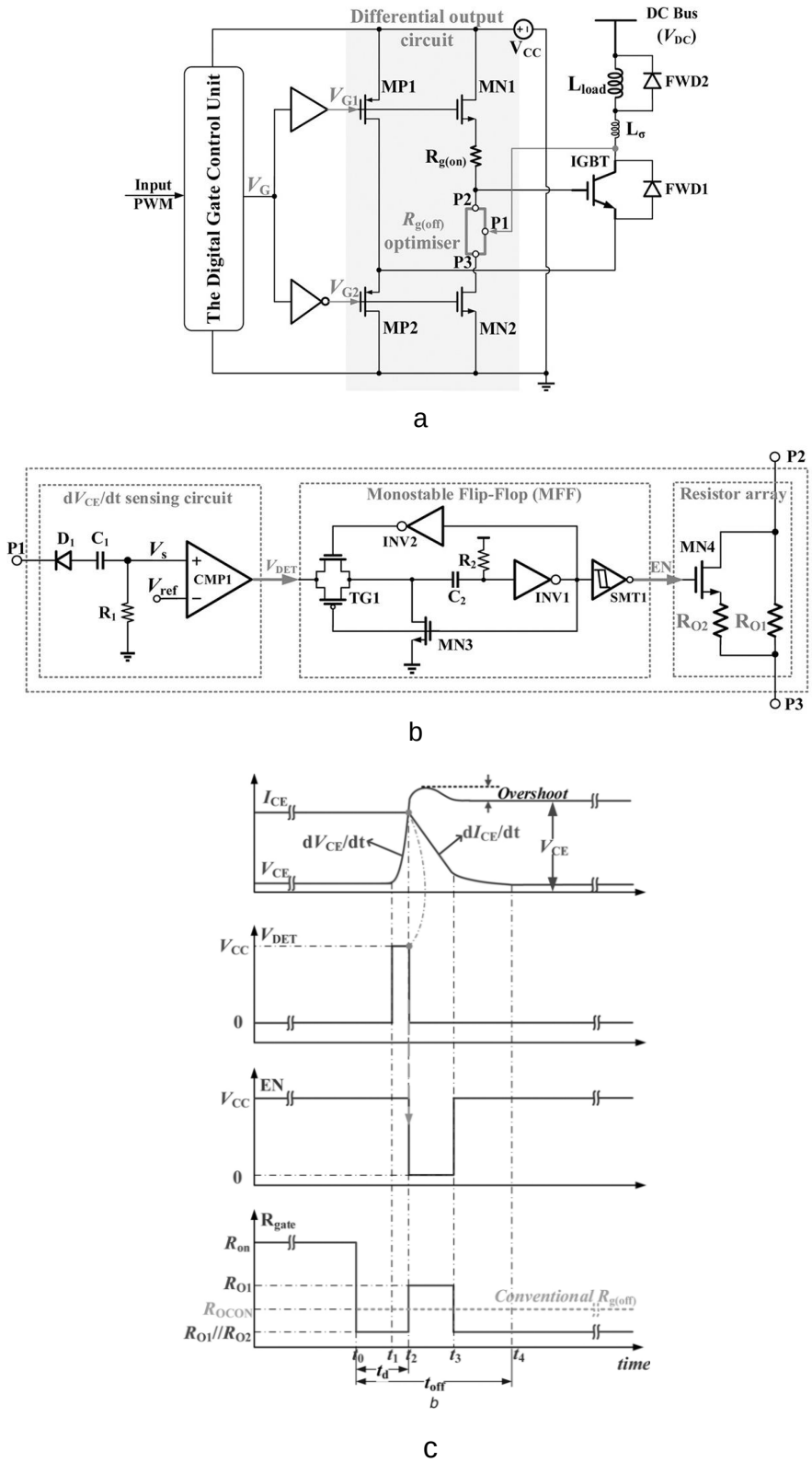

Fig. 1.17 An active gate driver with a monostable flip-flop adopted [39].

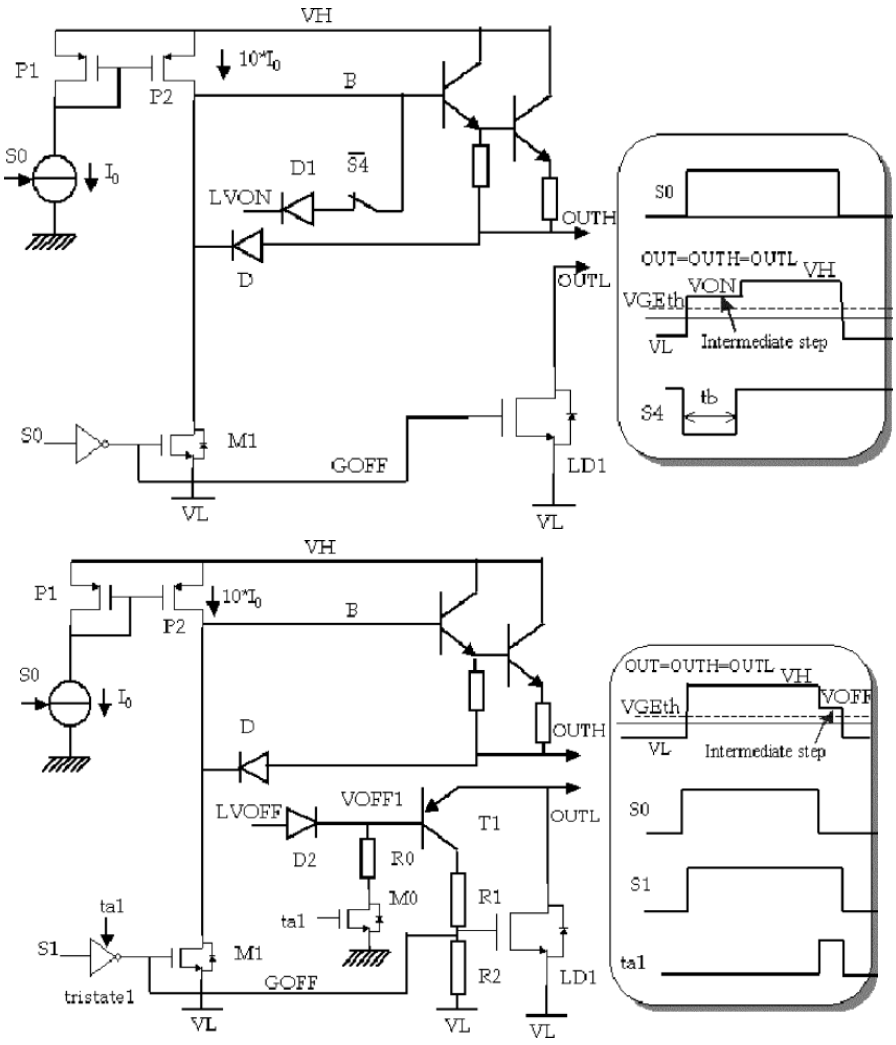

Fig. 1.18 An active gate driver with two-level driving voltages [41].

The driver in [41] applied two-level driving voltages for both turn-on and turn-off as shown in Fig. 1.18. In the turn-on, to protect the IGBT from over-current, risk of latch-up and to limit the EMI, the gate voltage was increased in two separate stages. By increasing the gate to an intermediate stage for a short time before the final turn-on, the IGBT collector current I_c and its slope dI_c/dt were limited. Hence, the peak current due to the diode reverse recovery was reduced. And a similar method was applied to introduce an intermediate stage to suppress the $V_{overshoot}$. However, the switching stages cannot be controlled independently. And the turn-off delay time cannot be controlled.

Closed-loop methods: these methods can identify switching stages and then apply separate drive currents, resistances, or voltages in certain stages, attempting to control transient stages independently [44-52].

In [44], switching behavior adjusted by current sources is proposed in Fig. 1.19: 1) a constant current source to supply large gate drive current based on PWM signal; 2) simple circuits using L_e and C_f to detect the dI_c/dt and dV_{ce}/dt signal; and 3) voltage

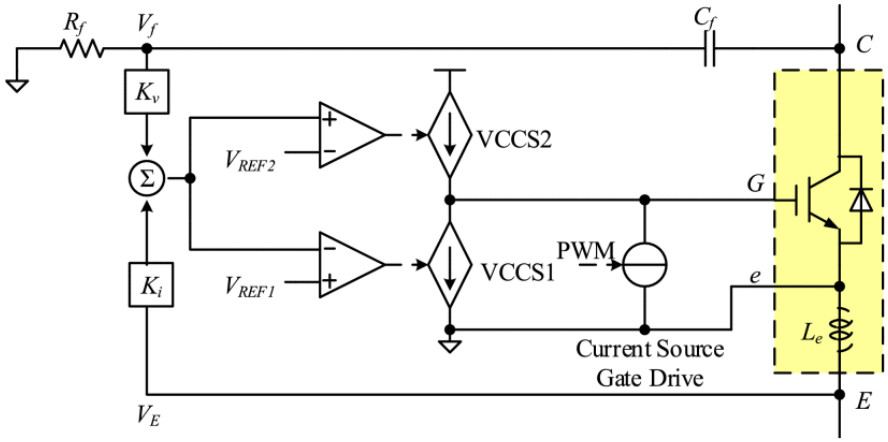

Fig. 1.19 An active gate driver with adjustable current source [44].

controlled current source circuits (VCCS1 and VCCS2) to generate feedback current to the gate terminal. When dI_c/dt or dV_{ce}/dt is detected, VCCS1 or VCCS2 generates extra current to the IGBT gate terminal, which adjusts the net gate drive current and then dI_c/dt and dV_{ce}/dt are controlled. As a result, the $I_{overshoot}$ and $V_{overshoot}$ can be regulated. But this method lacks the ability of online regulating, and three current sources are

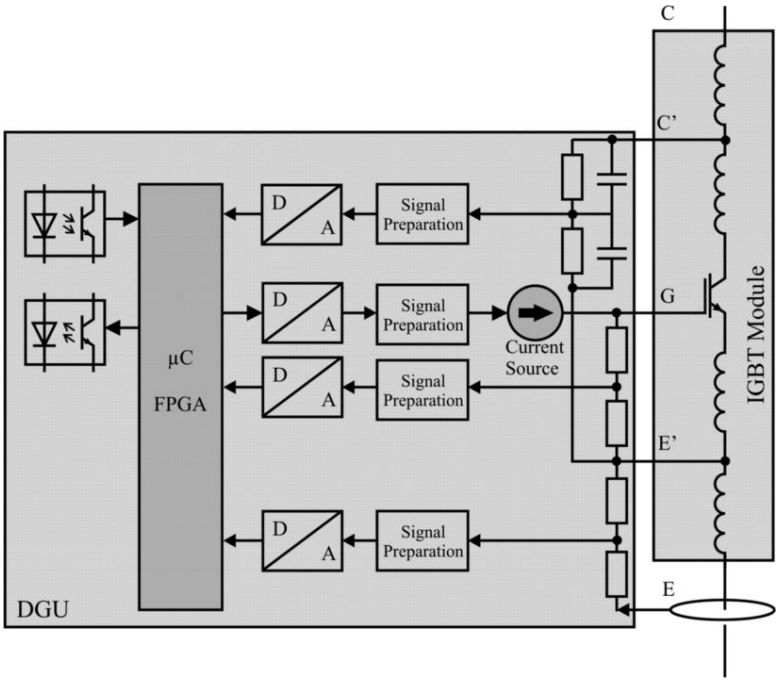

Fig. 1.20 An active gate driver with a field programmable gate array FPGA [47].

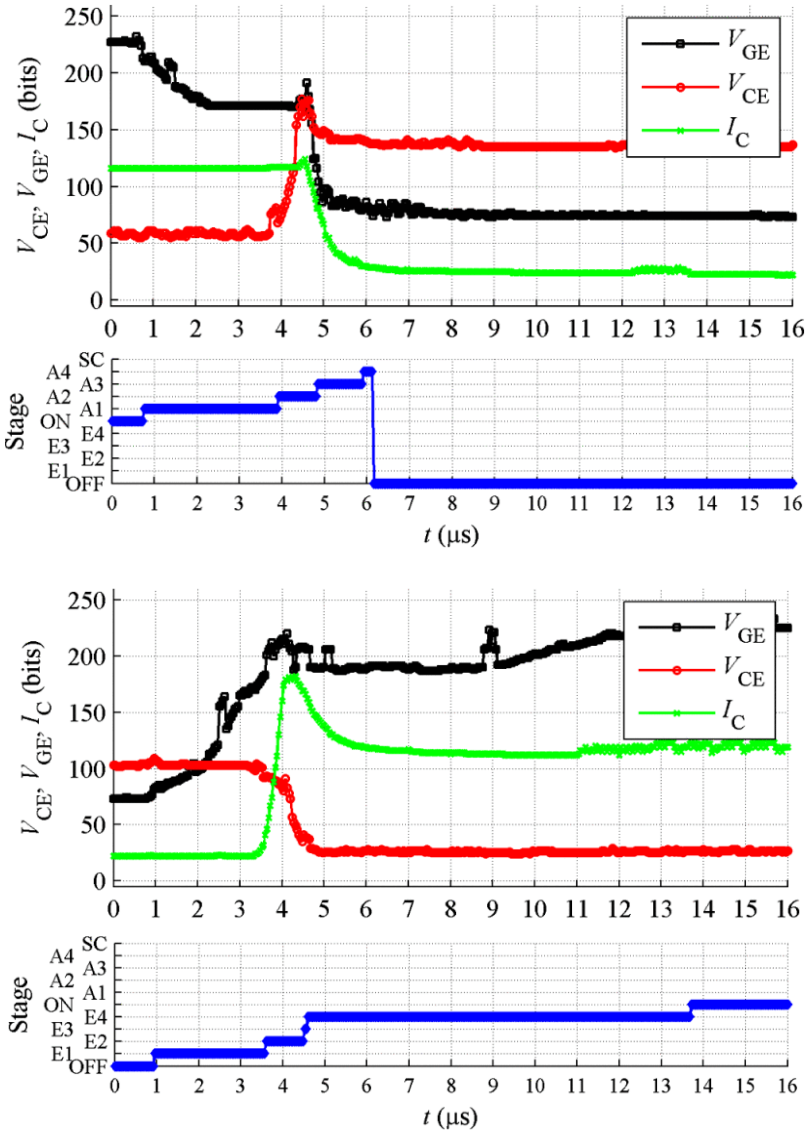

Fig. 1.21 Turn-off and turn-on waveforms that are divided into 4 stages [47].

necessary which results in energy consumption. Furthermore, the driver is almost as large as the IGBT module in the experiment platform leading to difficult integration in the future.

Dang et al. [47] propose an active gate driver with online and individual control for most switching stages by a field programmable gate array FPGA as shown in Fig. 1.20. The gate current is adjusted by resistors and capacitors connected to the IGBT, and the switching operations are divided into four stages for turn-on and turn-off as shown in the Fig. 1.21. Based on the acquired waveforms, the driver identifies the different stages and outputs a gate current command which is constant for each stage. Thus, the

switching transients can be influenced, for instance, the gate current in stage E2 controls the turn-on current slope dI_c/dt, while the gate current in stage A2 controls dV_{ce}/dt during turn-off. As a result, the switching loss can be reduced, but the voltage overshoot cannot be suppressed and the current overshoot even increased a lot. The reason is lacking of the function to control the dV_{ce}/dt in turn-on or dI_c/dt in turn-off.

In [49] and [50], varying amplitudes of PWM signals enable convenient online

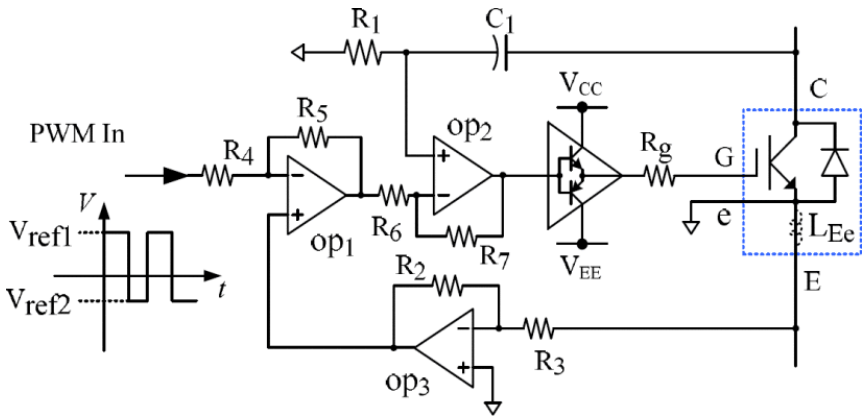

Fig. 1.22 An active gate driver with varying amplitudes of PWM signals [49-50].

switching regulating as shown in Fig. 1.22. During the IGBT turn-on and turn-off transients, a substantial voltage appears across the parasitic inductance, L_{Ee} (shown with a dotted line in Fig. 22). This voltage is linearly proportional to the rate of change of the IGBT collector current, dI_c/dt. and the voltage overshoot. The voltage is measured and adjusted by OP3, and fed to the positive input of OP1. The error between the control input voltage and the measured voltage overshoot is amplified and used to adaptively adjust the IGBT gate drive voltage. The IGBT switching speed can be actively manipulated, and hence the current overshoot and voltage overshoot can be controlled by varying the control input voltage reference, V_{ref1} and V_{ref2}. The experiment results show that voltage overshoot and current overshoot can be reduce a lot, but the switching loss increased to almost ten times of that under the conventional gate driving. It means the tradeoff of switching loss and overshoot cannot be improved. Moreover, dI_c/dt and dV_{ce}/dt are affected by the same signals and independent control is not available.

The above methods have one or more problems as follows:

1) Little flexibility to match IGBT switching operations accurately under various conditions.
2) Cannot control all of the stages during switching operations, such as current and voltage transients, turn-off delay in an accurate behavior.
3) Turn-on and turn-off cannot be controlled independently.
4) Many external components are necessary leading to a large size.
5) Cannot improve the tradeoff relationship of switching loss and voltage/current overshoot.

To solve those problems, a digital gate driver (DGD) is proposed [53-54]. The schematic diagram of the implemented DGD IC is shown in Fig. 1.23. In order to realize programmable 63-level drivability, 63 parallel drivers are connected to the gate of the

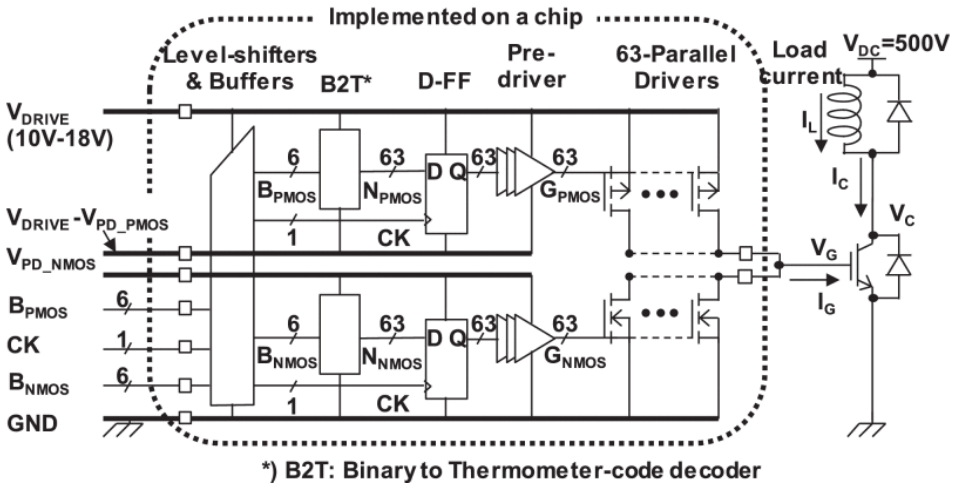

Fig. 1.23 The schematic of the digital gate driver [53].

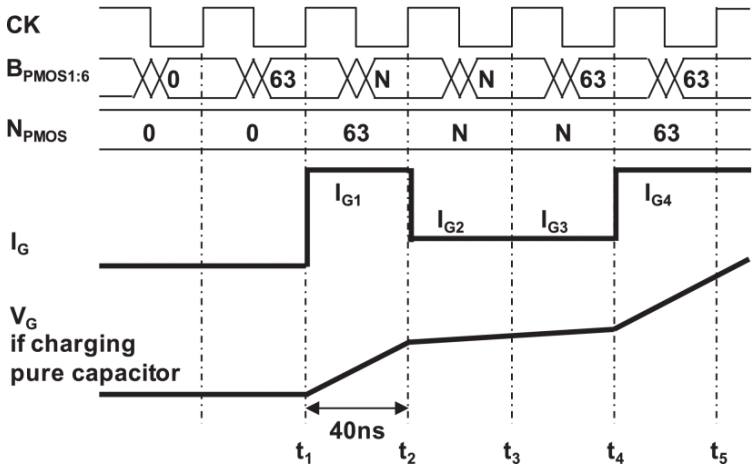

Fig. 1.24 Operation waveforms for 63 PMOS transistors to pull up V_G. [53].

power device and a 6-bit binary control signal, B_{PMOS} (B_{NMOS}), is applied to specify the number of activated P-type-MOS (PMOS) [N-type-MOS (NMOS)] driver transistors, n_{PMOS} (n_{NMOS}). A pair of 6-bit signals (B_{PMOS} and B_{NMOS}) are latched by the clock (CK). CK maximum frequency is 50 MHz and 40 ns time-step control of the drivability is achieved. The power supply voltage V_{DRIVE} DGD IC is 10 - 18 V. The voltage swing of input digital signals (B_{PMOS}, B_{NMOS}, and CK) is 5 V, and the swing is increased to V_{DRIVE} by level-shifters. By adjusting the predriver voltage swing, V_{PD_PMOS} and V_{PD_NMOS}, from 1.2 to 5 V, the output drivability of a single PMOS or NMOS can be tuned from 3 to 80 mA, which corresponds to the maximum gate current I_G from 0.19 A (= 3 mA*63) to 5 A (= 80 mA*63). Fig. 1.24 shows operation waveforms for 63 PMOS transistors to pull up V_G in DGD IC, which is similar to 63 NMOS transistors pulling down V_G. An arbitrary I_G waveform is generated by applying a control bit pattern (B_{PMOS} (B_{NMOS})) in each clock cycle with time-step and digitally specifying time and current pairs of t_i and I_{Gi} (i=1, 2, 3, . . . , *n*).

According to the presented mechanism of the DGD, it can be noted that this driver has a brilliant flexibility (63 levels of gate current for each binary signal) to match different power semiconductor devices (IGBT, MOSFET) with different input capacitance by n_{PMOS} (n_{NMOS}) and binary control signals. And because of the minimum 40 ns time-step, the switching operations can be controlled much more accurately than all of the mentioned drivers. Not only the well-known divided stages can be manipulated, but also more stages can be divided to manipulate the transient thoroughly. And the turn-on and turn-off can be controlled independently by n_{PMOS} and n_{NMOS}. As a result, both of the overshoot and switching loss can be reduced 20% to 46% compared to those under the conventional gate driving. Moreover, the size of main IC chip is only 2.5*2.5 mm^2, which is possible to be integrated into power modules.

1.4 The purpose and thesis organization

As discussed in the former section, new packages of IGBT modules can suppress the voltage overshoot dramatically, but they are much complicated than conventional wire bonded IGBT modules. And they cannot deal with the current overshoot in the turn-on transient. So, it is not enough to suppress the effect of parasitic inductance and improve the tradeoff of voltage/current overshoot and switching loss only by new package schemes. Applying active gate drivers into IGBT modules is proper to accomplish the purpose, especially the DGD []. But, the design of IGBT modules for this DGD has not been proposed. Furthermore, this current source digital gate driver will introduce gate voltage spike. Because the gate current is changed dramatically several times to adjust the switching speed, gate voltage spike is produced by L_g. There is a risk to destroy the digital gate driver IC due to the voltage spike, so the design of IGBT modules should be investigated. To integrate the DGD into the power modules as new type of digital IPM in the future, this thesis focuses on the design requirements of IGBT modules when the DGD is applied.

This thesis is organized as follows.

In chapter 1, the introduction of power modules and active gate driver were presented. And the necessity of designing power modules for the digital gate driver were discussed.

In chapter 2, the design requirements are proposed for half bridge IGBT modules. This chapter clarifies the effect of gate inductance L_g inside IGBT modules on gate voltage spikes when the DGD is employed. Three IGBT modules with different L_g were fabricated to implement double pulse tests by conventional gate driving and three-step digital gate driving to report the clarification of the effect of L_g inside IGBT modules and dI_g/dt on V_{g_spike}. And the change of gate driving vectors Δn, which led to a large change of I_g, is also investigated to show the effect on V_{g_spike}. Moreover, the effects of L_g and Δn on the switching tradeoff characteristics were analyzed to show the necessity of reducing L_g. Furthermore, the origin of the gate voltage spike is discussed by the oscillation of V_{g_spike}.

In chapter 3, the clarification of switching characteristics of power modules with two parallel-connected IGBTs driven by the DGD, which is designed by the previous works. This chapter focuses on the impact of L_g and emitter inductance L_e on V_{g_spike}, current share, and the switching tradeoff characteristics under conventional gate driving and digital gate driving. Five types of IGBT modules with different L_g and L_e were fabricated. Gate driving vectors n and the change of gate driving vectors Δn, which corresponds to large I_g and large transient of I_g respectively were also investigated to show the effect on V_{g_spike}. Moreover, according to the switching characteristics, the design requirements of IGBT modules with two parallel-connected chips are discussed.

In chapter 4, the occurrence mechanism of V_{g_spike} is clarified. The effect of input capacitance of IGBT on V_{g_spike} is clarified by using IGBT modules with the same L_g but different input capacitance. And the effect of DGD output impedance on V_{g_spike} is also clarified by parallel-connected external capacitance C_{ex} and different digital control vectors.

Finally, the chapter 5 summarizes the whole thesis. The design requirements of IGBT modules applying the DGD is proposed, and can be taken as fundamentals for integrating the DGD into IGBT modules in the future.

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CHAPTER 2. Design for power modules with one IGBT chip

2.1 Background

As the pioneer for the future plan of integrating the digital gate driver into power modules, the thermal performance is necessary to implement for safety. As usual, the maximum junction temperature of IGBT is about 150 ~ 200 ℃, but the maximum junction temperature of digital gate driver IC is only about 85 ~125 ℃. So, when the IC is integrated into IGBT modules, it is essential to set an enough distance away from IGBT chip to prevent thermal destruction.

Because the operation mechanism of the DGD is dynamically controlling the gate driving current during the switching transients, the transient change of gate current I_g will become complicated and aggressive, so V_{g_spike} is generated and have a risk to destroy the DGD [1-5]. As shown in Fig. 2.1 and Fig. 2.2 [5], the tradeoff of switching loss and overshoot was improved both in turn-off and turn-on, but there is a large V_{g_spike} as the n_{NMOS} and n_{PMOS} changed. Because the timing of V_{g_spike} corresponds to the change of digital control vectors, which means I_g is pulled up or pulled down [1-5], it can be expected that V_{g_spike} results from the coupling of dI_g/dt and gate inductance L_g inside IGBT power modules. In previous works, although the relation between current charge and stray inductance of the main circuit loop inside power modules at conventional gate driving for suppressing the collector voltage surge was reported [6-7], gate inductance design of IGBT module for DGD have not been investigated.

This chapter reports an experimental clarification of the effect of L_g inside IGBT modules and dI_g/dt on V_{g_spike}. Three IGBT modules with different L_g were fabricated, and the change of gate driving vectors Δn, which led to a large change of I_g, was also investigated to show the effect on V_{g_spike}. Moreover, the effects of L_g and Δn on the switching tradeoff characteristics were analyzed to show the necessity of reducing L_g.

Furthermore, the origin of the gate voltage spike is discussed by the oscillation of V_{g_spike}.

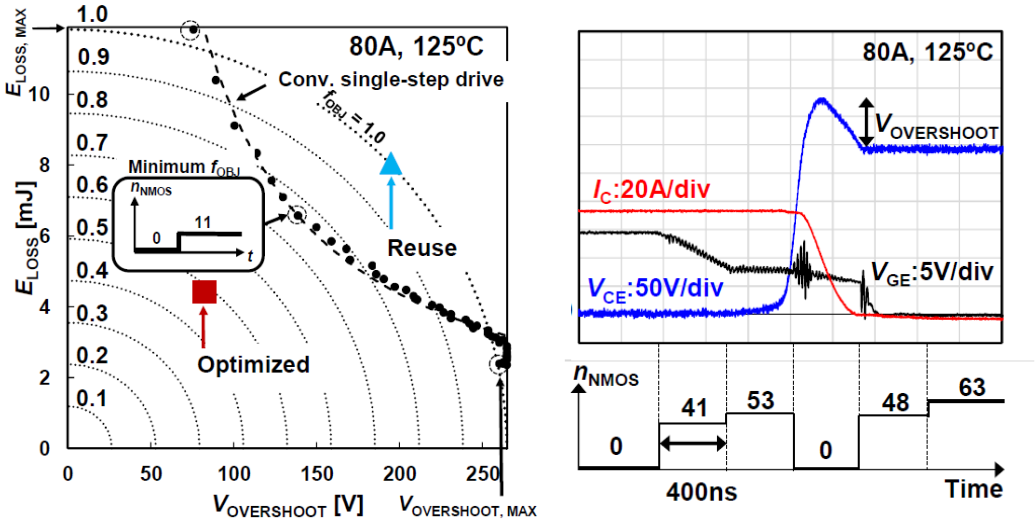


Fig. 2.1 The tradeoff of $V_{overshoot}$ and E_{off}; the turn-off waveforms.

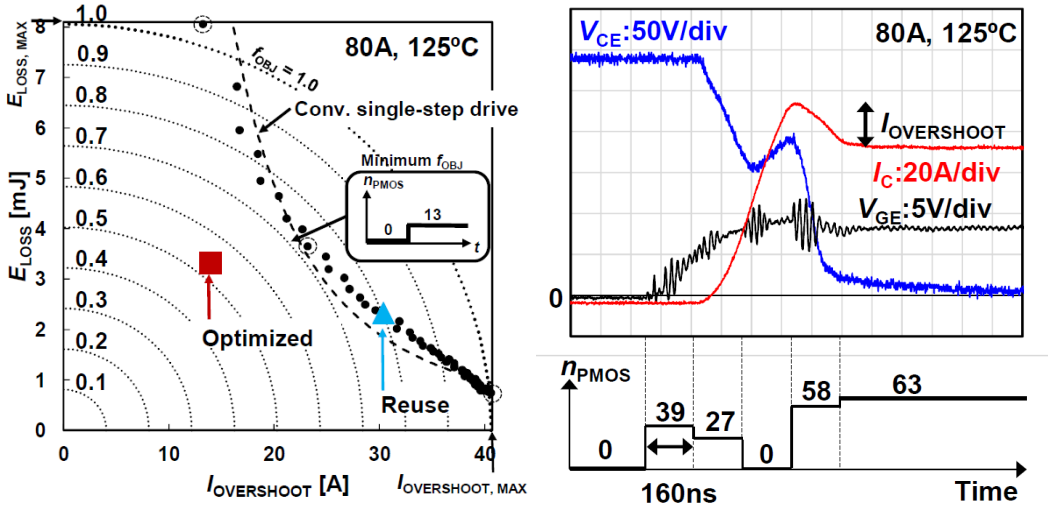


Fig. 2.2 The tradeoff of $I_{overshoot}$ and E_{on}; the turn-on waveforms.

2.2 Thermal simulation for IGBT modules and the digital gate driver

Figure 2.3 shows the schematic cross face of power modules, heat transfers from IGBT to IC through other components under the IGBT and bonding wires. And the module is cooled by the baseplate. T_{j_IGBT}, T_{j_IC}, T_c are junction temperature of IGBT

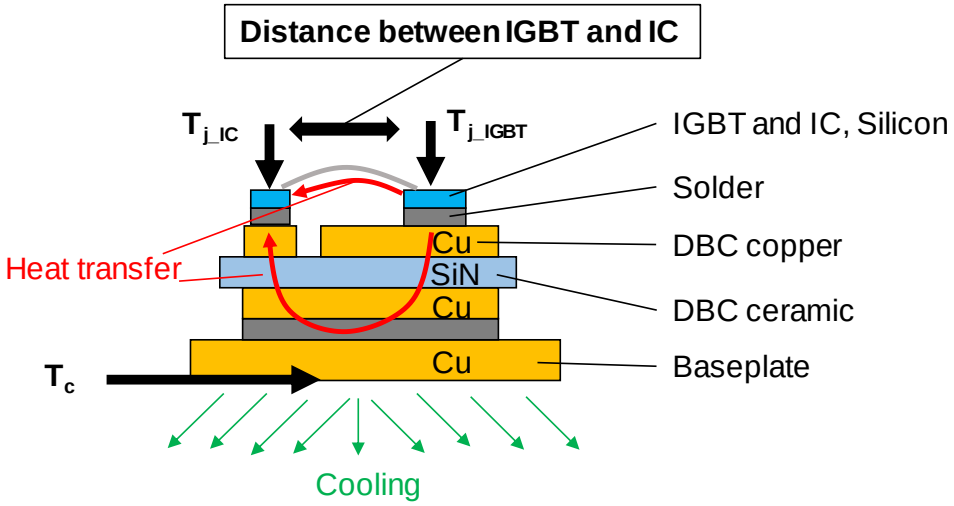


Fig. 2.3 The schematic cross face of power modules.

Table 2.1 Materials of different components of power modules

Material	Thermal conductivity (W/mK)	Heat capacity (J/kgK)	Density (kg/m3)
Si (IGBT, IC)	139	729	2340
Solder	73.2	226	7300
Copper	397	386	8960
SiN (DBC ceramic)	85	680	3220
Al (wires)	238	900	2700

chip, junction temperature of IC, and case temperature, respectively. Materials of components and characteristics that used in the simulation are shown in Table 2.1. All of the surfaces are set as isolation except the bottom face. The power source is inputted into the IGBT chip for 60 s, then cooled for 60 s. and the initial temperature is 25 ℃. The simulated temperature changes and distribution as the distance between IGBT and IC is 10 mm are shown in Fig. 2.4 and Fig. 2.5. T_{j_IGBT} was increased to 473 K (200 ℃),

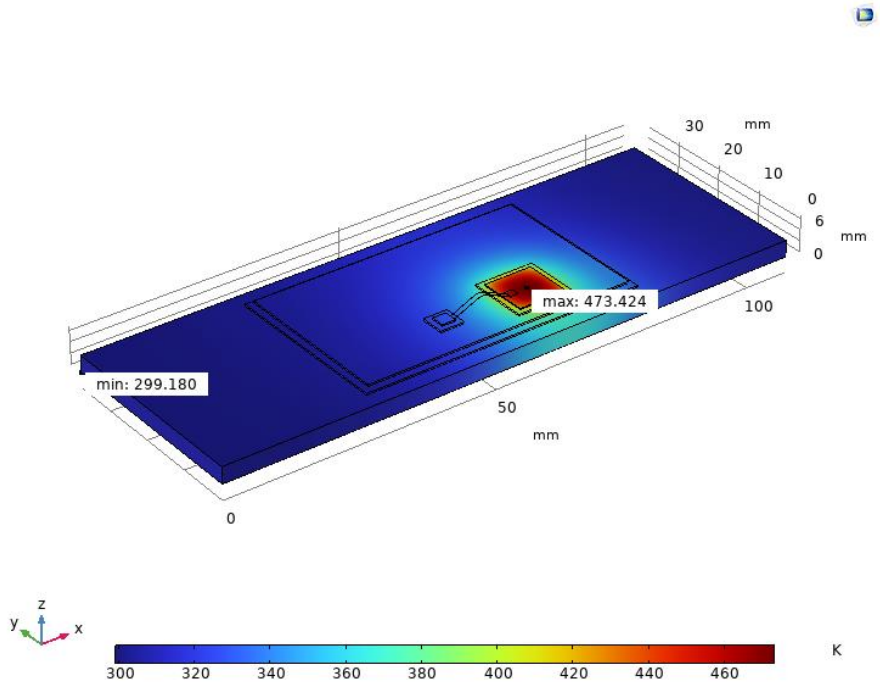


Fig. 2.4 The temperature distribution of power modules.

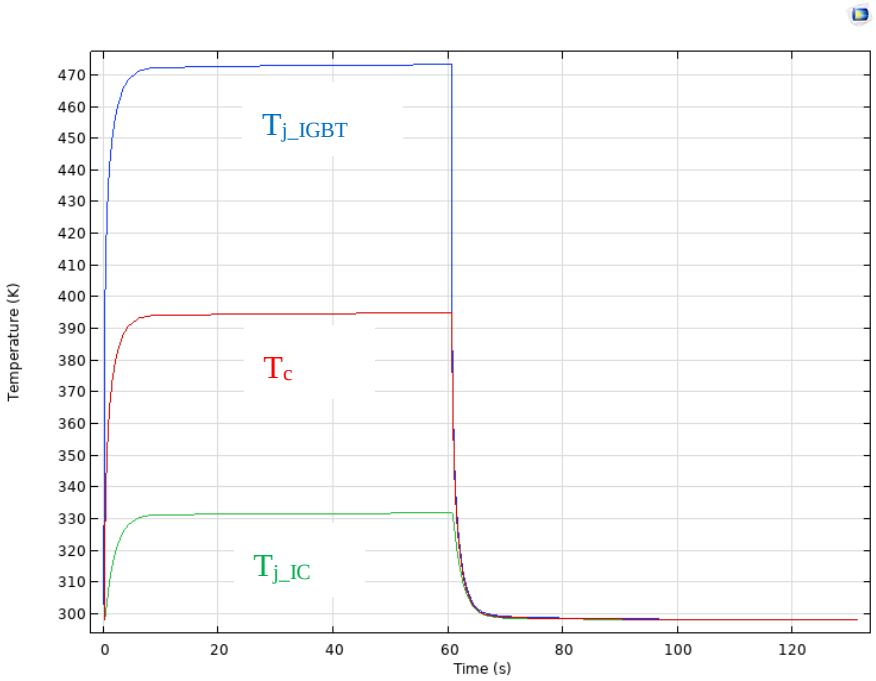


Fig. 2.5 The temperature of IGBT, digital gate driver IC, and power module case.

but T_{j_IC} was only 332 K (59 ℃) . It is obvious that the IC is safe under this condition. By changing the distance between IGBT and IC, the T_{j_IC} were plotted in Fig. 2.6. It is indicated that when the distance is more than 4 mm, T_{j_IC} does not reach 85 ℃. 4 mm is almost the minimum distance that can be used to integrate it into IGBT modules

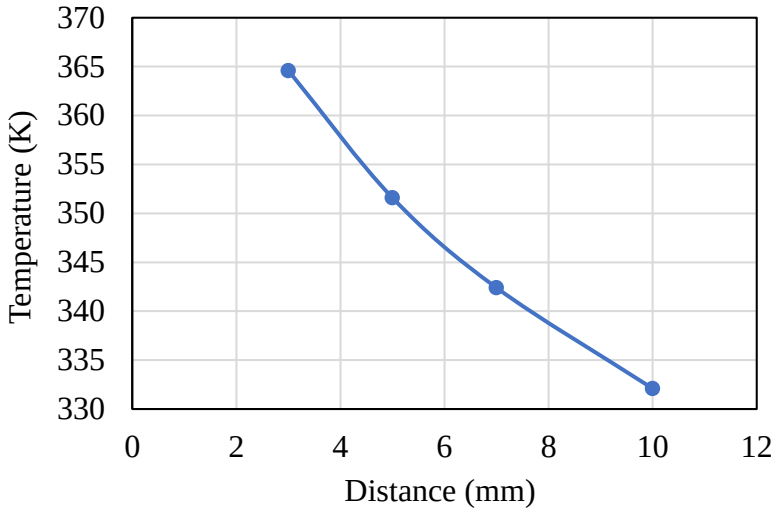


Fig. 2.6 The relationship of distance and $T_{j\text{-}IC}$.

considering other components, such as DBC boards and isolation gaps. Therefore, IC will not break down due to the thermal transferred from IGBT. So, following contents will focus on the influence of parasitic inductance.

2.3 The design of IGBT modules and double pulse tests

Three IGBT modules, whose breakdown voltage was 680V and rated current was 200A, with different L_g were fabricated. By applying different diameters and lengths of wires connecting IGBT chip and gate terminals, different L_g could be realized and the values were estimated by COMSOL Multiphysics. Fig. 2.7 shows the layout and model of IGBT modules. To realize different L_g, the IGBT was set up three different positions A, B, and C. To verify the validity of the calculated results, the inductance of parallel positioned two straight wires as shown in Fig. 2.8 considering mutual inductance was calculated by equations as followed [8],

$$L_{wire} = \frac{\mu_o \mu_r L}{\pi} \cosh\left(\frac{S}{D}\right)^{-1} \quad (1)$$

where S is spacing between conductors, D is conductor diameter, L is length of conductor, magnetic permeability in vacuum μ_o is $4\pi*10^{-7}$ H/m, and the μ_r is relative

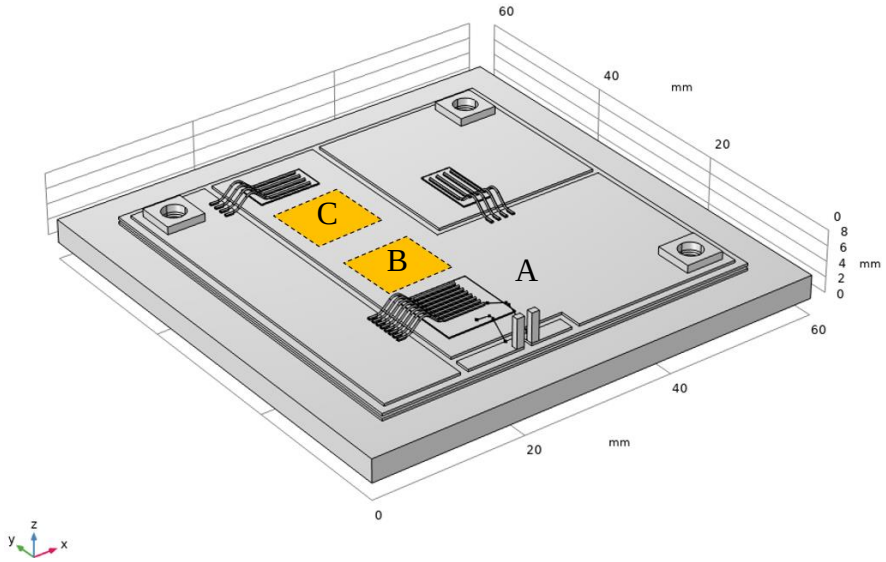


Fig. 2.7 The layout and 3D model of designed IGBT modules.

magnetic permeability. Table 2.2 shows the dimensions of gate wires and calculated L_g by two methods. The calculated results by two methods are similar, and the small difference is because of the equation in [8] is for straight wires specially. Therefore, the L_g calculated by COMSOL is verified.

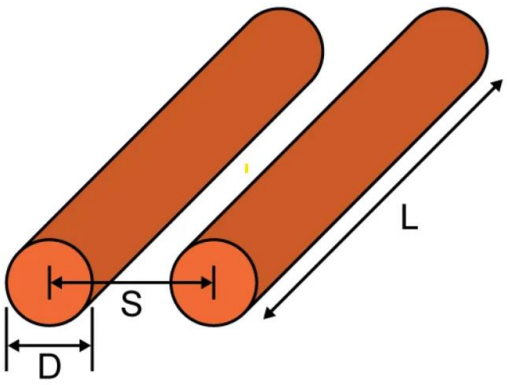


Fig. 2.8 Two wires for inductance calculation by [8].

Fig. 2.9 shows a photograph of Sample-B. The half-bridge circuit is a basic configuration of the power electronics circuit. In this work, the high-side IGBT was omitted from the half-bridge circuit, because the module was designed specifically for evaluating the switching characteristics of the low-side IGBT. Therefore, the results of this verification can also be applied to power electronics circuit design. Fig. 2.10 is the measured capacitance characteristics of the IGBT chip. C_{ge} was 8 nF, and C_{gc} was 0.28 nF at V_{ce} = 20 V.

Table 2.2 The dimension of gate wires and calculated L_g.

Sample	Wire length (mm)	Wire diameter (μm)	L_g by COMSOL (nH)	L_g by [5] (nH)
A	5, 7	300	7	6
B	22, 24	300	28	28
C	32, 34	50	54	49

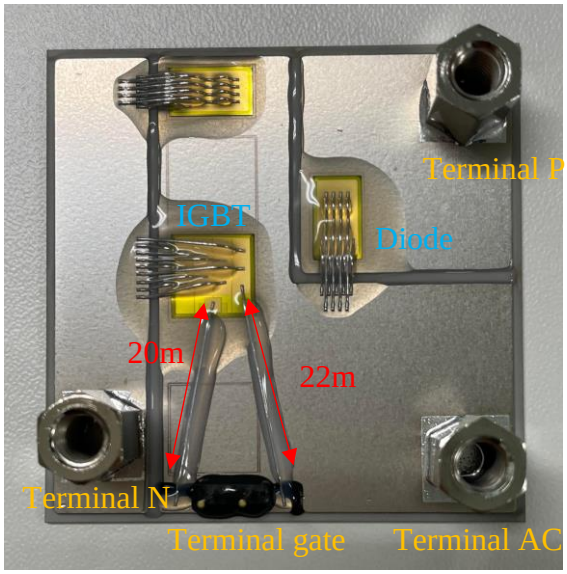


Fig. 2.9 The photograph of Sample-B.

Fig. 2.11 shows the circuit schematic for the double pulse test to measure the turn-on and turn-off characteristics of the above IGBT modules. Fig. 2.12 shows the photo of the experiment setup. To minimize the parasitic inductance of connecting wire, the digital gate driver was connected to the IGBT module directly by a terminal rather than wires. The stray inductance of the connection terminal was about only 2 nH, which was estimated by COMSOL. So, the parasitic inductance of the connecting part was negligibly small. The L_g in Fig. 2.11 represents the gate inductance inside IGBT modules. The measurement system included a 6-bit programmable DGD. To realize a programmable 63-level drivability in the programmable digital gate driver, 63 parallel transistors were connected to the gate of IGBT and a 6-bit control signal was plied to specify the number of activated NMOS and PMOS transistors n_{NMOS} and n_{PMOS} [1], [10].

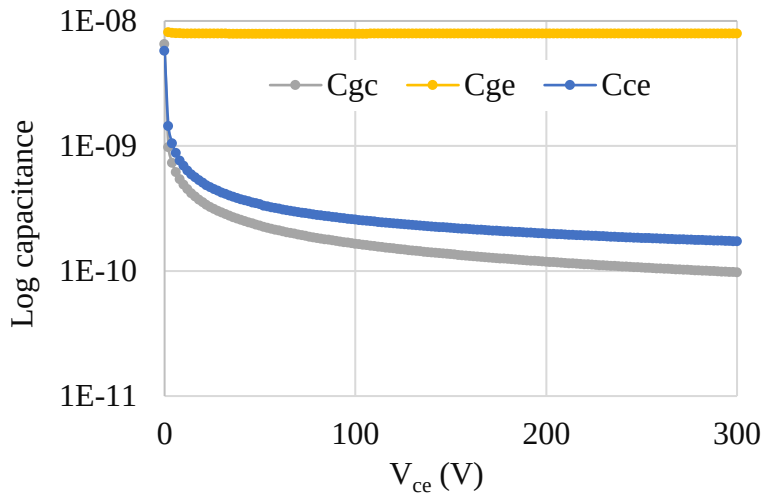


Fig. 2.10 The measured stray capacitance in IGBT chip.

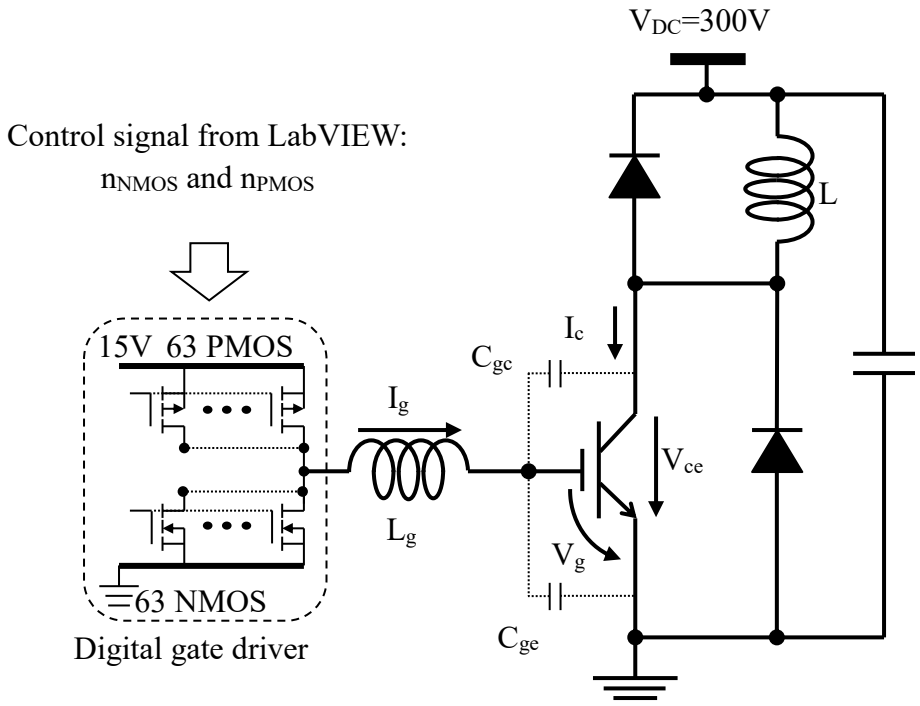


Fig. 2.11 Circuit schematic of experiment.

Current source three-step active gate drivers were proposed by previous papers [2-4]. Based on the same operation mechanism, the gate driving method was proposed as follows. Fig. 2.13 presents the turn-off and turn-on waveforms by the conventional gate driving without the digital gate control. The DGD output current I_g can be increased with n_{NMOS} and n_{PMOS} and controls turn-off and turn-on switching speeds. A constant of the n_{NMOS} or n_{PMOS} corresponds to the conventional gate driving shown in the figure. In this work, n_{NMOS} and n_{PMOS} were set to an integer from 5 to 63 to implement double

Fig. 2.12 The photo of experiment setup.

pulse tests without digital gate control. Voltage overshoot $V_{overshoot}$ in the turn-off period and current overshoot $I_{overshoot}$ in the turn-on period were defined as shown in Fig. 2.13a and Fig. 2.13b.

In the digital gate control, the n_{NMOS} and n_{PMOS} were set to three different values at each period *n1*, *n2*, and *n3* in the whole turn-off and turn-on stages as shown in Fig. 2.14. The *n1*, *n2*, and *n3* were also set to integers from 5 to 63. The V_{g_spike} was the change of V_g after the vector was changed from *n1* to *n2* as shown in Fig. 2.14a. Tables 2.3 and Table 2.4 show vectors employed in this chapter for turn-off and turn-on

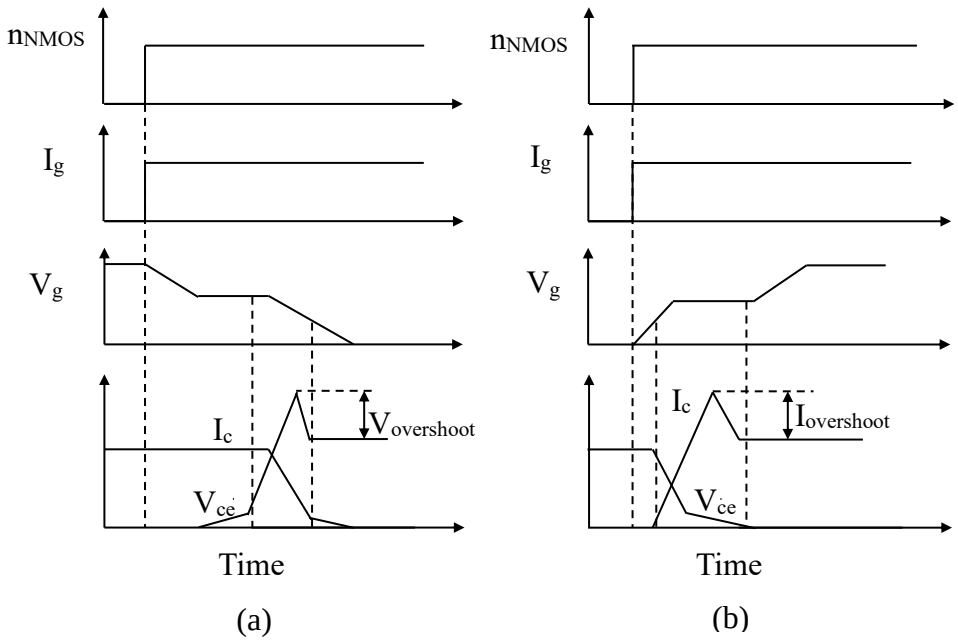


Fig. 2.13 (a) Turn-off and (b) turn-on waveforms by conventional gate driving without digital gate control.

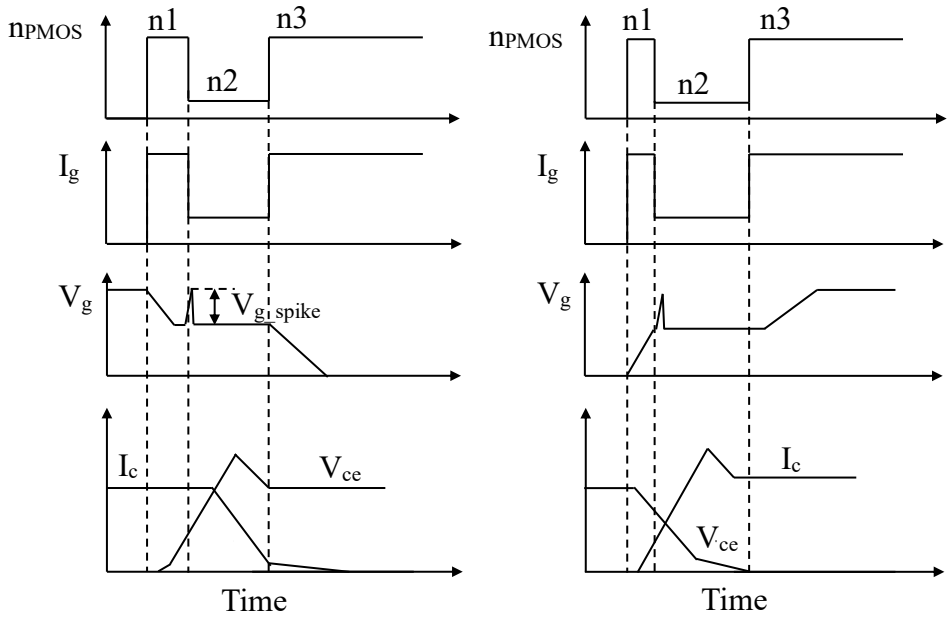


Fig. 2.14 (a) Turn-off and (b) turn-on waveforms with digital gate.

switching with digital gate control. In the turn-off waveform without digital gate control shown in Fig. 2.13a, the V_{ce} rises gradually when the I_c is still the load current, which results in energy loss in this stage. In the digital gate control of Pattern-a, the *n1* was set as the maximum of 63 to shorten the stage before I_c started to decrease. In the I_c

Table 2.3 Vectors employed in this chapter for turn-off.

Digital control pattern		n1	n2	n3
a	n_{NMOS}	63	5	63
		63	8	63
		63	10	63
		63	20	63
	Time (ns)	240	480	/
b	n_{NMOS}	20	5	63
		20	8	63
		20	10	63
		20	15	63
	Time (ns)	640	320	/

Table 2.4 Vectors employed in this chapter for turn-on.

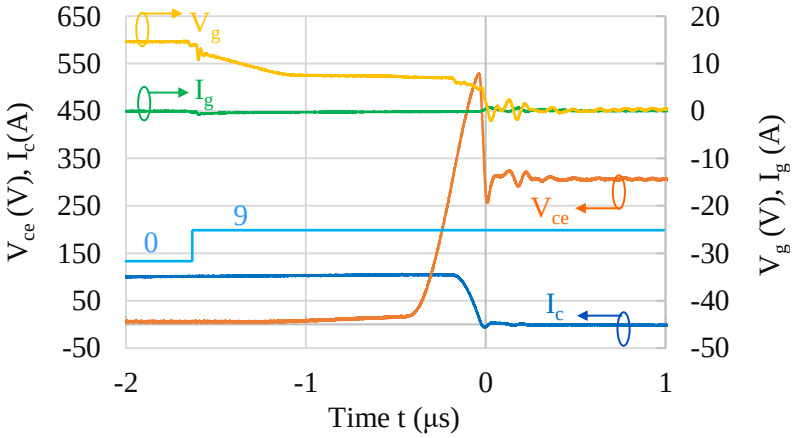
Digital control pattern		n1	n2	n3
a	n_{PMOS}	63	5	63
		63	8	63
		63	10	63
		63	20	63
	Time (ns)	80	480	/
b	n_{PMOS}	20	5	63
		20	8	63
		20	10	63
		20	15	63
	Time (ns)	320	320	/

decreasing stage, a large $V_{overshoot}$ occurs due to the large dI_c/dt, so the *n2* should be set as a small value to slow down the dI_c/dt. After that, the main stages correlated with $V_{overshoot}$ and E_{off} are almost passed, so the *n3* was set as 63 to complete the turn-off as soon as possible. In contrast, digital gate control Pattern-b, where *n1* was set as 20, was proposed to compare to Pattern-a to show the effect of Δn. The setup of vectors shown in Table 2.4 for turn-on was similar to that for the turn-off. To shorten the delay time during turn-on shown in Fig. 2.13b. *n1* was set as 63. And *n2* was set as 5 in Pattern-a to slow down the change of V_{ce} to decrease the $I_{overshoot}$. As same as Pattern-a, *n3* was set as 63 to complete the turn-on switching with a large voltage slew rate.

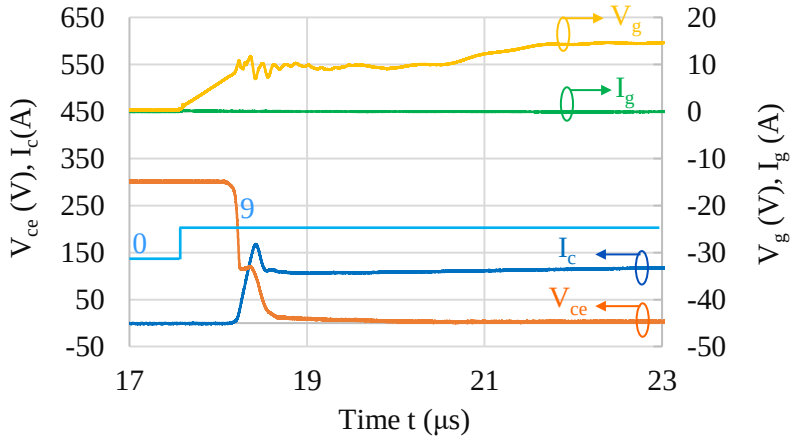
And the control signals of the DGD were generated by PXIe-5670 module in Fig. 2.12. The range of gate voltage was from 0 V to 15 V. In addition, the experiment system was operated under a supply voltage of 300 V and a load current of 100 A.

2.4 Results and discussion

Fig. 2.15 shows typical switching waveforms by conventional gate driving of Sample-C, whose L_g was 54 nH when n_{NMOS} and n_{PMOS} were set as a constant value of 9 in turn-off and turn-on periods. n_{NMOS} and n_{PMOS} were 0 before switching and then



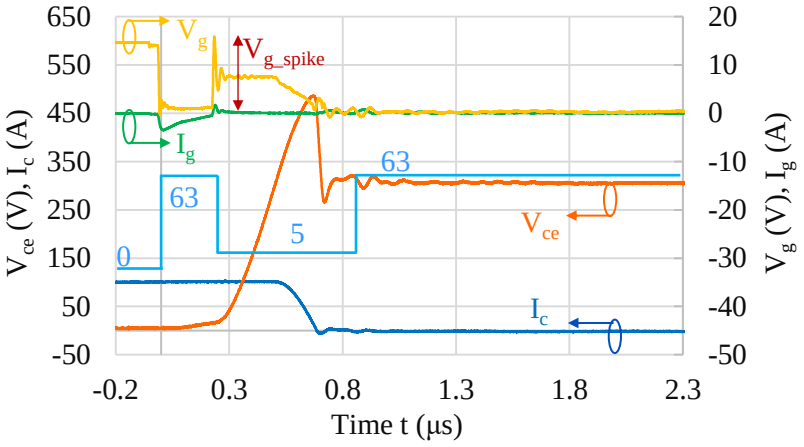
(a)



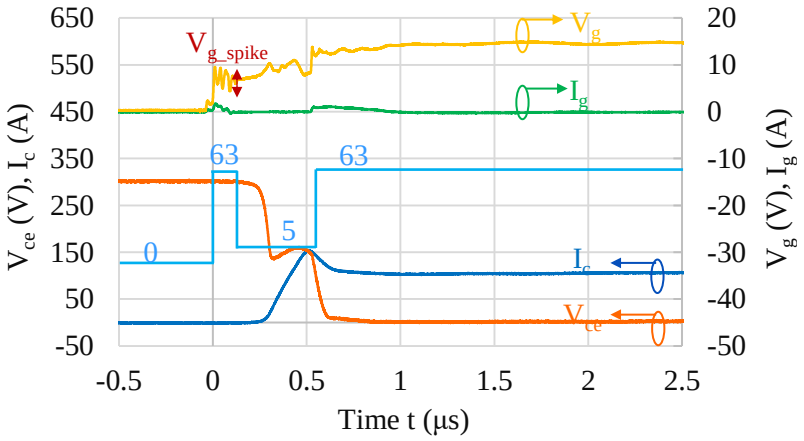
(b)

Fig. 2.15 (a) Turn-off and (b) turn-on waveforms without digital gate control when n_{NMOS} and n_{PMOS} were set as 9 for Sample-C.

rose to 9 during the switching period. Under this condition, $V_{overshoot}$ was 229.0 V and $I_{overshoot}$ was 68.1 A. The E_{off} and E_{on} were 8.9 mJ and 5.1 mJ, respectively. Fig. 2.16 shows the waveforms of Sample-C under the digital gate control of Pattern-a. In the turn-off period, the n_{NMOS} was pulled up to *n1* of 63 from 0 to start the turn-off, then n_{NMOS} was pulled down to *n2* of 5. Finally, the n_{NMOS} was kept as *n3* of 63 to complete



(a)

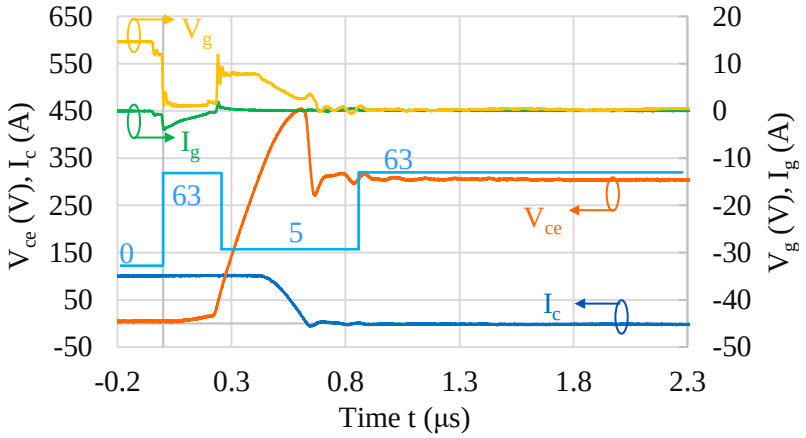


(b)

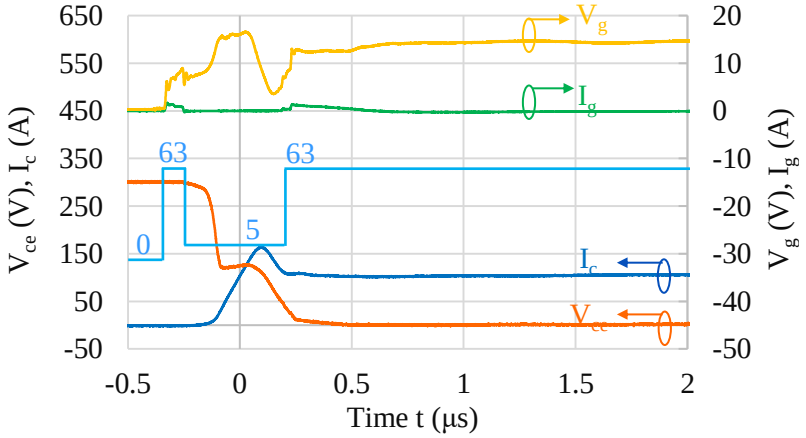
Fig. 2.16 (a) Turn-off and (b) turn-on waveforms with digital gate control Pattern-a for Sample-C.

the turn-off and keep the off-state. In the turn-on period, gate driving vectors were the same as in the turn-off, except for the corresponding time duration. Under this digital gate control, $V_{overshoot}$ and $I_{overshoot}$ were 188 V and 53.3 A. E_{off} and E_{on} were 8.4 mJ and 4.6 mJ. Compared to conventional gate driving without digital gate control, the $V_{overshoot}$ and $I_{overshoot}$ were reduced clearly, while the switching loss was almost kept at the same level. In addition, at the time when *n1* was pulled down to *n2*, which led to a large transient gradient of I_g, and large V_{g_spike} of 14.5 V was shown in the turn-off. In contrast, The V_{g_spike} in turn-on was small as 4.7 V because the I_g was smaller compared to that in the turn-off due to the difference of on-resistance between PMOS and NMOS transistors in DGD.

Fig. 2.17 shows the waveforms of Sample-A, whose L_g was 7nH, under the same digital gate control of Pattern-a in Fig. 2.16. Comparing to the results of Sample-C in Fig. 2.16, the V_{g_spike} in turn-off decreased to 10.3 V, and the V_{g_spike} in turn-on decreased to 2.9 V. It is obvious that the V_{g_spike} can be suppressed by reducing the L_g.



(a)

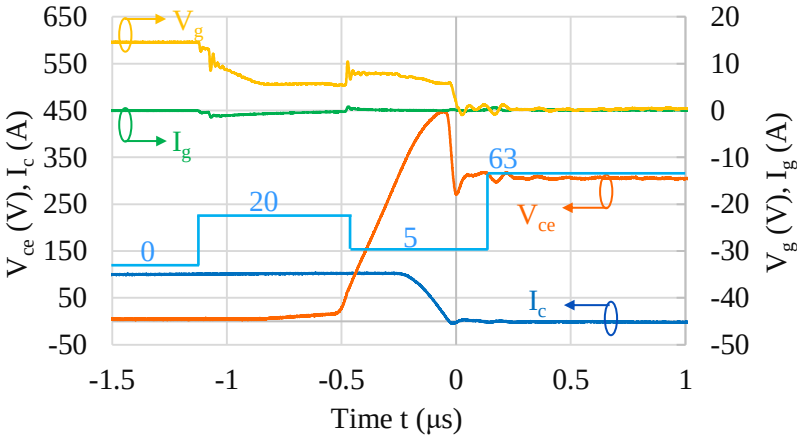


(b)

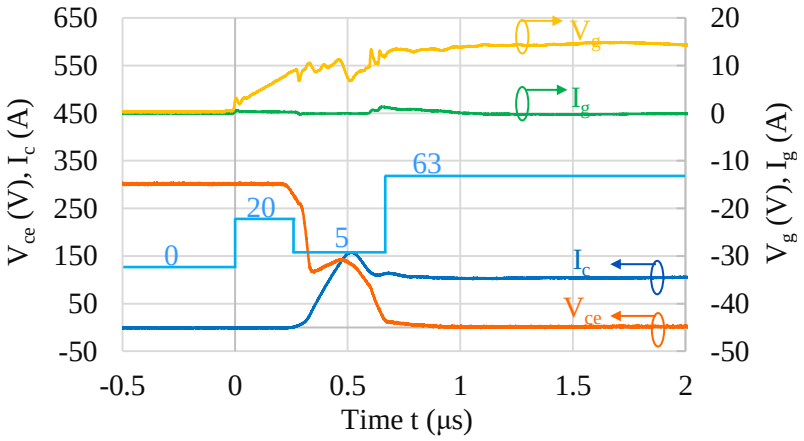
Fig. 2.17 (a) Turn-off and (b) turn-on waveforms with digital gate control Pattern-a for Sample-A.

Fig. 2.18 shows the waveforms of Sample-C under digital control of Pattern-b, in which *n1* was set as 20. Because of a smaller Δn than that in Fig. 2.16, the dI_g/dt became smaller. The V_{g_spike} in turn-off decreased to 4.5 V, and the V_{g_spike} in turn-on decreased to 3.9 V. It indicates that reducing Δn can also be an alternative to suppress V_{g_spike}.

The tradeoff between E_{off} and $V_{overshoot}$ in the turn-off switching and the tradeoff between E_{on} and $I_{overshoot}$ in the turn-on switching were improved by digital gate control



(a)



(b)

Fig. 2.18 (a) Turn-off and (b) turn-on waveforms with digital gate control Pattern-b for Sample-C.

compared to conventional gate driving as shown in Figs. 2.19 and 2.20. Because small vectors make the IGBT switching at a slow speed, the dI_c/dt and dV_{ce}/dt become smaller resulting in the overshoot being suppressed. However, due to the long switching period, switching loss increases. Therefore, the tradeoff relationship was shown in both turn-off and turn-on switching characteristics. In Fig. 2.19, both two digital control patterns improved the tradeoff. The loss in digital control Pattern-a obtained lower power loss than that in Pattern-b. It is because the time before V_{ce} began to rise at a large rate in Fig. 2.16a was about only half of that in Fig. 2.18a. In Fig. 2.20, the results also prove that both the two digital control patterns improved the tradeoff, and the improvement

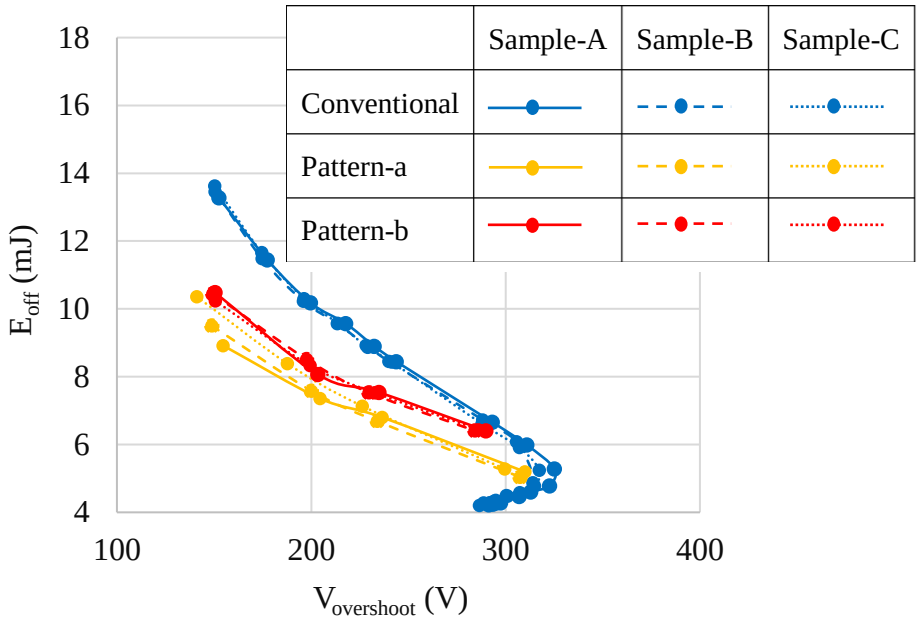


Fig. 2.19 Tradeoff between E_{off} and $V_{overshoot}$ improved by digital gate control.

was almost the same under the two patterns. It is because E_{on} and $I_{overshoot}$ were determined mainly by *n2* in the second period.

The tradeoff characteristics were almost independent of the L_g as shown in Fig. 2.19 and 2.20. It is verified that the tradeoff characteristics were determined mainly by the stray inductance in the main circuit loop L_e and L_c, and the gate drive signal was applied to the IGBT chip normally even at large L_g conditions. The tradeoff curve of Pattern-b

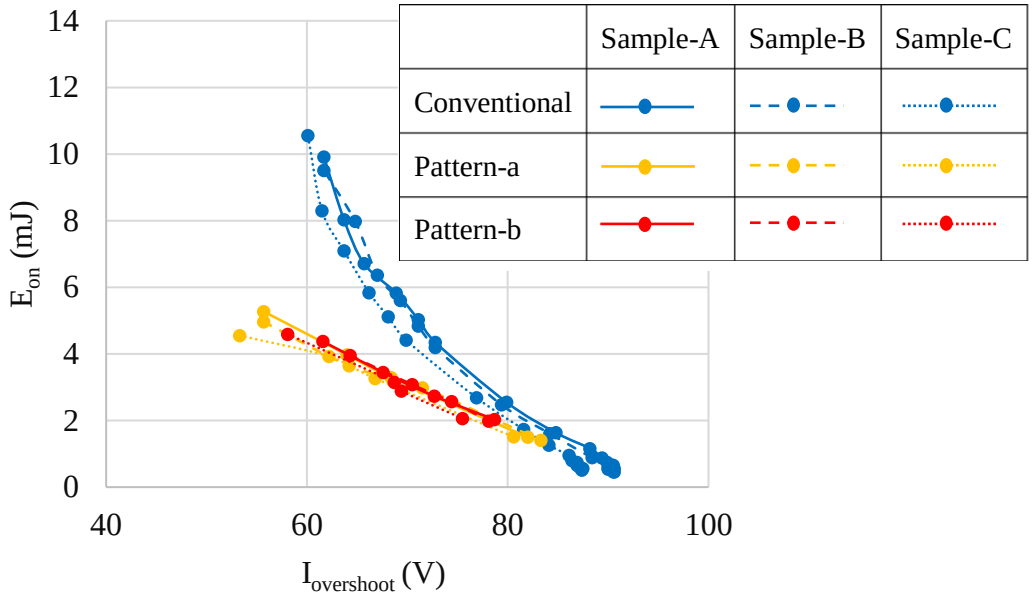


Fig. 2.20 Tradeoff between E_{on} and $I_{overshoot}$ improved by digital gate control.

for Sample-C was slightly different from those of Sample-A and Sample-B as shown in Fig. 2.20. It would be resulted from switching performance variations of IGBT chips.

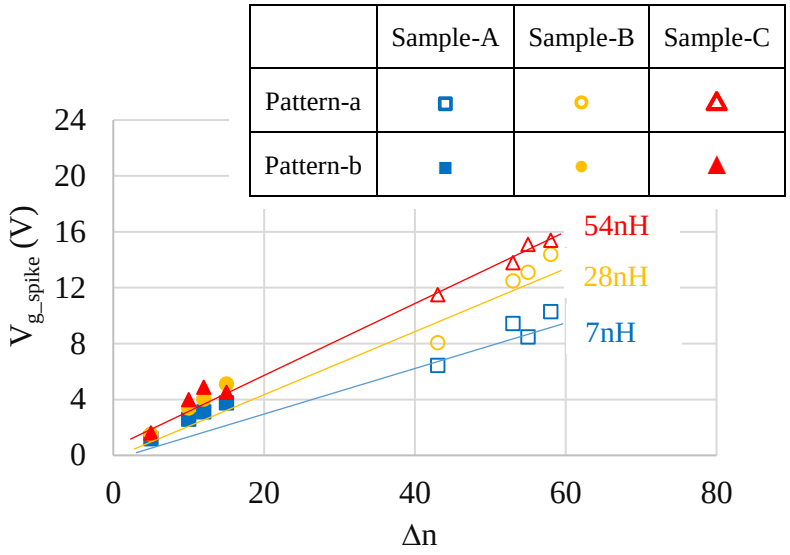


Fig. 2.21 The relation of V_{g_spike}, L_g, and Δn.

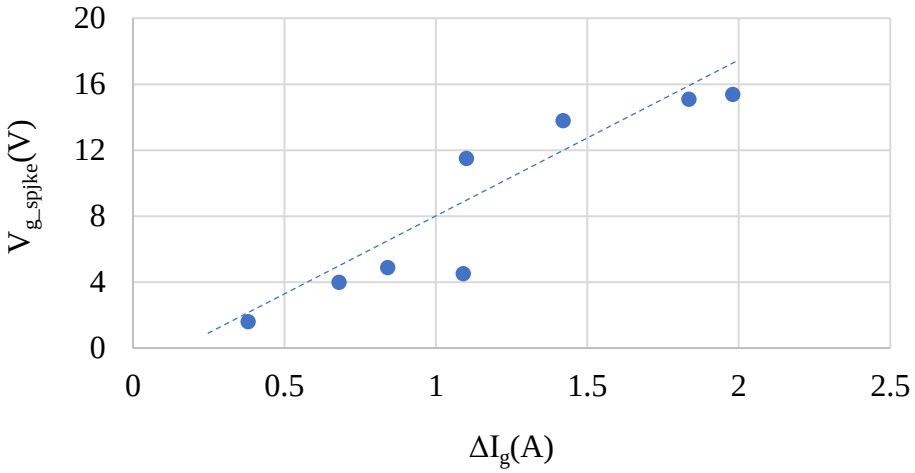


Fig. 2.22 The relation between V_{g_spike} and ΔI_g for Sample-C.

2.4.1 The influence of L_g and Δn (ΔI_g) on V_{g_spike}

Because the V_{g_spike} in turn-off was much smaller than that in turn-on, the V_{g_spike} in turn-off was focused to investigate. All three types of samples were implemented double pulse tests by digital gate control shown in Table 2.3. Fig. 2.21 shows the relation between V_{g_spike}, L_g, and Δn, which was the difference between *n1* and *n2* as shown in Table 2.3. It indicates that the V_{g_spike} was positively correlative to Δn and L_g.

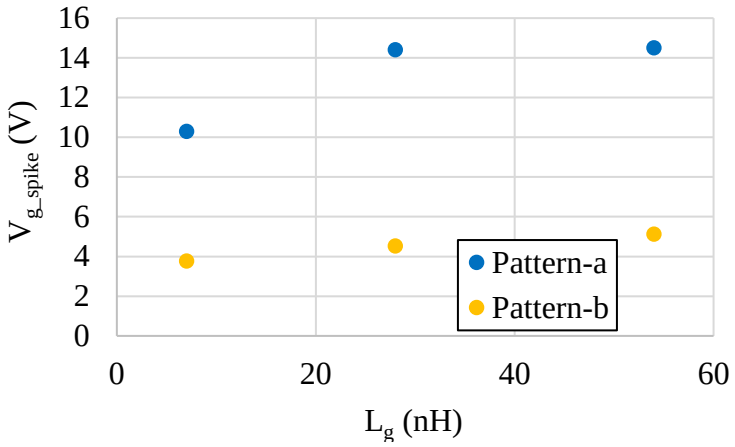


Fig. 2.23 The relation between V_{g_spike} and L_g for three samples in turn-off under digital gate control Pattern-a and Pattern-b.

Because the change of digital control vectors will introduce large gradient of I_g, the relationship of ΔI_g and V_{g_spike} is presented in Fig. 22, where the ΔI_g is the change of I_g at the timing when V_{g_spike} occurring. Fig. 22 shows the results for Sample-C. It is obvious that the V_{g_spike} is positively corresponding to ΔI_g. Furthermore, the relation between V_{g_spike} and L_g under the same digital gate control vectors (*n1*=63, *n2*=8, *n3* =63) is plotted in Fig. 2.23. Although V_{g_spike} was positively correlative to L_g, the relation was not linear. Therefore, it can be speculated there should be other elements, except for the L_g, affecting the V_{g_spike}.

2.4.2 The influence of L_g and Δn (ΔI_g) on tradeoff of switching loss and overshoot

It is discussed about the module and digital gate control designs to cope with both the improvement of the tradeoff and suppression of V_{g_spike} as follows. To appraise the improvement of the tradeoff, the objective function (f_{OBJ}) as given by Eq. (2) [1], [5] is employed. Small f_{OBJ} means good improvement of tradeoff.

$$f_{OBJ} = \sqrt{{E'_{off}}^2 + {V'_{overshoot}}^2} \tag{2}$$

Where,

$$E'_{off} = \frac{E_{off}}{E_{off,max}} \tag{3}$$

$$V'_{overshoot} = \frac{V_{overshoot}}{V_{overshoot,max}} \tag{4}$$

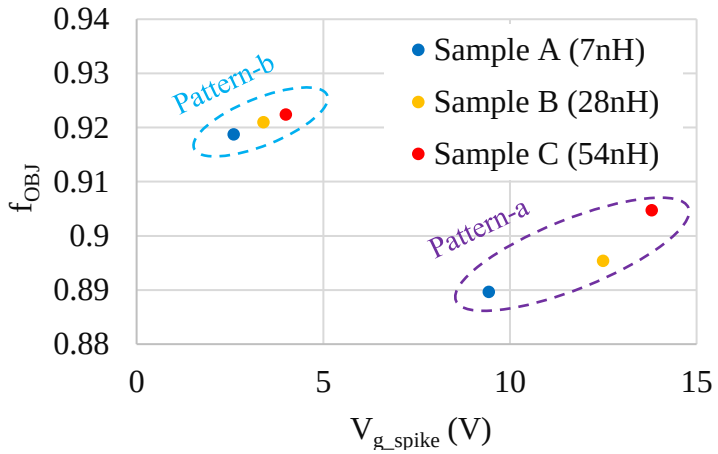


Fig. 2.24 The relation between f_{OBJ} , V_{g_spike}, and L_g

The subscript max signifies the maximum of the corresponding quantity from the experiment results. The relation between f_{OBJ} and V_{g_spike} under Pattern-a and Pattern-b conditions is plotted in Fig. 2.24. The Δn of Pattern-b was smaller than that of Pattern-a. Although the V_{g_spike} can be suppressed by decreasing Δn due to small dI_g/dt, for the same sample, Pattern-b had a larger f_{OBJ} than Pattern-a. This proves that the improvement of the tradeoff in the turn-off was weakened if Δn was decreased, which means was ΔI_g decreased. Moreover, Sample A, whose L_g was the smallest, had the smallest f_{OBJ} and V_{g_spike}. Therefore, it is the better choice to reduce the L_g to suppress the V_{g_spike} and ensure good improvement of the tradeoff for designing IGBT modules driven by the DGD.

2.4.3 The analyzation of oscillation of V_{g_spike}

To discuss the origin of the gate voltage spike, the oscillation cycle of V_{g_spike} after n_{NMOS} changed from *n1* to *n2* was analyzed. As shown in the schematic circuit in Fig.

2.11, the oscillation of V_{g_spike} would be introduced by the LC circuit in the gate loop, which includes L_g, C_{ge}, and C_{gc}. And the oscillation period T is given by

$$T = 2\pi\sqrt{C \times L} \tag{5}$$

Table 2.5 Calculated total inductance under digital pattern-a.

Sample	L_g (nH)	L' (nH)	L'' (nH)
A	7	0.86	25.08
B	28	1.26	37.65
C	54	2.68	65.95

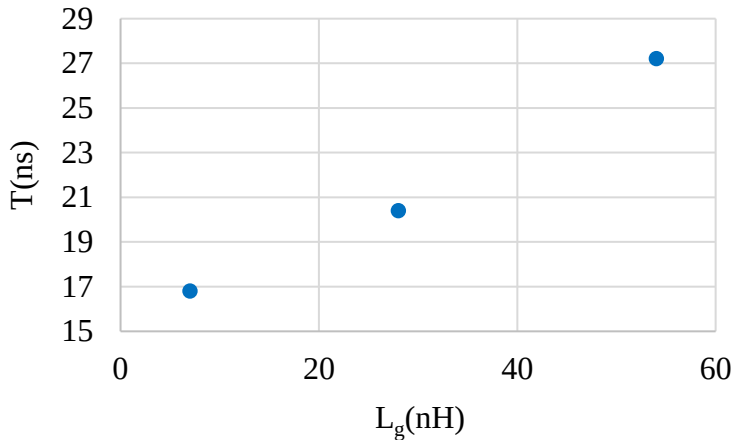


Fig. 2.25 The relation between T and L_g for three samples in turn-off under digital gate control Pattern-a.

According to the results of Pattern-a for three samples, the relation of T and L_g is plotted in Fig. 2.25. T was positively correlated with L_g, which was corresponding to Eq. (5). When *n1* rose to *n2*, C_{ge} is 8 nF and C_{gc} is 0.28 nF as shown in Fig. 2.10. By substituting T, C_{ge}, and C_{gc}, into Eq. (5), the total inductances of three samples are shown in Table 2.5. L' was the calculated total inductance when substituting T and C_{ge}, and L'' was the calculated total inductance when substituting T and C_{gc}. L' is much smaller than L_g, so V_{g_spike} does not result from the resonance of L_g and C_{ge}. Although L'' is about 10-20 nH larger than L_g, considering T is positively correlated to L_g.

Therefore, the V_{g_spike} would depend on the resonance of an LC circuit including L_g, C_{gc}, and other stray inductances. In Fig. 2.16, Fig. 2.17, and Fig. 2.18, there is an oscillation, whose oscillation cycle time is longer than V_{g_spike} happening after *n1*, and the oscillation is linked with changes in V_{ce} and I_c, it can be considered that the C_{gc} and L_e influence on the gate voltage.

2.5 Conclusion

This chapter demonstrated that the IC is safe as the IGBT is under operation by thermal simulation. And clarified the effect of gate inductance on gate voltage spikes when the IGBT modules are driven by a DGD. Although the digital gate control improves switching noise-loss tradeoff, a large gate voltage spike occurs in turn-off. The gate voltage spike was positively correlated with gate inductance and difference among gate control vectors (the change of gate current). Reducing the gate inductance inside IGBT modules driven by the DGD is necessary to cope with both the improvement of the tradeoff and suppression of gate voltage spikes. Furthermore, V_{g_spike} would be dependent on the resonance of an LC circuit including L_g, C_{gc}, and other stray inductances rather than an LC circuit including L_g and C_{ge}.

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CHAPTER 3. Design for parallel-connected IGBTs

3.1 Background

The former chapter introduced one IGBT chip modules as the digital driver is employed. This chapter focuses on parallel-connected IGBTs, which can enlarge the rating current in the power electronics application systems. As a main problem in parallel-connected IGBT chips in the power module, the current imbalance has been studied [1-7]. The current imbalance induces the reliability issues such as accelerated aging and degradation or destruction occurring in the IGBT chip. It is mainly caused by the differences in device characteristics, such as collector-emitter saturation voltage, threshold voltage, and stray inductance from asymmetric layout and gate signal delays [1-3]. This chapter is focused on the stray inductance that is one of main causes of the current imbalance at the module level.

The design considerations of L_g in IGBT modules including only one chip for suppressing V_{g_spike} as DGD is applied have been proposed in the former chapter. And there are many commercial parallel-connected-IGBTs modules that were designed under conventional gate driving. However, the switching characteristics of parallel-connected IGBTs driven by DGD have not been discussed. Furthermore, the design considerations of power modules with parallel-connected IGBT chips driven by DGD are not clear for suppressing the current imbalance and the V_{g_spike}.

This chapter reports an experimental clarification of switching characteristics of power modules with two parallel-connected IGBTs driven by a DGD, which is designed by the previous works [8-9]. This paper focuses on the impact of L_g and emitter inductance L_e on V_{g_spike}, current share, and the switching tradeoff characteristics under conventional gate driving and digital gate driving. Five types of IGBT modules with different L_g and L_e were fabricated. Gate driving vectors n and the change of gate driving vectors Δn, which corresponds to large I_g and large transient of I_g respectively were also investigated to show the effect on V_{g_spike}. Moreover, according to the

switching characteristics, the design considerations of IGBT modules with two parallel-connected chips are discussed.

3.2 The design of IGBT module and setup of double pulse test

Five types of IGBT modules with built-in two parallel-connected IGBT chips were fabricated. The breakdown voltage was 680 V and the rated current was 600 A. The IGBT chips are the same as those used in the chapter 2. And the measured

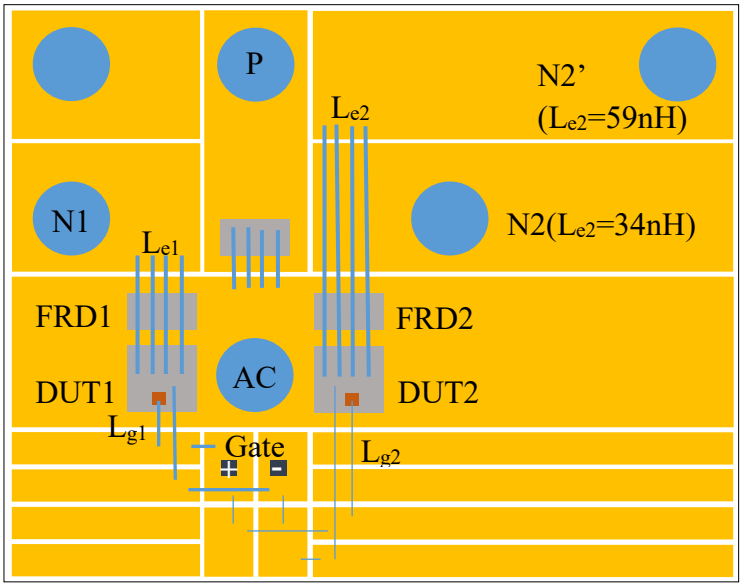

Fig. 3.1 The plane figure of Sample-D.

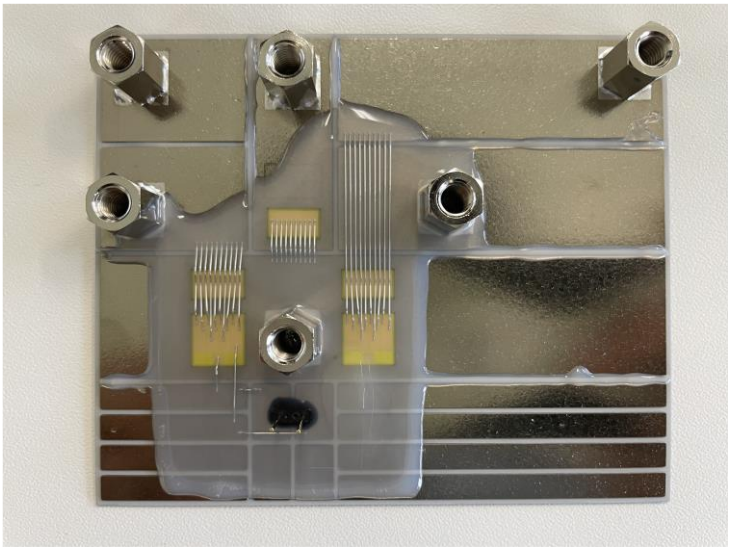

Fig. 3.2 The photo of Sample-D.

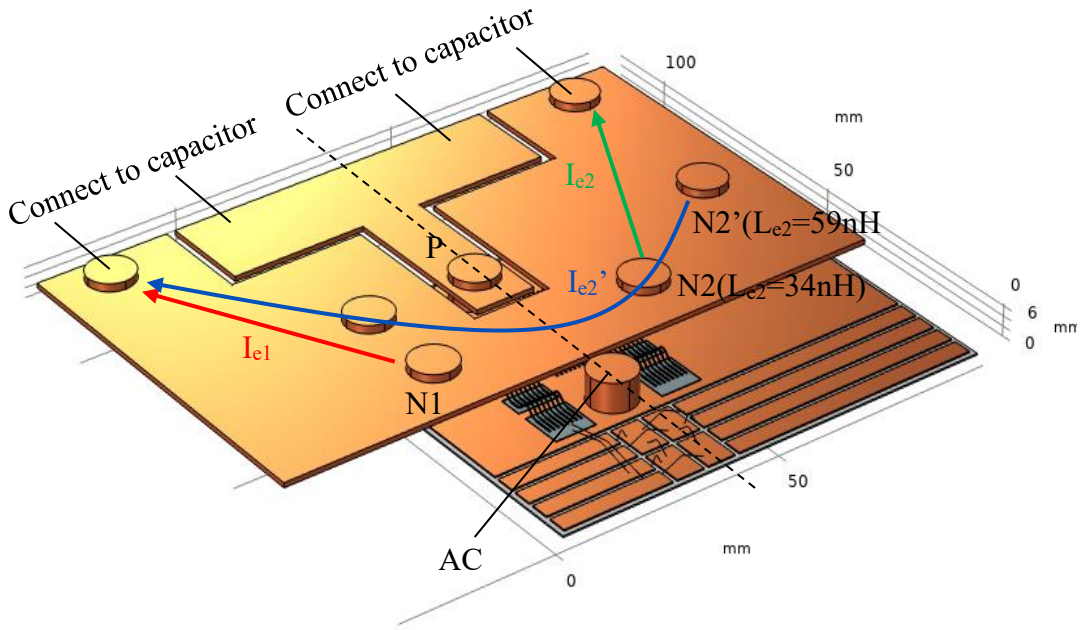

Fig. 3.3 IGBT module with the additional copper

characteristics are almost identical for different chips, so the effect of difference of characteristics can be neglected. To make sure the effect of inductance can be indicated obviously, the difference of inductance between two DUTs are set large enough. By applying different diameters and wire connection routes, different L_g could be realized and the values were estimated by COMSOL. Fig. 3.1 and Fig. 3.2 show the plane figure and photograph of Sample-D. There were two types of wire connection routes for L_g

Table 3.1 Dimensions of wires and calculated L_g and L_e

Route	Wire diameter (μm)	L (nH)
L_g	300	35
	30	68
L_e	300	34
	300	59

and L_e inside modules. To enlarge the difference of L_e of two IGBTs under test, DUT1 and DUT2, a copper board was designed as shown in Fig. 3.3. The emitter current of DUT1 I_{e1} flows through the red color route. As for modules with symmetric L_e, the emitter current of DUT2 I_{e2} flows through the green color route. Otherwise, the I_{e2} flows through the blue color route as the L_e is asymmetric. Table 3.1 shows the dimensions of wires and calculated L_g and L_e by COMSOL. In addition, the mutual inductance is

considered in the calculation. Table 3.2 shows the samples of IGBT modules with different combinations of the mentioned L_g and L_e in Sample-D. L_{g1} and L_{g2} are gate

Table 3.2 Combinations of L_g and L_e for different layouts

L_g	L_{e1}=34nH L_{e2}=34nH	L_{e1}=34nH, L_{e2}=59nH
L_{g1}=L_{g2}=35nH	A	C
L_{g1}=35nH, L_{g2}=68nH	B	D
L_{g1}=68nH, L_{g2}=35nH	/	E

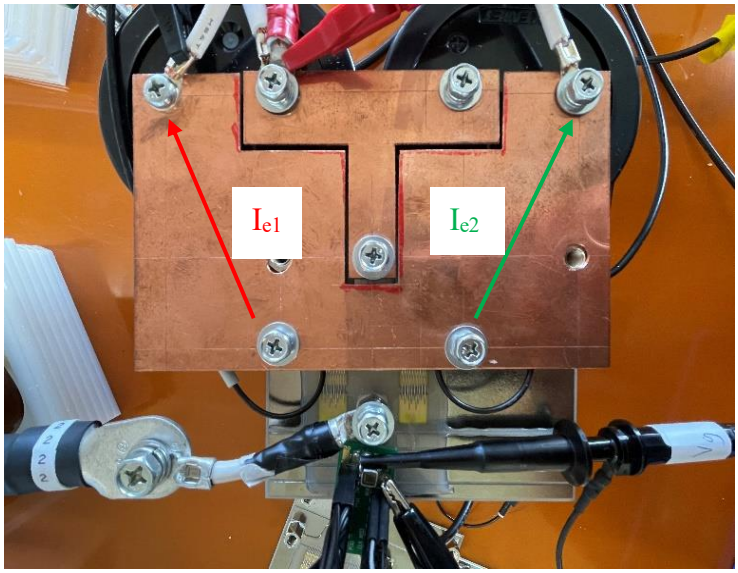

Fig. 3.4 The experiment setup for samples having symmetric L_e.

inductances of DUT1 and DUT2. L_{e1} and L_{e2} are the emitter inductances of DUT1 and DUT2. Fig. 3.4 and Fig. 3.5 are the experiment setup for samples that have symmetric L_e and asymmetric L_e. Sample-A has symmetric L_e and L_g. Sample-B has the same symmetric L_e as Sample-A but asymmetric L_g. Sample-C has symmetric L_g as Sample-A but the L_e is asymmetric. Sample-D shown in Fig. 3.2 has the same asymmetric L_e as Sample-C, and the same asymmetric L_g as Sample-B. Sample-E is an additional sample whose L_g of DUT1 and DUT2 were inverted from Sample-D. In this work, the high-side IGBT chip was omitted from the half-bridge circuit, because the modules were designed specifically for evaluating the switching characteristics of the low-side IGBT.

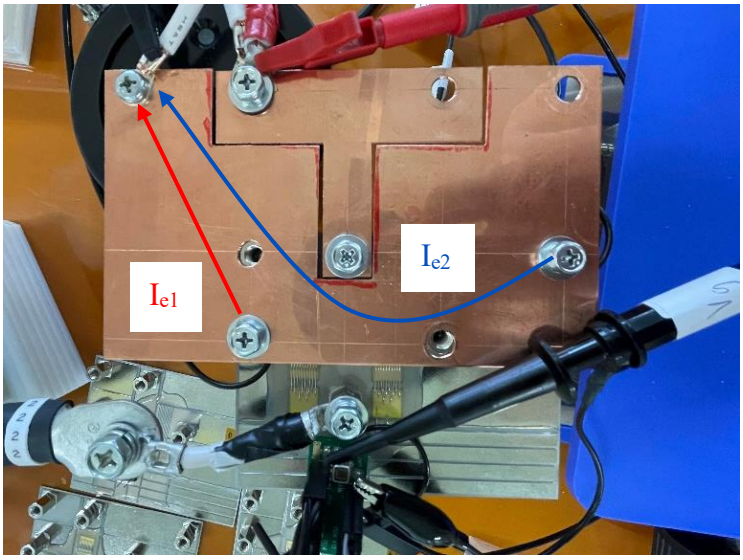

Fig. 3.5 The experiment setup for samples having asymmetric L_e.

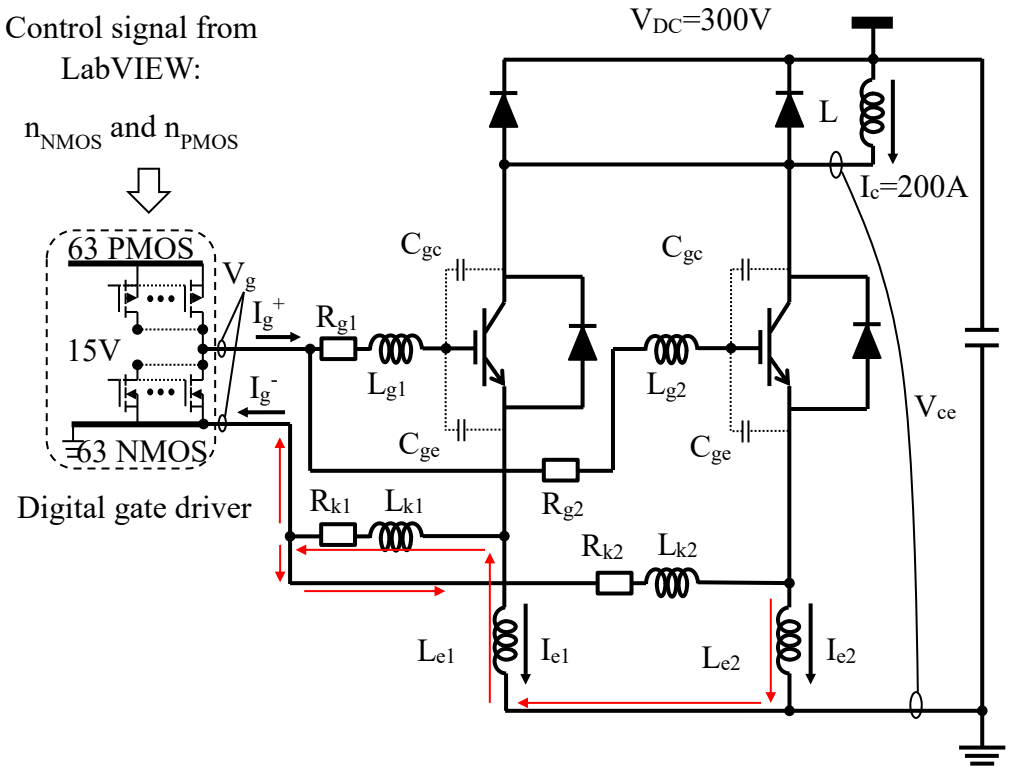

Fig. 3.6 The circuit schematic for the double pulse test.

Therefore, the results of this verification can also be applied to power electronics circuit design.

Fig. 3.6 shows the circuit schematic for the double pulse test to measure the turn-on and turn-off characteristics of the above IGBT modules. Based on the same gate-driving

Table 3.3 Three step digital gate driving for turn-off.

	n1	*n2*	*n3*
n_{NMOS}	63	5	63
	63	8	63
	63	10	63
	63	20	63
	63	40	63
Time (ns)	640	1040	/

Table 3.4 Three step digital gate driving for turn-on.

	n1	*n2*	*n3*
n_{PMOS}	63	5	63
	63	8	63
	63	10	63
	63	20	63
	63	40	63
Time (ns)	160	640	/

method in the former chapter, the gate-driving conditions were proposed as follows. n_{NMOS} and n_{PMOS} were set to an integer from 10 to 63 to implement double pulse tests under conventional gate driving. Because when n_{NMOS} and n_{PMOS} are less than 10, the switching time is too long to keep safe. In the digital gate driving, the n_{NMOS} and n_{PMOS} were set as three different values at each period *n1*, *n2*, and *n3* in the whole turn-off and turn-on stages as shown in Table 3.3 and Table 3.4.

The time of different stage in the switching operation is determined by the vectors. Once the *n1* is set as 63, the delay time is almost a constant value for modules with different layout. And the delay time was extracted from the waveforms under conventional gate control. The corresponding time for *n1* should be less than the delay time, otherwise vector 63 would invade into the current decreasing stage leading to a large $V_{overshoot}$. If the corresponding time for *n1* is too small, the delay time would be

governed by small *n2* which is equivalent to large gate resistance resulting in long delay time and large loss. If the corresponding time for *n2* is long enough to cover the time interval when $V_{overshoot}$ happens, the loss and $V_{overshoot}$ during this period can be suppressed. But if the corresponding time for *n2* is too long, the tail current will flow continuously for long time to enlarge the loss. The current imbalance is dependent on the stray inductance and *n2*, only if the corresponding time for *n2* in long enough to cover the $V_{overshoot}$, it is not affected by the time. In addition, we set the same the corresponding time for different modules. In addition, the experiment system was operated under a supply voltage of 300 V and a load current of 200 A.

3.3 Results and discussion

3.3.1 Turn-off waveforms under conventional gate driving

As for the conventional turn-off characteristics, the results of five types of samples are shown from Fig. 3.7 to Fig. 3.11. The n_{NMOS} was set as a constant value of 10. Fig. 3.7 and Fig. 3.8 show the results of Sample-A and Sample-B. L_{e1} was equal to L_{e2} in Sample-A and Sample-B, but L_{g1} was smaller than L_{g2} in Sample-B, while L_{g1} was equal to L_{g2} in Sample-A. Because the L_e was symmetric, the current share was equal in the two samples. The waveforms in Fig. 3.7 and Fig. 3.8 were almost the same, so it is

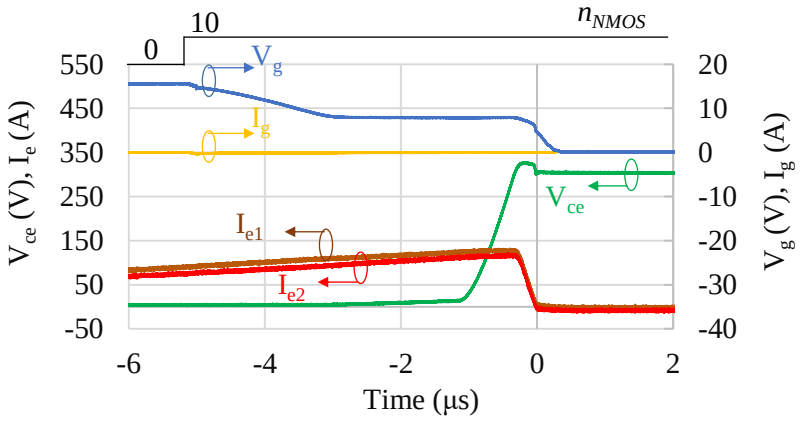

Fig. 3.7 Turn-off waveforms of Sample-A under conventional gate driving as n_{NMOS} is 10.

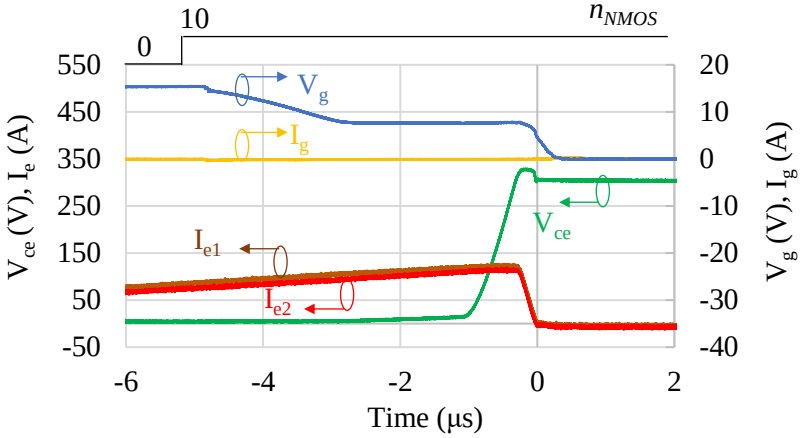

Fig. 3.8 Turn-off waveforms of Sample-B under conventional gate driving as n_{NMOS} is 10.

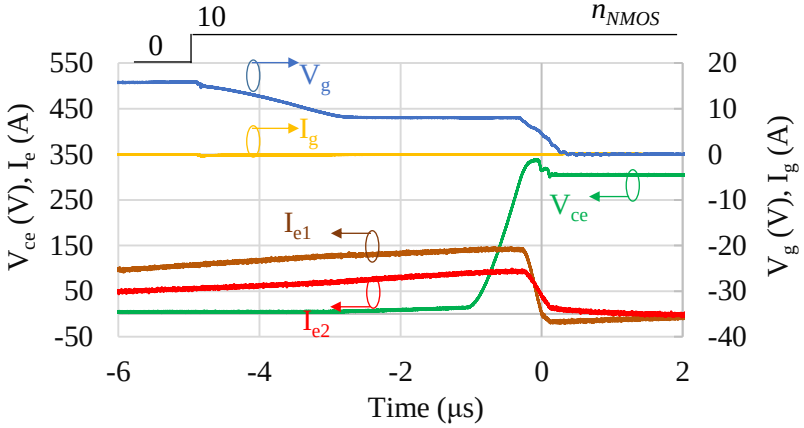

Fig. 3.9 Turn-off waveforms of Sample-C under conventional gate driving as n_{NMOS} is 10.

indicated that the asymmetric L_g did not influence turn-off characteristics as L_e was symmetric under conventional gate driving.

Fig. 3.9 shows the waveforms of Sample-C which has the same symmetric L_g as Sample-A, but asymmetric L_e. Due to the asymmetric L_e, the current was imbalanced during on stage. L_{e1} was smaller than L_{e2}, so the dI_{e1}/dt was larger than dI_{e2}/dt and I_{e1} was larger than I_{e2}. The tail current of I_{e1} was inverted to a large minus value after it reached zero, and decreased slowly. The large L_{e2} can suppress the decreased tendency of current I_{e2}. And voltage drop was induced due to the asymmetric L_e, so the tail current flowed through the red color route shown in Fig. 3.6. As for Sample-D, both the L_g and L_e were asymmetric, and the waveforms of Sample-D are shown in Fig. 3.10. It can be

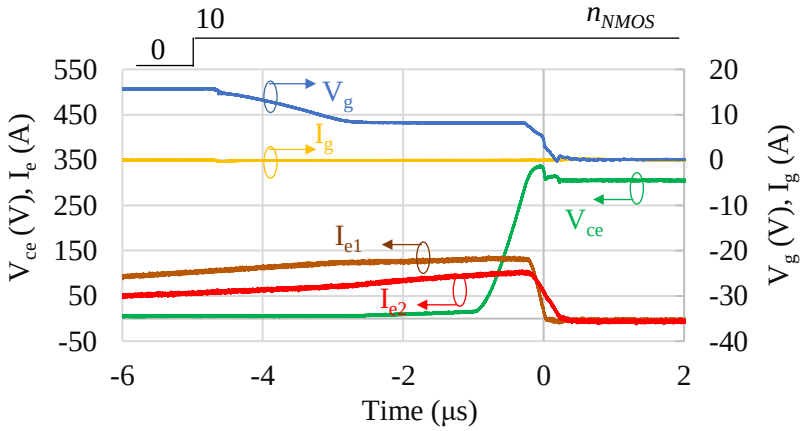

Fig. 3.10 Turn-off waveforms of Sample-D under conventional gate driving as n_{NMOS} is 10.

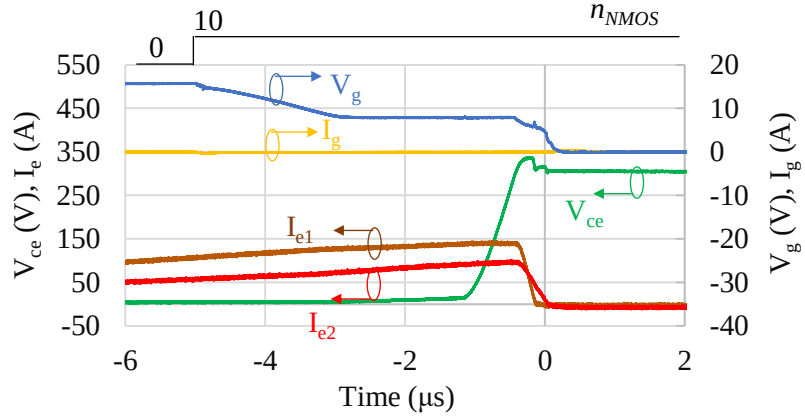

Fig. 3.11 Turn-off waveforms of Sample-E under conventional gate driving as n_{NMOS} is 10.

noted that dI_{e1}/dt was decreased a lot, while dI_{e2}/dt was increased a lot from Miller plateau. The reason for the phenomenon should be the large L_{g2} slowing down the turn-off process of DUT2, while DUT1 is turned off normally. Thanks to this, the current imbalance can be suppressed partly, thus the difference between E_{off} in two IGBTs can be decreased. The other important point is that the tail current of DUT1 in Sample-D was not inverted, which can also suppress the E_{off} compared to Sample-C. Because the resistance of the kelvin gate wire in Sample-D was about 1.4 Ω, but that in Sample-C was only 0.005 Ω, the current cannot flow through the route shown in Fig. 3.6. In Sample-C, the E_{off} of DUT1 and DUT2, E_{off1} and E_{off2}, were 34.9 mJ and 22.1 mJ. In contrast, E_{off1} and E_{off2} in Sample-D were 24.3 mJ and 22.5 mJ.

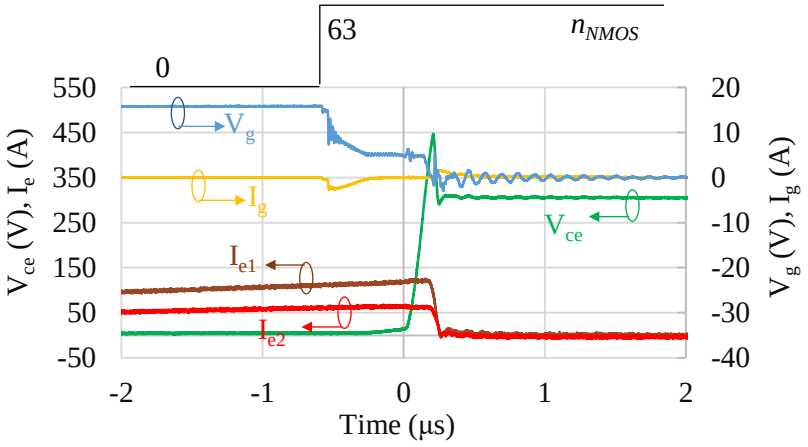

Fig. 3.12 Turn-off waveforms of Sample-E under conventional gate driving as n_{NMOS} is 63.

The results of Sample-E, whose L_{g1} and L_{g2} were equal to L_{g2} and L_{g1} in Sample-D, are shown in Fig. 3.11. Actually, dI_{e1}/dt should increase, while dI_{e2}/dt should decrease from Miller plateau as shown in Fig. 3.12, where the n_{NMOS} was set as 63. Because of the small n_{NMOS} in Fig. 3.11, the effect produced by L_g was suppressed. But the current imbalance was still enlarged compared to the results of Sample-D. As a result, E_{off1} and E_{off2} in Sample-E were 25.4 mJ and 21 mJ. The difference in E_{off} between two DUTs, ΔE_{off}, was larger than that in Sample-D.

Although the symmetric L_e was the best design for parallel-connected IGBTs in modules, it is difficult to accomplish in practice. For the parallel-connected IGBTs, it is a choice to employ the asymmetric L_g to suppress the current imbalance and turn-off loss imbalance in the turn-off interval.

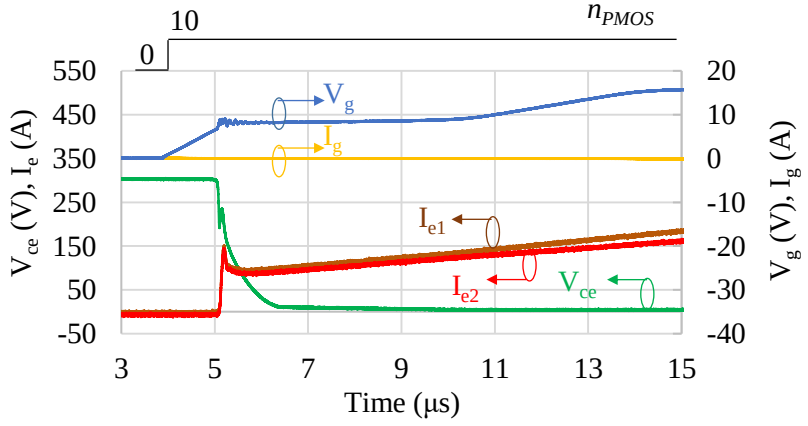

Fig. 3.13 Turn-on waveforms of Sample-A under conventional gate driving as n_{PMOS} is 10.

3.3.2 Turn-on waveforms under conventional gate driving

As for the conventional turn-on characteristics, the results of five types of samples are shown from Fig. 3.13 to Fig. 3.17. The n_{PMOS} is also set as a constant value of 10. Fig. 3.13 and Fig. 3.14 show the results of Sample-A and Sample-B. Just as the results of turn-off, there was not much difference in turn-on waveforms between the two samples, either. It can be indicated that the asymmetric L_g did not influence turn-on characteristics as L_e was symmetric under conventional gate driving.

Fig. 3.15 shows the waveforms of Sample-C. There was a large V_{g_spike} and large current imbalance during turn-on interval. Because L_{g1} was smaller than L_{g2}, the I_{e1} rose much faster than I_{e2}, and the overshoot of I_{e1} was much larger than that of I_{e2}.

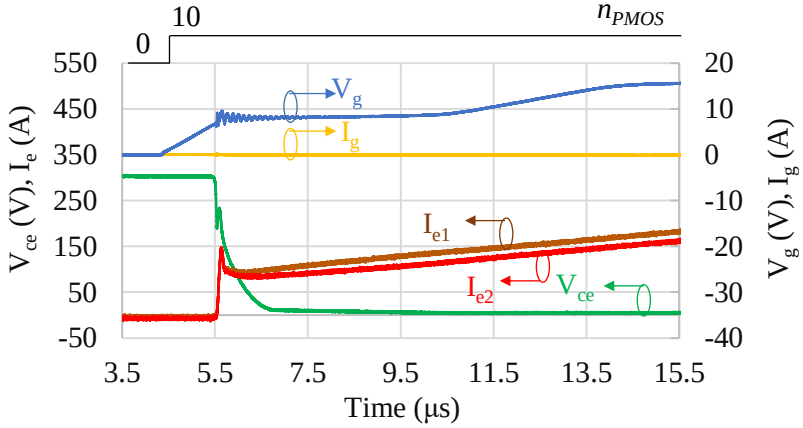

Fig. 3.14 Turn-on waveforms of Sample-B under conventional gate driving as n_{PMOS} is 10.

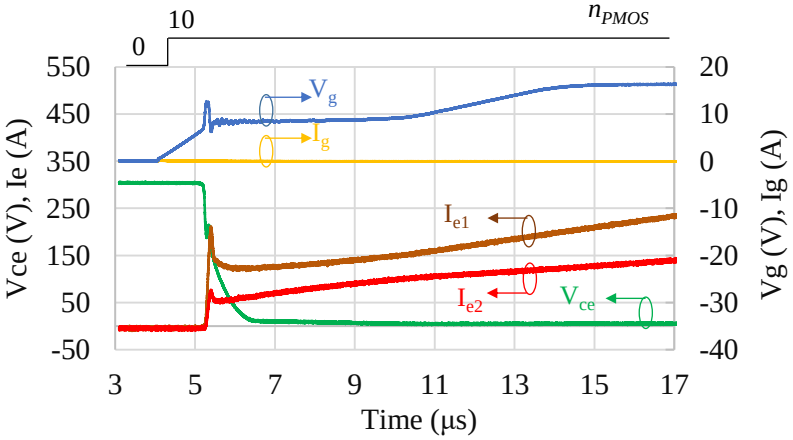

Fig. 3.15 Turn-on waveforms of Sample-C under conventional gate driving as n_{PMOS} is 10.

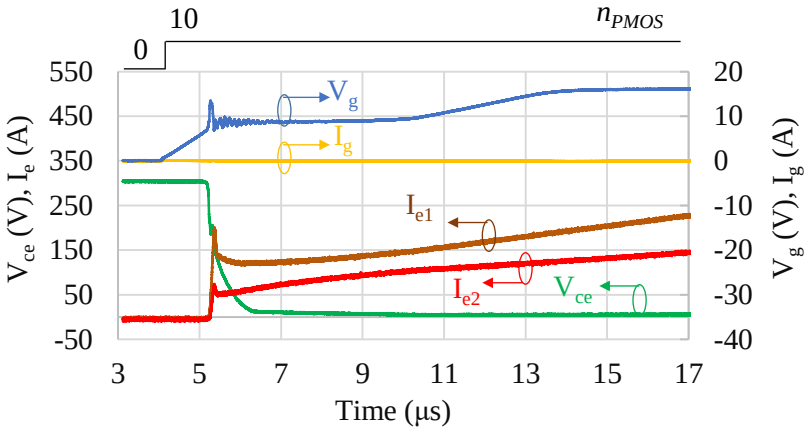

Fig. 3.16 Turn-on waveforms of Sample-D under conventional gate driving as n_{PMOS} is 10.

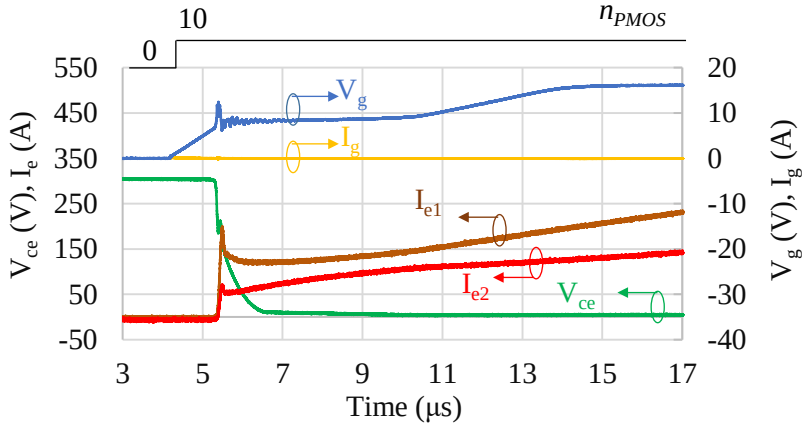

Fig. 3.17 Turn-on waveforms of Sample-E under conventional gate driving as n_{PMOS} is 10.

Comparing the results of Sample-A and Sample-B, it can be concluded that the V_{g_spike} was produced by the asymmetric L_e. Also, as for the waveforms of Sample-D and Sample-E shown in Fig. 3.16 and Fig. 3.17, which have the same L_e as Sample-C, although the L_g are different from each other and asymmetric, the V_{g_spike} was almost equal. The V_{g_spike} in Sample-C, Sample-D, and Sample-E were 12.7 V, 13.5 V, and 12.4 V. The results of Sample-D and Sample-E made it more certain that the V_{g_spike} was caused by the asymmetric L_e mainly.

To clarify the cause of the V_{g_spike} in the turn-on, the relation of V_{g_spike}, n_{PMOS}, and current difference between I_{e1} and I_{e2}, ΔI_e is plotted in Fig. 3.18, Fig. 3.19, and Fig. 3.20. In the Fig. 3.18, for all of the samples, with the increasing n_{PMOS}, which means large

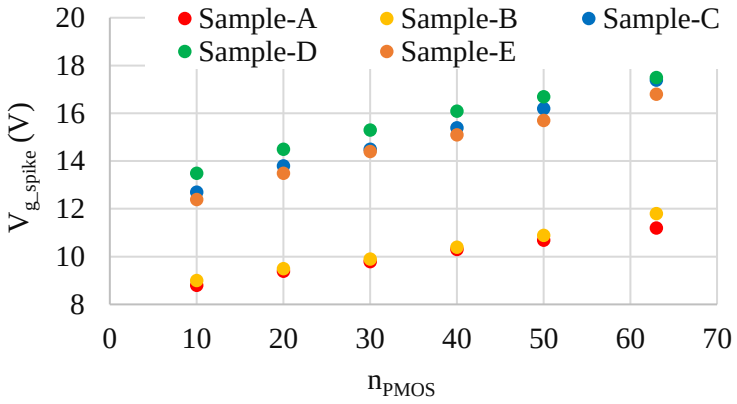

Fig. 3.18 The relation of V_{g_spike} and n_{PMOS}

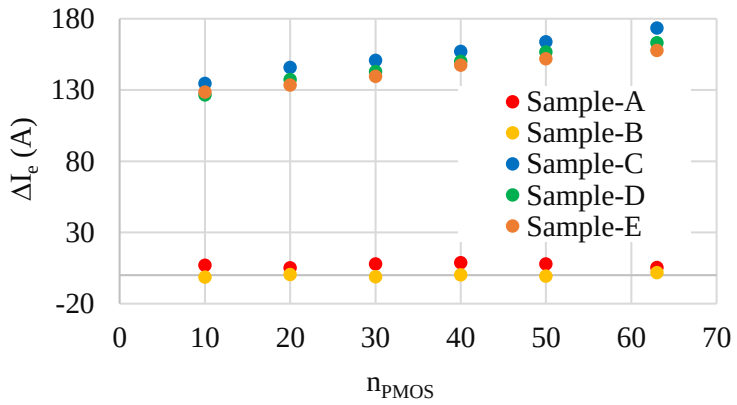

Fig. 3.19 The relation of n_{PMOS} and ΔI_e.

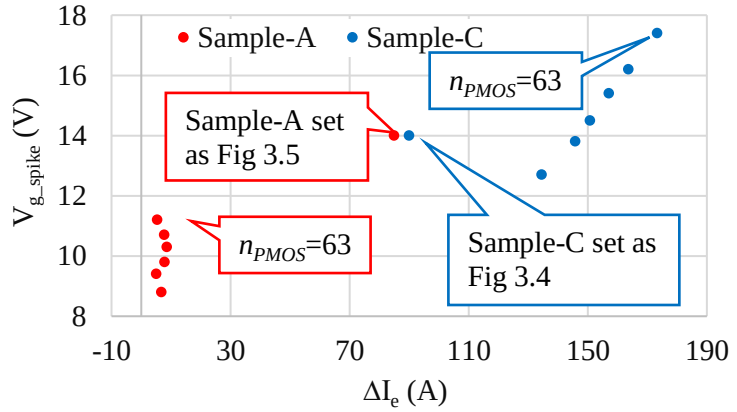

Fig. 3.20 The relation of V_{g_spike} and ΔI_e.86

gate current and high switching speed, the V_{g_spike} also increased. The V_{g_spike} of Sample-A and Sample-B, whose L_e was symmetric, were much smaller than those of Sample-C, Sample-D, and Sample-E, whose L_e were asymmetric. On the other hand, samples with the same L_e had similar V_{g_spike}. In the Fig. 3.19, no matter how much the n_{PMOS} was, there is almost no ΔI_e in Sample-A and Sample-B. As for Sample-C, Sample-D,

and Sample-E, the L_e was asymmetric, so with the increasing n_{PMOS} the ΔI_e also increased due to high switching speed. Fig. 3.20 shows that the V_{g_spike} was positively corresponding to ΔI_e. In addition, the Sample-A was connected as shown in Fig. 3.5 and the Sample-C was connected as shown in Fig. 3.4 to implement experiment under the condition where n_{PMOS} is 63. By change of emitter terminal connection, the ΔI_e increased to 85 A compared to the Sample-A connected as shown in Fig. 3.4, and ΔI_e decreased to 90 A compared to Sample-C connected as shown in Fig. 3.5 From these results, the V_{g_spike} is caused by ΔI_e, which is resulting from asymmetric L_e.

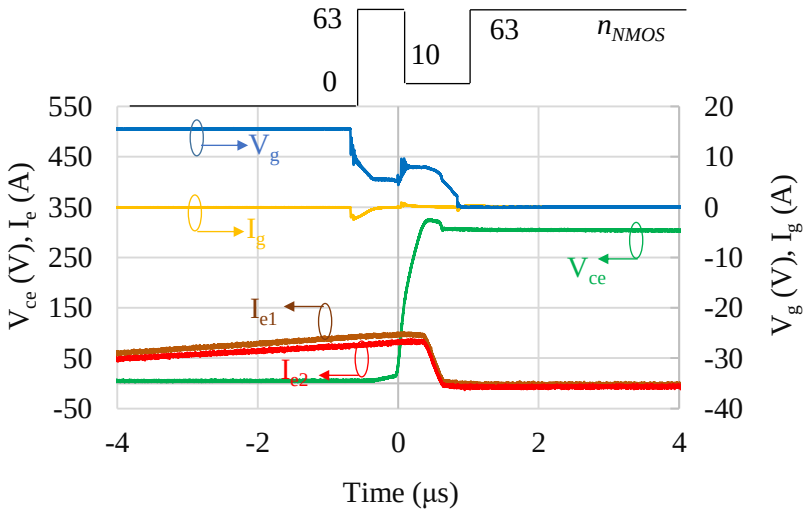

Fig. 3.21 Turn-off waveforms of Sample-A under digital gate driving.

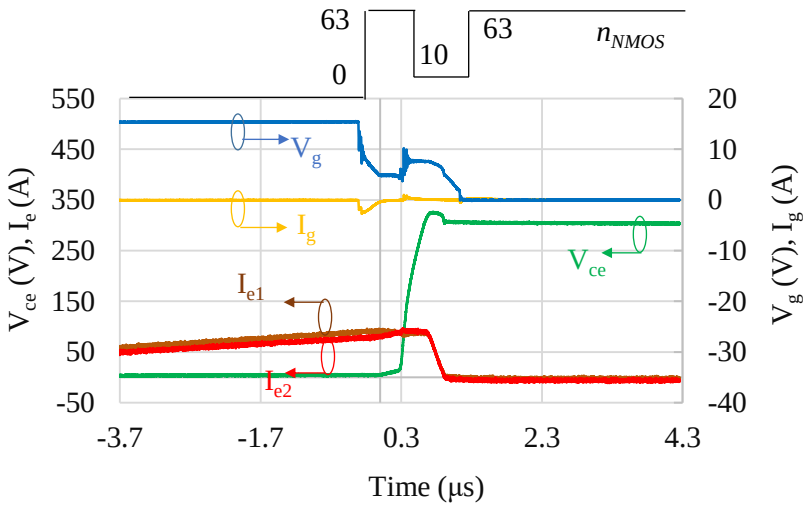

Fig 3.22 Turn-off waveforms of Sample-B under digital gate driving.

3.3.3 Turn-off waveforms under digital gate driving

The turn-off waveforms for five types of samples under three-step digital gate driving are shown from Fig. 3.21 to Fig. 3.25. The n_{NMOS} was pulled up to *n1* of 63 from 0 to start the turn-off, then n_{NMOS} was pulled down to *n2* of 10. Finally, the n_{NMOS} was kept as *n3* of 63 to complete the turn-off and keep the off-state. Fig. 3.21 and Fig. 3.22 show the waveforms of Sample-A and Sample-B. Because of the large value of *n1* and *n3*, the turn-off speed was much larger, which meant a smaller E_{off}, than that in conventional gate driving mentioned before. And the small value of *n2* can keep a small $V_{overshoot}$, 24.6 V, which was close to the 27.5 V in Fig. 7. E_{off1} and E_{off2} in Sample-A were 17.4

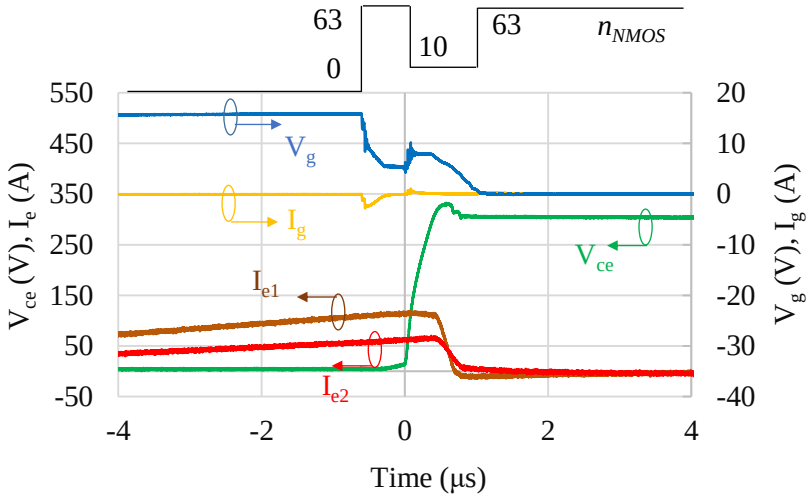

Fig. 3.23 Turn-off waveforms of Sample-C under digital gate driving.

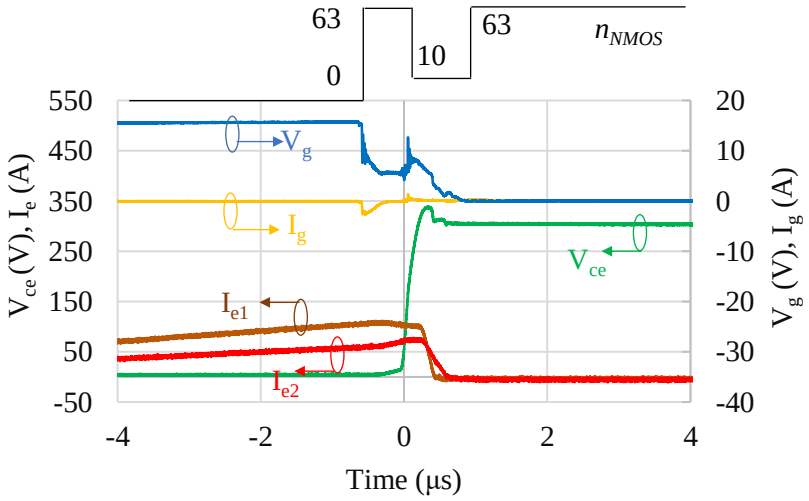

Fig. 3.24 Turn-off waveforms of Sample-D under digital gate driving.

mJ and 16.26 mJ, respectively. In contrast to this, the E_{off1} and E_{off2} were 24.3 mJ and 23.0 mJ in the mentioned conventional results as shown in Fig. 3.7. Also, the

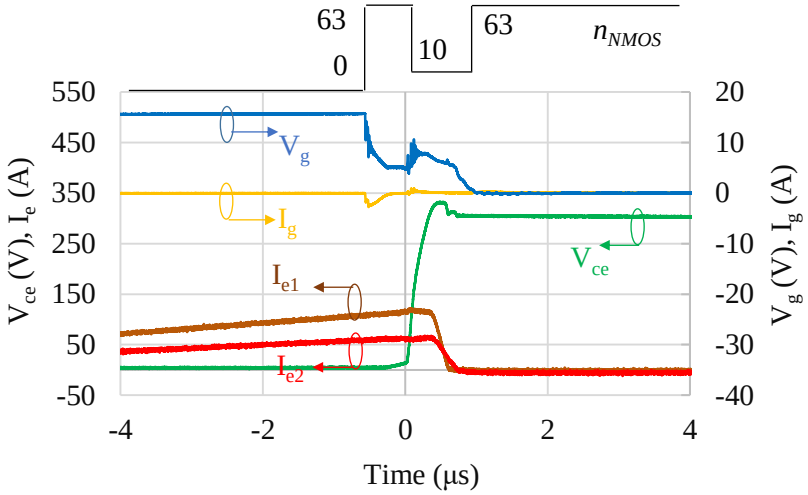

Fig. 3.25 Turn-off waveforms of Sample-E under digital gate driving.

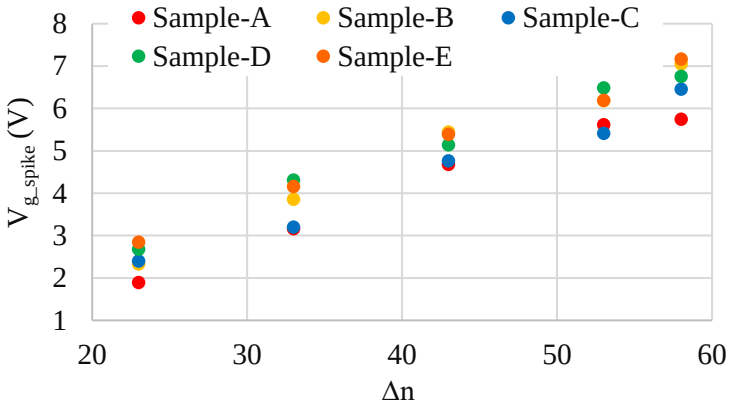

Fig. 3.26 The influence of L_g and Δn_{NMOS} on V_{g_spike}.

improvement of other samples was similar to that of Sample-A. However, V_{g_spike} was increased under digital gate driving clearly. This is caused by the L_g and the large transient gradient of I_g at the time when n_{NMOS} was pulled from 63 down to 10. The V_{g_spike} in Sample-A and Sample-B were 4.1 V and 5.2 V. The larger V_{g_spike} resulted from the larger L_g in Sample-B. In the experiment, the value of V_{g_spike} was unstable, so to improve the accuracy, the measurement for each sample was repeated five times, and employed the average value to show the influence of L_g and Δn_{NMOS} on V_{g_spike} in Fig. 3.26. It is clear that samples with small L_g, Sample-A and Sample-C, have small V_{g_spike}, and samples with large L_g, Sample-B, Sample-D, and Sample-E, have large V_{g_spike}.

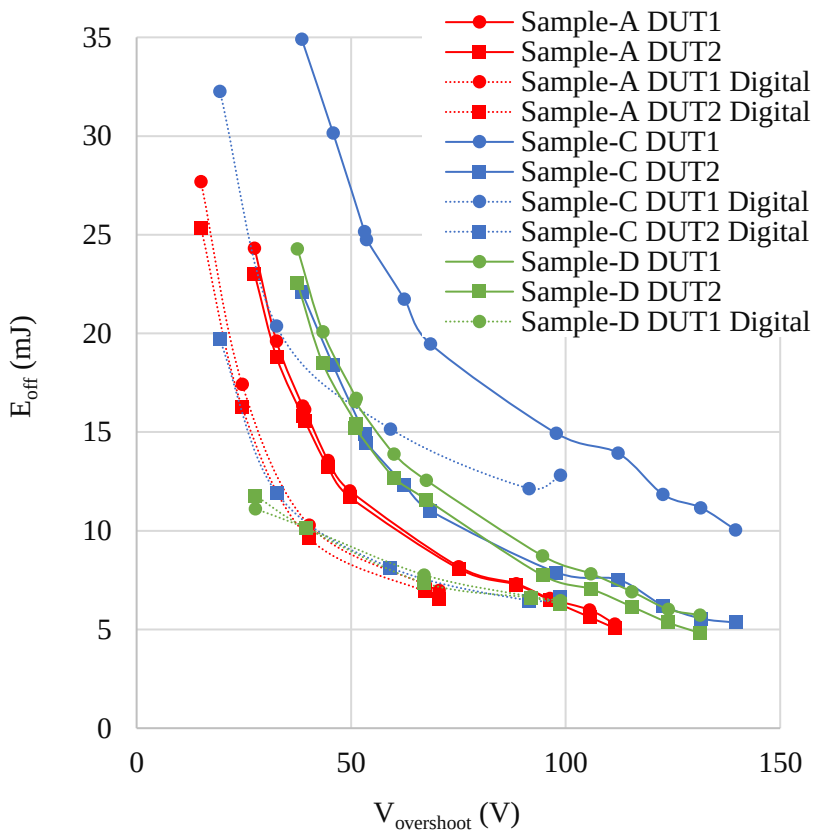

Fig. 3.27 The tradeoff relation of E_{off} and $V_{overshoot}$ under conventional gate driving and digital gate driving.

Moreover, the V_{g_spike} was positively corresponding to Δn_{NMOS} that generates a large transient gradient of I_g.

In Sample-C, Sample-D, and Sample-E, just as in the results under conventional gate driving, the current share was not equal due to asymmetric L_e as shown in Fig. 3.23, Fig. 3.24, and Fig. 3.25. But the effect of asymmetric L_g was more evident because the switching speed was enlarged a lot, especially in Sample-D and Sample-E. In Sample-D, dI_{e1}/dt decreased, while dI_{e2}/dt increased a lot from the Miller plateau more than that under the mentioned conventional conditions. In Sample-E, the change of dI_e/dt was also larger than before, but because the change was opposite to Sample-D, the ΔI_e and ΔE_{off} were enlarged. The E_{off1} and E_{off2} in Sample-D were 10.2 mJ and 10.1 mJ, while they were 13.6 mJ and 9.4 mJ in Sample-E. Also, the ΔE_{off} was decreased compared to that under the conventional gate driving in Fig. 3.10 and Fig. 3.11.

Fig. 3.27 shows the tradeoff relation between E_{off} and $V_{overshoot}$ under conventional gate driving and digital gate driving. It was found that the tradeoff can be improved by

the digital gate driving. As for the turn-off characteristics, Sample-A was the best design that has a good tradeoff and small V_{g_spike}. But in the actual IGBT modules, it is difficult to accomplish symmetric L_e and L_g. It is a choice to employ the asymmetric L_g to suppress the current imbalance and turn-off loss imbalance in the turn-off interval as Sample-D. But the small L_e should combine with small L_g, and large L_e should combine with large L_g. In addition, considering the digital gate driving, the asymmetric L_g should be suppressed as far as possible to prevent a large V_{g_spike}. Moreover, symmetric and small L_g combined with asymmetric L_e like Sample-C is the worst design according to the results.

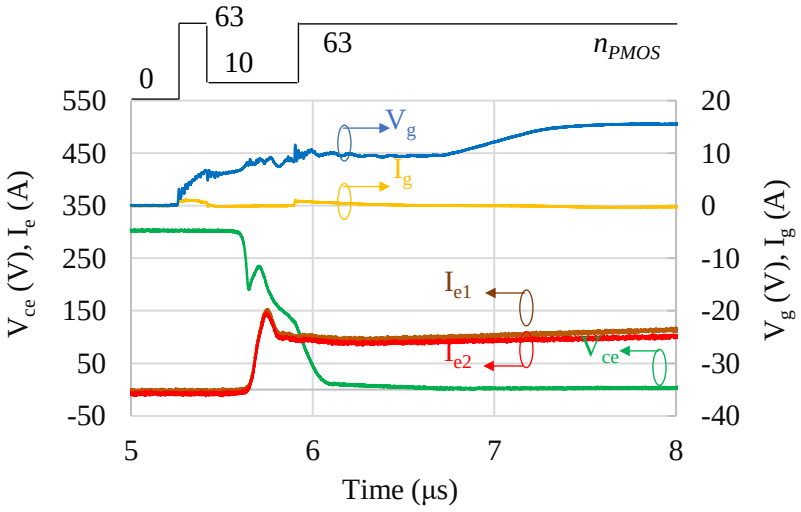

Fig. 3.28 Turn-on waveforms of Sample-A under digital gate driving.

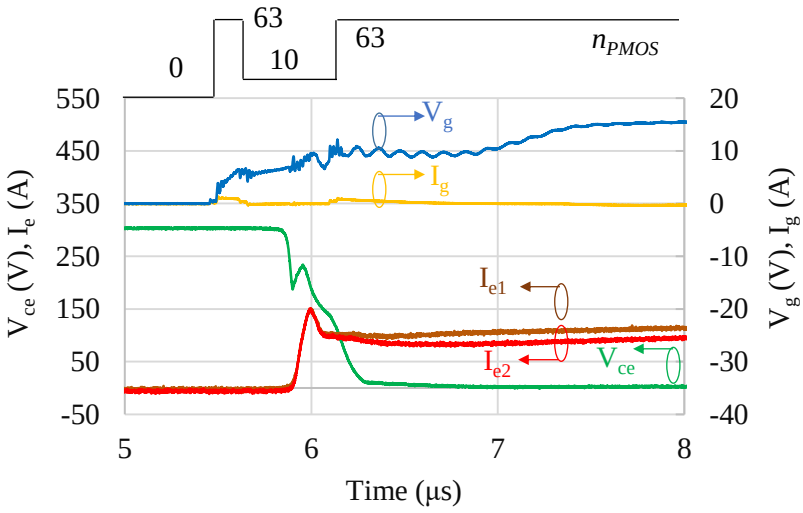

Fig. 3.29 Turn-on waveforms of Sample-B under digital gate driving.

3.3.4 Turn-on waveforms under digital gate driving

The turn-on waveforms for five types of samples under three-step digital gate driving are shown from Fig. 3.28 to Fig. 3.32. The value of n_{PMOS} was set as same as n_{NMOS} in

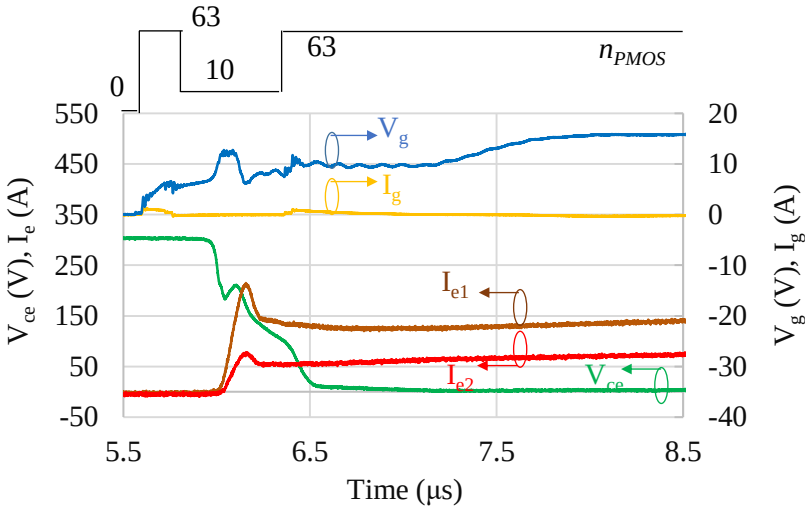

Fig. 3.30 Turn-on waveforms of Sample-C under digital gate driving.

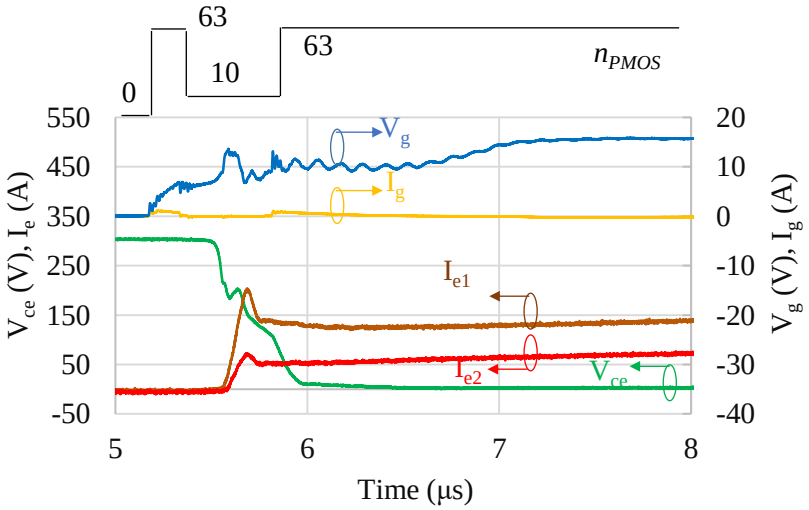

Fig. 3.31 Turn-on waveforms of Sample-D under digital gate driving.

turn-off, but the time duration was different. Fig. 3.28 and Fig. 3.29 show the waveforms of Sample-A and Sample-B. The $I_{overshoot}$ were 48.1 A and 47.9 A, which were at the same level as the conventional results shown in Fig. 3.13 and Fig. 3.14, 46.9 A and 45.1 A in Sample-A. But the E_{on} decreased from 14.8 mJ and 15.6 mJ to 6.5 mJ and 6.8 mJ, respectively. As the $I_{overshoot}$ was kept at the same level, the E_{on} of other samples was decreased, too.

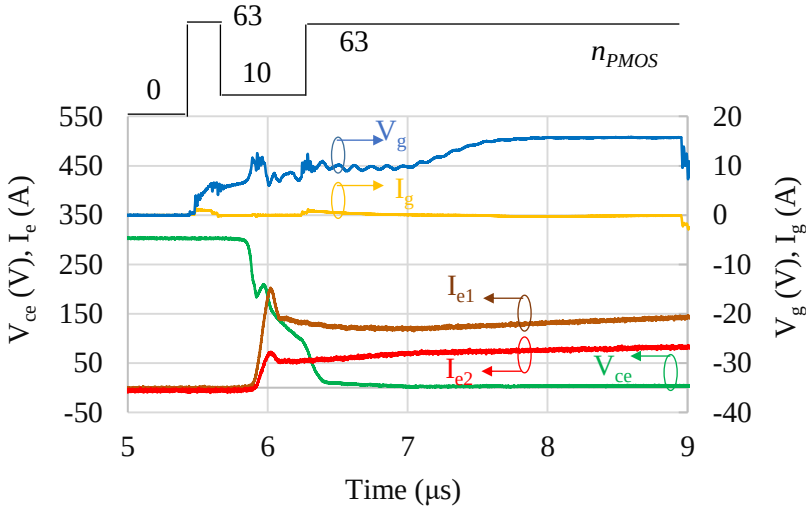

Fig. 3.32 Turn-on waveforms of Sample-E under digital gate driving.

Although the digital gate driving was applied, a large V_{g_spike} was not generated in all types of samples at the time when *n1* was pulled down to *n2* [16]. However, in Sample-C, Sample-D, and Sample-E, a V_{g_spike} was occurring during the *n2* interval, and the values were 12.8 V, 13.6 V, and 12.5 V. These values were very close to that

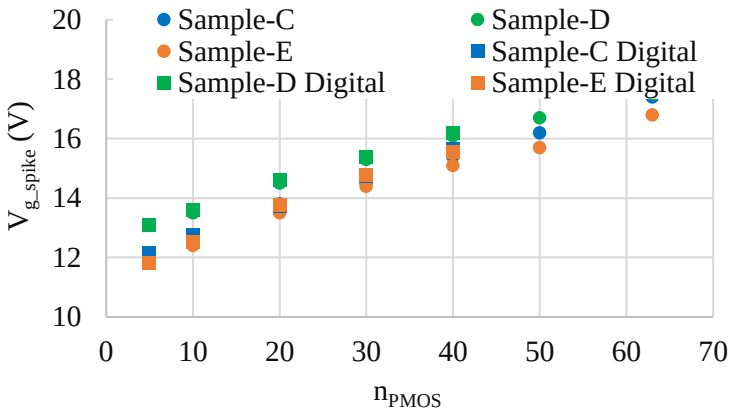

Fig. 3.33 The relation of V_{g_spike} and n_{PMOS}

under the mentioned conventional conditions in Fig. 3.15, Fig. 3.16, and Fig. 3.17. The comparison of V_{g_spike} between digital gate driving and conventional gate driving under different n_{PMOS} conditions are also shown in Fig. 3.33. The n_{PMOS} for digital gate driving in Fig. 3.33 represents *n2*. V_{g_spike} values were very close to that in the conventional gate driving under different n_{PMOS} conditions. This point also verified that the V_{g_spike} was generated by the current imbalance resulting from asymmetric L_e. Therefore, small V_{g_spike} and low E_{on} can be realized at the same time by the digital gate driving. In

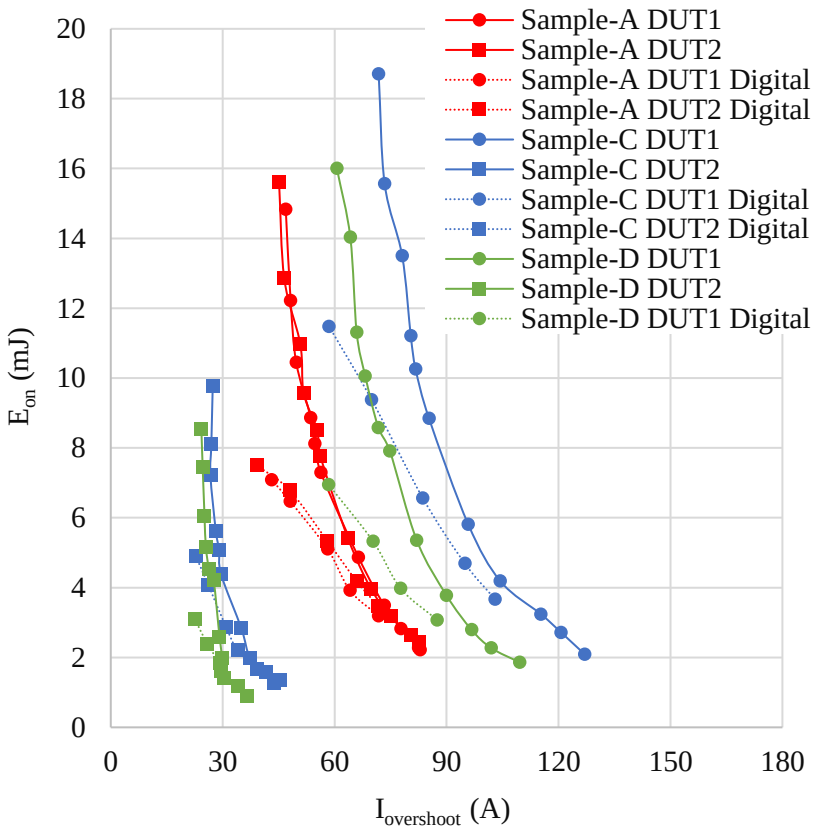

Fig. 3.34 The tradeoff relation of E_{on} and $I_{overshoot}$ under conventional gate driving and digital gate driving.

addition, the turn-on loss imbalance can also be suppressed when the L_e is asymmetric. For example, the E_{on} of DUT1 and DUT2, E_{on1} and E_{on2}, were 16 mJ and 8.5 mJ in Sample-D as shown in Fig. 3.16. But in Fig. 3.31, they were 7 mJ and 3.1 mJ. The difference between E_{on}, ΔE_{on} in Sample-D decreased from 7.5 mJ to 3.9 mJ. This is because the energy loss during *n1* and *n3* intervals was decreased. As for the ΔI_e in Fig. 3.30, 3.31, and 3.32, they were about 130, which were equal to the value as n_{POMS} was 3.10 in Fig. 3.19. And there was no current imbalance in Sample-A and Sample-B. Therefore, the current imbalance is only dependent on the Le and there no impact of the three-step digital gate control method on ΔI_e.

Fig. 3.34 shows the tradeoff relation of E_{on} and $I_{overshoot}$ under conventional gate driving and digital gate driving. It was found that the tradeoff can be improved by the digital gate driving, too. And the suppression of loss imbalance can also be improved even though L_e is asymmetric. As for the turn-on characteristics, it is not necessary to consider L_g for power module design, because the V_{g_spike} and current imbalance are

introduced by asymmetric L_e. And no matter whether in conventional gate driving or digital gate driving, the asymmetric L_e generates the current imbalance. But, thanks to the three-step digital gate driving, the ΔE_{on} and V_{g_spike} can be suppressed a lot.

3.4 Conclusion

This chapter clarified the effect of asymmetric L_g and L_e inside power modules with two parallel-connected IGBTs on switching characteristics under conventional gate driving and digital gate driving. Under conventional gate driving, the asymmetric L_e generated a current imbalance in turn-off and turn-on, and the current in DUT with a larger L_e was smaller than the other one. When the L_g was asymmetric, the larger L_g slowed down the turn-off process of the corresponding DUT to make the current concentrate on the DUT. Hence, the current imbalance can be suppressed by decreasing the current in the DUT with smaller L_e, while increasing the current in the DUT with larger L_e after the Miller plateau in the turn-off interval. In the turn-on, a large V_{g_spike} was generated and positively corresponded to the value of ΔI_e resulting from asymmetric L_e. And the V_{g_spike} can be suppressed by small n_{PMOS} that slows down the turn-on speed. Under digital gate driving, both the tradeoff in turn-off and turn-on could be improved. In the turn-off, because the effect of L_g became more evident than that in conventional gate driving, ΔI_e and ΔE_{off} could be decreased furthermore by asymmetric L_g when L_e was asymmetric. But large L_g would generate a large V_{g_spike}. In the turn-on, applying a small n_{PMOS} for *n2*, small V_{g_spike}, and low E_{on} can be realized at the same time when the L_e is asymmetric. And the ΔE_{on} can be suppressed a lot. According to the above switching characteristics, there is no doubt that symmetric L_e and L_g are the best design when digital gate driving is applied. And the priority is making L_e symmetric. When the symmetric L_e is difficult to realize in practice, the asymmetric L_g can be applied to suppress ΔI_e and ΔE_{off} introduced by the asymmetric L_e in turn-off. Also, the small L_e should combine with small L_g, and large L_e should combine with large L_g. In addition, considering the V_{g_spike} in turn-off, the asymmetric L_g should not

be too large and gate driving vectors should be adjusted. Moreover, symmetric L_g and small internal resistance combining with asymmetric L_e is the worst design, because the imbalanced current will flow through the kelvin wire leading to large turn-off loss.

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CHAPTER 4. The mechanism of gate voltage spike

4.1 Background

As presented in the former chapters, DGD dynamically controls the gate drive current during switching, leading to complex and intense variations in gate current I_g and the generation of V_{g_spike} which could potentially damage the DGD. In chapter 1, the occurrence of V_{g_spike} corresponds to changes in the digital control vector, specifically when I_g is raised or lowered [1-5]. According to the fundamental principles of LC resonance circuits, V_{g_spike} is believed to be generated by inductance and capacitance. Previous research has shown that the gate inductance L_g of IGBT modules results in larger V_{g_spike}, and changes in the gate drive vector Δn reflecting dI_g/dt leading to increased V_{g_spike} [6-7]. However, the origin and impact of capacitance are still not fully understood.

This chapter reports the effect of input capacitance of IGBT on V_{g_spike} using IGBT modules with the same L_g but different input capacitance. The effect of DGD output impedance on V_{g_spike} was clarified by parallel-connected external capacitance C_{ex} and different digital control vectors.

4.2 The setup of double pulse tests

Figure 4.1 represents the circuit diagram for the double pulse test used to measure the switching characteristics of the IGBT module. Fig. 4.2 displays the turn-off waveforms in both conventional gate driving and digital gate driving setups. The similar method was used to drive IGBTs. When n_{NMOS} remains constant, it corresponds to the conventional gate driving for turn-off depicted in Fig. 4.2a. In digital gate driving, the turn-off vectors using digital gate driving employed in this study are depicted in Fig. 2b. *n1* was set to a large value of 35 to shorten the duration before I_e begins to decrease. As n_{NMOS} decreases, the gate resistance can be considered to decrease correspondingly.

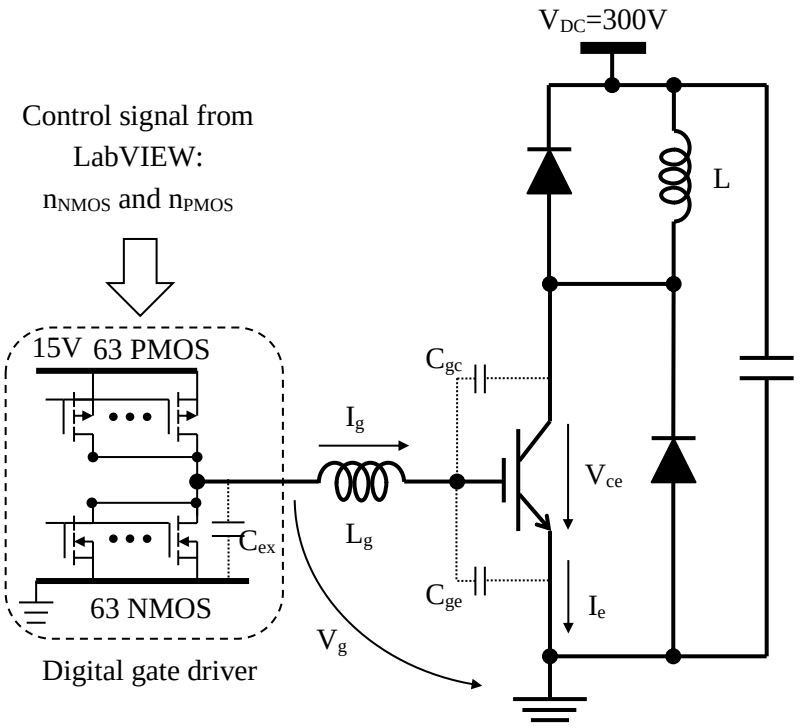


Fig. 4.1 Circuit schematic of experiment.

However, if *n1* is too large, dynamic avalanche in the IGBT occurs [8-9]. Hence, *n1* was set to 35 in this chapter. To suppress the gate voltage spike as small as that under the digital gate driving 35, 5, 63, the *n1*, *n2*, and *n3* should be set as about 5 in conventional gate driving. It is obvious that the turn-off delay time will prolong a lot, so the loss in this stage will be enlarged.

4.3 Effect of IGBT input capacitance on V_{g_spike}

Figure 4.3 presents the IGBT modules, specifically the FS50R12KT4_B15, FS75R12KT4_B15, and FS100R12N2T4 produced by Infineon, that were utilized for double pulse tests. These modules belong to the fourth generation 1200 V IGBTs, with respective current ratings of 50 A, 75 A, and 100 A. All three modules have identical package dimensions and nearly identical lengths of gate bonding wire, implying equal gate inductance across the modules. Based on the datasheet, the input capacitances are 2.8 nF, 4.3 nF, and 6.3 nF, respectively. The experiment setup is shown in Fig. 4.4.

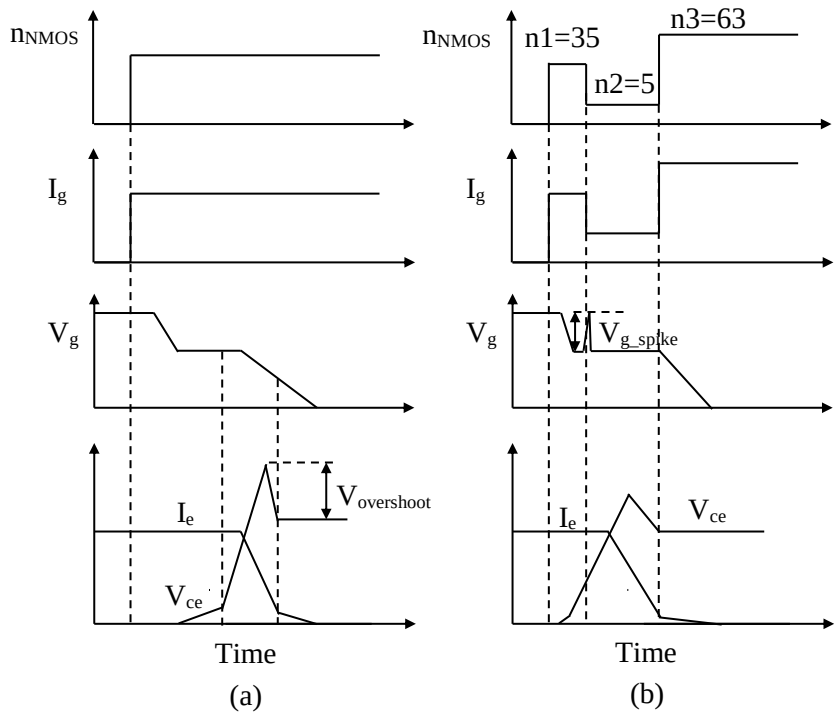
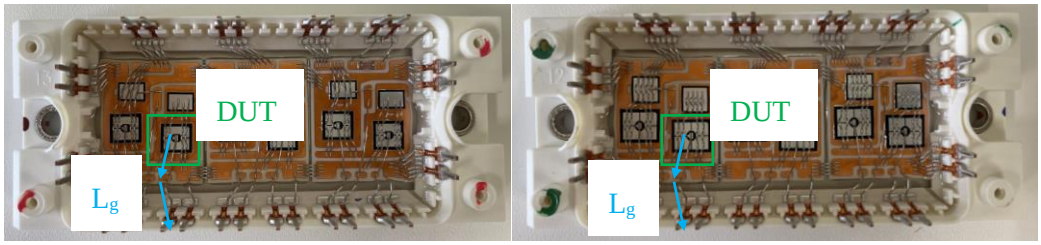
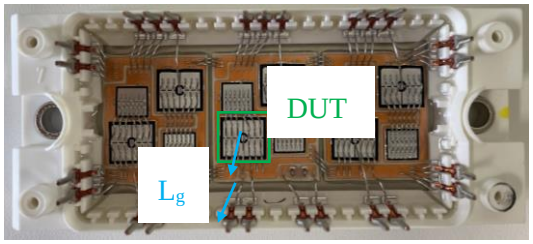


Fig. 4.2 Turn-off waveforms under (a) traditional gate driving and (b) digital gate driving.



FS50R12KT4_B15, 1200V/50A FS75R12KT4_B15, 1200V/75A



FS100R12N2T4,1200V/100A

Fig. 4.3 IGBT modules for double pulse test.

Figures 4.5, 4.6, and 4.7 show the turn-off waveforms of modules with rated currents of 50 A, 75 A, and 100 A, respectively. IGBTs with higher rated currents typically have larger input capacitances. To ensure consistent switching timings for the turn-off waveforms, the corresponding time interval were set to be longer. In each waveform,

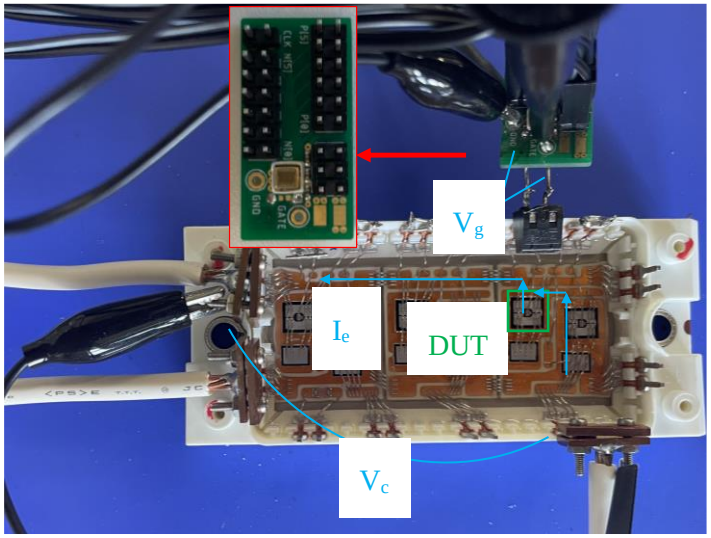


Fig. 4.4 Experiment circuit

the transition occurred from *n1* to *n2* before the voltage rising period, maintaining *n2* until beyond the voltage overshoot, and then switching to *n3*. The V_{g_spike} values observed in modules with rated currents of 50 A, 75 A, and 100 A were 6.67 V, 6.45 V, and 6.52 V, respectively. This demonstrates nearly identical levels. Consequently, it was deduced that V_{g_spike} is not directly correlated with the input capacitance of the IGBT.

4.4 Effect of DGD impedance on V_{g_spike}

To simulate the parasitic capacitance of the DGD, capacitors C_{ex} were connected in parallel to the gate terminal of the DGD, as illustrated in Fig. 4.1. In this section, double pulse tests were conducted on IGBT modules with a rated current of 50 A, employing C_{ex} values of 50 pF, 100 pF, 470 pF, 770 pF, and 1000 pF, as shown in Fig. 4.8.

Figures 4.9 to 4.13 show the turn-off waveforms with different C_{ex}. The 50 A-class IGBT module was used in hese tests, and the switching timings from *n1* to *n2* were kept consistent. The relationship between C_{ex} and V_{g_spike} is shown in Fig. 4.14. The overshoot was reduced slightly as shown in the Fig. 4.15. There is also a tradeoff relationship between E_{off} and $V_{overshoot}$ as C_{ex} is changed. As the C_{ex} was increased, the turn-off speed was slew down a little, so E_{off} was increased and $V_{overshoot}$ was decreased. As shown in Fig. 4.14 and Fig. 4.15, it is demonstrated that the V_{g_spike} and $V_{overshoot}$ are

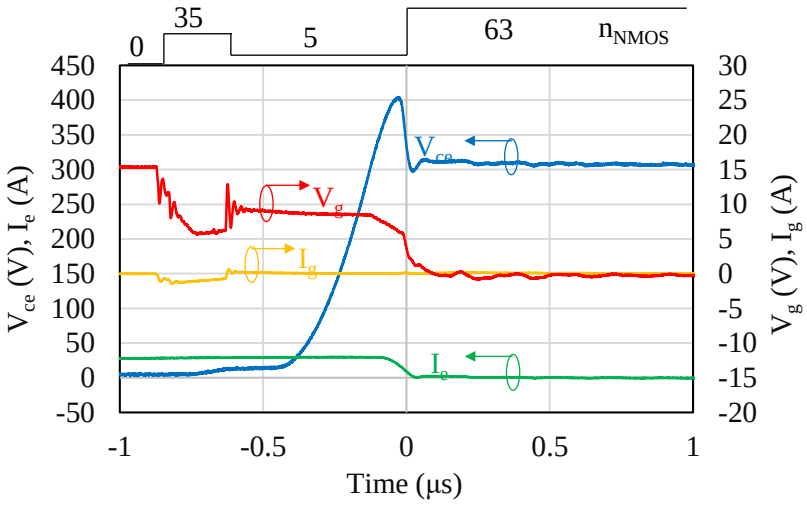


Fig. 4.5 Turn-off waveforms of 1200V/50A module.

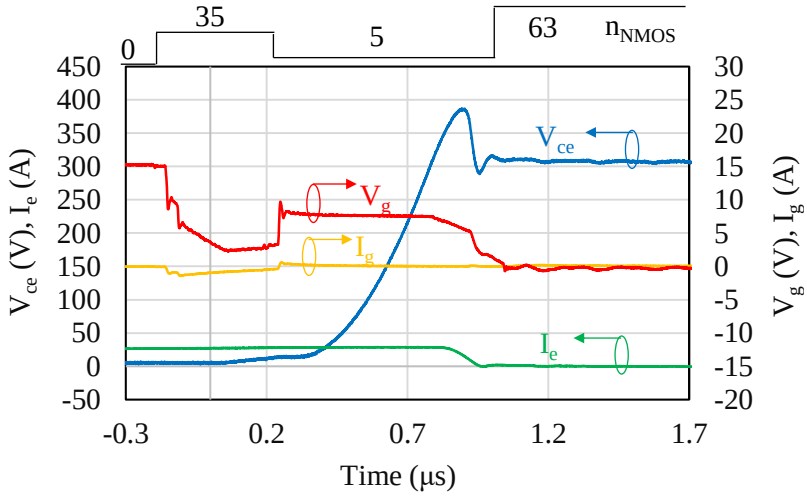


Fig. 4.6 Turn-off waveforms of 1200V/75A module.

decreased by increasing C_{ex}, but the E_{off} is increased. To present the improvement of turn-off performance, the results of the conventional gate driving where n_{NMOS} is 4 in the whole turn-off period are plotted in Fig. 4.15. Comparing to the results as C_{ex} was 1000 pF where overshoot was 97 V, the $V_{overshoot}$ was 94 V that they were at the same level. But the E_{off} as n_{NMOS} is 4 was increased to 2.8 mJ, while the E_{off} as C_{ex} is 1000 pF was 2.5 mJ. Although, the C_{ex} will slow down the turn-off speed leading to enlarged E_{off}, but thanks to the large value of n1 and n2 suppressing the loss, the E_{off} was even less than that in the conventional gate driving. Therefore, the increased C_{ex} can suppress V_{g_spike}, and the would be enlarged loss can be suppressed by digital gate driving. The

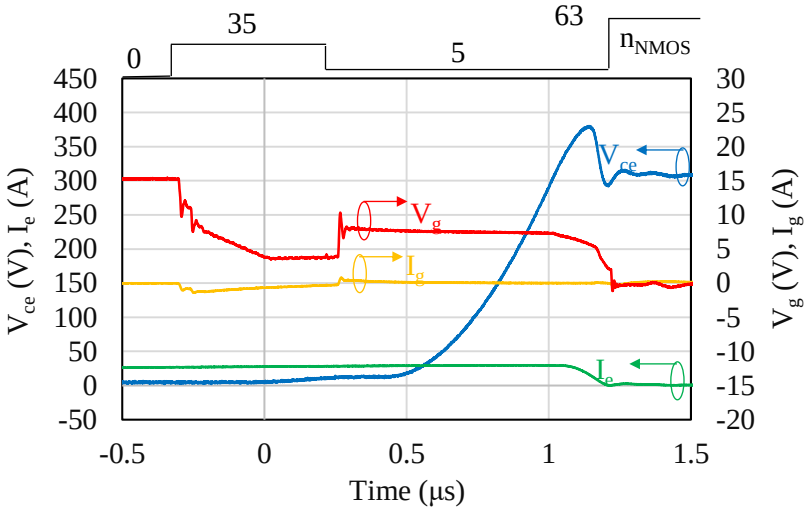


Fig. 4.7 Turn-off waveforms of 1200V/100A module.

Fig. 4.8 Parallel connection of DGD and C_{ex}.

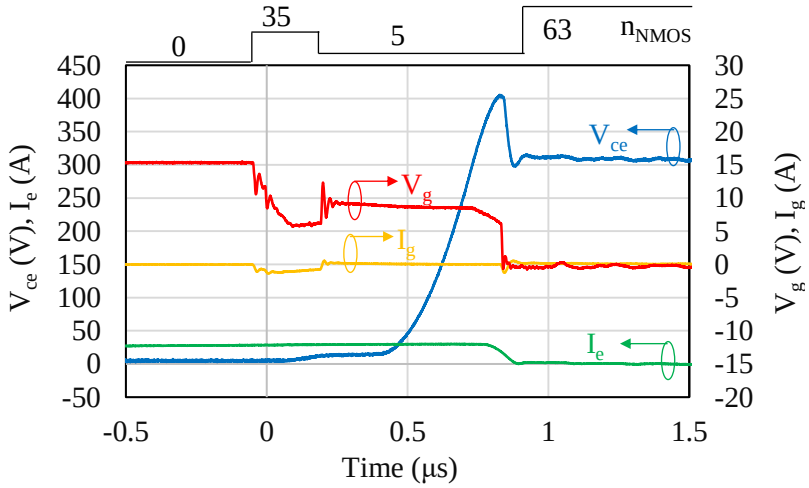


Fig. 4.9 Turn-off waveforms of 1200V/100A module as C_{ex} is 50pF.

Increasing C_{ex} decreased V_{g_spike}. Large parallel C_{ex} effectively decreases the output impedance of the DGD. Therefore, it is verified that the output impedance of the DGD

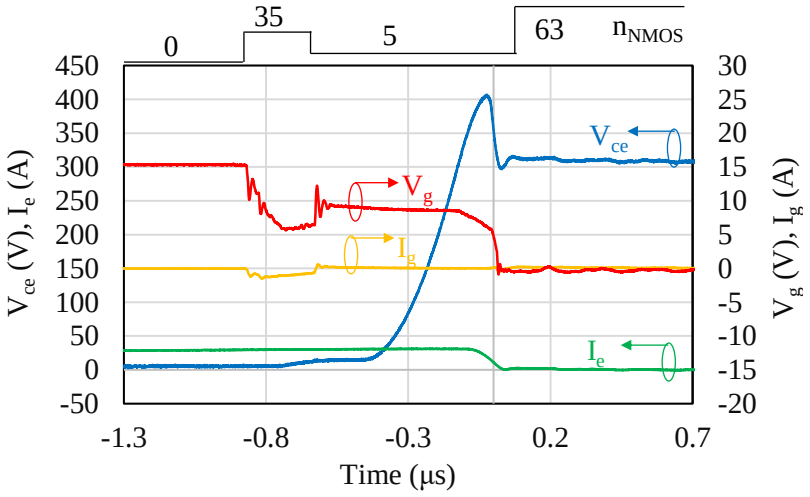


Fig. 4.10 Turn-off waveforms of 1200V/100A module as C_{ex} is 100pF.

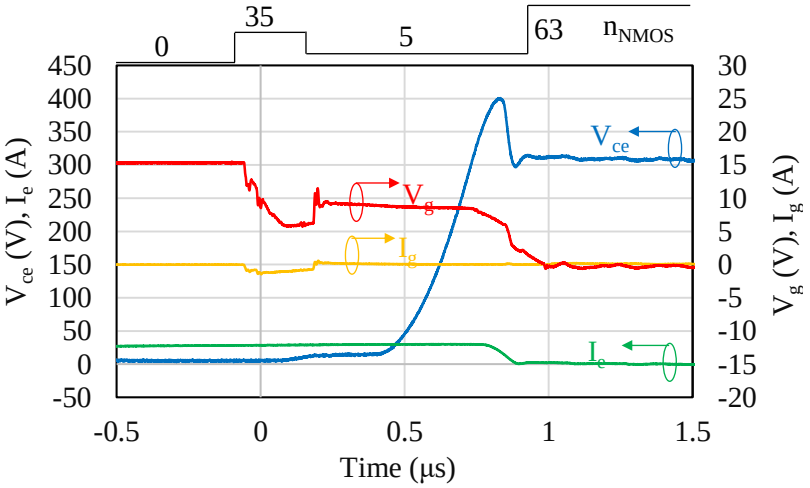


Fig. 4.11 Turn-off waveforms of 1200V/100A module as C_{ex} is 470pF.

influences on the V_{g_spike}. Next, turn-off waveforms were presented as DGD impedance was changed by control vector values. Fig. 4.16 shows the turn-off waveform when *n1* and *n2* were set to 40 and 10, respectively, in the absence of C_{ex}. The observed V_{g_spike} was 5.55V, which was more than 1 V lower than the condition shown in Fig. 4.5 even with the same Δn = 30 (*n1* = 35, *n2* = 5) setup. Decreasing *n2* essentially increases gate resistance, indicating higher DGD output impedance. Therefore, similar to the experiments manipulating parallel C_{ex} as mentioned earlier, it was confirmed that V_{g_spike} is influenced by the DGD output impedance.

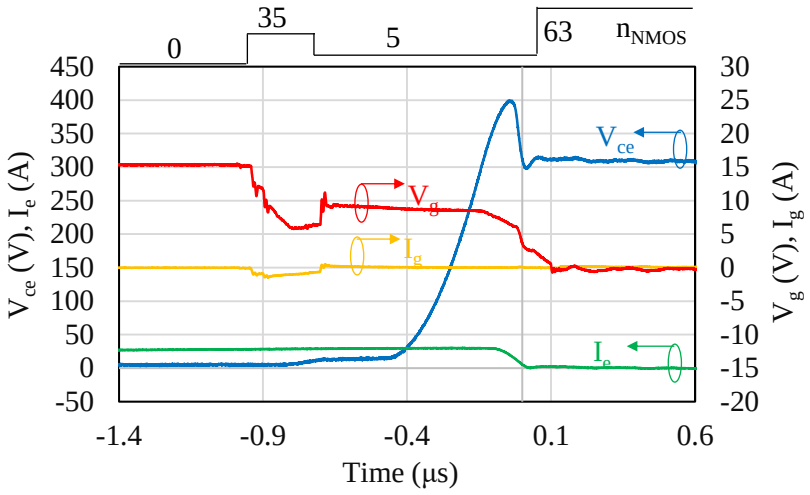


Fig. 4.12 Turn-off waveforms of 1200V/100A module as C_{ex} is 770pF.

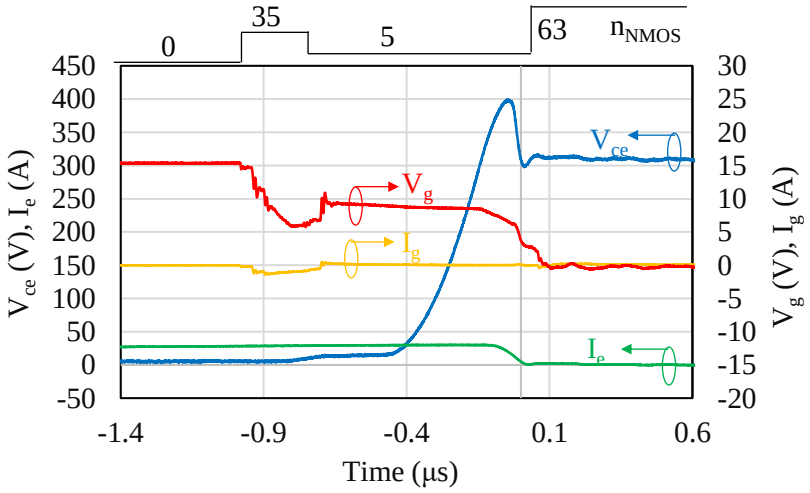


Fig. 4.13 Turn-off waveforms of 1200V/100A module as C_{ex} is 1000pF.

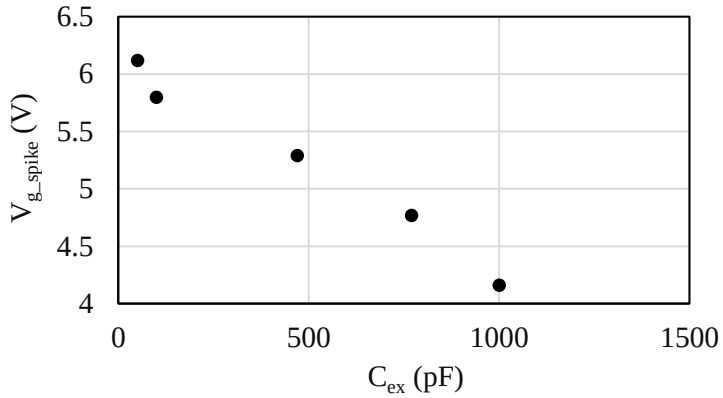


Fig. 4.14 The relationship of V_{g_spike} and C_{ex}.

In the chapter 2 and 3, it has been clarified that V_{g_spike} is proportional to the Δn between *n1* and *n2* [14-15]. This is because Δn determines ΔI_g, and V_{g_spike} is generated

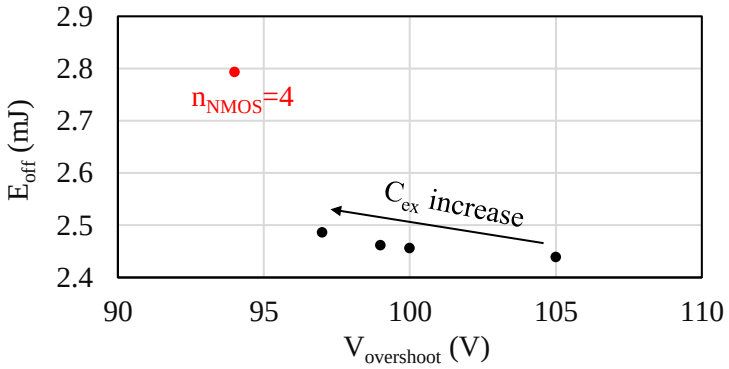


Fig. 4.15 The relationship of $V_{overshoot}$ and E_{off}.

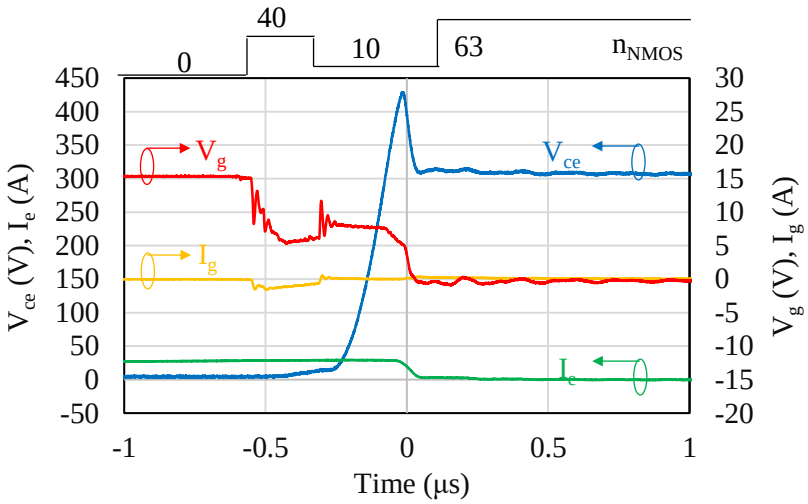


Fig. 4.16 Turn-off waveforms of 1200V/50A module as n1 is 40 and n2 is 10.

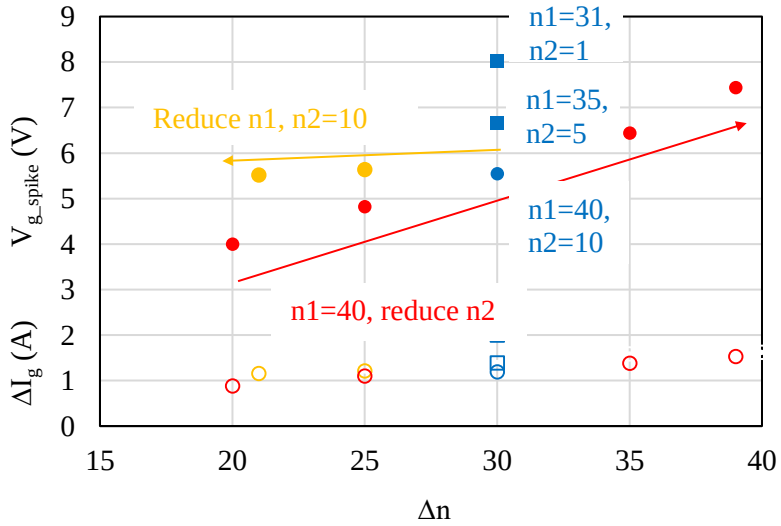


Fig. 4.17 The dependence of V_{g_spike} and ΔI_g on Δn.

by the combination of parasitic inductance L_g and ΔI_g. Considering that the output impedance of the DGD varies with control vectors, ΔI_g is changed by the control vectors.

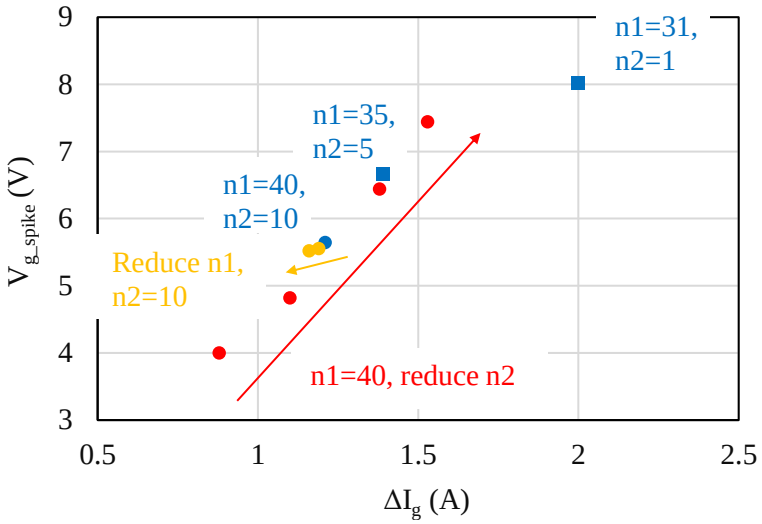


Fig. 4.18 The dependence of V_{g_spike} on ΔI_g.

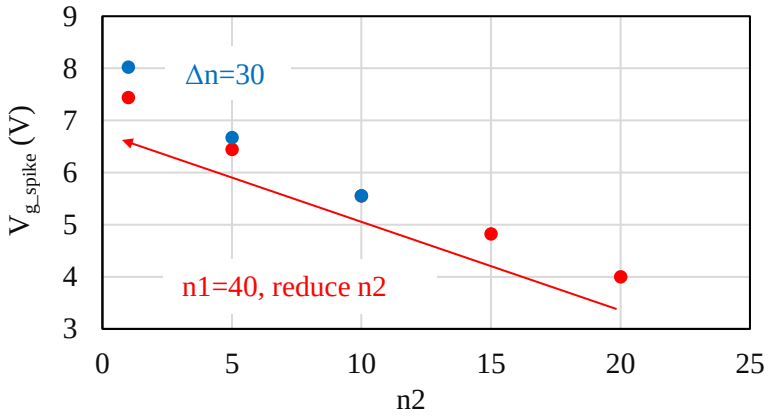


Fig. 4.19 The relationship of n2 and V_{g_spike}.

Consequently, V_{g_spike} depends on these control vectors. To further investigate this dependency, the results of three control patterns were tested, as shown in Fig. 4.17: 1) varying *n1* and *n2* while maintaining Δn = 30 (blue points), 2) decreasing *n2* while keeping *n1* constant at 40 (red points), and 3) increasing *n1* while maintaining *n2* at 10 (yellow points). The figure also includes the ΔI_g at the moment of transition from *n1* to *n2*.

In Pattern 1), despite a constant Δn, the decrease in n2 resulted in a significant increase in ΔI_g, consequently leading to an elevation increase in V_{g_spike}. In Pattern 2), the reduction in *n2* led to a larger Δn and, correspondingly, a substantial increase in ΔI_g, causing a significant rise in V_{g_spike}. However, in Pattern 3), the decrease in *n1* resulted in a smaller Δn, but the change in ΔI_g was minor and led to a small reduction in V_{g_spike}.

Summarizing the ΔI_g dependency of V_{g_spike} across these patterns, as presented in Fig. 4.18, it is evident that V_{g_spike} is nearly proportional to ΔI_g. Moreover, relationships of V_{g_spike} and *n2* for pattern 1) and pattern 2) are plotted in Fig. 4.19. In the pattern 1), when *n2* is decreased leading to large Δn and ΔI_g, there is large V_{g_spike} occurring. In the pattern 3), the V_{g_spike} also decreases with the decreased *n2*.

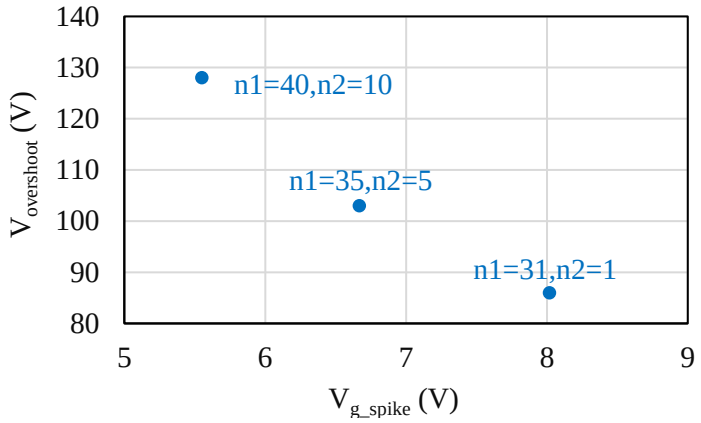


Fig. 4.20 The relationship of V_{g_spike} and $V_{overshoot}$ as Δn is 30.

Based on the aforementioned results, the mechanism behind V_{g_spike} generation is discussed. When the control vector of the DGD transitions from larger to smaller values, the output impedance of the DGD sharply increases. The parasitic gate inductance L_g serves as a current source, attempting to sustain the I_g flow. However, the rapid increase in output impedance hinders the flow of I_g, leading to a significant ΔI_g, which in turn causes the occurrence of V_{g_spike}. Since V_{g_spike} is proportional to both L_g and ΔI_g, when *n2* is large, the ability to sustain a certain I_g level is feasible, leading to a smaller ΔI_g and consequently reducing V_{g_spike}. The variation in DGD output impedance surpasses the impedance of the internal capacitance of the IGBT chip. Consequently, this mechanism results in equivalent V_{g_spike} values across IGBT modules even with different current ratings.

Finally, the consideration of collector voltage surge, $V_{overshoot}$ is discussed. As demonstrated in Fig. 4.16 and Fig. 4.5, increasing *n2* from 5 to 10 effectively reduced V_{g_spike}. Although the V_{g_spike} was decreased, $V_{overshoot}$ increased from 103V to 128V. This rise in $V_{overshoot}$ can be attributed to the accelerated turn-off speed resulting from

the larger *n2*, leading to a substantial increase in dI_e/dt. Consequently, there is a trade-off relationship between V_{g_spike} and $V_{overshoot}$ in Fig. 4.20 containing three points under three different conditions as Δn is kept as 30. From a viewpoint of safety operation, it becomes crucial to prioritize either minimizing V_{g_spike} or $V_{overshoot}$. Therefore, determining the appropriate *n2* setting necessitates careful consideration of this trade-off. Additionally, improvement of the V_{g_spike} - $V_{overshoot}$ trade-off requires the reduction of L_g.

4.5 Conclusion

This chapter reports the mechanism of the gate voltage spike generated during IGBT turn-off operation controlled by a DGD. Turn-off waveforms of IGBT modules with the same L_g but different input capacitances were measured, indicating that V_{g_spike} was not dependent on the IGBT input capacitance. Conversely, when C_{ex} was parallel connected to the DGD, increasing C_{ex} resulted in the reduction of V_{g_spike}. Furthermore, reducing V_{g_spike} was achieved by increasing the control vector value *n2*. These results verify that V_{g_spike} depends on the output impedance of the DGD. Variations in the DGD output impedance cause changes in ΔI_g, leading to the induction of V_{g_spike} due to L_g. Although increasing *n2* leads to V_{g_spike} reduction, it results in a trade-off where $V_{overshoot}$ increases. Improving this trade-off relationship necessitates the reduction of parasitic inductance.

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CHAPTER 5. Summary

Power modules are one of the most important key devices to improve the efficiency in electricity generation, transmission, distribution, and end-user applications to realize the carbon neutral. Improving the switching performance is vital to improve the efficiency of power systems. and suppress the gate voltage spike at the same time as the digital gate driver is applied. New packages of IGBT power modules and active gate drivers can improve the switching performance of IGBT modules at certain extent. Integrating the digital gate driver into IGBT modules is a method to fully take advantage of them. To integrate the DGD into the power modules as new type of digital IPM in the future, this thesis clarified the design requirements of IGBT modules when the DGD is applied.

Firstly, by experimental clarification of three one-IGBT-chip modules with different L_g, the occurrence of gate voltage spikes that pose a potential risk of damaging the DGD was reproduced. The trade-off between switching losses and overshoot was improved with digital gate control, but significant V_{g_spike} occurred during turn-off. It was observed that V_{g_spike} positively correlates with the changes in L_g and the gate drive vector. Achieving a balance between trade-off improvement and suppression of gate voltage spikes requires reducing the L_g of IGBT modules driven by DGD.

Subsequently, an examination of the switching characteristics of parallel-connected IGBT modules under digital gate control was conducted. Experimental results demonstrated that, during turn-off, the current imbalance caused by asymmetric L_e could be improved by varying L_g. And there is a similar relationship of V_{g_spike} and L_g as that in one-IGBT-chip modules. Interestingly, during turn-on, V_{g_spike} remained unaffected by L_g but was influenced by ΔI_e resulting from asymmetric L_e. Additionally, employing a small digital drive vector proved effective in suppressing current overshoot and addressing imbalances during turn-on caused by asymmetric L_e.

The design considerations for power modules driven by the digital gate driver can be summarized as follows. If an improvement is required where the tradeoff between $V_{overshoot}$ and E_{off} is such that the f_{obj} is not less than y, then Δn should exceed a specified value denoted as x. This is due to the observed negative relationship between f_{obj} and Δn illustrated in Figure 2.24. In the case where the critical voltage of the digital gate driver IC is 10 V, the intersection point of V_{g_spike} = 10 V and Δn = x in Fig. 2.21 must lie on a curve representing the relationship between V_{g_spike} and Δn. The corresponding L_g for this curve represents the maximum value of L_g capable of preventing overvoltage damage to the driver IC while achieving the required improvement in the tradeoff. It is worth noting that even though the critical voltage of the digital gate driver IC is 15 V presently, there is an expectation of the release of ICs with smaller critical voltages in the future, considering the reduction trend of IGBT driving voltage.

For parallel-connected IGBT modules with symmetric L_e, the total L_g design is similar to that of single IGBT chip modules. However, when L_e cannot be symmetric, consideration should also be given to the V_{g_spike} during turn-on. Another tradeoff arises concerning the enlargement of the difference in L_g corresponding to IGBTs to suppress V_{g_spike} during turn-on while maintaining a consistently small L_g to suppress V_{g_spike} during turn-off. Resolving this issue is important for proposing more practical design requirements for parallel-connected IGBT modules in the future.

Finally, the mechanism of gate voltage spike was clarified. To address this, the turn-off waveform was focused to investigate the influence of IGBT input capacitance on V_{g_spike} using IGBT modules with the same L_g and different input capacitances. The impact of parasitic capacitance and impedance in the DGD side using external capacitance C_{ex} and control vector value adjustments was implemented. Experimental results revealed that V_{g_spike} was independent of IGBT input capacitance. On the other hand, when C_{ex} was parallelized with DGD, increasing C_{ex} resulted in a reduction of V_{g_spike}. Additionally, enlarging the gate drive vector led to a decrease in V_{g_spike}. It was demonstrated that V_{g_spike} depends on the output impedance of DGD. Changes in DGD's

output impedance cause variations in I_g, generating V_{g_spike} due to induced voltage in L_g.

In this study, we conducted the design verification of IGBT modules applicable to the digital driver through simulations and experiments. In this thesis, the requirements to suppress gate voltage spike were proposed by experiment of fabricated IGBT modules and clarification of spike mechanism. And the design requirements to suppress current imbalance during switching period were also introduced for parallel IGBT modules. These results provide design direction for integrating the digital gate driver into IGBT modules in the future.

LIST OF PUBLICATIONS

Papers:

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1. **Zaiqi Lou**, Wataru Saito, Shin-ichi Nishizawa, Investigation of Acceptable Breakdown Voltage Variation for Parallel-Connected SiC MOSFETs during Unclamped Inductive Switching Test, *Japanese Journal of Applied Physics*, vol. 60, SBBD18, 2021.
2. **Zaiqi Lou**, Keiji Wada, Wataru Saito, Shin-ichi Nishizawa, Investigations on acceptable breakdown voltage variation of parallel-connected SiC MOSFETs applied to solid-state circuit breakers, *Microelectronics Reliability*, vol. 126, 114270, 2021.
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Doctor Course

5. **Zaiqi Lou**, Thatree Mamee, Katsuhiro Hata, Makoto Takamiya, Shin-ichi Nishizawa, and Wataru Saito, IGBT Power Module Design for Suppressing Gate Voltage Spike at Digital Gate Control, *IEEE Access*, vol. 11, pp. 6632-6640, 2023.
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