Enhanced mobility of Sn-doped Ge thin-films (≦50 nm) on insulator for fully depleted transistors by nucleation-controlled solid-phase crystallization

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ABSTRACT

High-speed fully depleted thin-film transistors (TFTs) for low-power consumption are required for next-generation electronics, such as three-dimensional large-scale integrated circuits and advanced system-in-displays. For this purpose, high-carrier-mobility semiconductor thin-films (thickness: $\leq\sim$50 nm) on insulator structures should be fabricated under low-temperature processing conditions ($\leq$500 °C). To achieve this, solid-phase crystallization of amorphous GeSn (a-GeSn) with low Sn concentration (2%) is investigated for a wide range of film thicknesses (30 − 200 nm), where thin a-Si underlayers (thickness: 0 − 20 nm) are introduced between a-GeSn films and substrates. GeSn is polycrystallized by annealing at 450 °C, keeping Si underlayers amorphous. Crystal grains of almost identical sizes are obtained for GeSn thicknesses of 30 − 50 nm, though grain sizes significantly decrease for thicknesses exceeding 50 nm owing to enhanced bulk nucleation. A detailed analysis of GeSn films (thickness: 50 nm) reveals that grain sizes are decreased by introducing a-Si underlayers (thickness: 3 − 20 nm), e.g., from $\sim$10 μm to 2 − 3 μm. This phenomenon is attributed to the change in dominant nucleation sites from the interface to the bulk, which significantly decreases grain-boundary scattering of carriers through a decrease in the barrier heights at grain boundaries. As a result, a high carrier mobility of 200 − 300 $cm^2/V\,s$ is realized for GeSn thin-films (thickness: 30 − 50 nm) grown with a-Si underlayers. The mobility (200 − 300 $cm^2/V\,s$) is the largest ever reported data for Ge and GeSn thin-films (thickness: 30 − 50 nm) grown at low temperatures ($\leq$500 °C). This technique will facilitate the realization of high-speed fully depleted TFTs for next-generation electronics.

Germanium is attracting much attention as channel materials for high-speed transistors, owing to its higher carrier mobility compared with Si.[1–5] To realize next-generation electronics, such as three-dimensional large-scale-integrated circuits (3D-LSIs) and advanced system-in-displays, Ge thin-film transistors (TFTs) should be fabricated on an insulator at low temperatures ($\leq$500 °C). Thus, the low-temperature formation of Ge-on-insulator (GOI) is a hot topic for semiconductor processing.[6,7] To achieve high speed and low-power operation, the development of fully depleted TFTs is desired. For this purpose, Ge thin-films with thicknesses below $\sim$50 nm are required.

Various formation methods, e.g., metal-induced lateral crystallization (MILC),[8,9] melt-growth by laser-annealing (LA),[10,11] flashlamp annealing (FLA),[12] and solid-phase crystallization (SPC),[13,14] have been investigated to obtain high quality GOIs. Among them, SPC has the advantages of no metal contamination or melting-induced surface ripple. These are very important advantages for high-density integration of TFTs.

We have therefore developed two-step SPC of amorphous Ge (a-Ge), i.e., 425 °C growth followed by 500 °C annealing, enabling independent control of grain growth and defect annihilation. This yields a GOI (Ge thickness: 50 nm) with a mobility of 140 $cm^2/V\,s$.[14] Although this value is higher than that ($\leq\sim$20 $cm^2/V\,s$) of oxide[15] and organic semiconductors,[16] the improvement in mobility ($\geq$200 $cm^2/V\,s$) is needed for the application of not only display-pixel drivers but also advanced electronic circuits such as information processors. Recently, Imajo *et al.* investigated the densification of a-Ge on GeO_2-coated substrates by substrate heating during Ge-deposition and obtained poly-Ge thick films (thickness: 500 nm) with high mobility (620 $cm^2/V\,s$).[17] However, owing to their large thickness (500 nm), the films cannot be used for fully depleted transistors.

On the other hand, Sn-doping into Ge is attracting much attention.[18–20] An important effect of Sn doping is the passivation of vacancy-related defects. Nakatsuka *et al.*[21] reported that the introduction of a small amount of Sn (∼2%) eliminates vacancy-related defects in Ge. Takeuchi *et al.*[22] investigated the effects of Sn-doping on mobility in poly-GeSn (thickness: 300 nm) grown by SPC (450 °C) and demonstrated mobility improvement from 30 to 130 $cm^2/V\,s$ by Sn doping (2%).

We comprehensively investigated SPC of a-GeSn on an insulator (fused quartz substrates) and clarified that the competition between interface nucleation and bulk nucleation significantly affects the electrical properties of grown films.[23] Consequently, we achieved high mobility (320 $cm^2/V\,s$) by selecting a Sn concentration (2%) and thickness (200 nm) to control competition between them.[23] However, in this previous study, mobility still degraded near insulating substrates (≤∼120 nm).[23] This indicates that crystal grains initiated from interface nucleation degrade mobility.

For the realization of fully depleted transistors with high mobility, mobility in Ge thin-films (thickness: ≤50 nm) should be improved. The above-mentioned finding in our previous study[23] leads to an idea that mobility can be improved by suppressing interface nucleation. Here, interface nucleation can be modulated by changing the interface energy. Because the interface energy of two materials depends on the surface energy of the respective materials,[24] interface energy can be changed by the surface energy of the substrates. The surface energy of fused quartz (∼70 mJ/m^2)[25] is significantly smaller compared with Ge (1.1 − 1.8 J/m^2).[26] However, a-Si has a surface energy (∼1 J/m^2)[27] similar to that of Ge. Thus, introduction of a-Si underlayers into a-GeSn/substrate interfaces will modulate interface nucleation in a-GeSn.

To examine this, in the present study we investigate the effects of introducing a-Si underlayers into a-GeSn/substrate interfaces on SPC characteristics and the electrical properties of grown films. We clarify that introduction of a-Si underlayers effectively suppresses interface nucleation. Consequently, poly-GeSn having very high mobility (∼300 $cm^2/V\,s$), which is the highest ever among reported data on Ge and GeSn thin-films (thickness: ≤50 nm) grown at low temperatures (≤500 °C),[12,14,23] is achieved.

In the experiment, a-Si (thickness: 0 − 20 nm) and a-GeSn (Sn concentration: 2%, thickness: 30 − 200 nm) were deposited on fused quartz substrates at room temperature using a molecular-beam deposition system (base pressure: $\sim 5 \times 10^{-10}$ Torr), then they were annealed at 350 °C for 10 min in the deposition chamber without breaking a vacuum. The sample structure is shown in Fig. 1. The samples were annealed (450 °C, 1 − 40 h) to induce SPC in the nitrogen environment using an electric furnace, where the sample temperatures were controlled using a thermocouple attached to the sample holder.

The crystallinity of the grown layers was investigated using Raman spectroscopy. Raman spectra of samples (GeSn thickness: 50 nm, Si thickness: 5 nm) before and after annealing (450 °C, 20 h) are shown in Fig. 1, together with the data on an annealed sample without a Si underlayer. After annealing, Raman peaks caused by Ge-Ge bonding in crystalline GeSn are observed. The spectra shown in Fig. 1 were obtained from the top-side of samples, and similar spectra were obtained from the top-side of other samples (Si thickness: 3, 10, and 20 nm). In addition, similar spectra were obtained from the back-side of samples through transparent substrates for all samples (Si thickness: 0 − 20 nm), and no peaks due to crystalline Si or SiGe were detected. This indicates that Si underlayers remain amorphous, and intermixing with GeSn is not generated by annealing for samples with a wide range of Si thicknesses (3 − 20 nm).

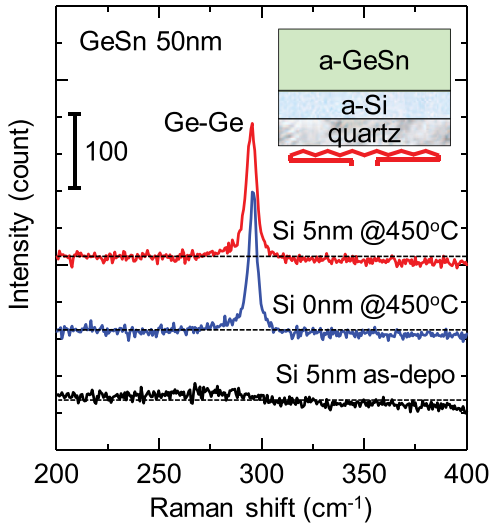

FIG. 1. Raman spectra of samples (GeSn thickness: 50 nm, Si thickness: 0 and 5 nm) before and after annealing (450 °C, 20 h). Raman measurements were performed from the top-side of the samples. The inset shows a schematic initial sample structure. The dotted lines show the baselines of the respective spectra.

Electrical properties of grown GeSn layers were evaluated using Hall effect measurements. The measurements indicated p-type conduction for all samples, which was attributed to acceptor levels of vacancy-related defects in Ge.[28,29] The mobility and the carrier concentration in grown films (GeSn thickness: 50 nm) are summarized as a function of Si thickness in Fig. 2(a). The mobility of samples with a-Si underlayers (thickness: 3 − 20 nm) becomes high (280 − 300 $cm^2/V\,s$) compared with that without an a-Si underlayer (∼220 $cm^2/V\,s$). However, carrier concentrations are constant ($\sim 5 \times 10^{17}\ cm^{-3}$) for all samples with or without a-Si underlayers in a wide range of a-Si thicknesses (0 − 20 nm). Because holes in grown films are generated from vacancy-related defects,[28,29] this result indicates that concentrations of vacancy-related defects in grown films are not changed by introduction of a-Si underlayers.

Grain structures were analyzed using electron backscattering diffraction (EBSD) measurements. Grain sizes for samples (GeSn thickness: 50 nm) are summarized as a function of a-Si underlayer thickness in Fig. 2(b), where typical EBSD images (Si thickness: 0 and 5 nm) are also shown. Grain sizes decreased from ∼10 to 2 − 3 μm upon introducing a-Si underlayers (thickness: 3 − 20 nm). Simultaneously, preferentially (100)-oriented grains for the sample without an a-Si underlayer change into randomly oriented grains, as shown in the EBSD images. This suggests that preferentially oriented interface nucleation is suppressed by the modulation of the interface energy through the introduction of a-Si underlayers, which makes randomly oriented bulk nucleation dominant. Interestingly, these results indicate that randomly oriented small-grain films of samples with a-Si underlayers show higher mobility than the preferentially oriented large-grain film of the sample without an a-Si underlayer.

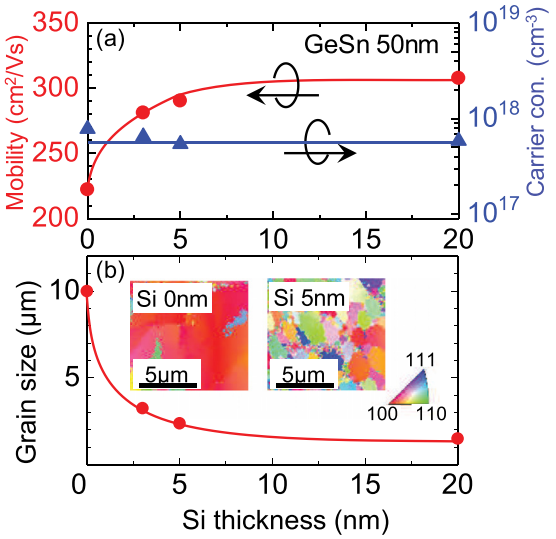

FIG. 2. Si underlayer thickness dependence of (a) carrier mobility and carrier concentration and (b) grain size for samples (GeSn thickness: 50 nm) after annealing (450 °C, 20 h). EBSD images of the samples (Si thickness: 0 and 5 nm) are also shown in (b).

Figure 2 indicates that the carrier mobility and grain sizes weakly depend on the a-Si thickness in the region of 3 – 5 nm. One possible reason is the local mixing of very thin a-Si films and GeSn films, which results in local direct contact of GeSn with the quartz substrates. However, no Raman peaks due to Si-Ge bonding were detected by Raman measurements. Further investigation is needed to reveal these phenomena.

To demonstrate that interface nucleation is retarded by the introduction of a-Si underlayers, crystal structures were investigated after short-time annealing. EBSD images (GeSn thickness: 50 nm, Si thickness: 0 and 5 nm) after annealing (450 °C) for 1, 1.5, and 2 h are shown in Fig. 3. It is noted that randomly colored small dots observed in the EBSD images for the sample without an a-Si underlayer (annealing time: 1 h) and the samples with an a-Si underlayer (annealing time: 1 and 1.5 h) were caused by errors in identifying the orientation of the EBSD analysis, and similar small dots were observed for a-GeSn films before annealing. For the sample without an a-Si underlayer,

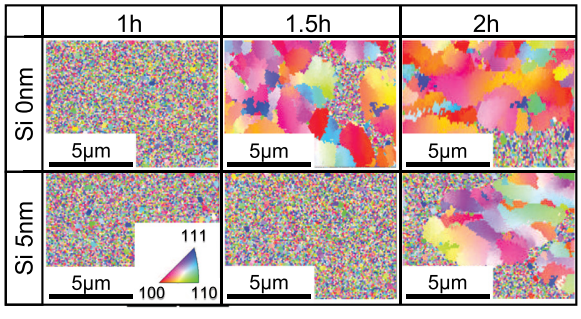

FIG. 3. EBSD images of samples (GeSn thickness: 50 nm) with different Si underlayer thicknesses (0 and 5 nm) after annealing at 450 °C for 1, 1.5, and 2 h.

preferentially (100)-oriented grains are observed from an annealing time of 1.5 h, where almost the whole area is covered with large crystal grains. However, a long annealing time (2 h) is required to detect crystal grains for the sample with an a-Si underlayer. Here, randomly oriented grains are dominant. Moreover, the fraction of the surface area covered with crystal grains for the sample (annealing time: 2 h) with an a-Si underlayer is smaller than that without an a-Si underlayer. These results clearly indicate that interface nucleation, dominant for the sample without an a-Si underlayer, is suppressed by the introduction of a-Si underlayers. Here, grain sizes become small by introducing a-Si underlayers, though nucleation becomes slow. This suggests that the areal density of interface nucleation is lower than that of bulk nucleation, and grain growth from interface nucleation is almost complete before bulk nucleation started.

To reveal the mechanism of mobility improvement, the electrical properties of grain boundaries are analyzed using a model proposed by Seto.[30] The mobility μ of polycrystalline semiconductors is expressed by the following equation:[30]

$$\mu = \frac{Lq}{\sqrt{2\pi m^* kT}} \exp\left(-\frac{E_B}{kT}\right), \tag{1}$$

where L is the crystal grain size, q the elementary charge, m^* the effective mass of carrier, k the Boltzmann constant, T the absolute temperature, and E_B the energy barrier height at grain boundaries. Here, the energy barrier height E_B is generated by trapping states with density Q_t at grain boundaries, and is given by the following equation:[30]

$$E_B = \frac{q^2 Q_t^2}{8\varepsilon N}, \tag{2}$$

where ε is the dielectric constant of the semiconductor and N the carrier concentration.

Figure 4(a) shows the Arrhenius plot of $\mu T^{1/2}$ (GeSn thickness: 50 nm, Si thickness: 0, 3, 5, and 20 nm). Respective data are fitted with straight lines, where slopes of lines are decreased for samples introduced with a-Si underlayers. From the slopes, the energy barrier height E_B is evaluated using Eq. (1), and the trapping state density Q_t is evaluated from E_B using Eq. (2). E_B and Q_t are summarized in Fig. 4(b). E_B for the sample without an a-Si underlayer is ~10 meV. The values significantly decreased to ~5 meV upon introducing a-Si underlayers. The figure also shows that Q_t decreased from $\sim 6 \times 10^{11}$ to $\sim 4 \times 10^{11}$ cm^{-2} upon introducing a-Si underlayers. These findings reveal that mobility improvement by the introduction of a-Si underlayers is caused by a significant decrease in energy barrier heights at grain boundaries because of a decrease in trapping state densities. Because bulk nucleation becomes dominant over interface nucleation by the introduction of a-Si underlayers, as revealed in Fig. 3, these results indicate that the boundaries of crystal grains initiated from interface nucleation show a higher density of trapping states compared with bulk nucleation. Further investigation is necessary to clarify the reason.

Crystal structures were investigated in more detail by transmission electron microscopy (TEM). Bright-field TEM and high-angle annular dark-field (HAADF) images of a sample (GeSn thickness: 50 nm, Si thickness: 5 nm) after annealing (450 °C, 20 h) are shown in Figs. 5(a) and 5(b), respectively. In addition, selected area electron diffraction (SAED) patterns obtained from regions #1 and #2 indicated in Fig. 5(a) are shown in Figs. 5(c) and 5(d), respectively. The SAED

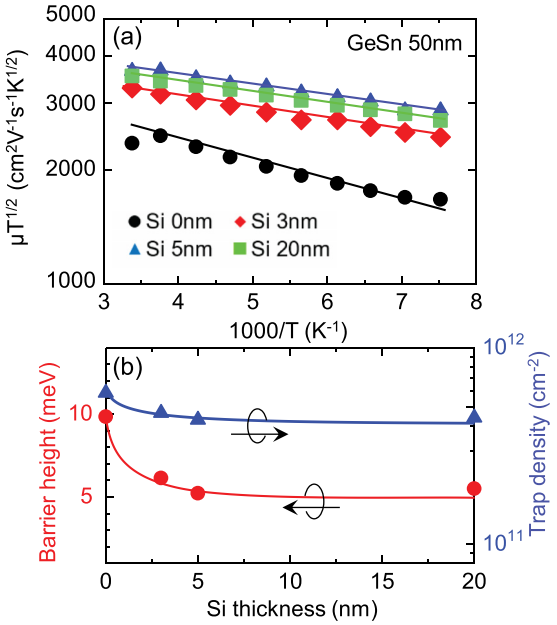

FIG. 4. (a) Arrhenius plot of $\mu T^{1/2}$ and (b) a-Si underlayer thickness dependence of the energy barrier height and the trapping state density at grain boundaries for samples (GeSn thickness: 50 nm, Si thickness: 0, 3, 5, and 20 nm) after annealing (450 °C, 20 h).

pattern shown in Fig. 5(c) indicates that the observed area consists of (131)-oriented crystal GeSn. However, the SAED pattern in Fig. 5(d) was obtained from region #2, where both GeSn and Si layers were included. The SAED pattern [Fig. 5(d)] consists of a diffraction pattern of (131)-oriented crystal GeSn and a halo pattern of amorphous Si. This indicates that Si underlayers remain amorphous, which agrees with the Raman measurement results.

The bright-field image [Fig. 5(a)] shows the flat top and bottom of the GeSn layer, and the HAADF image [Fig. 5(b)] indicates that Sn segregation, as reported for GeSn with a high Sn concentration (≥4.5%),[31] does not occur. These results clearly indicate that the introduction of a-Si underlayers does not deteriorate surface morphologies of grown GeSn layers or generate Sn segregation.

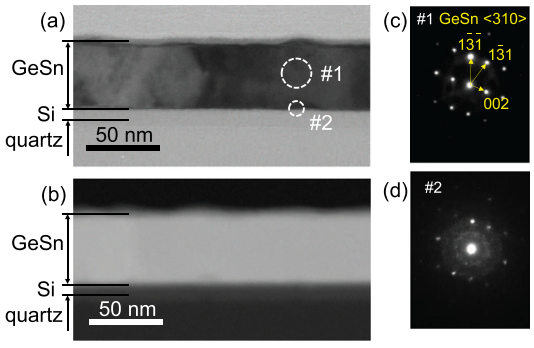

FIG. 5. (a) Bright-field TEM image, (b) HAADF image, and [(c) and (d)] SAED patterns of a sample (GeSn thickness: 50 nm, Si thickness: 5 nm) after annealing (450 °C, 20 h). The SAED patterns shown in (c) and (d) were obtained from regions #1 and #2, respectively, indicated by the circles in (a).

For advanced fully depleted TFTs with short channel lengths (≤100 nm), thinner GOI layers (thickness: ≤~30 nm) are required. Thus, we investigate the effects of GeSn thickness. The mobility and the carrier concentration of samples (GeSn thickness: 30 – 200 nm, Si thickness: 5 nm) are summarized as a function of GeSn thickness in Fig. 6(a). Upon decreasing GeSn thickness from 50 to 30 nm, mobility is decreased from ~300 to ~200 cm^2/V s, which suggests that the carrier mobility is limited by the interface scattering in addition to the grain-boundary scattering. Further study is needed to separate these scattering mechanisms. In the GeSn thickness region of 30 – 50 nm, carrier concentrations are almost constant at $\sim 5 \times 10^{17}\,cm^{-3}$. However, mobility is significantly decreased by increasing the GeSn

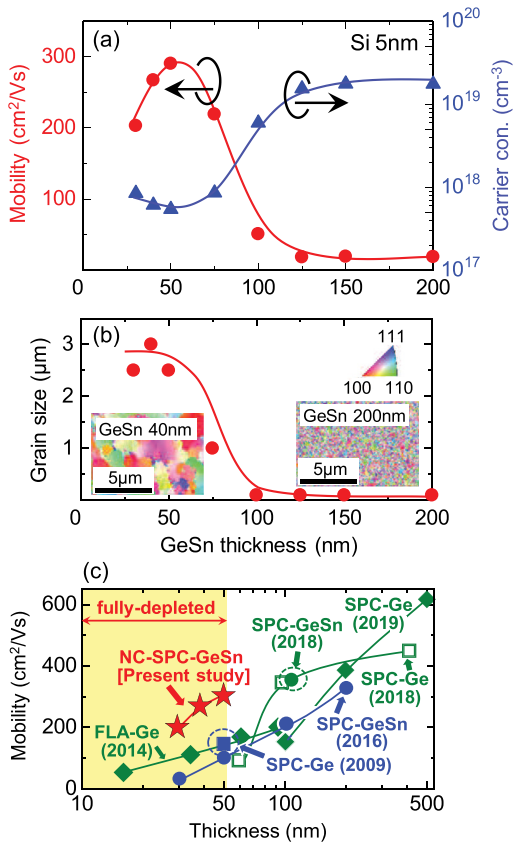

FIG. 6. GeSn thickness dependence of (a) mobility and carrier concentration and (b) grain size for samples (Si thickness: 5 nm) after annealing (450 °C), and (c) mobility of semiconductors grown on an insulator as a function of thickness. Annealing times for samples shown in (a) and (b) are 40 h (thickness: 30 nm) and 20 h (thickness: 40 – 200 nm). EBSD images of samples (GeSn thickness: 40 and 200 nm) are shown in (b). The mobility obtained in the present study [nucleation-controlled SPC (NC-SPC)] indicated by red symbols is compared with our previously reported data for SPC (≤500 °C) of pure a-Ge in 2009[14] and a-GeSn (Sn concentration: 2%) in 2016[23] indicated by blue symbols and other groups' data for SPC (≤500 °C) of pure a-Ge in 2018[32] and 2019[17] and a-GeSn (Sn concentration: 3%) in 2018,[33] and FLA of pure-Ge in 2014[12] indicated by green symbols in (c). The yellow hatching area in (c) indicates the thickness range for fully depleted transistors.

thickness above 50 nm. Simultaneously, carrier concentrations are increased toward $\sim 2 \times 10^{19}$ cm^{-3}.

Grain sizes of these samples, evaluated using EBSD, are summarized in Fig. 6(b), together with EBSD images (GeSn thickness: 40 and 200 nm). The grain sizes are almost constant ($2.5 - 3\ \mu$m) for a GeSn thickness of $30 - 50$ nm; however, they decreased below 1 μm for GeSn thicknesses above 50 nm due to the increase in areal densities of bulk nucleation with increasing GeSn thickness. These results explain well the decrease in mobility for GeSn thickness above 50 nm, shown in Fig. 6(a). However, the decrease in grain sizes for GeSn film thicknesses above 100 nm is very significant. Here, grain sizes ($\sim 0.1\ \mu$m) for GeSn thicknesses of $100 - 200$ nm obtained in the present study are almost equal to that of a thicker sample (GeSn thickness: 500 nm) without an a-Si underlayer.[23] This indicates that bulk nucleation becomes more dominant by the introduction of a-Si underlayers in the present study. Further study is needed to clarify details.

Figure 6(c) shows mobility obtained in the present study, and a comparison with the literature values for semiconductors directly grown on an insulator,[12,14,17,23,32,33] as a function of thickness, where data obtained by FLA[12] are shown together with those by SPC ($\leq 500\,^{\circ}$C). Since 2009, many researchers have intensively studied the growth techniques of Ge thin-films on an insulator. These efforts significantly improve the mobility of Ge films from ~ 140[14] to ~ 620 cm^2/V s.[17] However, most previous works employed Ge films with thicknesses above 100 nm, and no improvement has been obtained for thicknesses below 50 nm, essential to fully depleted devices. Figure 6(c) clearly shows that the mobility obtained using the present technique is the highest among the literature for thin (≤ 50 nm) Ge[12,14] and GeSn[23] films. In addition, the values of mobility ($200 - 300$ cm^2/V s) are significantly higher than those ($\leq \sim 20$ cm^2/V s) of other TFT channel materials, such as oxide semiconductors[15] and organic semiconductors.[16] Thus, the present technique is applicable to high-performance electronic circuits directly fabricated on LSIs and glass panels.

In summary, we have developed nucleation controlled SPC of GeSn on an insulator. By low-temperature annealing (450 °C) of a-GeSn/a-Si/fused quartz stacking structures, GeSn layers are polycrystallized while keeping Si underlayers amorphous. Introduction of a-Si underlayers (thickness: $3 - 20$ nm) suppresses interface nucleation in a-GeSn layers and makes bulk nucleation dominant over interface nucleation. Although this decreases grain sizes, e.g., from ~ 10 to $2 - 3\ \mu$m for a GeSn thickness of 50 nm, the energy barrier height at grain boundaries is significantly decreased, which remarkably increases the mobility. These phenomena are attributed to lower trapping state densities at the boundaries of crystal grains initiated from bulk nucleation compared with interface nucleation. Consequently, a very high mobility of $200 - 300$ cm^2/V s is realized for thin GeSn films (thickness: $30 - 50$ nm). This technique will facilitate the realization of high-speed fully depleted TFTs for low-power consumption essential to next-generation electronics, such as 3D-LSIs and systems-in-display.

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