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A New Method of The Active Gate Driver for Current Balancing in The Parallel MOSFET Circuits

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Abstract: MOSFETs are used in electronic circuits because they have high switching efficiency. Typically, MOSFETs are wired in parallel for applications that require high power. Theoretically, this circuit can multiply the current capability of parallel MOSFETs. However, even if all the MOSFETs in a parallel circuit have the same serial number and manufacturer, they might not necessarily have the same current characteristics. This could lead to issues with current imbalances, potentially causing harm to the MOSFETs, especially under severe circumstances. This study introduces a new Active Gate Driver (AGD) technique to balance the current in a parallel MOSFET circuit. The current difference can be used to modulate each MOSFET duty cycle. Specifically, the MOSFET with the smallest current capacity is configured as the Master, while the MOSFET following it is designated as the Slave. The interrupt time value for the duty cycle of each Slave MOSFET is influenced by the current differential between the Master and Slave. Consequently, different duty cycles for the Master and Slave MOSFETs can maintain the same current level. Based on the results of experiments conducted on three MOSFETs, it is evident that the AGD approach can effectively balance the current to an optimum level.

Keywords: Active gate driver; Current imbalance; MOSFET; Parallel circuit

1. Introduction

The development of electronic technology plays an important role in supporting a majority demand in various sectors, ranging from industry[1)], household needs, renewable energy[2)], electrical machines drivers[3)], and transportation[4)]. This development requires high-power and reliable electronic components. Sometimes, these power electronic components should function properly in harsh environments and have greater capabilities than other applications[4-7)]. Recently, MOSFETs have shown potential for high-power applicants due to high switching efficiency, high input impedance, fast switching speed, and low on-state resistance[8-12)]. However, sometimes a single MOSFET cannot withstand the high current, so multiple MOSFETs need to be assembled in parallel to increase current handling capability and improve reliability and system efficiency[8,9,13-24)]. A current imbalance phenomenon may occur in the parallel assembly MOSFET due to the difference in the characteristics of devices, inconsistencies in the parasitic loop parameters and the aging degree of the components. The current imbalance produces differentiation in transient current stress, power loss, and junction temperature among the MOSFETs, which affects a decline in device performance, increased thermal failure, and potentially leads to device failure[1,11,14-16,25-29)]. Therefore, the evenly current share control for parallel assembly MOSFETs is required. In recent years, several MOSFET driver methods have been studied to solve this issue. One of these methods is known as Active Gate Driver (AGD). However, there are still some challenges that need to be addressed.

The AGD is a sophisticated control technique used to enhance the switching performance of semiconductors, including MOSFETs. The AGD involves external driver circuitry that precisely controls the voltage applied to the MOSFET gate terminal, enabling rapid and precise switching. It overcomes the limitations of conventional passive gate driving methods by providing higher voltage slew rates, reduced switching losses, and improved efficiency. The AGD operates by utilizing high-speed transistors and capacitors to efficiently drive the MOSFET gate capacitance, resulting in faster switching transitions

and minimized high-impedance states. The primary objective is to achieve precise and predictable switching characteristics, leading to improved power conversion efficiency and reduced switching losses. AGD's responsiveness to dynamic load changes makes it suitable for high-frequency applications, maintaining reliable performance while enabling higher switching frequencies. In summary, AGD plays a crucial role in enhancing MOSFET performance, offering significant benefits in various applications, such as power electronic systems, motor drives, inverters, and switching power supplies[6,7,11].

Furthermore, AGD can be applied to solve the current imbalance in parallel MOSFET configurations. The AGD with the derating method idea is lowering the MOSFET rating performance to protect against potential overcurrent, even though it wastes the MOSFET potential[13]. The AGD method for gate control manipulation is a good current balancing technique with very small power loss, but it cannot guarantee consistent MOSFET performance in high-current applications[14,19,20]. Reference 15) describes an AGD method that involves MOSFET oscillation and overshooting reduction. However, this method increases losses in MOSFET switching. The Master and Slave method presented in[16,18] is an effective method to control current imbalances. However, the interrupt signal, which requires the use of a traditional operational amplifier circuit-based approach, may also have a higher susceptibility to electrical noise. This can degrade the performance of the control circuit and have a negative impact on the driver's reliability. Analog current-sharing methods use analog control with sensors and feedback control to adjust the gate voltage of each MOSFET to balance the current. This method makes the system more complex and more sensitive to other disturbances, especially noise, which can result in fluctuations in the control signal and compromise the accuracy of the current balance processing[17,24,32-34]. The AGD method dynamically regulates the MOSFET gate voltage to synchronize with the peak of drain current (Id) in each MOSFET on a closed-loop circuit. However, this approach leads to a significant gate time delay and requires a complex digital process[21-24,35].

This study describes a new MOSFET Active Gate Driver (AGD) method with the aim of achieving the same Id current with different PWM duty cycles or Ton on each MOSFET. The difference in each MOSFET current is used to regulate the PWM duty cycle of every MOSFET. The PWM duty cycle regulates the turning ON (which is defined as a Ton) and the turning OFF (Toff) of the MOSFET switching, thus influencing the current flow (Id) through it 15). The MOSFET with the smallest current capability is configured as the Master, whereas the other MOSFETs are designated as Slaves. The interrupt time value for the duty cycle of each Slave MOSFET is influenced by the current difference between the Master and Slaves. As a result, the duty cycles of the Slave MOSFETs can vary and be adjusted to balance the current flowing through each MOSFET.

2. Operation Principles and Methods

MOSFETs commonly use Pulse-Width Modulation (PWM) to determine Ton and Toff voltage supplies to control the average current delivered to a load. The PWM duty cycle represents the duration of the MOSFET that is in the active state during the switching process. It is directly proportional to the MOSFET current flow. When the duration of MOSFET operation in an active mode increases, the drain current of the MOSFET also increases. Consequently, an increase in the duty cycle results in a corresponding increase in the drain current, while a decrease in the duty cycle leads to a decrease in the drain current 21,32,36-40). Reference 34) explains that the correlation between the PWM duty cycle and Id (drain current) can be calculated by considering the internal characteristics of each MOSFET, as shown in Eq. 1. In the context of this research, the gate voltage (Vgs) was maintained at 12 Vdc, where Vth represents the voltage threshold of the MOSFET.

$$\mathrm{Id} = \frac{((Vgs - Vth) x dty x Ttotal\ x\ Gms)}{(\mathrm{Rtotal}\ \mathrm{x}\ \mathrm{Ciss})} \quad (1)$$

Ciss is the total capacitance of the MOSFET as seen from the input, obtained by summing the capacitance of the gate-source (Cgs) and the capacitance of the gate-drain (Cgd)[29-32]. Gms signifies the transconductance parameter inherent to the MOSFET[22]. The duty cycle of the PWM signal (dty) is a measure of the proportion of time the signal remains in the high state relative to its entire period. Meanwhile, the total switching time (Ttotal) depends on the microcontroller or PWM frequency used. In this study, a frequency of 8kHz was utilized, resulting in a total switching time of 125 μS. The total resistance (Rtotal) in the formulated equation includes not only the resistance of the load but also any other resistive elements within the circuit. Consistent with Eq. 1, the outcome of "$dtyxTtotal$" actually signifies the Ton (Turn-On Time) of the MOSFET switching process. Consequently, Id can be computed during switching events based on the Ton of the MOSFET.

$$\mathrm{Id} = \frac{((Vgs - Vth) x\ Ton\ x\ Gms)}{(\mathrm{Rtotal\ x\ Ciss})} \quad (2)$$

However, Eq. 2 used to calculate Id during switching events is typically more complex, as it depends on other factors such as load conditions and gate driver characteristics[29]. Furthermore, in this study, the manipulation and variation of Ton are crucial for achieving current balancing among individuals of each MOSFET. This dynamic control of Ton allows for precise current regulation and optimization, ensuring that each MOSFET carries an equal share of the load current.

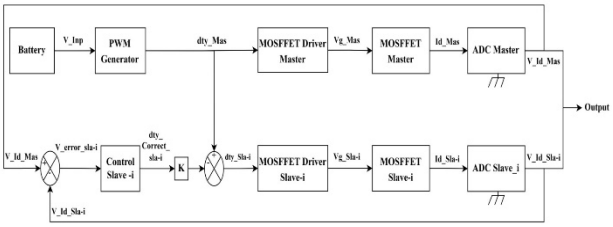


Fig. 1: Control Diagram of Current Balancing Process.

Fig. 1 shows a control diagram of MOSFETs current regulation. The current through the MOSFETs drain of Slave-i (i=1,2,…,n) is regulated until it reaches the same current as the Master. The comparison between two output voltages from ADC Master and Slave-i is used to program the feedback of MOSFET driver Slave-i. The program is compiled in a certain microcontroller to enable control PWM duty correction. The PWM duty cycle (dty) of each Slave-i MOSFET will reduced if the current sensor reading indicates a higher current flow through the MOSFET of Slave-i than the Master MOSFET.

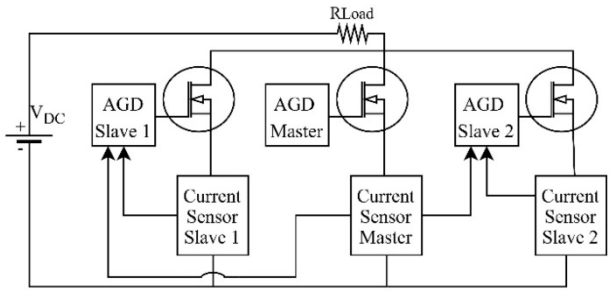


Fig. 2: Circuit Configuration of MOSFETs Parallel Connection.

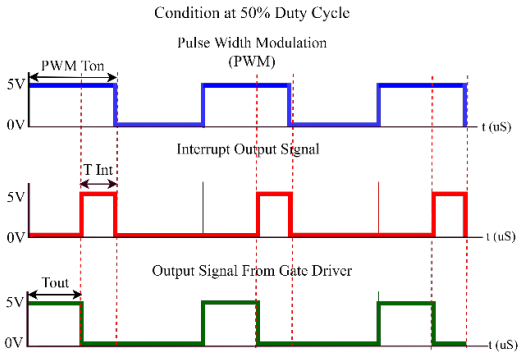


Fig. 3: Interrupt Scheme for Reducing PWM Duty Cycle.

The key idea of the proposed driving system is shown in Fig. 2. At first, a typical test circuit with three parallel MOSFETs is set up, where the drain current (Id) of three devices is measured through three current sensors. In the initial phase the AGD Master generates PWM signal input for the MOSFETs according to input reference 40). Furthermore, the AGD Slave-i undertakes to drain current (Id) balancing duties for the MOSFETs Slave by adjusting the PWM Ton for each MOSFET. Specifically, the AGD Slave-i acquires current information from the current sensors of both the Master and Slave-i, recognizes the current error and executes the current balancing algorithm. Then, the PWM duty cycle (dty) Or specifically the switching on time (Ton) of each MOSFET is adjusted using an interrupt signal (T Int) from the AGD Slave-i in a closed-loop manner. The closed-loop control is realized by the current sensors. An example of an interrupt signal that cuts the PWM waveform is shown in Fig. 3.

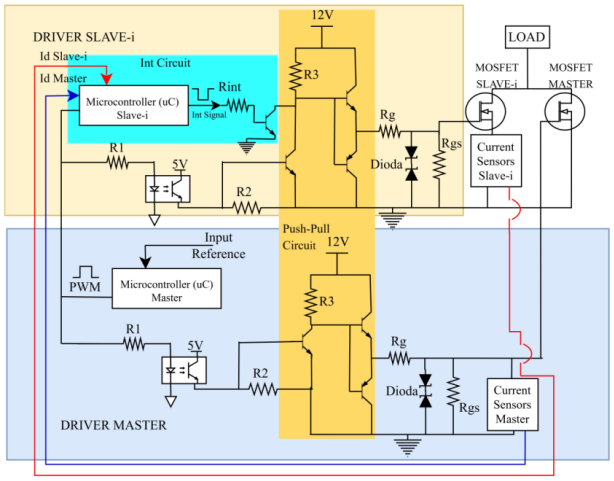


Fig. 4: AGD Circuit.

The proposed AGD consists of AGD Master and Slave-i as shown in Fig. 4. Each AGD has an optocoupler for the purpose of isolating control signals and segregating low-power devices from high-power devices[17]. This allows safe control of high-power devices without adversely affecting the operation of the microcontroller (uC) Master. The push-pull transistor circuit is a power amplifier to amplify the voltage from 5V to 12V 20). R1 is a voltage limiter from the microcontroller (µC) to the optocoupler. Generally, the value range of R1 is 10 to 100 Ω. R2, R3 and Rint are the voltage limiter of the transistor, typically in 1k Ω[17]. Rg is the current limiter for the MOSFET gate and the speed regulator of MOSFET charge-discharge capacitance. A Zener diode is used to avoid gate surge voltage and electrostatic discharge on the circuit. Meanwhile, the resistor gate to the source (Rgs) is a resistor to reduce the voltage of the MOSFET gate to the source. The value is 1k to 10k Ω[17].

A circuit configuration of MOSFETs with AGD on a parallel connection is depicted in Fig. 4. The configuration circuit consists of three microcontrollers (µC). One microcontroller (µC) 1 functions as a PWM generator for the AGD Master, while the other microcontroller (µC) 2 serves as the Slave MOSFET. The microcontrollers (µC) 2 interrupt and calculate the time delay based on input from Master (Id master) and Slave (Id slave-i) current sensors. The reference for current balancing is according to the Master-Slave concept[18]. The MOSFET with the smallest current value is defined as Master and the others are Slaves.

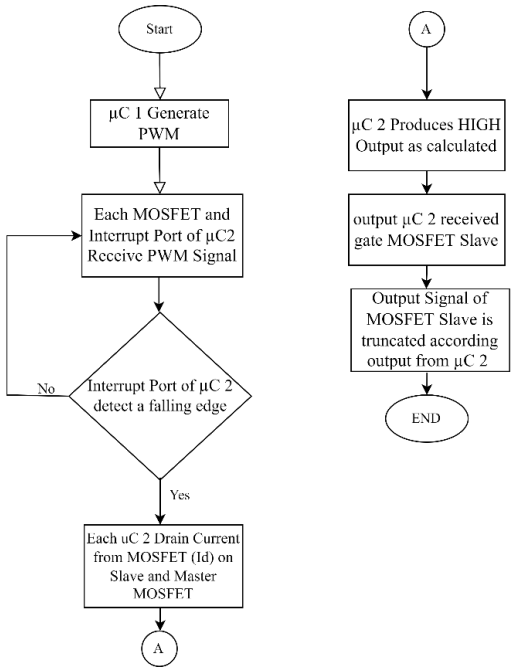


Fig. 5: Flowchart of Current Balancing Process.

In the current balancing process of Fig. 5, the PWM signal from the microcontroller (µC) 1 is received by each MOSFET and the microcontroller (µC) 2 as an interrupt trigger. Microcontroller (µC) 2 reads the drain current (Id) from the Master MOSFET and Slave when a falling edge trigger is detected from the PWM signal. The difference value between the Slave and Master MOSFETs, along with the duty cycle value of the Master, serves as the primary criteria for computing the microcontroller (µC) 2 output signal, which determines the interrupt time. This signal plays a crucial role in achieving precise Ton or Duty Cycle adjustments for each Slave-i. The interrupt time value is calculated based on programming calculations, taking into account the total switching time on the MOSFET (µS) and the ADC input of the potentiometer (used as a reference for the duty cycle of the PWM signal) in a 10-bit state, as per Eq. 3.

$$\text{Interrupt time} = \frac{k2a}{1023} \times \frac{ADC\ port}{1023} \times Ttotal \qquad (3)$$

The k2a is the difference between the ADC port values of the current sensors of Master MOSFET and Slave MOSFET. The ADC value is in a 10-bit so the k2a and ADC port in Eq. 3 are divided by 1023, while the total switching time is 125 µS.

The microcontroller output (µC) 2 received by each Slave MOSFET will affect the trimming of the gate driver output signal for each MOSFET. A special condition occurs when the duty cycle is 0% and 100%, which is the falling edge trigger cannot be found. As a result, the execution process is not carried out in an interrupt condition. For the 0% condition, due to the absence of a current difference, there is no execution process for this condition. Meanwhile, when the condition is 100%, the falling edge trigger cannot be obtained, resulting in the execution process not being carried out in an interrupt condition.

The analysis of the experiment data is carried out by comparing the MOSFET performance when tested without AGD and with AGD. The experiment records the current (Id) flow of each MOSFET for a certain duration. The test was carried out on three MOSFETs in parallel assembly with a dummy load of three bulbs, which is equivalent to a resistive load of 288W and an inductive load of 120W.

3. Results and Discussion

Experiments results are presented with MOSFET arranged in parallel connection using both without AGD or conventional gate driver (CGD) and with AGD. The test was carried out on three MOSFETs with a dummy load connected by separate planar copper busbars. The dummy load is three 12V bulbs equivalent to a resistive load of 288W and an inductive load of 120W. The parallel assembly MOSFETs and gate driver are connected on different boards to avoid heat conduction produced by the MOSFET dissipation. The PWM and AGD waveform was recorded using the Instrustar ISDS205A 2-channel digital oscilloscope. Furthermore, the MOSFET drain-source current (Id) was recorded using a datalogger Labjack T7 with a sampling time of 20 µS for 1 S. The experimental setup can be seen in Fig. 6 and Fig. 7.

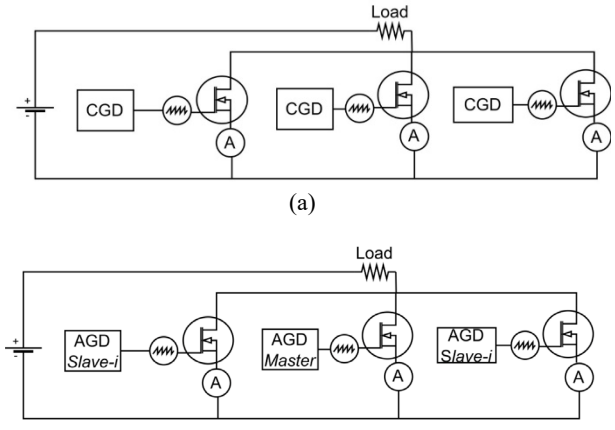


Fig. 6: Circuit of Experimental setup on The Study (a) Without AGD (CGD), and (b) With AGD.

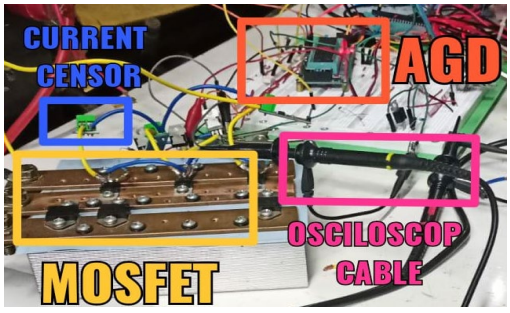
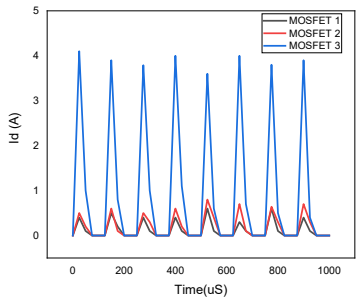
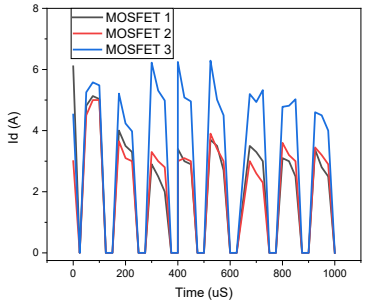


Fig. 7: Photograph of Experimental setup on The Study.

3.1 Testing without AGD on Resistive Load



(a)



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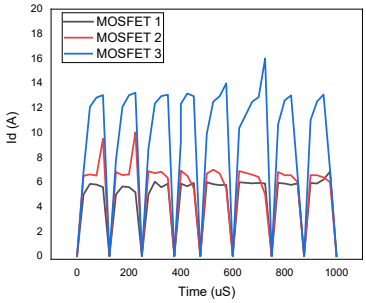


(c)

Fig. 8: Test Results Without AGD, (a). 25%, (b). 50%, (c). 75%.

Fig. 8. illustrates the imbalance in Id current that occurs without AGD or when using a conventional gate driver (CGD) in three different duty cycle conditions. In situations where the duty cycle or total current increases, a significant impact is observed in the deviation of MOSFET current values despite the consistent PWM signals. This observed current imbalance can be attributed to device characteristic mismatches, non-symmetrical circuit layouts, and cooling conditions in the parallel MOSFET connection[19,29,30].

Under a 15% duty cycle, each MOSFET exhibits relatively similar Id current values. However, as the duty cycle increases to 50%, an imbalance occurs between MOSFETs 1 and 2, while MOSFET 3 takes most of the load current, resulting in the most significant deviation, as evident in Fig. 8(b). Fig. 8(c) demonstrates that MOSFET 3 exhibits the most pronounced deviation, reaching 9 A at a 75% duty cycle, while MOSFET 1 has the lowest Id current value. It is essential to note that in these situations, the peak current of MOSFET 3 approaches 16 A due to this imbalance, thereby increasing the risk of module failure. The disparity in MOSFET current distribution can have critical implications for the reliability and performance of power electronic systems, particularly when used in applications with resistive loads. The non-uniform current distribution in the parallel configuration can lead to uneven heating, potential hotspots, and reduced overall efficiency[1,23]. Based on the above experimental result, this AGD study selected MOSFET 1 with the lowest current value as the Master MOSFET and the others as Slave MOSFETs.

3.2 Testing with AGD on Resistive Load

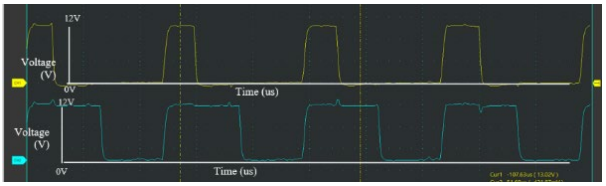
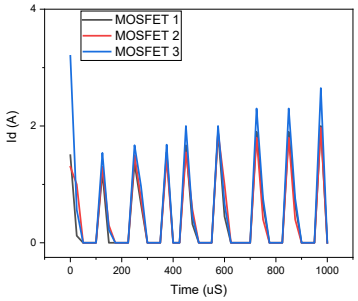
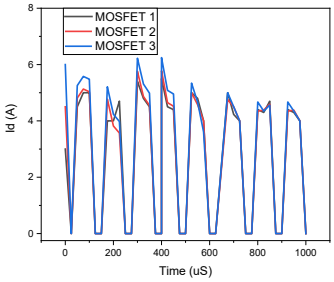


Fig. 9: Output Waveform AGD MOSFET 1 (Blue Color) and AGD MOSFET 3 (Yellow Color).

The test using AGD with the same power module and test conditions without AGD were obtained. In the system, one MOSFET is defined as Master and two as Slaves. The output waveform of AGD MOSFET 1 (Master) and MOSFET 3 (Slave) under a 50% PWM duty cycle on an oscilloscope is in Fig. 9. The result shows the proposed AGD circuit can cut off the PWM signal and reduce the turn-on switching time (Ton) from 76,5 µS to 32,5 µS.



(a)



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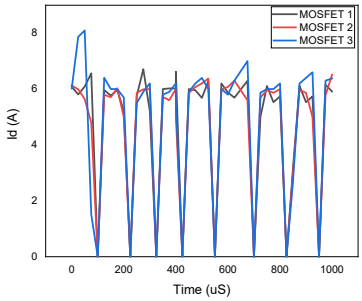


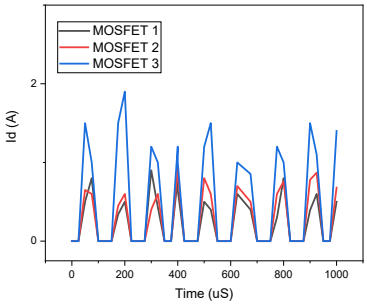
(c)

Fig. 10: Test Results With AGD, (a). 25%, (b). 50%, (c). 75%.

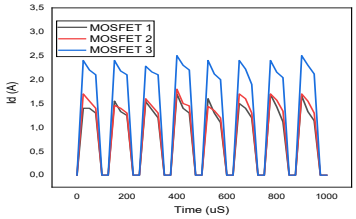
Based on the testing conducted with AGD as shown in Fig. 10, the current between each MOSFET is balanced in all duty cycle conditions. As seen in Fig. 10(a), the Id value of MOSFET 3 can be lowered to align with the other MOSFETs. Meanwhile, in Fig. 10(b), the Id values of each MOSFET experience spikes or ringing, but adjustments to the Ton values of the Slave MOSFETs can synchronize the Id values. This is particularly noticeable in conditions with the largest current difference when testing without AGD (duty cycle of 75%). In that state, the current value between MOSFETs can be balanced and stable at 6 A. The changes in turn-on switching time (Ton) affect the value of the current flowing (Id) of the MOSFET according to ref[15,41] and Eq. 3. The proposed AGD can reduce Id deviation by 80% compared to without AGD at each duty cycle condition and the current value between MOSFETs can be balanced.

According to the result, the proposed method can overcome the problems in several previous studies. The application of a simple digital process can reduce delay time in the balancing process[21-23]. Directly applying simple components with a microcontroller (μC) can ensure the durability of the system, reduce the power consumption of the system, increase cost-efficiency, and be robust against electrical noise[23-28,31-35]. To further demonstrate the advantages of the proposed AGD method, experiments with inductive loads have been carried out.

3.3 Testing on Inductive Load



(a)



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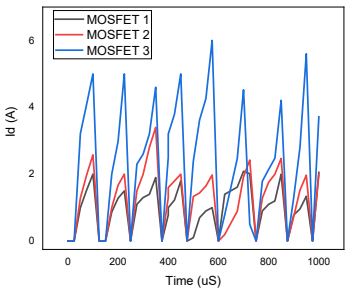
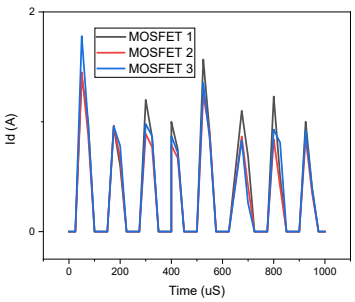


(c)

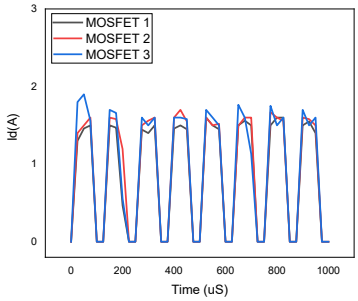
Fig. 11: Test Results Without AGD on inductive load, (a). 25%, (b). 50%, (c). 75%.

In Fig. 11, the performance of MOSFETs without AGD is illustrated under inductive load conditions with varying duty cycles. The total load current being switched is 10 A, and the duty cycle is increased from 25% to 75% (with a 25% resolution) to highlight the Id imbalance conditions. There is a deviation in MOSFET 3 compared to the other MOSFETs, ranging from 1-3 A under all duty cycle conditions. Additionally, MOSFET 1 exhibits the lowest Id value when compared to the other MOSFETs, particularly at the 75% duty cycle condition.

Moreover, peak current occurrences are observed in each MOSFET, influenced by the inductance characteristics of the load. Inductive loads, such as electric motors, can display abrupt current spikes that occur during power-on or power-off events due to the gradual formation or collapse of the magnetic field within the inductor. These temporary peak current spikes have the potential to impact the overall system performance and should be taken into consideration during the design and operation of power electronic systems[32,35,41].



(a)



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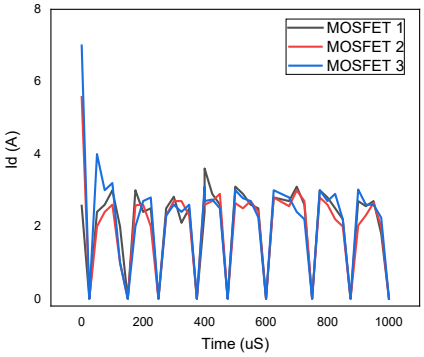

(c)

Fig. 12: Test Results With AGD on inductive load, (a). 25%, (b). 50%, (c). 75%.

According to the test with the AGD shown in Fig. 12, the implementation of active gate drivers for MOSFETs in a parallel configuration has successfully balanced the current differences, even in the presence of fluctuations in the inductive load. The proposed AGD function to precisely and responsively control the Ton of each Slave MOSFET, allowing for rapid adjustments to changes in load demand. As a result, AGD can provide more accurate current regulation for each MOSFET, reducing current imbalances, and preventing excessive current peaks. This helps improve overall system efficiency and ensures MOSFETs operate optimally.

Based on the experimental findings with resistive and inductive loads, the proposed AGD effectively reduces Id deviation by 80% compared to without AGD and addresses the current unbalance in specific load and duty cycle conditions. However, fluctuations are observed during switching transitions. Hence, further development and additional modifications to the AGD are required. With improved current distribution and the ability to handle fluctuations, the system becomes more efficient, durable, and stable in operation. Nonetheless, the utilization of the proposed AGD provides significant advantages in enhancing the performance and reliability of power electronic systems with resistive and inductive loads.

Based on the experimental results, the implementation of AGD has shown the potential to significantly increase the load capacity of paralleled MOSFETs, ranging from 2 to 3 times compared to configurations without AGD. However, it is essential to consider the specific specifications and characteristics of the MOSFETs used in the circuit, as the extent of capacity improvement may vary based on their performance capabilities. Hence, careful matching of MOSFETs and the integration of AGD are crucial in maximizing the load capacity enhancement in parallel MOSFET arrangements.

The success of the current balancing method in the parallel assembled MOSFET is indicated by its capability to improve performance and overcome the damage risk to each MOSFET [19]. The impact of the current difference between Master and Slave MOSFETs on overall reliability for more than three parallel assemblies will be studied in future work.

4. Conclusion

This paper proposed a new method of AGD to control the current of MOSFETs in parallel. The AGD driver consists of three separate gate drivers to set the Ton switching time of each MOSFET. With the proposed design, the time value of the Ton or duty cycle between MOSFET is properly adjusted. The Id difference between the Master and Slave MOSFET, which previously reached 2 to 3 can be balanced. Experimental results with a total resistive load of 288W and inductive load have proven that the AGD method can overcome the current imbalance in the MOSFET assembled in parallel. Furthermore, it improves performance, ensures equal current sharing, and overcomes the risk of damage to each MOSFET. Additionally, The advantage of this method is that the control system can be customized to suit the specific needs of a particular application, allowing for optimization of performance to control current unbalance under different operating conditions. Last but not least, a module consisting of several MOSFETs connected in parallel is expected to be more robust under dynamic loads.

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