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https://doi.org/10.5109/6793669

出版情報：Evergreen. 10 (2), pp.1100-1105, 2023-06. 九州大学グリーンテクノロジー研究教育センター
バージョン：

Design and Implementation of Soft Error Resilient 14T SRAM Cell

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(Received February 1, 2022; Revised May 14, 2023; accepted May 14, 2023).

Abstract: As part of this effort, the CC14T, cross-coupled memory cell with 14 transistor architecture has been proposed, with defence against soft errors such as single event upsets (SEUs). The CC14T cell is presented, which consists of 4 cross-coupled input-split inverters and four access transistors. The cell achieves optimum SEU tolerance owing to a feedback structure among its internal nodes. It has been implemented and analyzed under 40nm regime, and the findings demonstrate that it consumes 43.01 nW of power with supply voltage of 0.8V and takes 6.64 percent and 15.5 percent less time to write and read than a typical 6T SRAM cell. As compared to the other cell considered, the CC14T cell has a faster write access time and higher stability due to its soft error resistance.

Keywords: Single Event Upset, Soft Error, SRAM

1. Introduction

One of the most extensively utilised memory devices in contemporary circuits and systems is static random access memories (SRAM)[1)]. Power dissipation is one of the most important aspects of modern nano-scale VLSI architecture[2)]. Ultra-low power (ULP) operation is crucial in VLSI circuits for space applications where there are few energy resources available[3)]. Low-cost satellites have an even smaller power budget since the use of bulky batteries and power sources is restricted, which also reduces the overall weight of the satellite. Reducing the supply voltage (Vdd)[4)] and having all chip components operate in the subthreshold region[5)] are two of the most efficient ways to achieve low power. However, low supply voltage design faces challenges like high delay, temperature variation and also the circuit becomes more sensitive to radiation effect as compared to the high supply voltage[6)]. A further important problem is that voltage scaling[7)], which is extensively utilized in ultra-low power devices like medical devices and smart grids etc[8)], reduces the speed and stability of SRAM[9)]. Meanwhile, in nano-scale CMOS technologies, with the aggressive decrement in feature size of transistor, SRAM-circuit integration has attained high density with great improvement in its performance. Also, small transistor feature sizes result in small supply voltages and node capacitances. Because of their high integrated density, SRAM is more susceptible to soft error. These are errors which makes a signal or data corrupted. Thus, as a result of particle strikes from alpha particles[10)], protons[11)], neutrons[11)], electrons[11)], and heavy ions[12)], SRAM is becoming more vulnerable to soft glitches. Soft errors can cause data corruption, execution errors, and in the worst-case scenario system crashes. One major cause of these soft errors is the single event upsets (SEUs) from cosmic rays. In radiation environment, SEU is the most important reason of VLSI circuit failure due to the strike of radiation[13)].

A single node in a storage module, such as a memory cell or flop, can have its data or state changed by a particle strike, leading to a soft glitch. It's known as a single-event upset in this situation (SEU). When the particle collides with a reverse-biased p-n junction, such as a transistor diffusion-bulk junction, the injected charge is transmitted by drift and produces a transient current pulse that modifies the node voltage. Data loss happens when the collected charge (Qcoll) exceeds the critical charge (Qcrit) kept in the sensitive node. Qcrit[14)] is the smallest charge that can be applied to a sensitive node to produce a memory bit flip. Storage elements can retain incorrect values as a result of SEUs, resulting in circuit and device errors and failures. However, with technology scaling, Qcrit decreases[15)]. Therefore, IC creators and makers must perform radiation hardening method against SEUs in order to increase circuit and device robustness, whereas the recently introduced FinFET based technology can decrease the rate of soft error[16)], but still require valuable and scalable solution to make it resilient and tolerant of soft error.

Therefore, reliability of SRAM due to soft error is still a concern. To tolerate SEUs, many sets of latches, memory cells and flops have been proposed by researchers. For flip flops, hardening is considered in the two designs in references 17) and 18) and the two designs in references 19) and 20) consider hardening for latches.

Therefore, it is critical to develop novel systems to address SRAM-reliability issues in terms of soft errors. The probable reduction of single-event upset is a key method for improving their radiation-hardened results. Due to its compatibility with CMOS commercial processes and low cost, radiation-hardened-by-design (RHBD) is recognised as a successful technique for improving the circuit's radiation endurance.

The order of the remaining text is as follows. The two prior memory cells that were compared are explained in Section 2. The proposed memory cell design's working and SEU recovery analyses are discussed in Section 3. The experimental findings and a comparison table are presented in Section 4. The work is summarised in Section 5.

2. Previous Memory Cells

2.1 6T SRAM Cell

With four transistors for keeping values - two PMOS and two NMOS transistors, and two additional NMOS transistors for access operations, the standard memory cell has a 6T configuration.[21] Figure 1 depicts a basic 6T SRAM cell in an illustration.

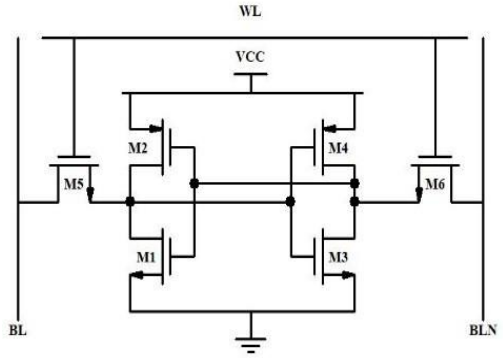

Fig. 1: Six-transistor (6T) CMOS SRAM cell.

Because of its simple and easy design with a smaller number of transistors, it is highly used for different applications. However, it lacks the property of being tolerant and resilient to soft errors.

2.2 QUCCE10T Cell

With two p-type and two n-type latch structures at the titular supply voltage, the quadruple cross-coupled storage cell with 10 transistors (QUCCE10T) is designed for extremely reliable high density terrestrial applications[22].

There are four storage nodes with the names A, B, Q, and QN included in the QUCCE10T memory unit. The output nodes Q and QN are linked to bit lines BL and BLB by pass gates N5 and N6. While word line WL is in a high logic state, the two access transistors N5 and N6 are enforced to operate. It is takeninto account that the saved state is "0". As seen in Figure 2, Nodes A, Q, QN, and B have the logic states "1," "0," "1," and "0," respectively.

In terms of robustness, the QUCCE10T is about 2 times the minimum critical charge in comparison with 6T cell. Thus, it has the ability to tolerate SEU.

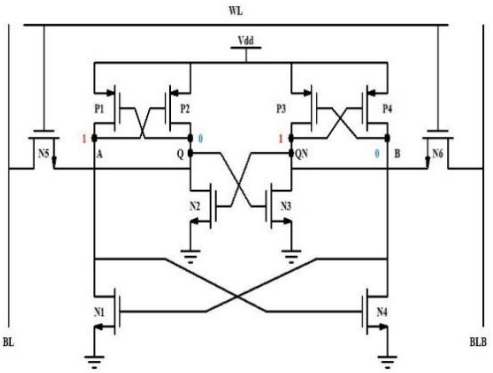

Fig 2: Schematic of QUCCE10T

3. Proposed CC14T Cell

3.1 Schematic and Basic Operations

Figure 3 shows a schematic for the proposed 14T cell. It can be seen that the memory cell has 14 transistors, with P1 to P4 serving as the PMOS pull-up transistors, N1, N2, N3, N4, N9, and N10 serving as the NMOS pull-down transistors, and N5 to N8 serving as the access transistors. The input and output lines for the write and read operations, respectively, are bit-lines BL and BLN. When WL is high, the access transistors are turned ON, enabling the execution of read and write operations. WL is the word line that works as the switch for the access transistors. Additionally, the access transistors are turned OFF to implement the hold state when WL is low. The nodes for storing the data are I1, I2, I3 and I4.

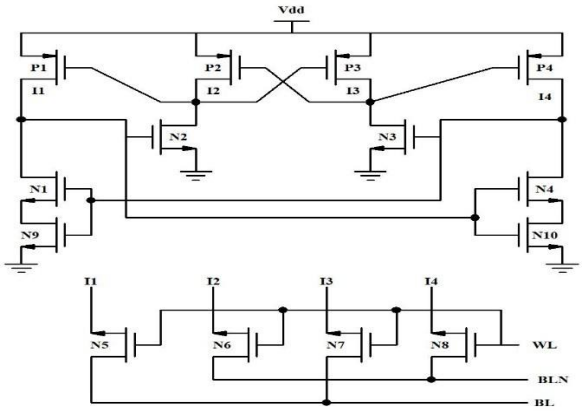

Fig 3: Schematic of CC14T

The following is an explanation of the fundamental functions of the proposed 14T cell. Let's begin by setting the nodes to I1=I3=1 and I2=I4=0. Now let's look at the scenario of writing 0; during this operation, a precharge circuitry charges both bit lines BL and BLN to Vdd. One of the bit lines is caused to discharge to zero using write driver circuitry after the bit lines have been charged (in this case, BL). Next, the WL is asserted to high which turns ON the access transistors. Since I1=0, N2, N4 and N10 are OFF. BLN charges I4 to 1 which turns ON N1, N3 and N9. As N3 turns ON, node I3 discharges to zero leading to turning ON of P2. Thus, charging node I2 to 1, turning OFF P1. And since N1 and N9 are ON, node I1 discharges to 0 resulting in I1=0, I2=1, I3=0 and I4=1 respectively, explaining the execution of successful write 0. It is to be noted that the pull up ratio (PR), i.e., the ratio of access transistor to that of pull up transistor must be greater than 1. Figure 4 illustrates the waveform of the simulated read/write operation of the presented cell.

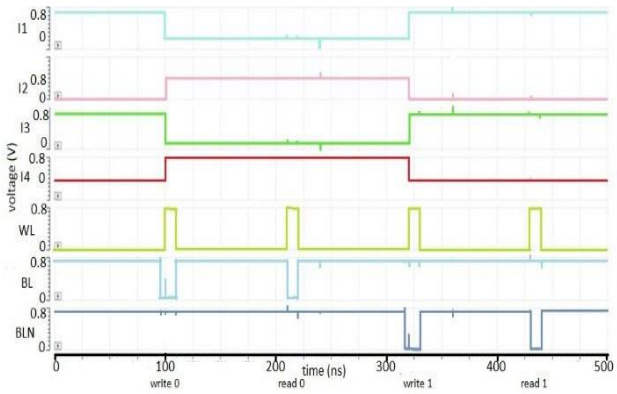

Fig 4: Simulation output waveform of read and write operation of CC14T cell.

Now, let us take the instance of reading 0. With the help of the precharge circuit, the bit-lines are charged to Vdd. The WL is asserted to 1 turning ON the access transistors. The BL discharges to 0 through N1 and N9 and also through N3. And BLN remains constant at Vdd. The difference between BL and BLN is calculated. In this case, the difference is negative, so we have a successful read 0 operation. For read 1 operation[23], the difference needs to be positive, owing to the discharge of BLN and a constant BL. To achieve a proper read operation the cell ratio (CR), i.e., the ratio between access transistor and pull-down transistor must be less than 1[24-31].

3.2 SEU Recovery Analysis

In this section, we shall illustrate the recovery analysis of the proposed 14T cell. Let the state of the storage node be as follows, I1=I3=1 and I2=I4=0.

Case1: Node I1 is affected.

The radiation particle striking Node I1, momentarily changes its value from 1 to 0. Thus N2, N4 and N10 turns OFF for the time being. Now since Node I3 is not affected, thus P2 and P4 are still OFF and hence Node I2 and Node I4 holds its original state of 0. So, N1 and N9 are still OFF and P1 still ON leading to the self-recovery of the Node I1 back to its original state of 1.

Similarly, when Node I2 is affected, same self-recovery analysis can be taken into account.

Case2: Node I3 is affected.

The radiation strike at Node I3 temporarily changes its value from 1 to 0, temporarily turning ON P2 and P4. Thus, Node I2 will have a weak value 1. Since Node I1 is not affected, so N2 stays ON and makes N2 strong 0, neutralizing the weak 1 making Node I2 maintain its correct value. Similarly, with Node I4. As the P4 is changed to ON temporarily, Node I4 has weak 1. But since Node I1=1, unaffected, therefore, N4 and N10 are still ON making Node I4 strong 0. Thus, P3 stays ON and Node I3 self recovers to its original state of 1.

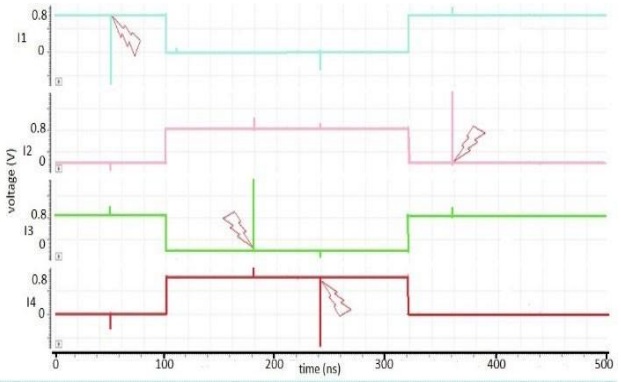

Fig 5: Simulation of SEU self-recovery analysis.

Case3: Node I4 is affected.

Node I4 becomes 1 momentarily turning ON N1 and N9 for the time being leading to a weak 0 at Node I1 (as N1 turned ON). However, as Node I2 is not affected, therefore P1 stays ON making Node I1 hold its strong 1. Thus, N4 and N10 are still ON. Likewise, Node I3 has weak 0 (as N3 turned ON). But as Node I2 is not affected, so P3 stays ON leading to a strong 1 at Node I3. This makes P4 still OFF and thus Node I4 returns back to its

original state of 0.

To sum up, we can say that the proposed 14T cell reveals a successful capability of self-recovering from a SEU.

The recovery analysis of the SEU is shown in the Figure 5. We can see that at 50ns, there is an attack of SEU at node I1, resulting in flipping of the data from 1 to 0. But, as we can see from the waveform, the node I1 has self-recovered itself back to its original state of 1. Similarly, we can observe from waveform at different point of time, and at different nodes, SEUs have been recovered successfully. The SEU attacks have been mimicked using an exponential current source with a rise and fall time constant of 0.1ps and 3ps respectively[25].

The cell has been implemented using 0.8V supply voltage in 40nm CMOS technology. And the simulations were performed using CADENCE Virtuoso tool.

4. Observation and Evaluation Results

In this section, the results of the comparative analysis and the evaluation for the CC14T cell, QUCCE10T cell and the traditional 6T cell are taken into account. All cells were implemented using the same implementation conditions as those defined in the previous section. In terms of SEU resistance, power consumption, write access time and read access time, Table 1 displays the efficiency and overhead contrast performance of unhardened and hardened variant of memory cells.

Table 1. Comparison results of different parameters of the memory cells.

Parameters	**Types of Memory Designs**		
	6T	**QUCCE10T**	**CC14T**
WAT (0) ps	226.27	228.36	216.17
WAT (1) ps	218.33	225.37	203.82
RAT ps	5.28	4.36	4.46
Power nW	32.95	112.3	43.01
SEU Recovery	Fail	Pass	Pass

Firstly, let's go through the reliability comparison results. Table 1 shows that all cells, with the exception of the 6T cell, are SEU hardened, ensuring better stability and good resistance. To conclude, the proposed CC14T cells ought to have significantly improved robustness and resiliency.

Let us consider about the overhead comparison findings now.

Table 1 shows that, 6T cell consumes the least amount of power as it has only 6 transistors. Due to its decreased current competition in its feedback loops and use of stacked transistors, the proposed CC14T cell has just 23.38% more power than a 6T cell and 61.70% less power than a QUCCE10T.

The suggested CC14T cell outperforms the 6T and QUCCE10T cells in terms of write access time (0) by 4.46% and 5.33%, respectively. In a similar vein, the CC14T cell's write access time (1) is 6.64% and 9.56% faster than those of the 6T and QUCCE10T cells, respectively. The proposed cell's read access time is 4.46 ps as well. Due to its usage of extra access transistors, the CC14T also has the lowest WAT value.

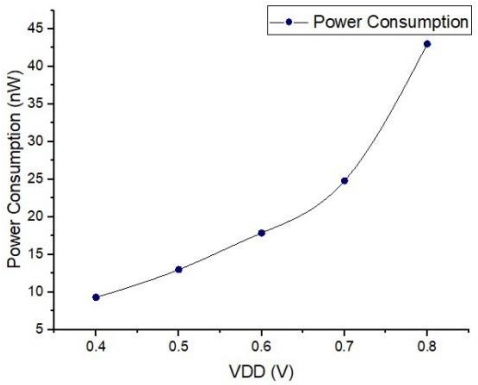

Fig 6: Variation of power consumption of CC14T cell with respect to supply voltage

The graph in Figure 6 depicts the impact of variation in supply voltage on power consumption values, showing as supply voltage decreases, the power consumption also decreases holding the proper output at this range.

To conclude, the CC14T cell has been successfully hardened. The proposed cell has lower overhead than current state-of-the-art hardened cell, particularly in terms power dissipation, and write access time.

5. Conclusion

We have found that a very reliable CC14T cell that had been presented is effectively toughened against SEUs which in today's world, where CMOS technology keeps on shrinking, would help modern day memory units to stand against such kind of glitches and recover from soft errors including SEUs. It is highly tolerant and resilient from the soft error attack. Also, along with being resilient to soft errors, it has comparatively lesser power and high speed of access in respect of the other state-of-the-art memory cell. Lastly, this cell can be used in applications where high efficiency and resiliency is needed, such as aerospace, nuclear power plants, and banking.

Nomenclature

WAT(0)	Write access time while writing 0 (ps)
WAT(1)	Write access time while writing 1 (ps)
RAT	Read access time (ps)

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