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Space Vector Modulation for Nine-Switch Converter Employing Three Phase Loads

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Abstract: Different power utilities require different voltage levels and sources (AC/DC) for its operation. In this process converters are required where lot of power is being wasted in components as switching & conduction losses. One way to reduce losses is to reduce the number of switches in the converter. This paper proposes a nine-switch converter where two loads are controlled using a single inverter having nine-switches resulting in less conduction & switching losses as well as less space and cost. Finally, this work shows the simulation of nine-switch converter operating with space vector modulation and employing two three phase loads.

Keywords: Pulse Width Modulation (PWM), Space Vector PWM (SVPWM), nine-switch converter (NSC), Sinusoidal PWM (SPWM)

1. Introduction

Energy sources are limited in nature and power demands are getting increased continuously, so there is a need to utilize power in such a way that the present demands can be fulfilled keeping the future demands reserved as well. Various studies are going on for the establishment of a Sustainable Society[1)]. Power electronics is playing an important role in achieving the abovesaid goal. There are numerous areas on which works are being carried out to reduce the power requirements such as reduction of power electronics switches in converters[2)], designing of solar AC systems[3)], design of new generation wind turbines[4)], analyzing wind turbines for better efficiency[5)]. This paper deals about implementation of power electronics converter to operate multiple loads simultaneously with lesser switches. Talking about loads specifically motors, they have become a part of day-to-day life, mostly in industrial applications where there is a need of motors for almost each and every application. Controlling motors is becoming a tough task as each motor requires its own control mechanism. A lot of control strategies are suggested for the control mechanism like an individual inverter for individual loads or few loads can be connected in a parallel and then connected with the inverter, but there are many demerits associated with the each control method like the first one where individual inverters are used makes the system complex and bulky , the conduction losses and switching losses are also more in first case while in second case where loads are in parallel the main issue comes with the independent control of the motors. Now a days to reduce the number of components in a converter is a vital area of focus for the researchers, whether its active component or passive component. This results in the reduction of losses and lowering the overall cost of the converter[6)]. Taking into consideration the reduction of passive components a familiar example is direct and indirect matrix converter[7)] whose output behave as same as a conventional Voltage Source Inverter without having storage capacitors connected[8)]. Reduction of active semiconductor switching elements are also a matter of research. A nine-switch converter works as similar as a back-to-back converter which is having 25% lesser switches then back-to-back converter[9)]. Conventionally sinusoidal pulse width modulation (SPWM) technique was the PWM technique that was used in the converter. But the control employing SPWM was not smooth in relation with the harmonics inserted and good quality waveform[10)]. Talking about two level inverter space vector pulse width modulation technique is much better as compared to different PWM techniques[11)]. Also, there are other techniques in SVPWM which are now a days being used in cascaded H-bridge inverters[12)] and modular multilevel inverters[13)] which are being used in place of other modulation schemes[14)]. Space Vector PWM technique results in improved bus voltage utilization and is having less commutation losses[15)]. In this method the space-vector modulation scheme is shown for the gating

control of the proposed nine-switch converter, where the result will be shown by appropriate simulation of the circuit in SIMULINK.

2. Nine-Switch Converter Structure

Figure 1 depicts a typical back-to-back converter with 12 switches that controls two different loads. The first load is controlled by the upper two switches SA, SB, SC, and SA', SB' and SC', while the second load is controlled by the lower switches SU, SV, SW, and SU', SV', SW'. Merging of the switches SA', SB', SC', SU', SV', SW' gives rise to a new topology of inverter which is further gives rise to a new topology of inverter which is further

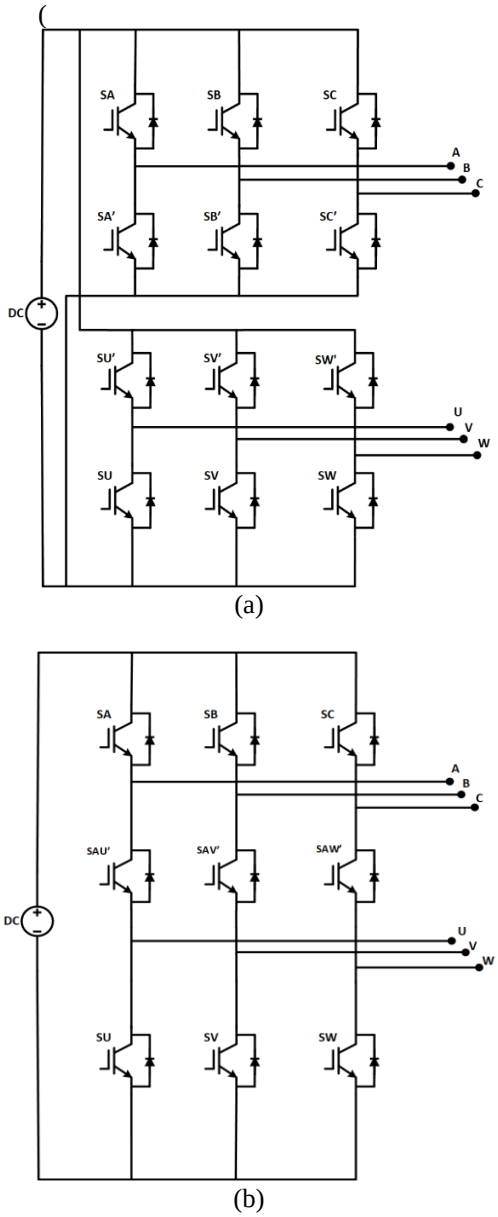


Fig. 1: (a) 12 switches Back-to-Back Converter circuit
(b) Nine-Switch converter circuit

called as nine-switch converter. This is shown in Fig.1 (b), It can be seen that that after merging, the new converter formed is having nine switches in total. The combination of SA, SB, SC, SAU', SAV', SAW' is inverter 1 while the SU, SV, SW and SAU', SAV', SAW' is inverter 2.

2.1. Operating principle of Nine-Switch Converter

It was discovered after comparing Figs. 1(a) and 1(b) that the two legs of back-to-back converters are combined to create the nine-switch converter. The NSC converter's pulse width modulation design is currently a source of concern. In a normal 12 switch converter, only SY and SX—where Y is U, V, or W and X is A, B, or C—are independent switches. The other 6 switches are dependent. The gating pulse for independent switches is produced utilising the three phase modulating references when compared to a single carrier or by employing two separate carriers, while the logical inversion of the signals is applied to the dependent switches. When merging is done then the gating signal for upper and lower switch of the nine-switch converter are generated using the same process while for the middle switch the gating signal is generated by the logical XOR of gating pulse of upper and lower switch. One thing that is needed to be understood is that the switches are now not dependent or independent as the previous case of back-to-back converter. A pulse width modulator now generates the signal for the first inverter and the second inverter. The reference signal in this case will be generated using space vector PWM technique. The operating modes of nine switch converter can be tabulated as table 1.

Table 1. Nine-switch converter (NSC) switching states

Switching State	SX	SXY	SY
1	On	Off	On
0	Off	On	On
-1	On	On	Off

Figure 2 (a) and (b) shows the mode of working of a Nine-Switch Converter. Observing fig 2 (a), mode 1 of NSC, the lower leg is shown i.e., SY where Y=U, V, W is in on state and in the fig 2 (b), mode 2 of the NSC, the upper leg is shown i.e., SX where X=A, B, C is in on state. The upper load is represented by A, B, C and the lower load by U, V, W.

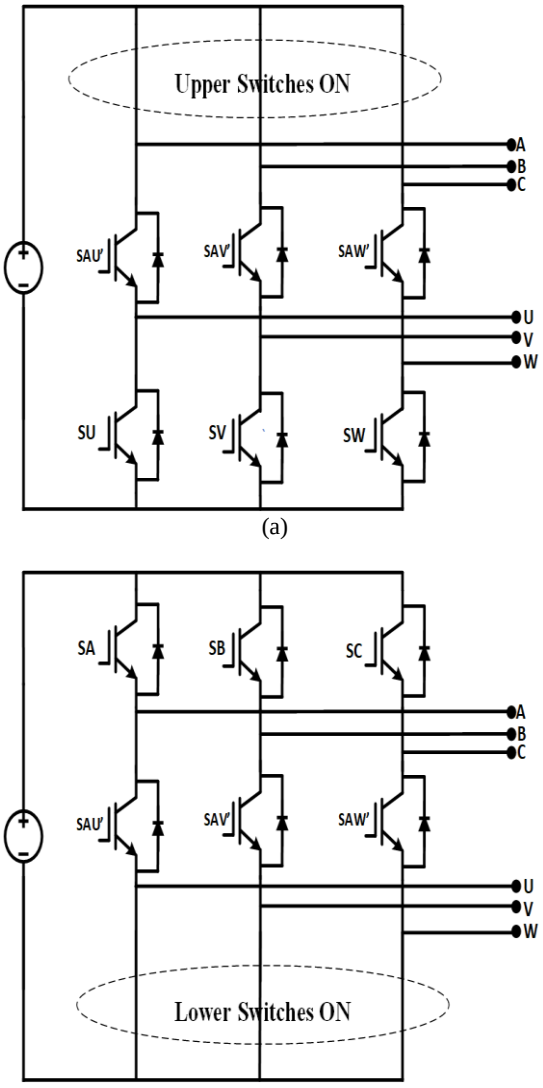


Fig. 2: Operating Modes (a) Mode 1 of NSC (b) Mode 2 of NSC

2.2 Pulse width modulation for NSC based on Carrier[16])

In figure 3 carrier-based pulse width modulation is shown. For the two phases, two reference signals are generated (upper and lower). The upper reference signal (V_{ref} Upper) is for upper output and lower reference signal (V_{ref} Lower) is for lower output. The reference signal (upper) is compared with the carrier signal for the upper switch and the reference signal (lower) is compared with the carrier for the lower switch. By this process the gate signal for respectively upper (S_{upper}) and lower signal (S_{lower}) are generated. Logical XOR of the upper and lower switch gate pulse generates the gate pulse for the middle switch (S_{middle}). Switching states can be derived from two modes one in which the states are obtained by two reference which are in phase and second case in which the states are obtained by the references which are displaced by a finite phase. Figure 3 shows the switching states where the gate pulse is obtained by two out of phase references.

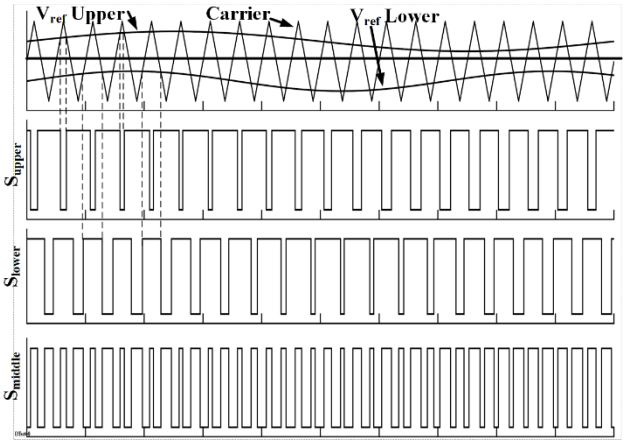


Fig. 3: Carrier based PWM for NSC

Realizing the signal for comparison: Assuming the reference of Inverter 1 (Upper Switches) and Inverter 2 (Lower Switches) is given by equation 1 and equation 2. The gate pulses for Inverter 1 are created by comparing the upper side of the triangular carrier wave and for the Inverter 2 gate pulses are created by comparing with the lower side of the triangular wave.

$$V_{I1}^{ref} = A_1 \sin 2\pi f_1 t + \varphi_1 \quad (1)$$

$$V_{I2}^{ref} = A_2 \sin 2\pi f_2 t + \varphi_2 \quad (2)$$

Where A_1 and A_2 are the amplitudes for the two references and similarly f_1 and f_2 and φ_1 and φ_2 are the frequencies and phases respectively.

The modulation rate that is generally taken is given by

$$m = \frac{V_{ref}}{\frac{E_{dc}}{2}} \quad (3)$$

where E_{dc} is the dc voltage source.

An offset is needed to be introduced in the carrier-based approach so that the two comparisons can be done on two sides of the carrier signal. An offset of E/4 are added and subtracted from the reference 1 and reference 2 respectively while calculating the carrier-based approach. Since the lower reference is compared at lower side so it is compared with negative logical values. The generation of gate signals are shown in fig 4

$$m_{I1} = (V_{I1}^{ref} + E/4)/(E_{dc}/2) \quad (4)$$

$$m_{I2} = (V_{I2}^{ref} + E/4)/(E_{dc}/2) \quad (5)$$

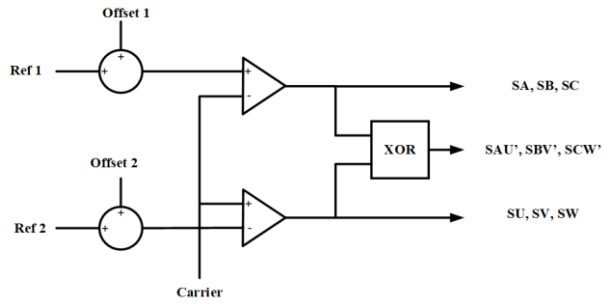


Fig 4: Method of generating gate signals using carrier-based approach

2.3. Space Vector Approach for Nine Switch Converter

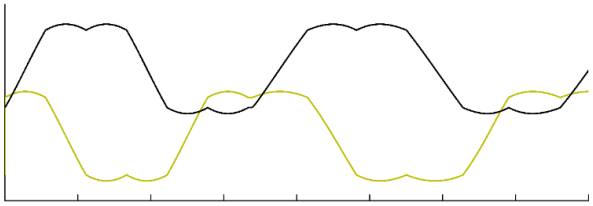


Fig. 5: Modified reference wave using space vector modulation with added triplen offsets

Space vector approach is a novel technique which can be used with nine-switch converter for working with two different loads[17]. In this approach the reference waves are modified using space vector modulation technique. Figure 5 shows the modified references waveform with SVM technique. As mentioned previously an offset is required to generate the gating signals properly when compared with a single carrier signal, the modulating references[18] that are

$$V_a(t) = M_1 Sin(\omega_1 t + \varphi_1) + Offset\ 1 \quad (6)$$

$$V_b(t) = M_1 Sin\left(\omega_1 t + \varphi_1 - \frac{2\pi}{3}\right) + Offset\ 2 \quad (7)$$

$$V_c(t) = M_1 Sin\left(\omega_1 t + \varphi_1 + \frac{2\pi}{3}\right) + Offset\ 3 \quad (8)$$

$$V_u(t) = M_2 Sin(\omega_2 t + \varphi_2) + Offset\ 4 \quad (9)$$

$$V_v(t) = M_2 Sin\left(\omega_2 t + \varphi_2 - \frac{2\pi}{3}\right) + Offset\ 5 \quad (10)$$

$$V_w(t) = M_2 Sin\left(\omega_2 t + \varphi_2 + \frac{2\pi}{3}\right) + Offset\ 6 \quad (11)$$

Where offset 1=2=3 and offset 4=5=6

M_1 and M_2 are the amplitudes or can be said as modulation ratio. φ_1, φ_2 and ω_1, ω_2 are the phase shifts and frequencies respectively for the three phases for two legs. Offsets are added to gain benefits in performances such as quality of wave form is improved[19][20][21]. The set V_a, V_b, V_c are shifted upwards by adding offsets so that it touches the positive carrier peak, similarly the set V_u, V_v, and V_w is shifted downward till it reaches the negative carrier peak. The shifting is done by adding or subtracting dc offset to the signal[22].

The carrier-based switching vector[23] for pulse width modulation is shown in figure 6.

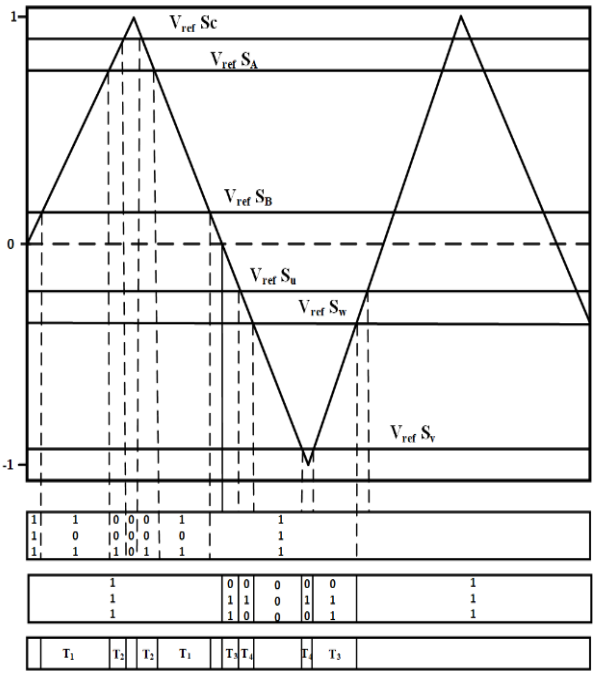
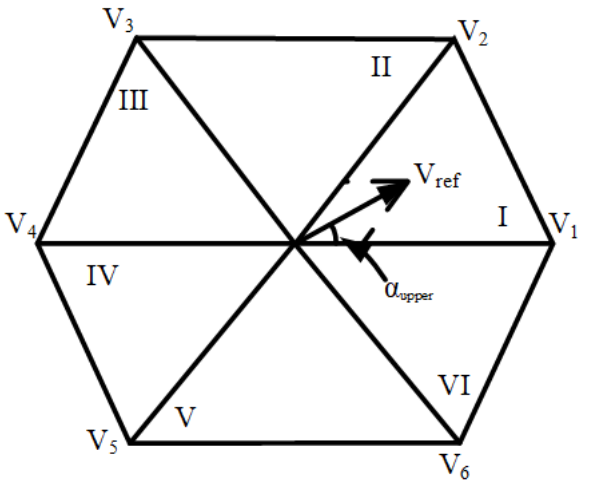


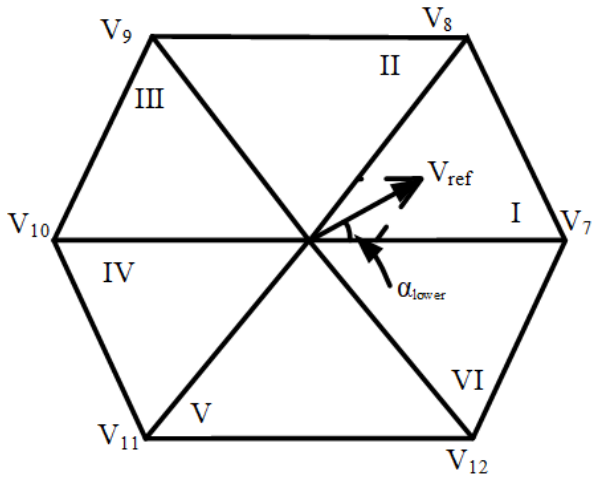
Fig 6: Carrier based switching vector for PWM

Table 2. Switching Vector for state vector modulation for NSC

Vector	First Leg	Second Leg	Third Leg	Type
1	1	0	0	**Upper Switches SA, SB, SC are active**
2	1	1	0	
3	0	1	0	
4	0	1	1	
5	0	0	1	
6	1	0	1	
7	-1	1	1	**Lower Switches SU, SV, SW are active**
8	-1	-1	1	
9	1	-1	1	
10	1	-1	-1	
11	1	1	-1	
12	-1	1	-1	
13	1	1	1	**Zero**
14	0	0	0	
15	-1	-1	-1	



(a)



(b)

Fig. 7: Nine-switch converter space vector diagram (a) upper switches (b) lower switches

The switching vector diagram for nice switch converter (NSC) is shown in figure 7(a) and 7(b).

Voltage utilization improvement and realization[24].

In a nine-switch converter[25-27] a common dc voltage source is shared between two inverters i.e., Inverter 1 and Inverter 2 for upper and lower load respectively. Generally, the voltage utilization for each inverter is equal. However, this voltage utilization can be changed by changing the offset values given to reference signals. Upper signals are added with an offset of 1- M_1 to equation (3), (4) and (5) and M_2 – 1 to equation (6), (7) and (8), Where M_1 and M_2 are the amplitude and modulation ratios which are normalized. It is possible to change the utilization by changing the values of M_1 and M_2keeping in mind the values are given so that the signal remains in the adequate range of carrier signal.

3. Simulation Results

A simulation has been performed to validate the applicability of nine-switch converter using space vector method. Two different reference signals are generated using space vector approach. The upper reference signal is generated with a sine wave of frequency 50 Hz having an amplitude of 100 V, the lower reference signal is generated with a sine wave of frequency 60 Hz having an amplitude of 100 V. Upper inverter and lower inverter is connected with two three phase loads each for one inverter. Table 3 shows the simulation parameters.

Table 3. Simulation parameters

Parameters	Symbol	Value
Voltage Source (DC)	E	100 Volts
Carrier frequency	*f*	10^3 Hz
Inductance	L	0.1 Henry
Resistance	R	10 ohms

4. Results and Discussion

Fig 8 shows the switching of the upper, middle and lower switches going upside down. Clearly as mentioned in the working part of the converter, the middle switches are the logical XOR of rest two. Figure 9 shows the phase current of the load connected to the upper converter, i.e., SA, SB, SC and SAU', SAV' and SAW' and figure 10 shows the phase currents of the lower converter i.e., SU, SV, SW and SAU', SAV' and SAW'. The currents are smooth which shows the independent control of the two loads. The load 1 is operating at 50 Hz and load 2 is operating at 60 Hz. The process of

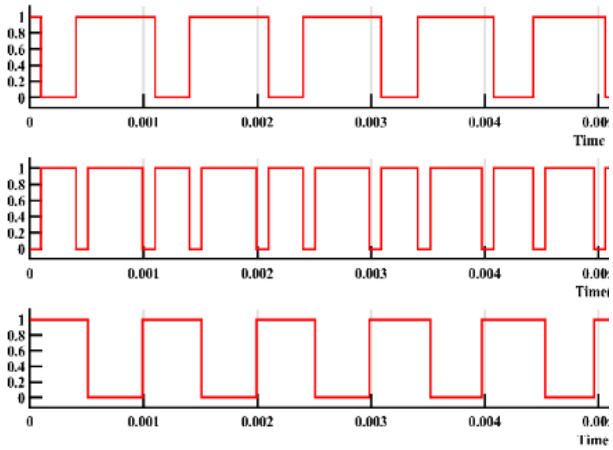


Fig. 8: Switching pulse obtained for upper switches, middle switches and lower switches

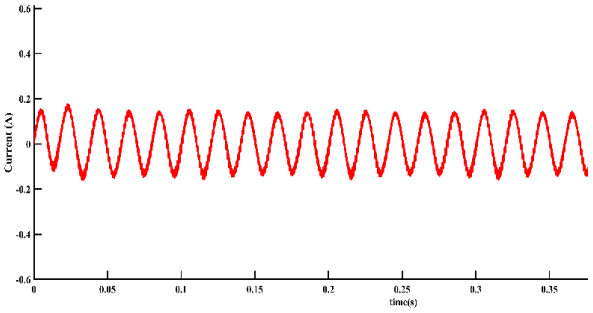


Fig. 9: Simulated current of load 1 connected to upper inverter(phase)

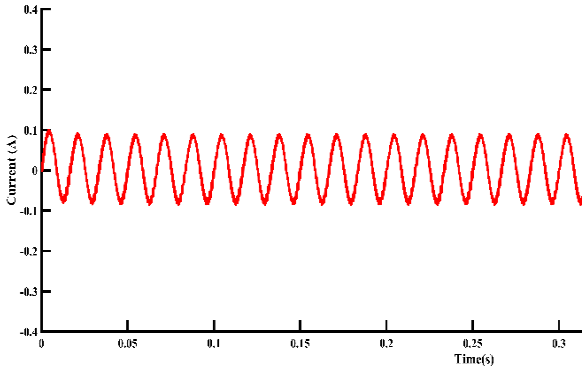


Fig 10: Simulated current of load 2 connected to lower inverter (phase)

generation of gating signal is same as the process of generation for three level inverters. The gating pulses for the upper inverter and the lower inverters is generated by comparison with triangular carrier signal in upper and lower half and for the middle switch logical XOR of the upper switch gate pulses and lower switch gate pulses are executed. Offsets play an important role in deciding the power distribution between the loads. However, it is found that there are stills some ripple in the output current waveform which is mainly due to the interference between upper inverter and lower inverter. Moreover, nine switch converters are a major boost in the inverter area as it reduces 25% of the switches which ultimately leads to lower conduction and switching losses. Also due to a smaller number of switches, complexity of the circuit reduces due to a smaller number of gating circuits required and less space required for the converter.

5. Conclusion

The applicability of space vector modulation (SVPWM) to the nine-switch converter employing two different three phase loads was analysed. The waveform of currents for each phase clearly shows that two three phase loads can be controlled independently by the converter. The need of adding offset is also explained in this paper. The simulation is also performed so as to verify the output current of the inverters for the loads.

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