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Dhandapani, Vaithiyanathan
Department of Electronics and Communication Engineering, National Institute of Technology Delhi

Alok Kumar Mishra
Department of Electronics and Communication Engineering, National Institute of Technology Delhi

Thakur, Richa
Department of Electronics and Communication Engineering, National Institute of Technology Delhi

Chopra, Urvashi
Department of Electronics and Communication Engineering, National Institute of Technology Delhi

他

https://doi.org/10.5109/6793656

出版情報：Evergreen. 10 (2), pp.1010-1016, 2023-06. 九州大学グリーンテクノロジー研究教育センター
バージョン：

Performance Analysis of Pulse Triggered Flip-Flop

Vaithiyanathan Dhandapani[1,*], Alok Kumar Mishra[1], Richa Thakur[1], Urvashi Chopra[1], Britto Pari J[2]

[1]Department of Electronics and Communication Engineering, National Institute of Technology Delhi, India – 110040

[2]Department of Electronics and Communication Engineering, Vel Tech Rangarajan Dr.Sagunthala R&D Institute of Science and Technology, Chennai – 600062, India

*Author to whom correspondence should be addressed:
E-mail: dvaithiyanathan@nitdelhi.ac.in

(Received February 1, 2022; Revised May 14, 2023; accepted May 14, 2023).

Abstract: The power efficiency and speed are two main concerns in any digital as well as analog circuit design. In this work, we analyze the pulse-triggered flip-flop (PTFF). In PTFF have two main stages, the pulse generator (PG) and the latch circuitry. We have utilized PG that has four transistors which is less than the number of transistors comparison to the previously used PGs. The design has been implemented on Cadence Virtuoso using 22nm CMOS cell library. The various parameters like data-to-output (D-to-Q) delay, leakage power and power-delay product (PDP) are being compared with existing flip-flop circuits like master-slave flip-flop (MSFF), DFF and conventional PTFF. The modified PTFF shows 24.3% improvement in D-to-Q delay and 18.1% improvement in PDP as contrast to the conventional PTFF.

Keywords: Flip-Flop, Pulse Generator, Low Power, Power Delay Product, CMOS

1. Introduction

In the digital world the semiconductor memory cell used as a storage device for storing one bit of information either 0 or 1. Flip-Flop (FF) designs underwent lots of advancement with the novel process technology and over the years new FF designs with improved speed, low voltage requirement and low power have been reported. As power efficiency is one of the major concerns and Flip-Flops along with the clock circulation set-up alone constitutes 20% to 45% of power in any digital circuit[1, 2]. Thus for minimizing the power dissipation, various low power and high speed FF has been proposed over past several years[3-19]. The FFs are mainly divided into four groups: Pulse Triggered FFs (PTFF) [12], Dual edge Triggered FF (DETFF)[13], toolbar Transmission Gate FFs (TGFF) and Master Slave FFs (MSFF). Due to its single latch structure, PTFF is more commonly used as compared to TGFF and MSFF. Thus PTFF has lower power consumption and better speed.

1.1 Pulse Triggered Flip Flop

The PTFF has two main stages, called as pulse generator (PG) and a flip-flop or latch stage. The pulse generation in PTFF can be classified as implicit PTFF (IPTFF) in Fig. 1 and explicit type PTFF (EPTFF) in Fig.2. In an IPTFF the PG is one component of the latch design. While in case of an EPTFF, PG and latch circuits are separated. Due to the separate PG circuitry, EPTFF consume more power.

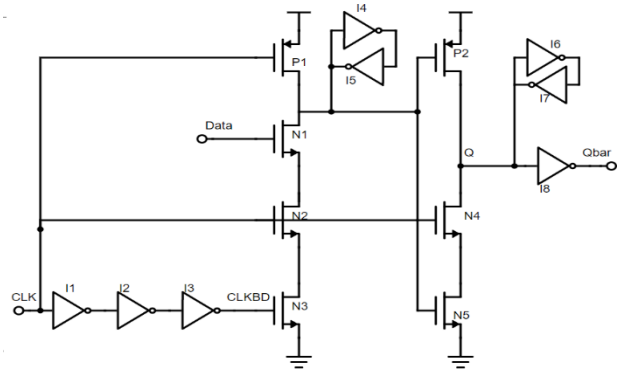

Fig 1: Implicit Pulse Triggered Flip-Flop[3)]

However if there are many FFs in the circuit and the same PG is being shared by several FFs than the EPTFF are more power efficient in comparison to the IPTFF. In addition to that IPTFF has longer discharging path, due to this logic separation from the latch EPTFF are comparatively faster in operation.

The conventional EPTFF named as explicit pulse triggered data close to output FF in Fig. 2. The FF in Fig. 2 is NAND based logic, in the circuit transistors P1 and N2 are connected to the pulse clock (Pulse_ck) due to the

reduced ON time of the transistor N2. Due to this current dissipation is gets reduced and hence there is minor reduction in the power dissipation also. The I1 and I2 have been used to retain node X value and the shortest path of this circuit has three transistors. In this circuit the main setback is the long transition delay time from 0 to 1. It is mainly because of input data which must passes through the transistors N1 and N4. Due to this pulse clock must turn on the transistor N3 in order to modify the assessment of node Q. At the same time another setback of the circuit is that the node X is discharged through N1 and N2 transistors. This is not considering the data in each rising edge of the clock. Because of these factors there is raise in the power dissipation[8].

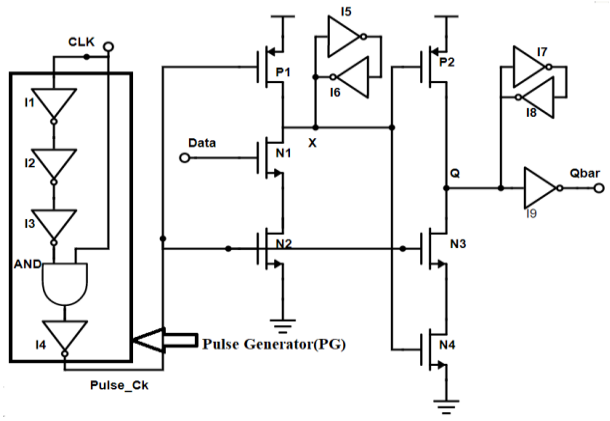

Fig 2: Explicit PTFF[3]

1.2 Dual Edge Triggered Flip-Flop

The DETFFs in principle has capability to transfer data in both the rising as well as falling edge of clock pulse. The circuit of conventional DETFF is in Fig. 3. As compared to single edge triggered FF the DETFF transferring data to the output more accurately. But at the same time due to their complex architecture it dissipates more power.

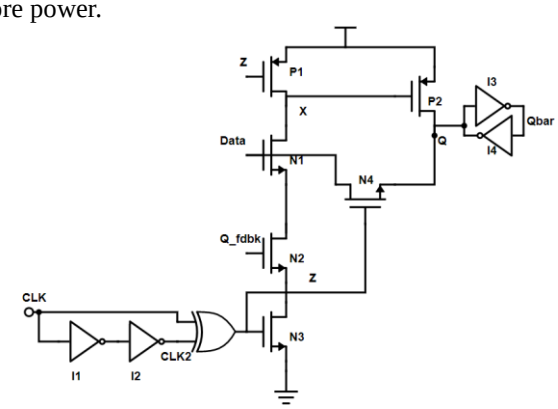

Fig 3: Dual Edge Triggered FF[4]

1.3 Master Slave Flip-Flop

Cascading of master and slave latches as in Fig. 4 is the MSFF. The logic schematic of conventional SR latch based MSFF using MOS transistor is in Fig. 5. When clock = 0, the master latch is transparent. At that time input data passed through the AND-OR-Invert gates. The output of the node X3 is always complementary to the applied input. When clock = 1, the slave latch becomes transparent. The slave latch also consists of two AND-OR-Invert gates and a NOT gate.

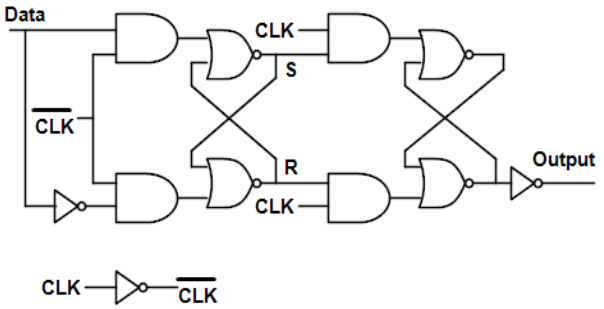

Fig 4: Conventional SR latch based MSFF[5]

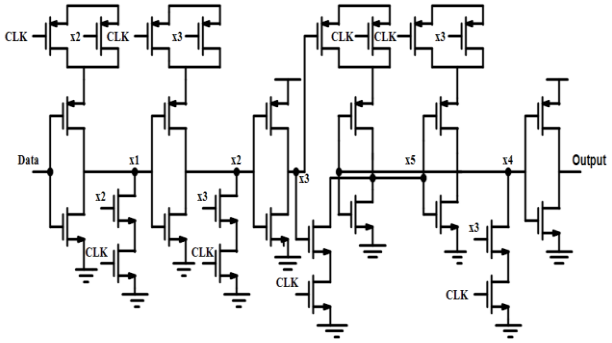

Fig 5: Conventional MSFF circuit[5]

The topologically compressed MSFF (TCMSFF) is in Fig. 6. In the circuit the number of transistors is reduced from 28 to 21 in comparison to the conventional MSFF. In TCMSFF the number of transistor are drive unswervingly by the clock signal are three. This leads to major lessening in power dissipation[7].

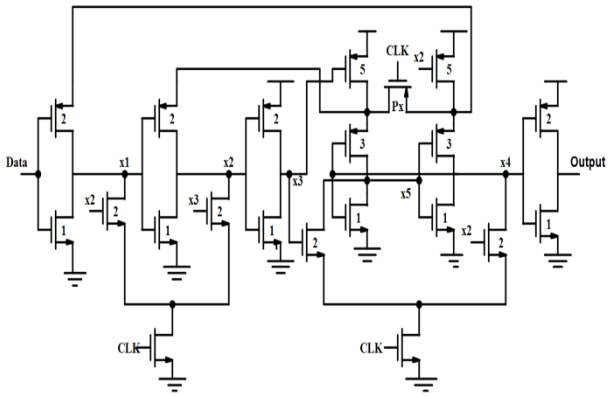

Fig 6: Topologically Compressed FF[6]

So, compare to the conventional MSFF, the TCFF design has three optimized factors. First it uses single phased clock, and second is reduction in the transistors driven directly by the clock and the third factor is, it uses lesser number of transistor in the circuit. At the same time the major drawback of TCFF is that, the design has a longer setup time despite of the significant enhancement in the power consumption[20-28].

1.4 Transmission gate Flip-Flop

The TGFF in Fig.7 comprises two transmission gate based latches. Its main drawback is that even if the input is static, there is sustained power consumption.

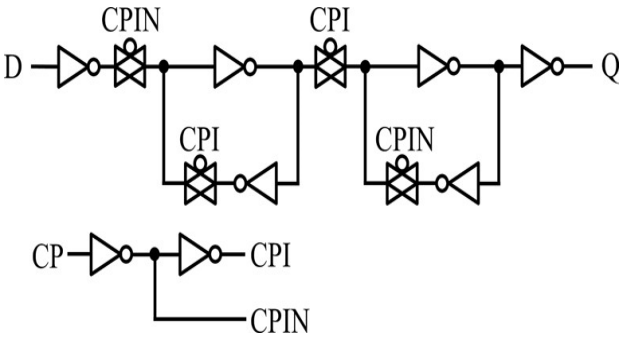

Fig 7: Schematic of TGFF[7]

Rest of paper flow is as follows: The reported and modified circuits of various FF are illustrated in Section 2. In Section 3 describes the experimental environment and result analysis and finally paper concluded in Section 4.

2. Modified pulse triggered flip-flop

PTFF is most widely used because of its single latch structure, better speed and it is more power efficient. As we aware that the PTFF has two blocks that is PG and flip-flop or latch. The pulse generator is used for triggering the latch. On the basis of whether the PG is a part of the latch circuitry or not, it is either implicit PTFF or explicit PTFF. The modified EPTFF (MEPTFF) is in Fig. 8. The PG presented in[8] as shown in rectangular box in Fig. 8, has been used to generate the trigger pulse.

The pulse generator circuit used in the modified explicit PTFF is in Fig. 9, consists of only four transistors. This leads to the reduction in power consumption when compared to the other pulse generators. In all other PG, several NOT gates were used to generate delay, but an improved NOT gate is used in the modified circuit. When Clk =0, only transistor TP1 is ON and transistors TN1, TN2 and TN3 are OFF. Since the transistor TP1 is ON, the state of node A gets changed. When Clk=1, first the transistor TN1 turns ON and after some time turns ON the TN2 and TN3. This is due to the size of TN3 transistor is larger in comparison to the TN1 and TN2. After a small time, the node A gets discharged. This is due to the transistors TN2 and TN1 which would act like pull down transistors. So, the Clk_pulse value is changed to 0. But since there is a delay time of TN1 and TN2 NMOS transistors so a pulse is generated in node Clk_pulse and the width of the generated pulse is enough to turn ON the other transistors used in the circuit. The TN1 and TN2 transistors size should be smaller in size than transistor TN3. So that the minimum clock pulse is allowed to pass through the TN3 transistor before discharging node A. The simulation waveform of the pulse generator has been shown in Fig. 10.

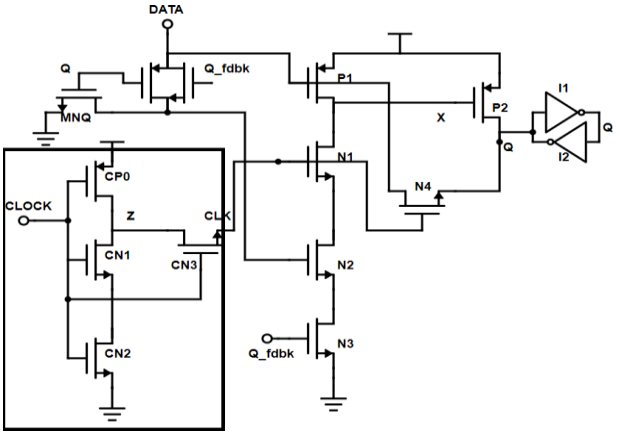

Fig 8: Conventional explicit PTFF 8) with modified PG

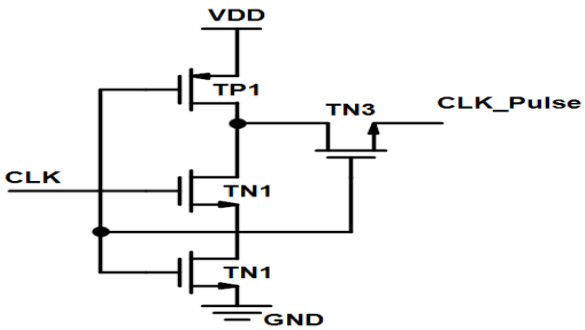

Fig 9: Schematic of the Pulse Generator

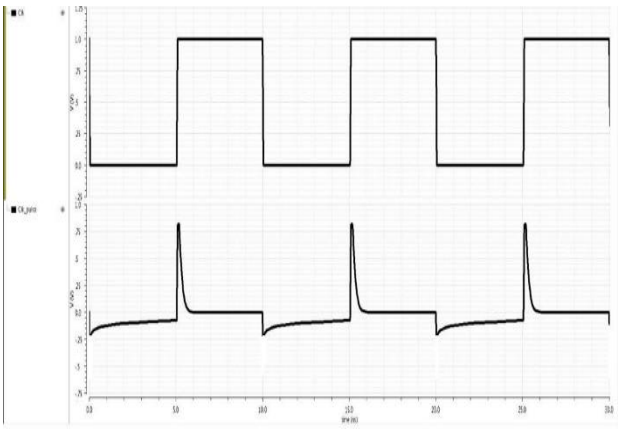

Fig 10: Simulation waveform of the PG

The second stage of an explicit PTFF is latch circuit. The latch is used to store one bit of binary data in the form of 0 or 1. The schematic of used latch and their simulation waveforms has been presented in Fig. 11 and 12 respectively. The complete circuit of modified FF in this work is shown in the Fig 13 and the simulation waveforms of conventional PTFF and MSFF were presented in Fig 14-16 respectively.

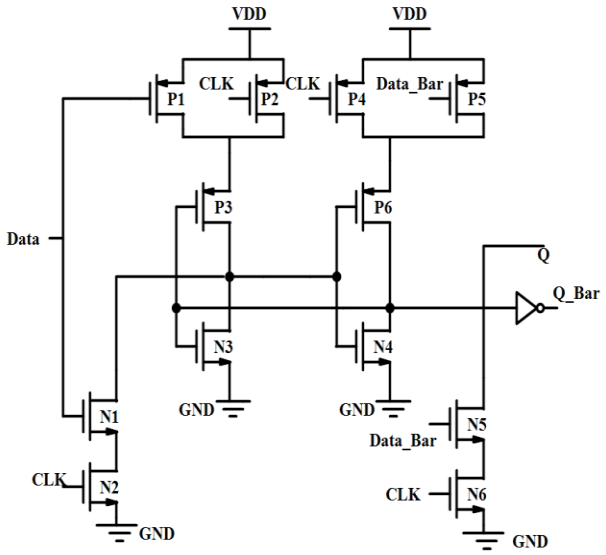

Fig. 11: Schematic of the D FF

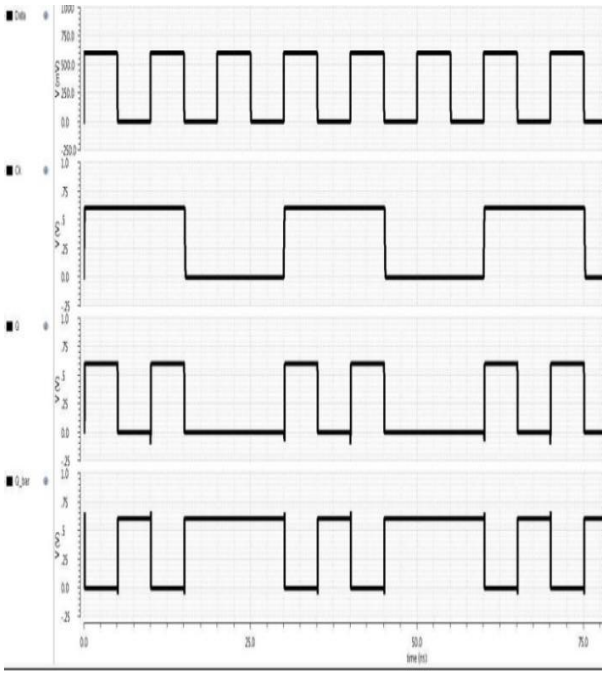

Fig 12: Simulation Waveform of the D FF

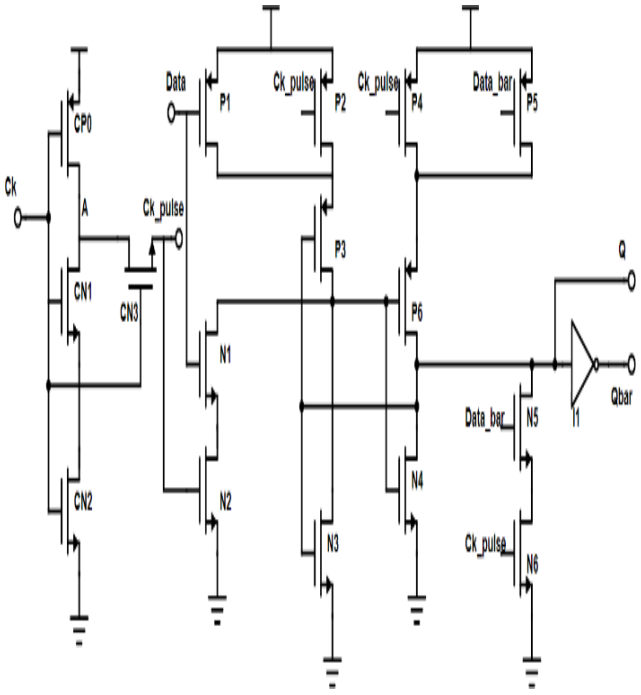

Fig. 13: Schematic of Modified explicit PTFF

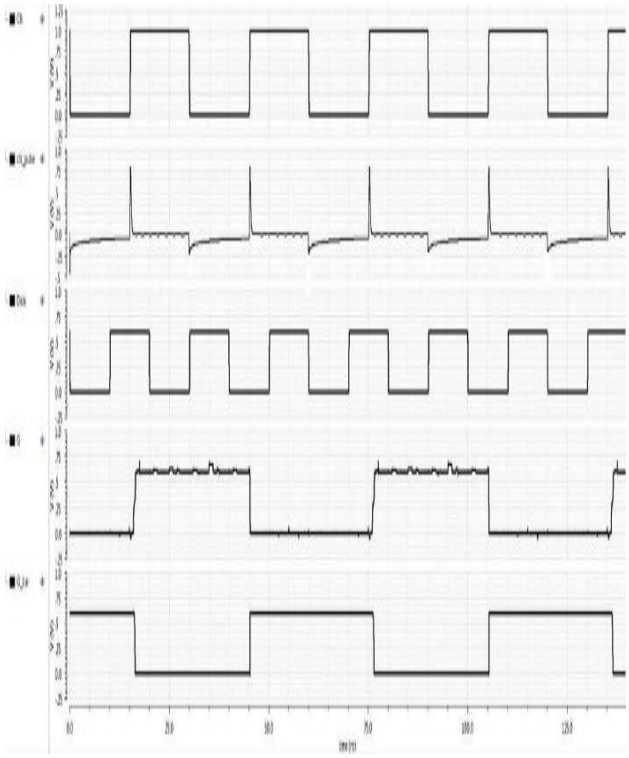

Fig 14: Simulation waveform of the modified explicit

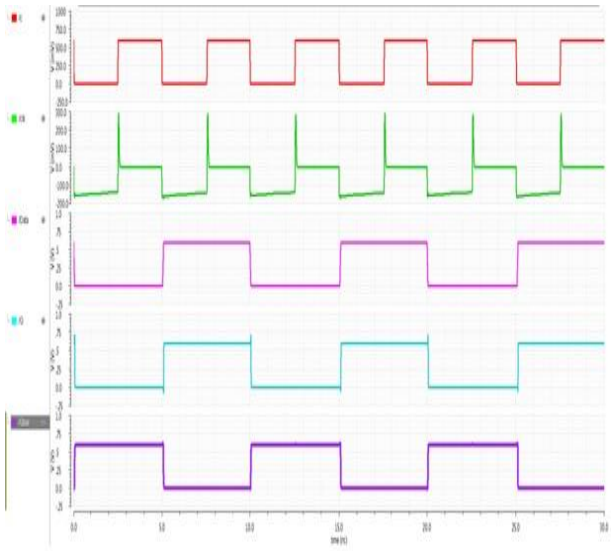

Fig 15:.Simulation Waveform of the Conventional PTFF

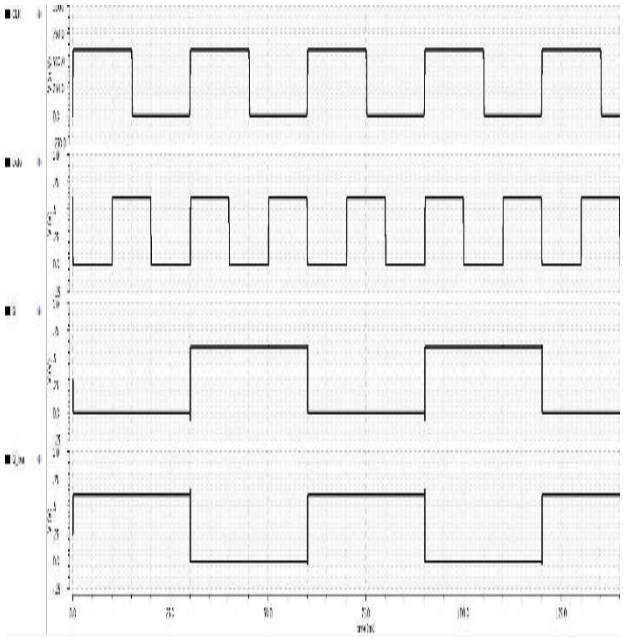

Fig 16: Simulation Waveform of the MSFF PTFF

3. Implementation and experimental evaluation

This section includes the comparison of the modified explicit PTFF with the existing low power FFs like the conventional PTFF, MSFF and D-FF. Various performance indices like power leakage in the standby mode (for various combinations of clock and data), D-to-Q Delay, Clk-to-Q Delay, Power Delay Product (PDP) have been used for the comparison. All the results have been simulated using Cadence Virtuoso tool.

3.1 Evaluation of the leakage power in standby mode

Table 1. Power Leakage(nW) in standby mode at Vdd = 0.6V

(CLK,Data)	DFF	MSFF	Conventional PTFF	Modified PTFF
(0,0)	87.318	130.376	74.53	72.87
(0,1)	43.866	66.78	58.97	37.874
(1,0)	79.54	89.65	81.12	82.67
(1,1)	27.14	46.98	39.73	21.23
Average	59.47	83.45	63.58	53.6

The standby mode involves connecting Clk and Data with DC Voltage signals. The comparison results of the leakage power in standby mode at 0.6 V value of Vdd is presented in Table 1 and Fig.17. There is an improvement of 16.67% in the leakage power as compared to the conventional PTFF. Fig. 18 is the simulation results of the current at different values of the supply voltage are 0.6V, 0.8V and 1V.

3.2 Evaluation of the leakage power in Standby Mode

The performance evaluation of various FF on the basis of various parameters like transistor count, Clk-to-Q delay, D-to-Q delay, Power Dissipation and overall PDP is presented in the Table 2. From the table 2 it is observed that the modified PTFF for D-to-Q delay and power consumption improvement is about 24.3% and 36.12 % when compared to the conventional PTFF respectively with slight increase in Clk-to-Q Delay.

Table 2. Performance Analysis of the various Flip Flops at Vdd=0.6 V

Parameter	MSFF	DFF	Conventional PTFF	This Work
Number of Transistors	28	14	17	18
D-to-Q Delay(ns)	45.2	37.68	19.5	14.76
Clk-to-Q Delay(ns)	30.17	19.92	27.54	29.92
Power dissipation (nW)	83.45	59.47	63.58	53.66
***PDPDtoQ*(pJ)**	3.771	2.24	1.24	0.792
***PDPC toQ*(pJ)**	2.517	1.184	1.75	1.605

4. Conclusion

Reducing the power consumption is a growing concern in today's world. In this work, we presented the circuit to improve the performance of PTFF in terms of power, delay and PDP has been proposed. As the Flip Flops are the basic storage devices in any digital circuit, so the improvement in above mentioned parameters can improve the memory cell and microprocessor performance. Simulations have been performed on

Cadence Virtuoso tool. Despite a slight increase in Clk-to-Q Delay, the power consumption is reduced. Various performance indices like power consumption, D-to-Q delay, and PDP have been used for the comparison. The results show that there is an improvement in the performance of the proposed PTFF in comparison with other Flip-Flop architectures like MSFF, DFF and conventional PTFF. The proposed PTFF shows 24.3% improvement in D-to-Q Delay and 18.1% improvement in PDP as compared to the conventional PTFF.

Competing interests

The authors declare that there is no conflict of interest.

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