High Efficiency and Highly Linear CMOS Power Amplifiers for Radio Frequency Wireless Applications

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High Efficiency and Highly Linear CMOS Power Amplifiers for Radio Frequency Wireless Applications

By

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A DOCTORAL THESIS
SUBMITTED TO THE GRADUATE SCHOOL OF INFORMATION SCIENCE AND ELECTRICAL ENGINEERING IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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Graduate School of Information Science and Electrical Engineering
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2023

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ABSTRACT

Power amplifiers (PAs) are considered to be one of the most important parts of any recently wireless communication systems. These fabricated PAs usually suffer from challenges that should be considered during the designing process. Also, and due to the growing demands for employing advanced modulated high peak-to-average power ratio (PAPR) signals, fabricated radio frequency (RF) PAs generally need to operate at deeper back-off power levels that results in decreasing the operating efficiencies. Furthermore, their operating bandwidth and their non-linear behaviors ought to be strictly considered to meet the requirements of modern wireless communication systems.

Thus, lots of work has been introduced to enhance the operating bandwidth and efficiency of the manufactured PAs in order to minimize the wasted energy that almost converted into thermal emissions which harms the ecosystem of our planet. Additionally, by reducing the non-linear behaviors of the employed PAs, receivers can deliver the transmitted signals with minimum distortions that evolves the quality of the service introduced to the customers around the world. Therefore, this thesis focuses on designing and fabricating highly linear and efficient RF PAs using 0.18-µm complementary metal-oxide semiconductor (CMOS) technology.

In this dissertation, first, A two-stage wideband CMOS PA is proposed that uses a superimposed staggered technique and defected-ground-structure (DGS) resonators to achieve a flat gain response over a wide frequency range and higher power added efficiency (PAE). The wideband main stage of the PA is designed at the center frequency and the designed dual-band driver stage is added to satisfy the flat gain response over the extended bandwidth of interest. DGS resonators are used to decrease the insertion losses of the employed matching circuits. The manufactured CMOS PA achieved a measured power gain of 12 dB with an overall chip area of 0.564 mm^2 and a saturated output power of 16.6 dBm. The implemented wideband CMOS PA realizes the smallest reported group delay variations (±66 psec.) over the whole bandwidth of interest. It also gives among the best PAE (18.7%) and fractional bandwidth (44.4%) so far. Furthermore, the designed PA achieves small measured error vector magnitude (EVM), that is considered to be suitable for the use in modern wireless applications at sub-*mm*-wave frequency bands, when it is tested with a 400-MHz fifth generation-new radio (5G-NR) signal of 64-QAM modulated signal.

Secondly, A technique for a three-tunable phase compensator is presented and applied in the design of a *K*-band CMOS PA. The suggested phase compensation circuit is mainly used for improving the attainable PAE of the stacked transistor configurations. This improvement can be realized by limiting the effect of the phase shift issues occurred at the stacked configurations. Additionally, the proposed low-pass phase compensator helps to suppress high harmonic signals. The CMOS PA is composed of two stages, a driver stage and a main stage, both built using two-stacked transistor configurations. The resulting RF PA achieved a power gain of 12.8 dB at 23 GHz, an 18.3% PAE and a saturated output power of 16.0 dBm, while occupying an area of 0.604 mm^2 with the utilized pads.

Thirdly, A new two-stage CMOS PA for K-band frequencies is introduced, featuring a capacitive-feedbacked cold-phase compensator (Cold-PC) linearizer and PAE enhancer. The Cold-PC includes a cold-FET analog pre-distorter with a proposed capacitive-feedback technique to improve the linearity of the implemented CMOS PA consuming lower chip area and smaller insertion loss. Later, a low-pass two-tunable phase compensator is designed to reduce phase shift and improve the realized PAE of the employed stacked transistor configuration. The fabricated PA has a measured power gain of 13.4 dB, maximum PAE of 21.2%, and saturated output power of 15 dBm, consuming a chip area of 0.58 mm^2 including the pads. Engaging the Cold-PC also leads to a decrease in EVM distortions of the 400-MHz 64-QAM 5G-NR amplified modulated signal and an enhancement of one-dB compression point's output power (OP_{1dB}) and its PAE by 2.5 dB and 7%, respectively, which, to the best of authors' knowledge, is the highest improvement of the reported *K*-band CMOS PA's linearizers.

Finally, A *C*-band CMOS PA with a capacitive feedbacked analog pre-distorter is introduced. The effect of modifying the width of the utilized cold-FET on the designed PA's linear behavior is presented. The implemented RF PA with the cold-FET linearizer gives at 5 GHz a measured power gain of 10.1 dB, a maximum PAE of 31.9%, a P_{sat} of 15.3 dBm, consuming a chip area of 0.67 mm^2, with the employed pads. The suggested linearizer enhances both the measured OP_{1dB} and its PAE as well. Furthermore, Utilizing the proposed capacitive feedbacked linearizer results in a decrease of the measured EVM distortions of the amplified 64-QAM 100-MHz 5G-NR modulated signal.

ACKNOWLEDGMENT

All praises to the Almighty Allah (SWT), the most magnificent and powerful, that by Allah's will, I am able to successfully complete my Ph.D. thesis as part of the requirements of my Ph.D. study in the Graduate School of Information Science and Electrical Engineering (ISEE), Kyushu University, Japan.

First of all, I would like to express my gratefulness and sincerely to thank my doctoral advisor, Professor Ramesh K. Pokharel for his guidance, encouragement and understanding throughout my research here. I have been inspired by the high standards that he sets for himself and his sharp focus and deep devotion to whatever he works on. I also would like to thank Dr. Adel Barakat for his time and knowledge sharing, which is definitely helpful to deeper my knowledge as well as to enhance my research skills. Furthermore, I want to express my sincere gratitude towards Professor H. Kanaya of the Faculty of Information Science and Electrical Engineering, Kyushu University, and Professor K. Okada of the Faculty of Electrical and Electronic Engineering, Tokyo Institute of Technology, for their support during the measurements.

To my fellow lab mates, thank you for the cheerful environment that we have shared together which makes me feel welcomed.

I would like to take the chance to thank Egyptian and Japanese Governments and the Ministry of Higher Education of the Arab Republic of Egypt for awarding me the scholarship of Egypt-Japan Education Partnership (EJEP) to complete my studies towards the Ph. D. degree.

A lot of credit goes to my father, Eng. Zakaria Alngar, who unfortunately passed away during my studies in Japan and before completing this journey, for his unconditional support, encouragement, and prayers.

To my family, I cannot say in words how lucky I am to constantly receive encouragement and prayers from you. My mother and my siblings, thank you very much for your endless love and support. Also, thanks for the good times spent with my kids, Hafsa and Habiba, that undoubtedly relieved stress during the study period.

Finally, I am deeply grateful to my wife, for her love, encouragement, and support all the way through this journey.

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LIST OF ABBREVIATIONS

3G	Third generation
3GPP	Third Generation Partnership Project
4G	Fourth generation
5G	Fifth generation
5G-NR	Fifth generation-new radio
π-PC	π-phase compensator
ac	Alternative current
AM-AM	Amplitude-modulation-to-amplitude-modulation
AM-PM	Amplitude-modulation-to-phase-modulation
APD	Analog pre-distorter
BW	Bandwidth
BW_{3dB}	Three-dB bandwidth
CDMA	Code-division multiple access
CF-APD	Capacitive feedbacked-analog pre-distorter
CMOS	Complementary metal-oxide semiconductor
Cold-FET	Cold-field effect transistor
Cold-PC	Cold-phase compensator
CS	Common source (
CW	Continuous wave
dc	Direct current
DGS	Defected ground structure
EM	Electro-magnetic
EVM	Error vector magnitude
FBW	Fractional Bandwidth
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
GD	Group delay
H-field	Magnetic field

IEEE	Institute of Electrical and Electronics Engineers
IMD	Intermodulation distortions
IMD3	Third order intermodulation distortions
IMD5	Fifth order intermodulation distortions
InP	Indium phosphide
IP3	Third-order intercept point
LC-PC	Inductive and capacitive-phase compensator
LNA	Low noise amplifier
LTI	Linear time invariant
LTV	Linear time variant
M_1	1st metal layer of the used technology
M_6	Sixth metal layer of the used technology
mm	Millimeter
MMIC	Monolithic microwave integrated circuits
MSL	Microstrip line
OFDM	Orthogonal frequency-division multiplexing
OP_{1dB}	Output power of 1-dB compression point
PA	Power amplifier
PAE	power added efficiency
PAE_{max}	Maximum attainable power added efficiency
PAPR	Peak to average power ratio
pHEMT	Pesudomorphic High-electron-mobility transistor
P_{IIP3}	Input third order intercept point
P_{OIP3}	Output third order intercept point
P_{sat}	Saturated output power
QAM	Quadrature amplitude modulation
Q-Factor	Quality Factor
Q-point	Quiescent point
RF	Radio frequency
SDB	Superimposed dual band
Sh-CTT	Shunt capacitance tuning technique

Sh-ITT	Shunt-inductive tuning techniques
Si	Silicon
SiGe	Silicon–germanium
S-ITT	Series-inductive tuning technique
S-parameters	Scattering parameters
ST	Stacked transistors
STC	Stacked transistor configurations

CHAPTER 1: INTRODUCTION

1.1. Motivation

Today's trends in the entire world go towards the online applications that are considered to be the easiest, cheapest, and safest way to accomplish our daily-life routines, especially after the Covid-19 pandemic. These applications such as shopping, paying bills, banking, business meetings, booking hotels and transportations, and even using autonomous vehicles, depend by some means on transferring data wirelessly. These transferred data must be received with high accuracy and high data rates to meet the market requirements, which require using varying and wide frequency bands and high peak to average power ratio (PAPR) signals with advanced and complex modulation techniques. Thus, the evolution of the generations of the wireless communication systems phenomenally grows to satisfy these business demands and enhancing our quality of life particularly in last fifty years, as shown in Fig. 1-1.

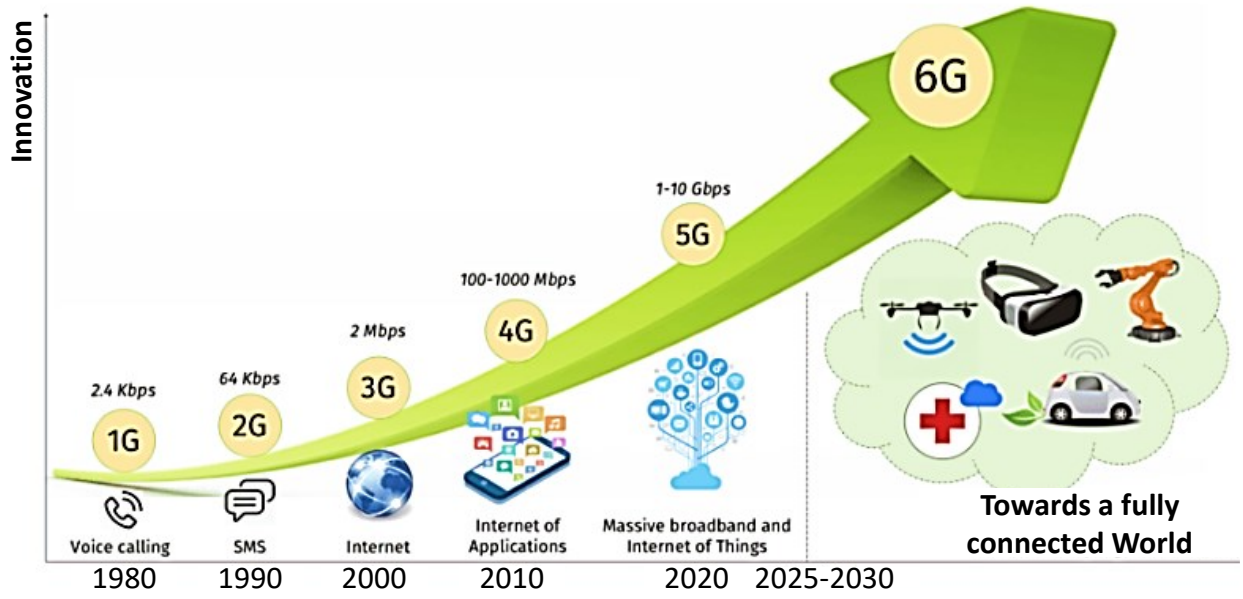


Fig. 1-1. Evolution of the wireless generations towards a fully connected world.

At the majority of these wireless communication systems, power amplifiers (PAs) are playing a vital role in designing transceivers' front ends. Accordingly, enhancing the performance of the

employed radio frequency (RF) PA would undoubtedly improve the whole system performance, as illustrated in Fig. 1-2.

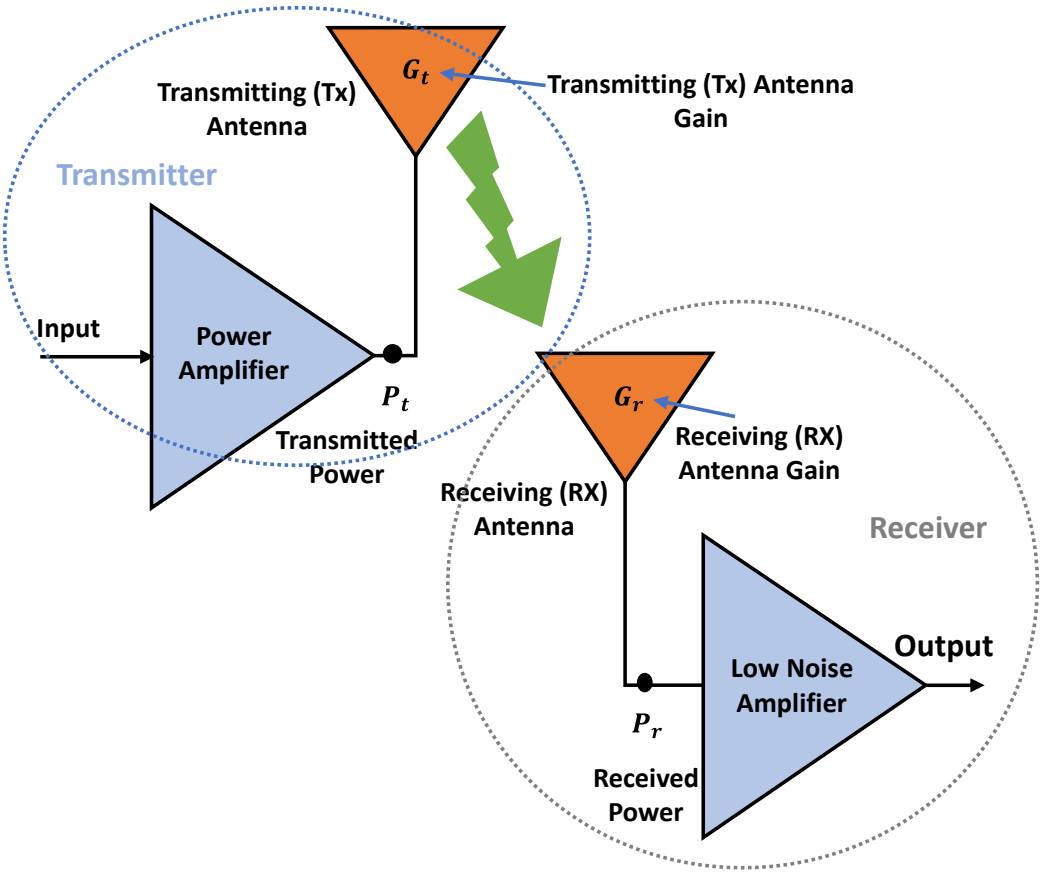


Fig. 1-2. Portion of the wireless transceiver frond-end.

Designing a PA with higher efficiency has become applicable, thanks to the progress of the transistors' manufacturing technologies. However, designing a highly linear and efficient RF PAs dealing with the modern wireless communication systems is still challenging. Due to the nature of the used highly PAPR signals with modern modulation techniques such as quadrature amplitude modulation (QAM), code-division multiple access (CDMA) and orthogonal frequency-division multiplexing (OFDM) techniques [1]. Thus, RF PAs usually operate at higher power back-off levels from their saturation levels to ensure a proper signal delivery with minimum signal distortions and lower interferences at the adjacent channels for achieving the required standards by the governing global authorities such as Institute of Electrical and Electronics Engineers (IEEE) and Third Generation Partnership Project (3GPP) standards. Unfortunately, operating at these higher back-off levels is accompanied by the reduction of the operating efficiencies [2]. Thus, lots

of work has been introduced for enhancing the overall efficiency of the designed RF PAs and improving their linear behaviors in order to enhance the quality of the received signals and save the waste of energy converted mainly into thermal emissions due to the environmental aspects, expanding battery life, and reducing in the cooling, noise, and operating expenses.

1.2. Objectives

The objective of this dissertation is to design and fabricate highly linear and efficient RF complementary metal-oxide semiconductor (CMOS) PAs. This research focuses on four key points:

- Improving the efficiency of the designed RF CMOS PA by employing high Quality (Q-) factor on-chip defected ground structure (DGS) resonators.
- Extending the operating bandwidth (BW) with maximally flat gain response by using a proposed superimposed dual-band configuration.
- Decreasing the intermediate phase shift problem of the stacked transistor configurations (STCs) by employing a suggested phase compensation technique.
- Enhancing the linear behavior of the designed CMOS PAs by using a proposed capacitive feedbacked linearizer.

1.3. Outlines

The thesis is organized as follows:

Chapter 2 illustrates the fundamental concepts of designing RF PAs. Where it describes the main trade-offs of designing RF PAs and different commonly used techniques for enhancing the linearity of PAs. Chapter 3 introduces a designed wideband CMOS PA using a proposed superimposed dual-band configuration and DGS resonators. While in chapter 4, a proposed π-phase compensation technique is employed to improve the power added efficiency of the fabricated stacked *K*-band CMOS PA. Furthermore, A new capacitive feedbacked analog pre-distorter technique is introduced, in chapter 5, to enhance the linear behavior of two fabricated *K*-band and *C*-band CMOS PAs. Finally, chapter 6 includes the conclusion of the dissertation and some suggested points for future work.

CHAPTER 2: POWER AMPLIFIERS AND ENHANCEMENT TECHNIQUES

2.1. Introduction

PAs is one of the most important parts in wireless transceiver designs that is usually located in before the transmitting antenna, as shown in Fig. 1-2. PAs generally determines the amount of the transmitted signal. Therefore, its performance, particularly its efficiency, dominates a significant portion of the whole performance of the wireless communication system. PAs are used to convert a certain part of the direct current (dc) power fed by the used supply voltage into an RF signal that is transmitted carrying the information towards the RF receiver. The amount and the quality of the converted alternative current (ac) signal is mainly attributed to the performance of the employed PA. Thus, several researches have been done to achieve the required performance for each application such as utilizing new manufacturing technologies and modifying new topologies and techniques for designing both active and passive parts of these RF PAs [2], [3].

In general, PAs are divided into two main categories [4]:

- Linear mode amplifiers: These amplifiers are classified according to the amount of the dc biasing current that determines the conduction angles for each class. Hence, this category can also be named as controlled conduction angle amplifiers. These classes are named as Class A, Class AB, Class B, and Class C.
- Switching and current mode amplifiers: The active transistors, in this mode of operation, are considered to be a switch that is turned on and off periodically through the whole operating cycle such as Class D and Class E. While in Class F, a harmonically tunned resonator is used in the output network to enhance the efficiency of the designed PA. These types of PAs are currently out of study in this dissertation.

2.2. Linear Mode RF Power Amplifiers

Designing the linear mode of operation is somehow similar to matching concepts of the small-signal low noise amplifier (LNA) design. Even so, the main difference in designing the PA over the small-signal amplifier is designing proper matching networks. The load and source-pull techniques are usually used to get the optimum source and load impedances that give best efficiency or highest output power of the implemented PA rather than using the conjugately matched technique. For the reason that PAs normally operate at their non-linear saturation regions to deliver higher output power levels.

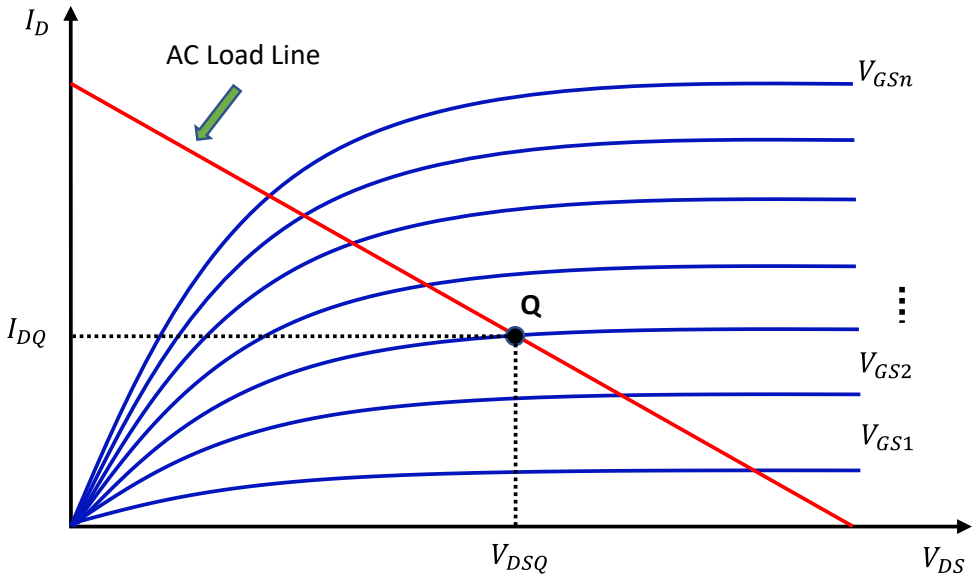


Fig. 2-1. IV characteristics of the n-channel Transistor in Class A amplifier.

In highly varying envelope signals employing today's modulation schemes, the linear mode amplifiers are quite advantageous that should maintain the amplitude and phase of the amplified signal in a good balance. In contrast, the best potential transmitting performance of the constant envelope signals can be accomplished without the need of using these linear amplification methods. Also, dealing with wide bandwidth at millimeter (*mm*-)wave frequency bands in switching mode amplifiers are quite challenging especially with designing the harmonic control circuitry that achieve additional complexity [4]. For that reason, all the designed RF PAs in this study are designed depending on the concept of the linear mode amplifiers where the key differences between the commonly used classes are explained in the following sections as well as some related RF PA's designing concepts.

2.2.1. Class A Power Amplifier

The active device of the PA, in class A mode, stays in the ON-state during the full input cycle. That means the transistor's quiescent (Q-) point is typically in the middle of the I-V characteristics, as shown in Fig. 2-1. A one-stage class A amplifier is basically presented in Fig. 2-2 where its equivalent voltage and current sinusoidal waveforms are simplified in Fig. 2-3(a) and Fig. 2-3(b), respectively.

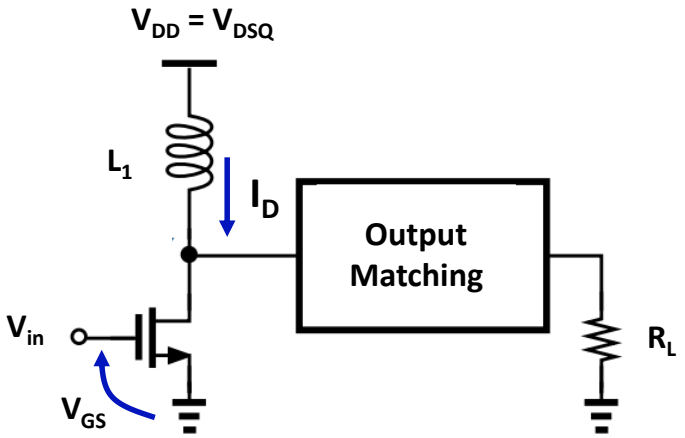


Fig. 2-2. Class A power amplifier.

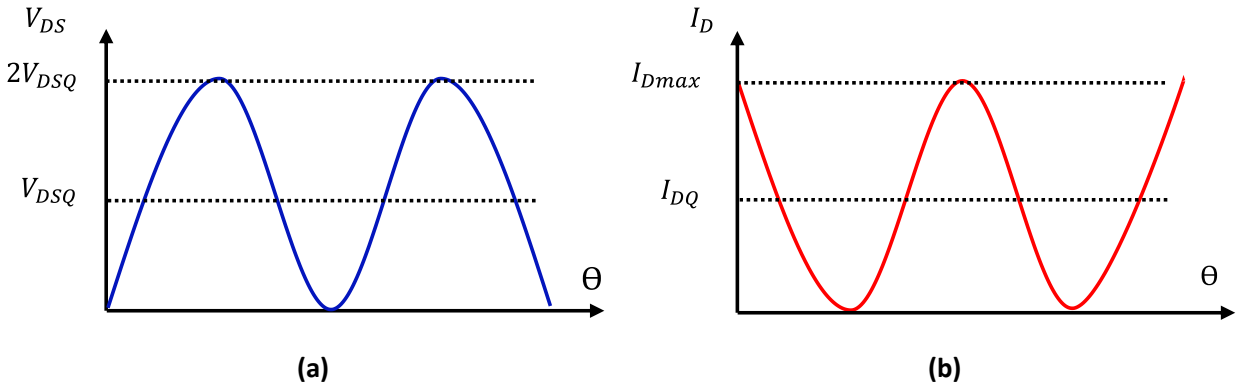


Fig. 2-3.Class A amplifier's voltage and current sinusoidal waveforms

As shown in Fig. 2-2, The total dc power consumed (P_{dc}) by the class A amplifier and the RF output power (P_{out}) can be determined as follows:

$$P_{dc} = V_{DSQ} I_{DQ} \tag{2.2.1}$$

$$P_{out} = \frac{V_{DSmax} - V_{DSmin}}{2\sqrt{2}} \times \frac{I_{Dmax} - I_{Dmin}}{2\sqrt{2}} \quad (2.2.2)$$

For simplicity, the signals of V_{DSmin} and I_{Dmin} can be ignored. Also, for estimating the maximum attainable drain efficiency (η), the V_{Dsmax} and I_{Dmax} should approximately equal $2V_{DSQ}$ and $2I_{DQ}$, respectively. Consequently, the maximum attainable drain efficiency resulting from utilizing the class A power amplifier ($\eta_{Class-A}$) can be determined as follows:

$$\eta_{Class-A} = \frac{P_{out}}{P_{dc}} \times 100\% = 50\% \quad (2.2.3)$$

Fortunately, the transistor used in class A amplifiers can realize high power gains and remain at its linear behavior for most of the operating cycle range. It is worthy to mention that the maximum realized drain efficiency of Class A amplifiers occurs only when the transistor is fully loaded with the output signal. Sadly, the calculated efficiency of the class A PA degrades proportionally to the back-off power level ($\eta_{Class-A,BO}$), as described in (2.2.4). This problem will be worsened while dealing with high PAPR signals.

$$\eta_{Class-A,BO} = \frac{P_{BO}}{P_{DC}} \times 100\% < 50\% \quad (2.2.4)$$

2.2.2. Class AB and B Power Amplifiers

In class AB PAs the gate-source dc bias voltage (V_{GS}) of the transistor is decreased to reach its threshold voltage in case of Class B amplifier mode, as illustrated in Fig. 2-4. This reduction in the assigned V_{GS} decreases the dc quiescent drain current which in turn leads to improve the achieved efficiency of the designed PA. Where the voltage and current signals of the general class AB PA are demonstrated in Fig. 2-5. Due to moving the Q-point closer to the threshold voltage, the positive half cycle of the input signal has the ability to push the output current to I_{max}, however its negative half cycle pushes V_{GS} to lower than the threshold voltage that results in moving the employed transistor to its cut-off region. This illustrates why the voltage and current waveforms are truncated in Fig. 2-5. Extracting the fundamental signal can be performed using a shunt

connected harmonic termination that should be considered in designing the output matching network.

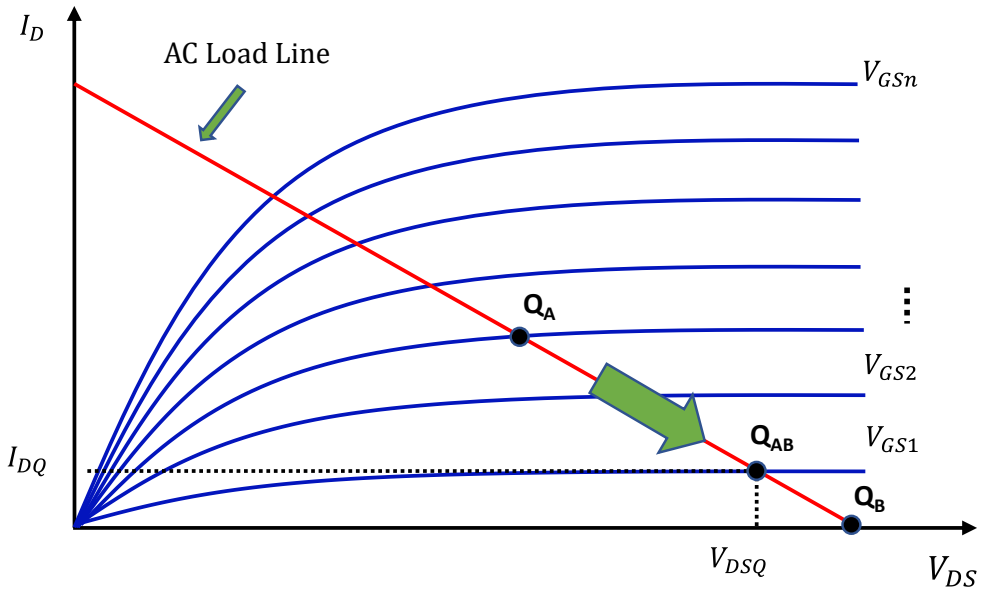


Fig. 2-4. IV characteristics of the n-channel Transistor in Class AB and B amplifiers.

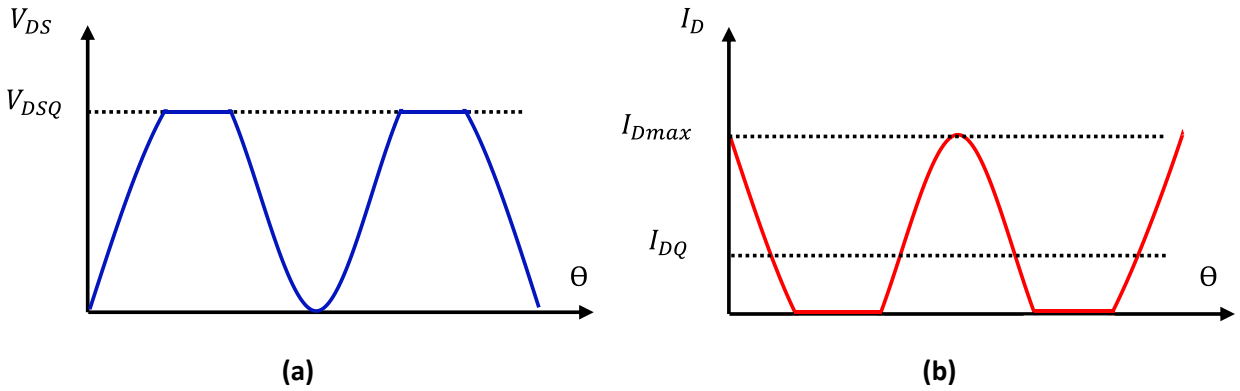


Fig. 2-5. Class AB amplifier's voltage and current sinusoidal waveforms

By assuming that class B amplifier has a zero-dc biasing current that is biased exactly at the transistor's threshold voltage. The fundamental signal of the output current ($I_{(1)}$) and its dc equivalent component (I_{dc}) can be determined as follows:

$$I_{(1)} = \frac{I_{max}}{2} \qquad (2.2.5)$$

$$I_{dc} = \frac{I_{max}}{\pi} \tag{2.2.6}$$

As derived in case of class A amplifier, the RF output power and the equivalent DC consumed power are given as follows:

$$P_{RF} = \frac{I_{max}}{\sqrt{2}} \times \frac{V_{DSmax} - V_{DSmin}}{2\sqrt{2}} = \frac{(V_{DSmax} - V_{DSmin})I_{max}}{4} \tag{2.2.7}$$

$$P_{dc} = \frac{I_{max}}{\pi} \times V_{DD} = \frac{V_{DD}I_{max}}{\pi} \tag{2.2.8}$$

As illustrated in (2.2.7), the maximum attainable efficiency can occur only for the maximum loading output signal where $V_{DSmax} - V_{DSmin} = V_{DD}$. Where, the maximum attainable efficiency can reach up to 78.5% (π/4). Thus, the maximum attainable drain efficiency of class AB power amplifier is between 50% to 78.5% depending on how the gate biasing voltage is close to the transistor threshold voltage.

2.2.3. Class C Power Amplifier

In class C mode configurations, the active used transistor is only turned on for lower than half of the cycle attributable to the reduction in the conduction angle compared with class B amplifiers. The dc biasing voltage at the transistor's gate terminal in class C mode is reduced to levels below the threshold voltage of the working transistor to improve the achieved drain efficiency. This reduction in the operating conduction angle comes at expense of diminishing the linear behavior and the delivered output power of the implemented RF PA. This is the reason why class C amplifiers have been utilized in limited practical designs and applications. Finally, the primary trade-offs between the linear mode RF PAs are summarized in Fig. 2-6 and Fig. 2-7. Where class AB configuration can achieve the highest output power while the drain efficiency increases with decreasing the conduction angle to reach theoretically 100% at zero conduction angle, as shown in Fig. 2-6. Also, the drain efficiency of the previously discussed PA configurations phenomenally decreases with increasing the power back-off level, as illustrated in Fig. 2-7. Where the Iq shown in Fig. 2-7 is the normalized quiescent current.

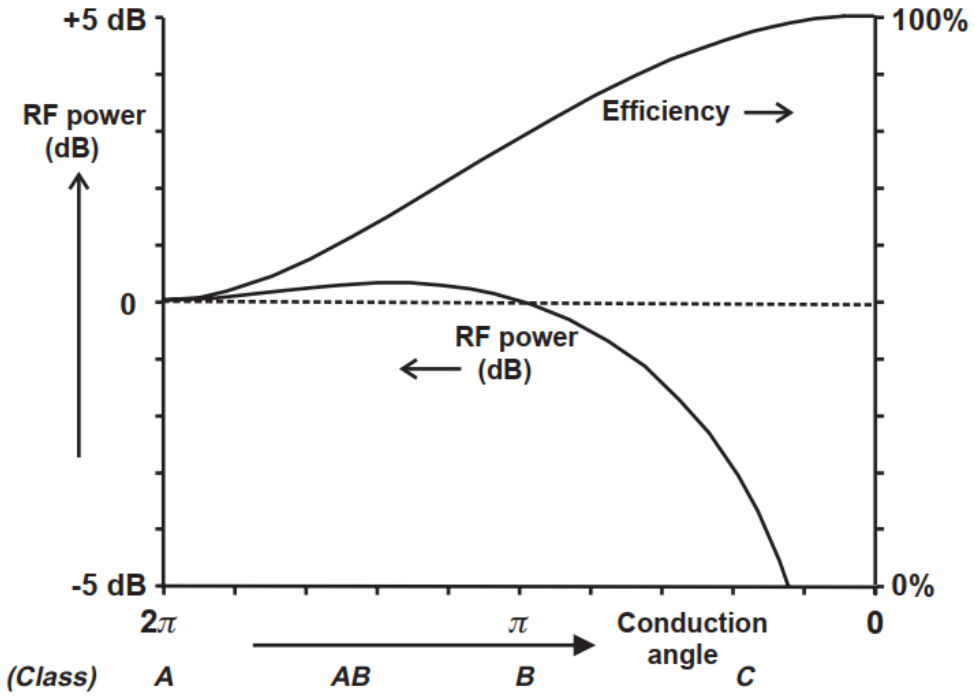


Fig. 2-6. Variations of RF output power of the linear mode amplifiers according to changing the operating conduction angle [2].

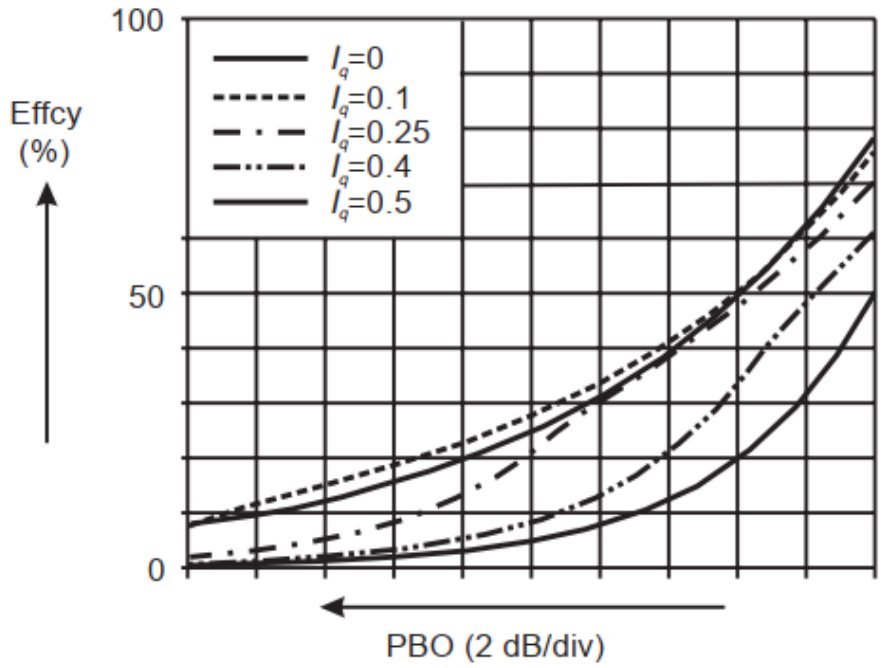


Fig. 2-7. Variations of realized efficiency of the linear mode amplifiers according to changing the back-off power levels [2].

2.3. Power Amplifiers Key Trade-offs

The performance of any designed RF PA can be generally characterized by its power gain, operating bandwidth, stability, linearity, efficiency, maximum output power, and its design reliability, as demonstrated in Fig. 2-8. It is worthy to mention that the performance of the designed PAs especially at high frequency bands would be enhanced by using advanced technologies. For example, using scaled down CMOS transistors that have lower channel lengths can be used for getting higher gain responses and higher efficiencies. However, it has higher costs compared with the older CMOS technologies. In designing PAs, the power added efficiency (PAE) is usually utilized rather than using the drain efficiency because PAs usually has lower power gain characteristics specially at higher frequency bands. Thus, the value of PAE considers the input power level (P_{in}) along with the delivered output power (P_{out}) and the dc power consumption (P_{dc}) as expressed in (2.3.1).

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.3.1}$$

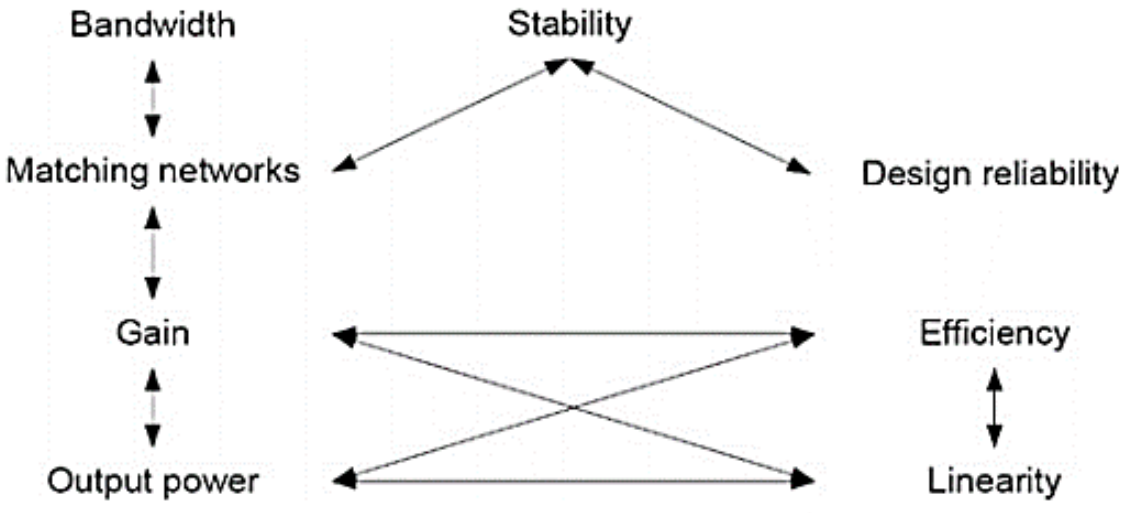


Fig. 2-8. Trade-offs of RF PAs [4].

2.4. Today's Market Technologies for Power Amplifiers Design

Most of PA's parameters such as gain, efficiency, frequency of operation are mainly dependent on the selected active device and its size. Therefore, manufacturing technologies for the used active

transistors have extraordinarily been scaled-down and evolved during last decades to meet the need of business markets and the requirements of transition from one generation to the next, particularly in CMOS technologies, as presented in Fig. 2-9 and Fig. 2-10, and Fig. 2-11.

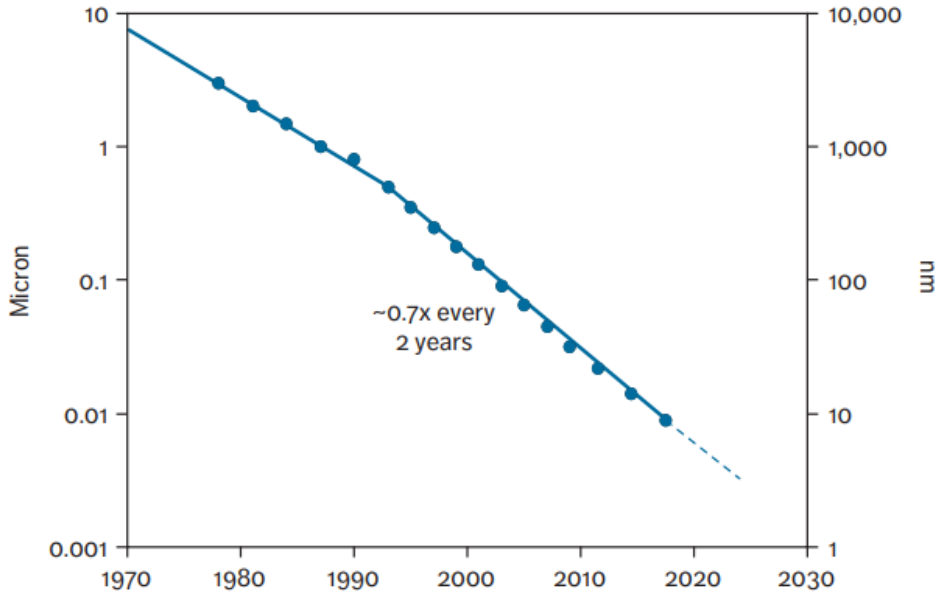


Fig. 2-9. Transistor scaling trends for Intel technologies [5].

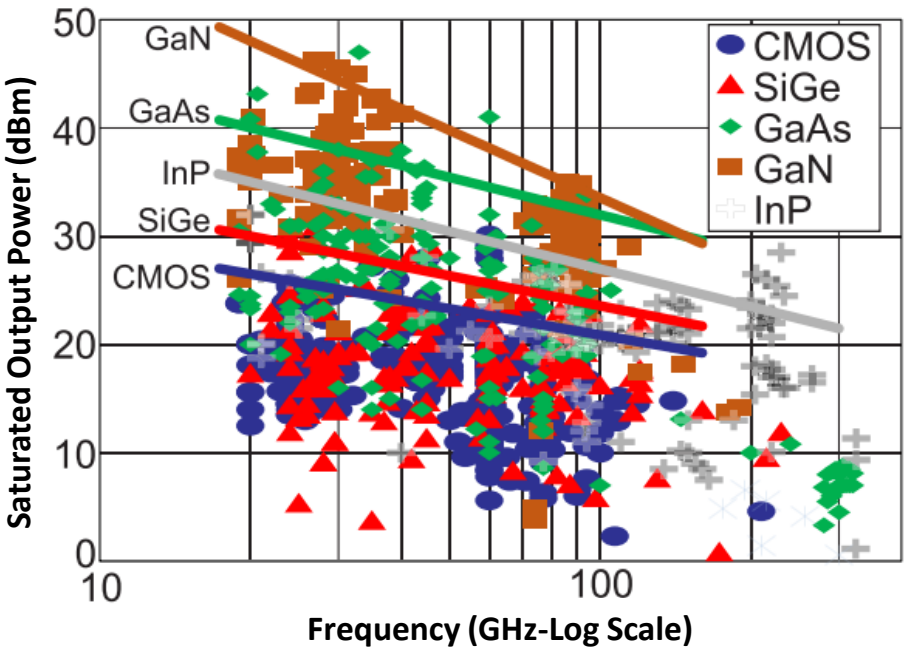


Fig. 2-10. Survey of implemented RF PAs illustrating the variation of the saturated output power versus frequency of operation according to the engaged fabricating technologies [6].

These days, there is an energetic competition between the commonly used device technologies such as, Gallium nitride (GaN), Gallium arsenide (GaAs) and Pesudomorphic High-electron-mobility transistor (pHEMT), silicon–germanium (SiGe), Indium phosphide (InP), and CMOS technologies, to dominate today's market of the wireless communications, as illustrated in Fig. 2-10. The implemented PAs, utilized for designing the base-stations of the fourth generation (4G) wireless communication systems, usually are fabricated using GaN and pHEMT technologies that achieve higher output power levels, as shown in Fig. 2-11. While the handsets transceivers are designed using SiGe and CMOS PAs for their highly integration capability and lower costs.

Table 2-1. SEMICONDUCTOR MATERIALS CHARACTERISITCS OF COMMON ACTIVE COMPONENTS [7].

Property	**Si**	**GaAs**	**GaN**
Bandgap (eV)	1.1	1.43	3.4
Electron mobility ($cm^2/V*s$)	1350	6000	1000
Hole mobility ($cm^2/V*s$)	450	330	30
Saturation field (V/cm)	$1*10^7$	$1*10^7$	$2*10^7$
Saturation Velocity (cm/s)	$8*10^3$	$3*10^3$	$15*10^3$
Breakdown filed (V/cm)	$7*10^5$	$7*10^5$	$35*10^5$
Thermal conductivity (W/cm*K)	1.5	0.46	1.7
Dielectric constant	11.9	12.5	9.5

Fortunately, The required output power levels for fifth generation (5G)'s RF PAs is lower compared with the third generation (3G) and 4G PAs owing to using multiple amplifiers and applying enhanced directionality techniques [8]. Hence, the scaled CMOS technology can be employed for implementing both base-stations and handset cells, as illustrated in Fig. 2-11. Where the leading semiconductor material properties are listed and compared in Table 2-1.

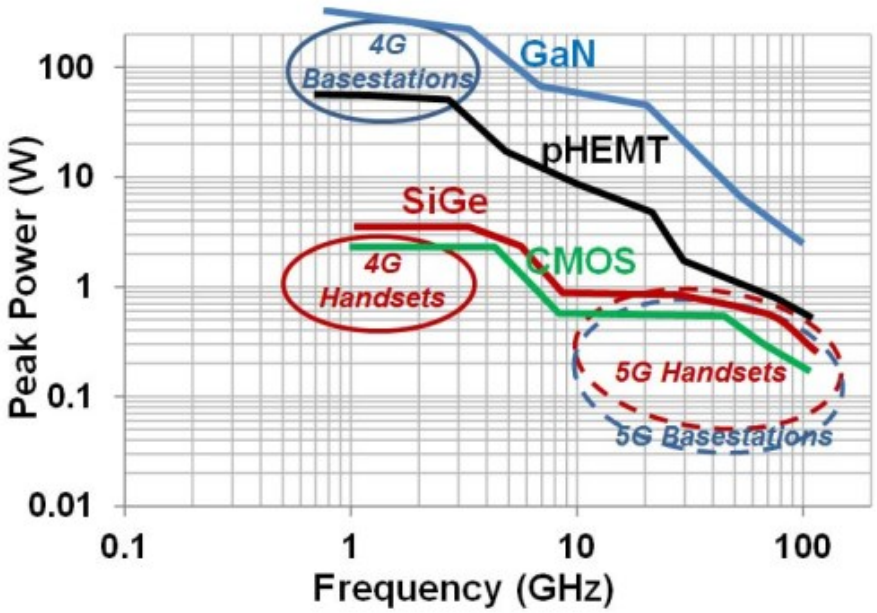


Fig. 2-11. Commonly used manufacturing technologies in 4G and 5G business market [8].

2.5. Load/Source Pull Technique

Load/Source-pull technique is the technique that refers to extracting the optimal performance from the device under test [9]. This device will be the designed CMOS PA in this study. In load and source-pull simulations or measurements the load and source impedances are changed in both its real and imaginary components to get the optimal performance of the PA. It is commonly known that the passive components are linear, and they can be fully characterized using the linear scattering (S)-parameters. This assumption is still valid even in RF frequency bands [10]. However, in designing RF PAs, the employed active transistors have non-linear behaviors that cannot be accurately characterized utilizing the frequency-dependent S-parameters. For instance, the output volage signal and the corresponding current are not linearly related in active non-linear transistors. Where this non-linearity produces undesirable spectral growth, deteriorating harmonics signals, and intermodulation distortions that should be wisely considered while dealing with such non-linear components. Unlike the linear cases, where their optimal performances are directly dependent on the S-parameters of the device under test, the optimal loading conditions of the RF PAs are identifying considering the non-linear behaviors of the employed transistors [11]. Where the correct choice of the input and output impedances guarantee the enhancement of the

overall trade-off performance of the designed PAs. This selection of the impedance terminations, as illustrated in Fig. 2-12, can be done through load and source pull techniques [12]. The variations of the load and source impedances can be done using a high accurate computer-added design tool such as Cadence and Keysight ADS simulators while the load and source-pull measurements can be accomplished by utilizing a suitable impedance tuner. Physically, as shown in Fig. 2-12, extracting the desired parameters can be done by using an input and output tuners that changes the source (Γ_S) and load (Γ_L) reflection coefficients, respectively [13].

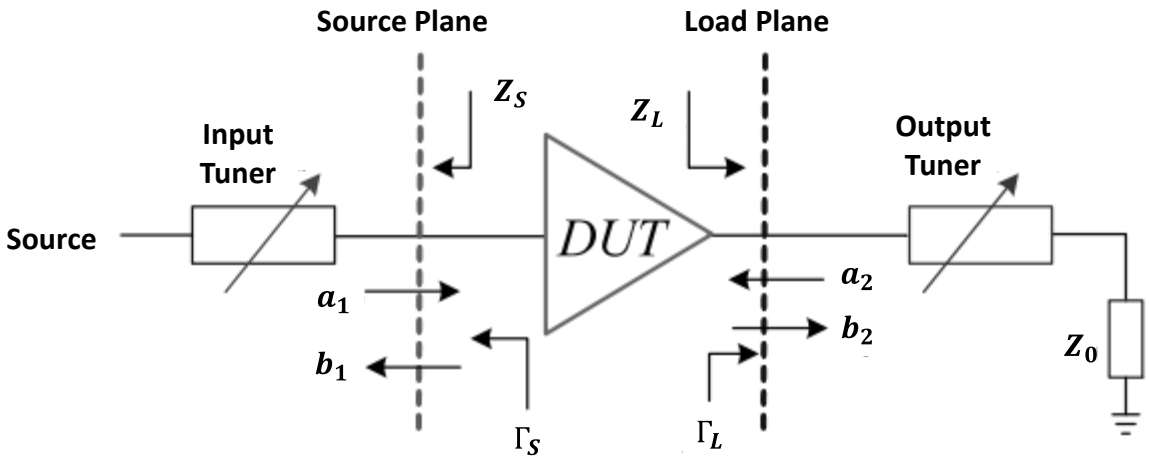


Fig. 2-12. Load and source-pull techniques using output and input tuners [13].

Where source impedance (Z_S), and the load impedance (Z_L) are related with Γ_S and Γ_L, respectively by the following equations:

$$\Gamma_S = \frac{a_1}{b_1} \tag{2.5.1}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.5.2}$$

$$\Gamma_L = \frac{a_2}{b_2} \tag{2.5.3}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.5.4}$$

Z_0 is the characteristic impedance of the system where the implemented PA will be employed which is normally (50 Ω) system.

2.6. Power Amplifier Linearization Techniques

This section focuses on the common linearization techniques utilized to improve the linear behaviors of RF PAs.

2.6.1. Linearity Related Fundamental Concepts

2.6.1.1. Linear Time Invariant/Variant System

The linear time invariant (LTI) system is described by utilizing its impulse response ($h(t)$) where the LTI's output signal ($S_{out}(t)$) is determined by using the convolution relationship according to its input signal ($S_{in}(t)$) as follows:

$$S_{out}(t) = S_{in}(t) * h(t) \tag{2.6.1}$$

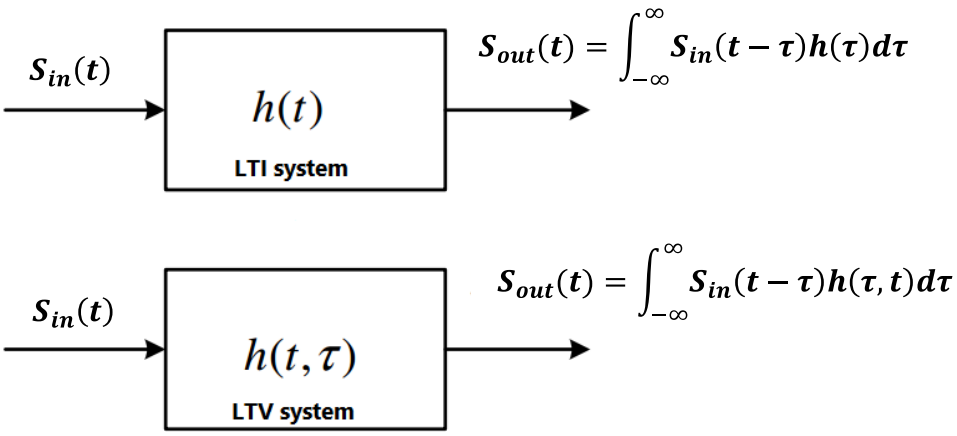


Fig. 2-13. Difference between LTI and LTV systems.

Alternatively, the linear time variant (LTV) system is a system whose output signal depends on the corresponding input signal and the moment of the observation as well. Where the impulse response of that LTV system varies according to the moment of observation, as shown in (2.6.2). The difference between the LTI and LTV systems are summarized in Fig. 2-13.

$$S_{out}(t) = S_{in}(t) * h(t,\tau) \tag{2.6.2}$$

2.6.1.2. Memoryless Non-Linear System

In non-linear systems without memory effect problem, their output responses depend only on the instantaneous input signals and their non-linear system's coefficients (b_k), as presented in the following equation

$$S_{out}(t) = \sum_{k=1}^{K} {S_{in}}^{k}(t)\left|{S_{in}}^{k}(t)\right|^{k-1} \tag{2.6.3}$$

2.6.1.1. Memory Non-Linear System

In the non-linear system, which has a memory effect, the output response of that system does not depend only on the instantaneous input signal and its non-linear system's coefficients but also depends on the past values of the input signal. These systems are usually characterized using Volterra series, as described in (2.6.4).

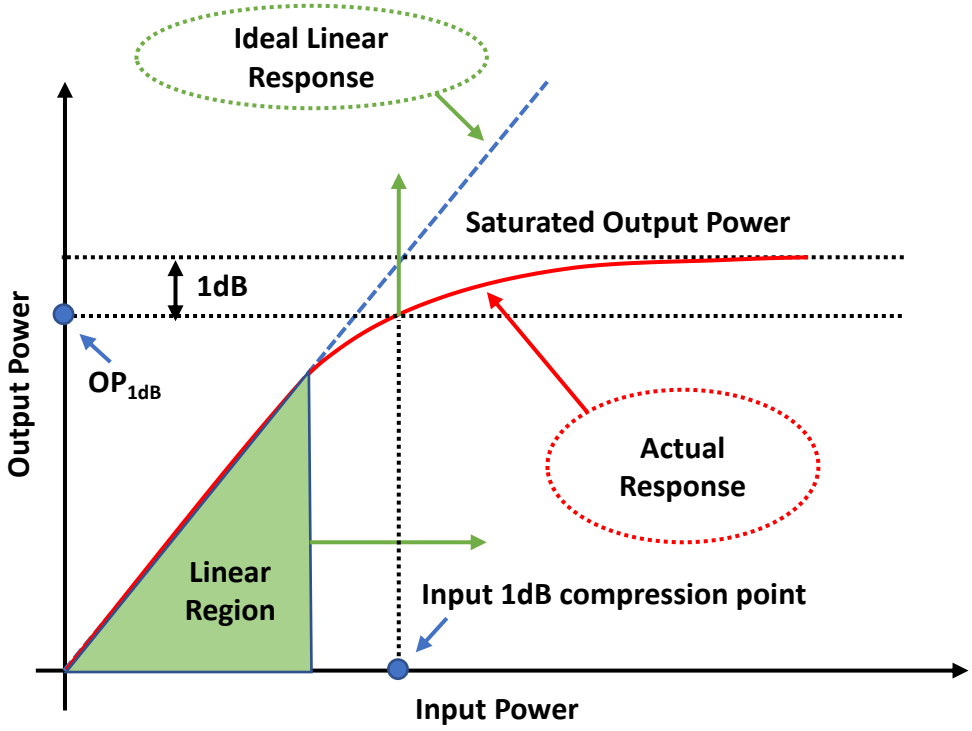


Fig. 2-14. One-dB compression point.

$$S_{out}(t) = h_0 + \sum_{k=1}^{K}\sum_{i_1}^{M} \dots \sum_{i_p=0}^{M} h_p(i_1, i_2, \dots, i_p)\prod_{j=1}^{K} S_{in}(t - i_j) \tag{2.6.4}$$

Where M and K are the memory depth and the non-linearity order of the Volterra model, respectively. It is worth to mention that the constant (h_0) is usually taken to be zero by suitable choice of output level and other non-linear impulse responses $h_p(i_1, i_2, \dots, i_p)$.

2.6.1.2. One-dB Compression Point.

The compression characteristics of the PA refers to the gain reduction occurred in the output response of the practical designed PA due to its non-linear behavior. Thus, the one-dB compression point is the point where the delivered output power has a 1 dB reduction compared with the full linear PA, as demonstrated in Fig. 2-14. The green area, as illustrated in Fig. 2-14, is considered to be the linear region of the practical PA. It is clearly shown that expanding the output 1-dB compression point (OP_{1dB}) would improve the linear behavior of the implemented PA and decrease the resulting distortions on the amplified signal, especially while dealing with high PAPR signals.

2.6.1.3. Third-Order Intercept Point

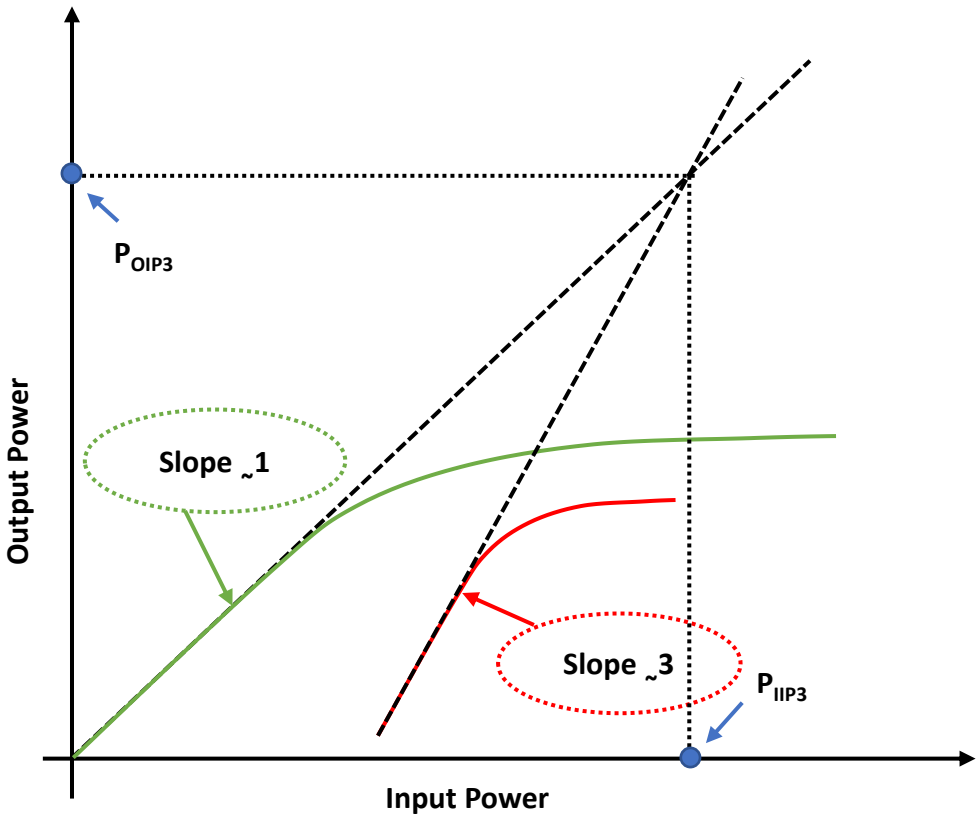


Fig. 2-15. Third-order intercept point.

The resulting intersection point when the first order power product equals to the third order power product is called the third-order intercept point (IP3), as shown in Fig. 2-15. Where increasing the input and output third order intercept points (P_{IIP3} and P_{OIP3}, respectively) reduces the non-linearity of RF PAs. The resulting distortions, caused by this problem, should be wisely considered particularly when dealing with multi-tone input signals.

2.6.1.4. AM-AM and AM-PM Distortions

For any non-linear practical PA, the amplified signal is distorted in terms of its amplitude and phase with changing the power level of the input signal. These deviations in the amplitude of the output signal called amplitude-modulation-to-amplitude-modulation (AM-AM) distortions while the deviations occurred in phase are called amplitude-modulation-to-phase-modulation (AM-PM) distortions.

2.6.1.5. Third and Fifth-Order Intermodulation Distortions

Intermodulation distortions (IMD) are one of the most direct methods to figure out the linear behavior of RF PAs. The IMD orders are determined using generated spurious products comes from the non-linear behavior of the device under test related to the corresponding two-tone input signal. Considering all those resulting several orders would be very complex task. As a result, it is sufficient to use two-tone input signal (S_{in}) with the same signal magnitude (A_m) and small frequency spacing ($\Delta\omega$), as described in (2.6.5) to calculate third and fifth order of the IMD (IMD3 and IMD5, respectively).

$$S_{in} = A_m.\{\cos(\omega + \Delta\omega/2) + \cos(\omega - \Delta\omega/2)\} \tag{2.6.5}$$

2.6.1.6. Error Vector Magnitude Distortions

The value of the error vector magnitude (EVM) distortion is an indication for the errors occurred in both amplitude and phase of the amplified output signal at different amplitudes of the feeding signal (amplitude modulated signal), as illustrated in Fig. 2-16. Where the average EVM distortion is given by the following equation

$$EVM\ (dB) = 20\log_{10}\left(\frac{\sqrt{\frac{1}{N}\sum_{n=0}^{N-1} I_{err}^2[n] + Q_{err}^2[n]}}{NR_{EVM}}\right) \tag{2.6.6}$$

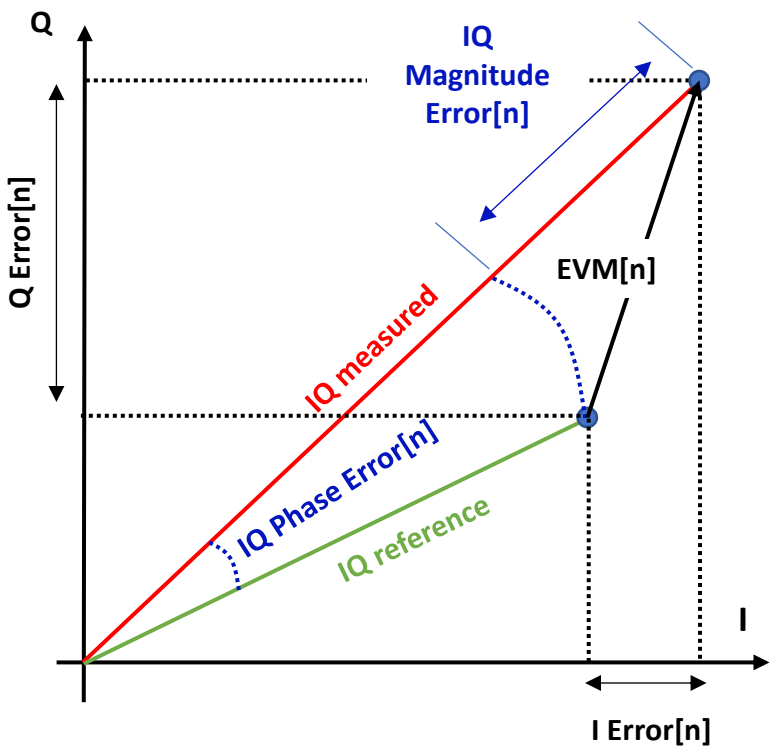


Fig. 2-16. Error Vector Magnitude Distortions.

Where I_{err} and Q_{err} are the errors of the in-phase (I) and the quadrature-phase (Q) signals between the measured signal and the reference one, respectively. N, n, and NR_{EVM} are the number of tested symbols, the symbol index, and the EVM normalization reference, respectively. The EVM measurement is a comprehensive metric that describes the distortions occurred in the amplified signal compared with the AM-PM distortions and the two-tone IMD test, in particular with using a high PAPR and advanced amplitude modulated signals. Consequently, some specifications pose strict constraints for EVM values to guarantee appropriate signal delivery. Where one of EVM's limit values, according to Third Generation Partnership Project (3GPP) standards, equal -15 dB, -18 dB, and -22 dB for 4, 16, and 64 QAM modulated signals, respectively [14].

2.6.2. Common RF Linearization Techniques

Linearization techniques are mainly employed for minimizing the distortions of the amplified output signals for fulfilling a proper signal delivery at the received point and decreasing the possible interference resulted signals at adjacent channels. Therefore, lots of work have been

introduced to enhance the linear behavior of the designed RF PAs. Feedback, feedforward, predistortion techniques are three commonly utilized linearization techniques for RF transceiver designs [15].

2.6.2.1. Feedback Linearization Technique

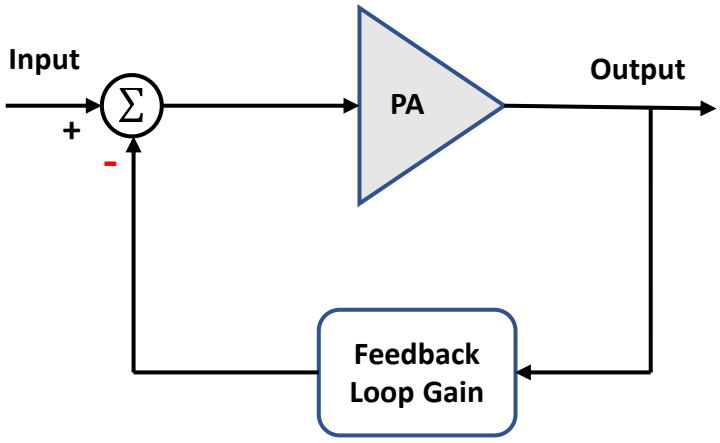


Fig. 2-17. Feedback linearization technique.

A high level of linearization can be provided by applying the feedback topology based on the feedback loop concept, that is usually employed in control systems. Fig. 2-17 shows that a sample of the output RF signal is feedbacked again to be subtracted from the input signal via a feedback loop circuit that offers a certain gain to the feedbacked signal before accomplishing the subtraction process. Many developed versions have been introduced to enhance the performance of the feedbacked linearization technique such as employing envelope, polar, and cartesian feedback improved techniques. Unfortunately, designers should ensure that the proposed feedback loop circuit should offer small signal delays in the subtracted signal to guarantee the stability of the whole system, particularly when dealing with high RF bands. Furthermore, the resulting reduction of the overall gain with utilizing such feedbacked linearization technique and also the difficulty in manufacturing ideal components over wide range of frequencies in particular with engaging cheaper CMOS fabricating technologies. These drawbacks restrict the use of this technique in narrowband applications [16], [17].

2.6.2.2. Feedforward Linearization Technique

In feedforward linearization technique, there are two main loops illustrated in Fig. 2-18. The first loop is existed for cancelling the signal itself and getting only the distorting signal while the other loop is existed for minimizing the distorting signal and getting the output signal amplified with only the linear region (G_0) [18].

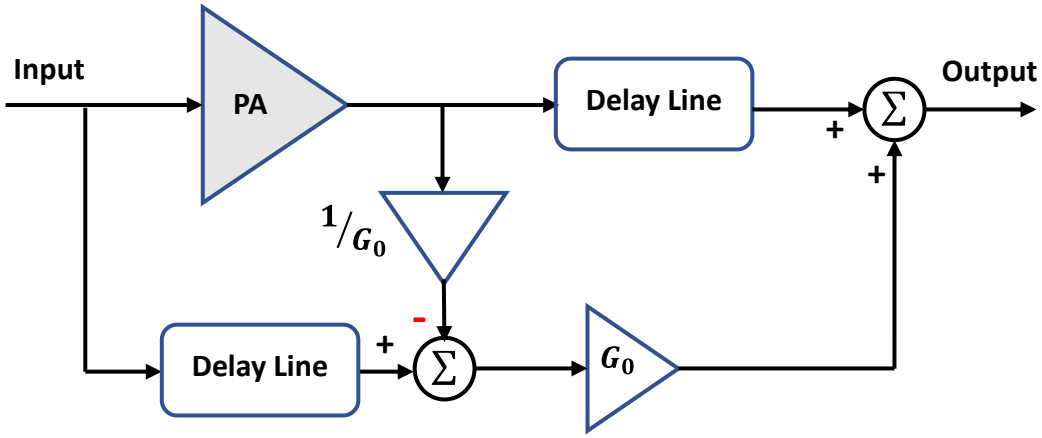


Fig. 2-18. Feedforward linearization technique.

A copy of the output RF signal is amplified by $^1/_{G_0}$ in the first loop. Subsequently this signal is subtracted from the original input signal after estimating the required delays to guarantee the stability of the whole system. The resulting signal is the anti-phased of the resulted distorting signal of the non-linear PA. This anti-phase distorting signal is amplified again, in the second loop, to be added to the output distorted signal after satisfying a proper time aligning. Finally, the output signal should be the amplified signal devoid of any distortions. As described above, Employing the feedforward technique minimizes the distortions coming from the non-linearity of the designed PAs. Thus, this technique is employed widely in RF communication systems that can deals with broadband signals. Unfortunately, the linear gain of the used amplifiers should be precisely matched. Also, this technique suffers from its higher complexity and higher sensitivity to the time alignments in both first and second loops which is similar to the previous feedback linearization technique [15], [19].

2.6.2.3. Pre-distortion Linearization Technique

In the pre-distortion linearization technique, a designed pre-distorter which has a specific non-linear characteristic is added before the implemented PA, as demonstrated in Fig. 2-19(a). For minimizing the non-linearity of the PA, the characteristic of the added pre-distorter has to be in the opposite way to the non-linear compression characteristic of the designed PA, as shown in Fig. 2-19(b) and Fig. 2-19(c). This technique is frequently used in RF transceiver designs. As the pre-distortion linearization technique is considered to be a cost saving and a power efficient technique. It also can deal with wide modulation bandwidth and multi-tone signals [15], [20]–[22].

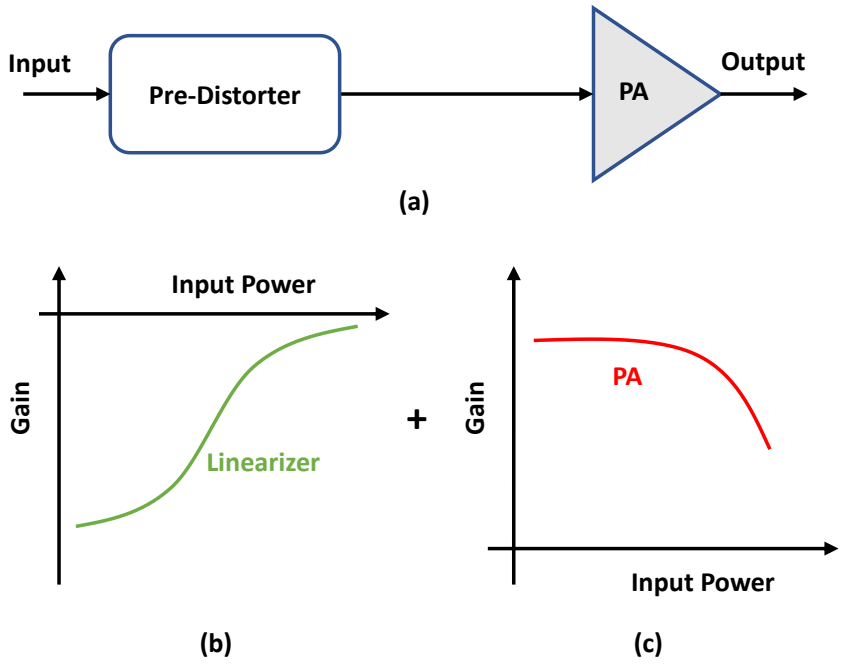


Fig. 2-19. Pre-distortion linearization technique (a) Block diagram (b) Pre-distorter characteristic (c) PA characteristic.

2.7. Conclusion

- This chapter has discussed the fundamental concepts of designing RF PAs and covered different manufacturing technologies in today's market employed in designing high performance PAs.
- This chapter, moreover, has illustrated the need for enhancing the linearity of the designed RF PAs and the commonly used linearization techniques.

CHAPTER 3: DESIGN OF *K*-BAND CMOS WIDEBAND POWER AMPLIFIER

3.1. Introduction and Literature Review

Implementing wideband RF transceivers have been recently growing as a consequence of the significantly dependence of dealing with wider bandwidths and higher data rates in today's wireless communication systems. Among those new wireless trends, satellite communications and automotive radar systems have used *K*-band and *Ku*-band frequencies [23]. RF PAs, in such applications, are one of the main sections that should be wisely implemented.

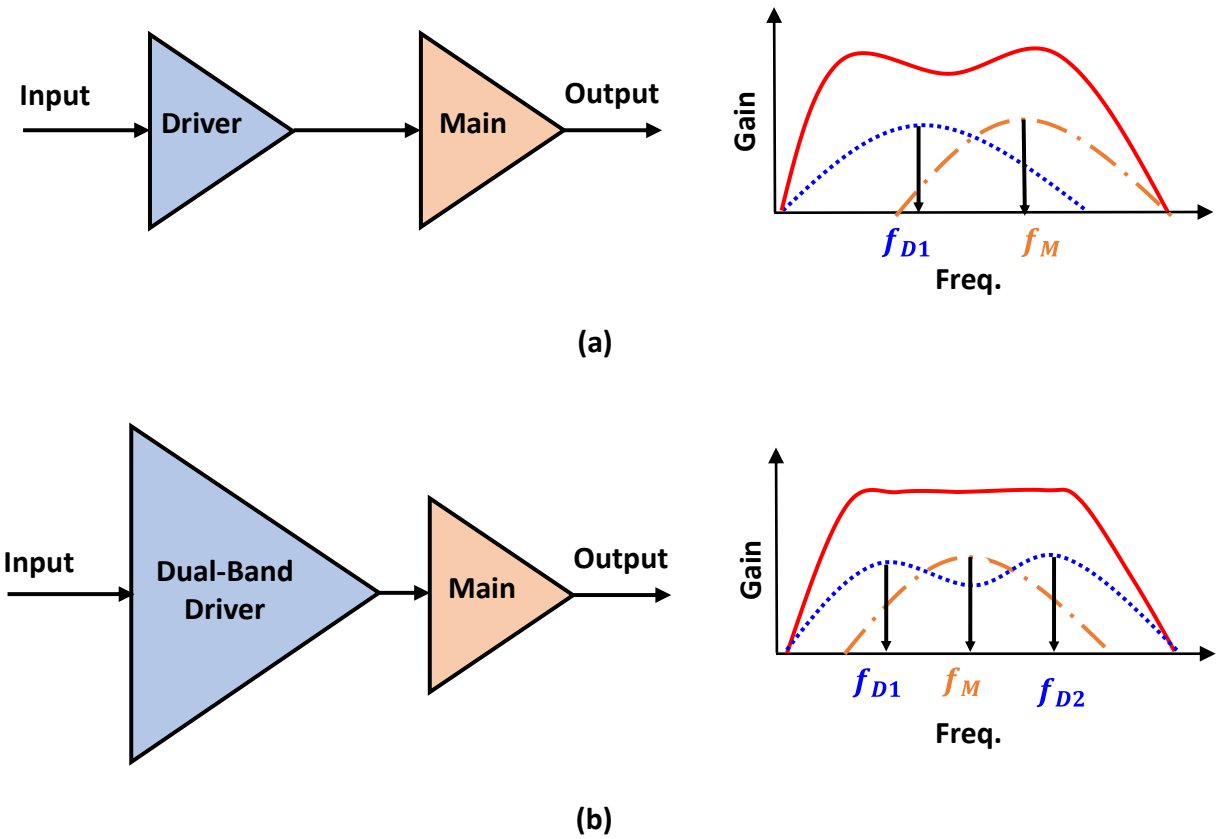


Fig. 3-1. Staggered tunning techniques (a) Conventional (b) Proposed.

Several wideband techniques have been presented in implementing CMOS PAs in *mm*-wave and quasi-*mm*-wave frequency bands [24], [25]. Using distributed RF PAs is a common technique for getting lower return losses and wideband gain characteristics. However, designing their

wideband output matching networks for getting their optimum output power levels is challenging and deteriorates their saturated output power and their realized PAEs due to the associated losses [26]. Moreover, utilizing staggering technique is one of the effective methods used for designing wideband RF PAs [27], [28]. Where this staggered method is presented by designing the driver and main stages at different center frequencies, as shown in Fig. 3-1(a). However, the achieved gain response of these RF PAs usually deteriorates when targeting wider bandwidths that require using a resistive feedback topology at the main stage [29], that will decrease the designed PA's achieved power gain or by designing an interstage impedance transformer with added loss [30]. An alternative approach is introduced by Sapawi et.al. [31] which is to increase the number of cascaded stages, which are positioned at different frequencies, to improve the flatness of the realized gain response. Still, this gain flatness comes at the cost of reduced PAE, increased signal distortions, and variations in group delay (GD) and consumed bigger chip areas.

In this chapter, A two-stage wideband RF PA using a 0.18-µm CMOS technology is presented. This RF PA utilizes a suggested superimposed staggered technique and defected-ground-structure (DGS) inductors to achieve higher PAE and optimal gain flatness across a wide frequency range of 14-22 GHz. The design involves creating a wideband peaking main stage at the center frequency, and then implementing a superimposed dual-band driver stage to achieve the optimal gain flatness over the entire bandwidth, as illustrated in Fig. 3-1(b).

This chapter explains, in section 3.2, the suggested superimposed staggering technique. While in section 3.3, the high Q-factor built-in DGS resonators are introduced and compared with the foundry spiral inductors. The implementation and the measured performance are demonstrated and compared with the other recent published studies, as illustrated in Sections 3.4. Finally, section 3.5 concludes the key points of this chapter.

3.2. Proposed Superimposed Staggering Technique

As mentioned before, the proposed wideband *K*-band CMOS PA is designed using two stages (SDB driver stage and main stage). The driver stage consists of two stacked transistors (STs) and the main stage is presented as a common source (CS) configuration. The number of the used STs and their sizes ought to be selected pursuing for their optimal performances. The use of a stacked configuration in RF PA can usually lead to higher power gain and larger saturated output power (P_{sat}), as well as reduced drain-gate and drain-source swings. However, in practice, the number of

STs used must be carefully selected due to limitations in CMOS technology and its parasitics, phase shift at the intermediate nodes, operating frequency, and load mismatch analysis [32]. To determine the optimal number of STs for the proposed CMOS PA, amplifiers using one, two, three, and four 160/0.18 µm STs were designed and compared in terms of performance, as shown in Fig. 3-2.

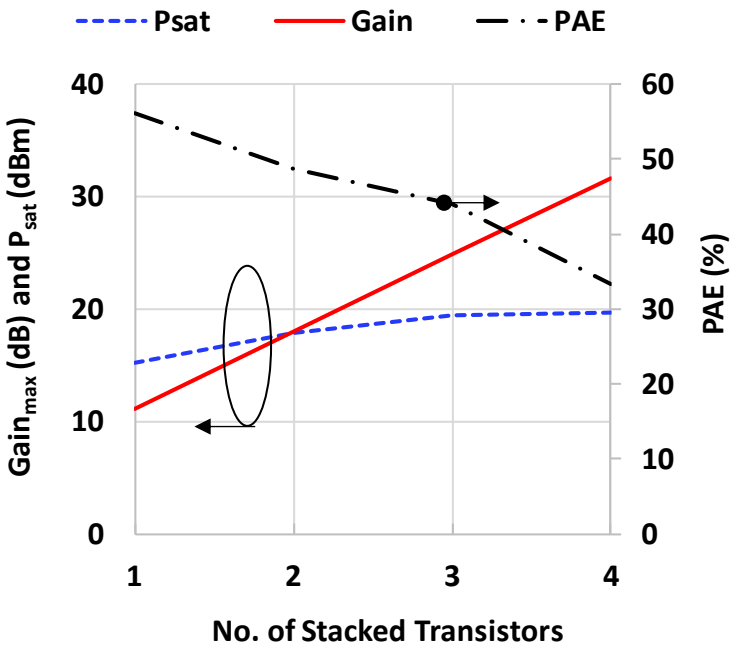


Fig. 3-2. Trade-offs occur in the performance of stacked configurations due to changing the number of the used stacked transistors. The results are accomplished using equal transistor sizes (160/0.18µm) and same frequency of operation (18 GHz) to make a fair comparison.

Increasing the number of stacked transistors will undoubtedly increase the maximum attainable gain from each single stage. However, increasing the used number of stacked transistors, as illustrated in Fig. 3-2, reduces the maximum attainable PAE due to the increased dc power consumption. Also, increasing the number of the used stacked transistors at higher frequencies suffers from stability issues and phase shifts at the intermediate nodes that should be strictly considered. Thus, authors thought that using wider CS transistor configuration (570/0.18µm) for the main stage would increase the PAE of the designed CMOS PA, while raising its gain by using two-stacked transistor configuration in designing the driver stage (160/0.18µm). This topology (2-cascaded transistor driver stage and CS main stage) is also employed to enhance the PAE of the designed RF PAs in particular with using the same technology node [30]. Designing a two-stage

wideband PA with an extended BW technique maintaining a suitable power gain flatness instead of increasing the number of employed cascaded stages would improve the performance of the implemented CMOS PA and reduce the resulting signal distortions. As a consequence of the main stage of the RF PA deals with higher power levels, the designed CS wideband main stage of the PA is designed to peak at the center frequency where its 3-dB bandwidth (BW_{3dB}) covers the BW of interest in spite of its realized gain flatness. Afterwards, the introduced driver stage is designed to have a dual-band characteristics at the frequency edges of the BW (f_{D1} and f_{D2}), as shown in Fig. 3-1(b).

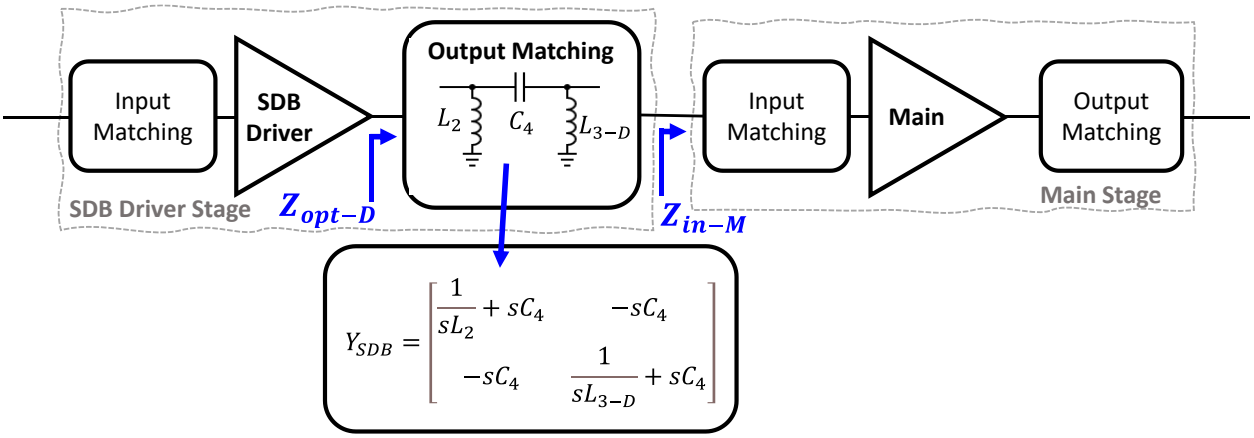


Fig. 3-3. Converting the π output network of the SDB driver stage to its equivalent Y-parameters.

Where, its input network is designed to convert the optimum source impedance of the driver stage at f_{D1} to the 50 Ω source impedance. While the output matching circuit of the driver stage is designed to convert the optimum load impedance of the driver stage at f_{D2}, extracted from the load-pull simulation to the input impedance of the main stage. The elements of the output matching circuit of the driver stage ought to be designed to introduce an appropriate trajectory of the main stage's input impedance (Z_{in-M}) and the optimum load impedance of the driver stage (Z_{opt-D}) to guarantee a good gain flatness, as illustrated in Fig. 3-3 and the following equations:

Calculating the Y-parameters of the output matching circuit of the SDB driver stage (Y_{SDB}):

$$Y_{SDB} = \begin{bmatrix} \frac{1}{sL_2} + sC_4 & -sC_4 \\ -sC_4 & \frac{1}{sL_{3-D}} + sC_4 \end{bmatrix} \quad (3.2.1)$$

$$|Y_{SDB}| = \left(\frac{1}{sL_2} + sC_4\right)\left(\frac{1}{sL_{3-D}} + sC_4\right) - sC_4 * sC_4 \tag{3.2.2}$$

$$B = |Y_{SDB}| = C_4(A^{-1} + L_2^{-1} + L_{3-D}^{-1})$$
$$\text{A}=s^2L_2L_{3-D}C_4 \tag{3.2.3}$$

Calculating the Z-parameters of the output matching circuit of the SDB driver stage (Z_{SDB}) from its equivalent Y parameters:

$$Z_{SDB} = \frac{1}{B}\begin{bmatrix} \frac{1}{sL_{3-D}} + sC_4 & sC_4 \\ sC_4 & \frac{1}{sL_2} + sC_4 \end{bmatrix} \tag{3.2.4}$$

$$Z_{SDB} = \frac{1}{BsL_2L_{3-D}}\begin{bmatrix} L_2 + s^2L_2L_{3-D}C_4 & s^2L_2L_{3-D}C_4 \\ s^2L_2L_{3-D}C_4 & L_{3-D} + s^2L_2L_{3-D}C_4 \end{bmatrix} \tag{3.2.5}$$

$$Z_{SDB} = \frac{1}{BsL_2L_{3-D}}\begin{bmatrix} L_2 + A & A \\ A & L_{3-D} + A \end{bmatrix}$$
$$\text{A}=s^2L_2L_{3-D}C_4 \tag{3.2.6}$$

Determining the equivalent input impedance from the Z-parameters of the π-output network of the SDB driver stage:

$$Z_{out} = Z_{22} - \frac{Z_{12}Z_{21}}{Z_{11} + Z_S} \tag{3.2.7}$$

$$Z_{out} = \frac{1}{C_4(A^{-1}+L_2^{-1}+L_{3-D}^{-1})\,SL_2L_{3-D}}\{(L_{3-D} + A) - \frac{A*A}{L_2+A+Z_S}\} \tag{3.2.8}$$

$$Z_{out} = \frac{S}{1+S^2C_4L_{3-D}+S^2C_4L_2}\{(L_{3-D} + A) - \frac{A^2}{L_2+A+Z_S}\} \tag{3.2.9}$$

$$Z_{out} = \frac{S\left(L_{3-D} + A\left(1 - \frac{A}{L_2 + A + Z_S}\right)\right)}{1 + S^2C_4L_{3-D} + S^2C_4L_2}$$
$$\text{A}=s^2L_2L_{3-D}C_4 \tag{3.2.10}$$

$$Z_{in-M}^{*} = \frac{S\left(L_{3-D} + A\left(1 - \frac{A}{L_2 + A + Z_{opt-D}^{*}}\right)\right)}{1 + S^2 C_4 L_{3-D} + S^2 C_4 L_2} \qquad (3.2.11)$$

$$A = s^2 L_2 L_{3-D} C_4$$

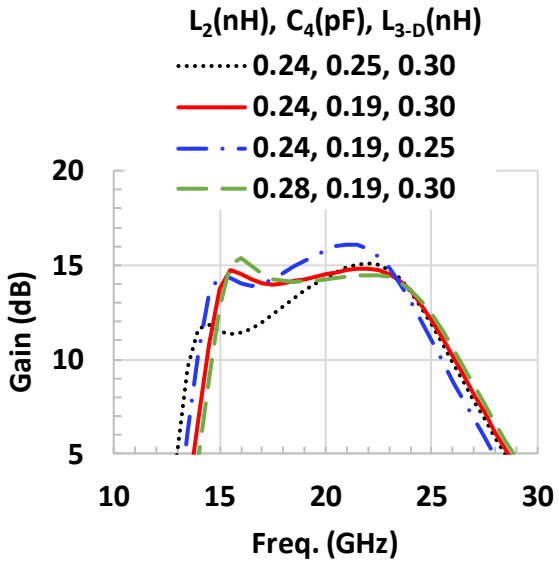


Fig. 3-4. Simulation results that illustrate the effect of changing the values of L_2, C_4, and L_{3-D} on the gain flatness of the designed two-stage PA.

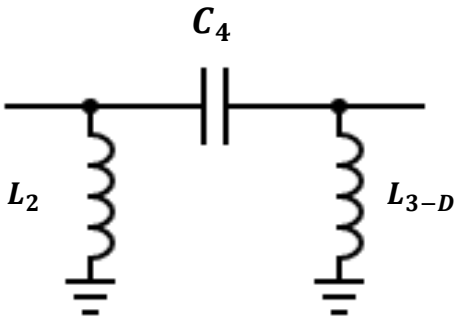


Fig. 3-5. Driver stage's output matching circuit.

Due to the accompanying parasitics at RF frequency bands, these elements of the driver stage's output network should be optimized, as illustrated in Fig. 3-4, to fulfill the optimal matching criteria and perfect power gain flatness. Thus, the final values of L_2, C_4, and L_{3-D} are 0.24 nH, 0.19 pF, and 0.3 nH, respectively. Also, the output impedance of the driver stage is intentionally designed as a π-network, as clarified in Fig. 3-5, where L_2 is connected to the dc power supply (V_{DD1}).

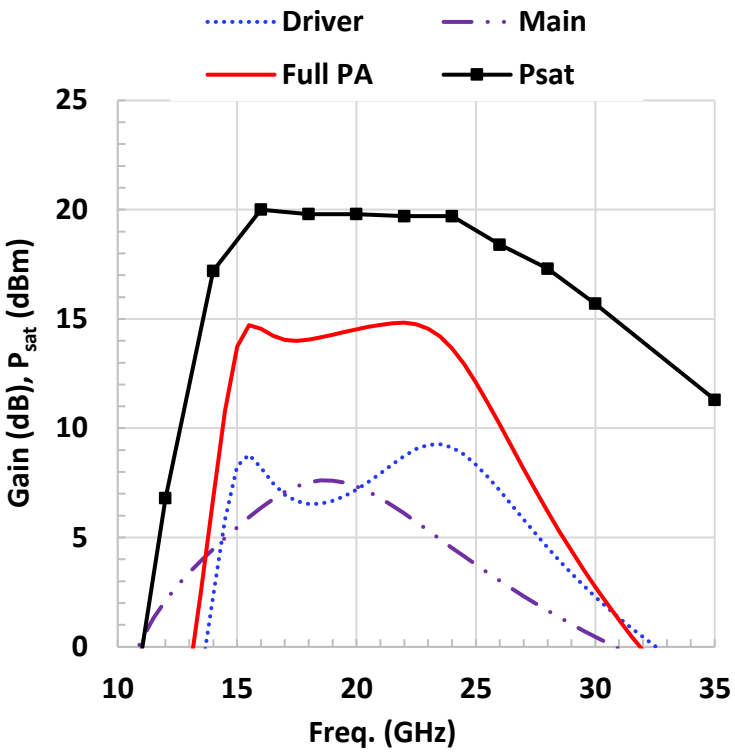


Fig. 3-6. Driver stage, main stage, and overall simulated gain responses of the designed staggered PA's as well as the resulting P_{sat}.

Finally, the simulation results for the designed CMOS wideband PA, including the performance of the SDB driver stage and the peaking main stage, are illustrated in Fig. 3-6. Additionally, it can be seen that the PA maintains an approximately consistent P_{sat} across the entire desired bandwidth.

3.3. Defected Ground Structure Resonators

It is common to say that the delivered output power and the PAE of the designed RF PAs are limited substantially by the insertion losses of the utilized matching networks especially by the output matching circuits.

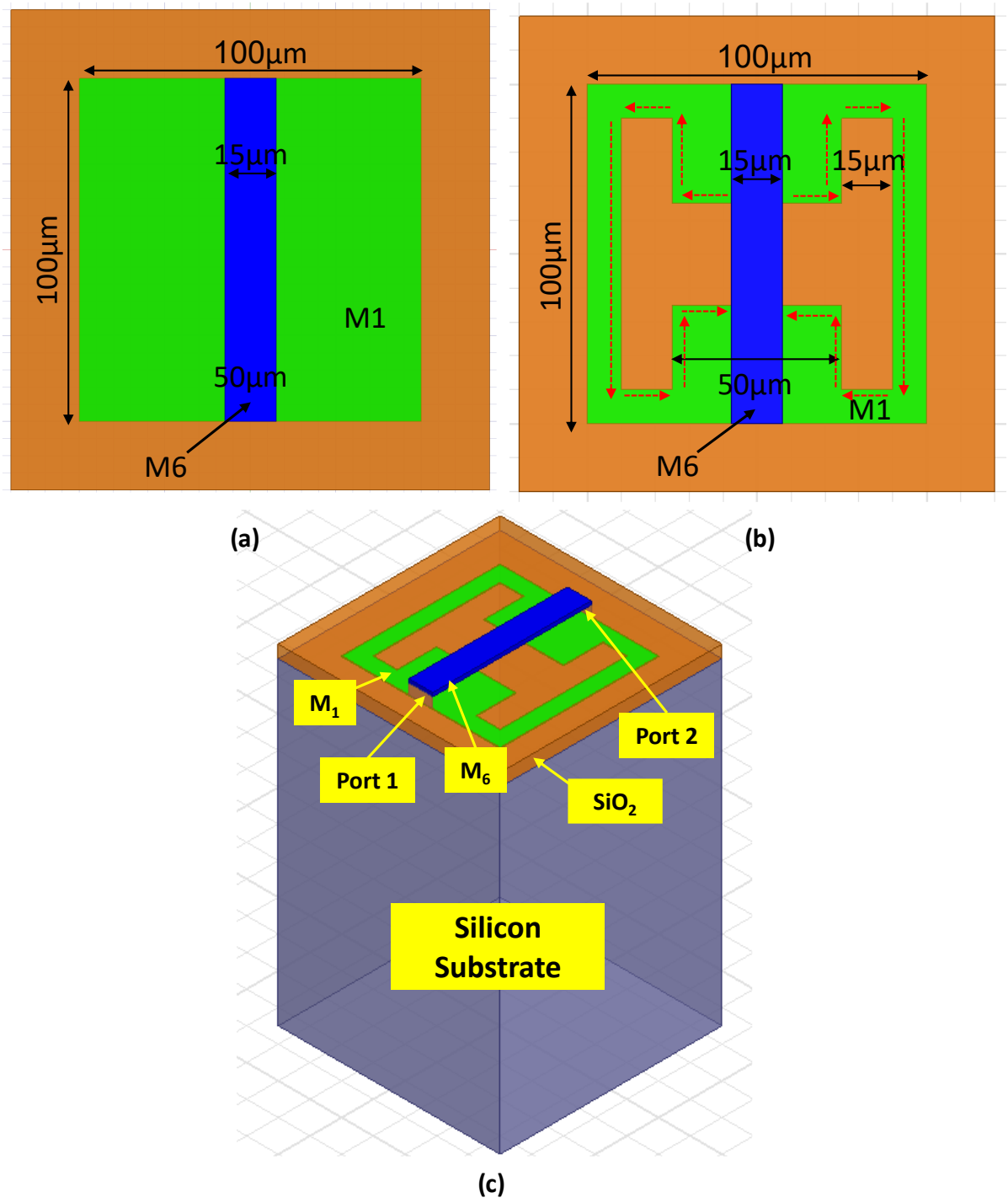


Fig. 3-7. Comparison between the MSL and DGS topology (a) MSL (b) DGS resonator (c) Three-dimension view of the DGS resonator.

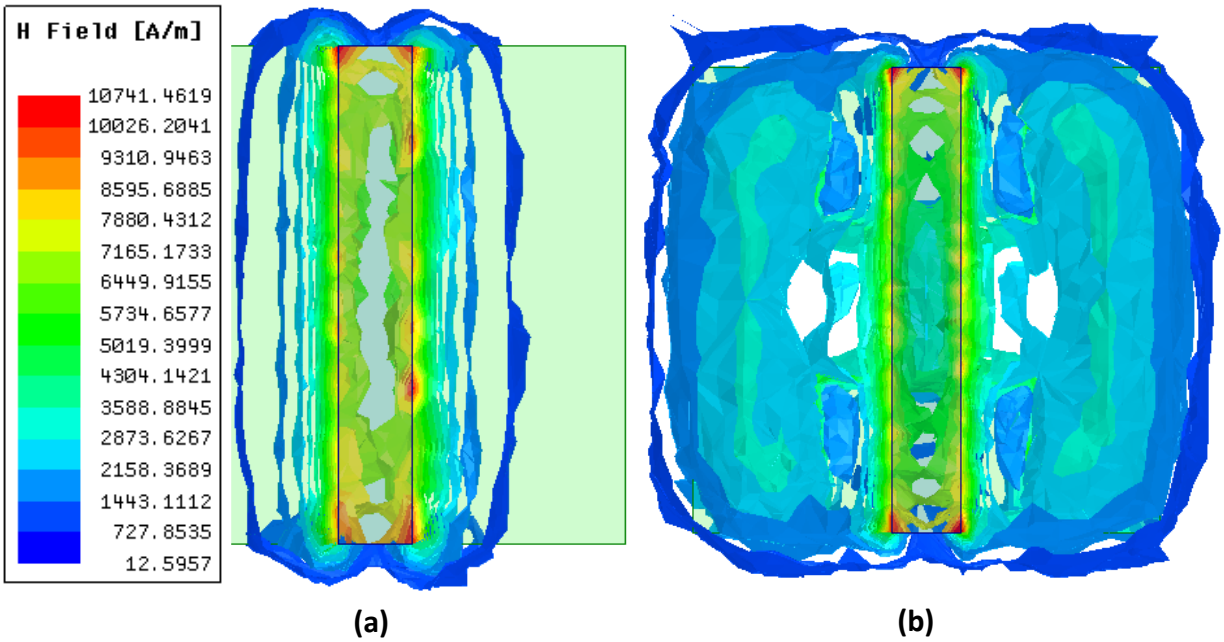


Fig. 3-8. H-field distribution of (a) MSL (b) DGS topology.

Many techniques were proposed to increase Q-factors of the on-chip spiral inductors to diminish the insertion losses of the used matching networks [33], [34]. However, these methods require additional post-processing steps, which raise the fabrication cost. In this work, DGS resonators are employed as a low-cost and high-quality alternative to these expensive methods. The DGS topology is a developed topology from the on-chip microstrip line (MSL) where its ground plane is etched to form a resonator with lower loss, as shown in Fig. 3-7(a) and Fig. 3-7(b). The three-dimension view of the DGS topology is illustrated in Fig. 3-7(c). In the DGS topology, the MSL is used to activate the etched ground plane, which breaks up the fields and creates a DGS resonator with a specific frequency notch, as shown in Fig. 3-8. The magnetic field distribution (H-field) is extended to cover higher area which in turn leads to increase the achieved inductance value and the overall Q-factor specifically at lower frequency bands, as demonstrated in Fig. 3-9. Unluckily, the self-resonant frequency is decreased compared with the original MSL. This implemented DGS resonator can be utilized as a high Q-factor virtual inductor far below this notch frequency. Such DGS inductors have commonly been employed to design voltage-controlled oscillators with lower phase noise characteristics [35], [36].

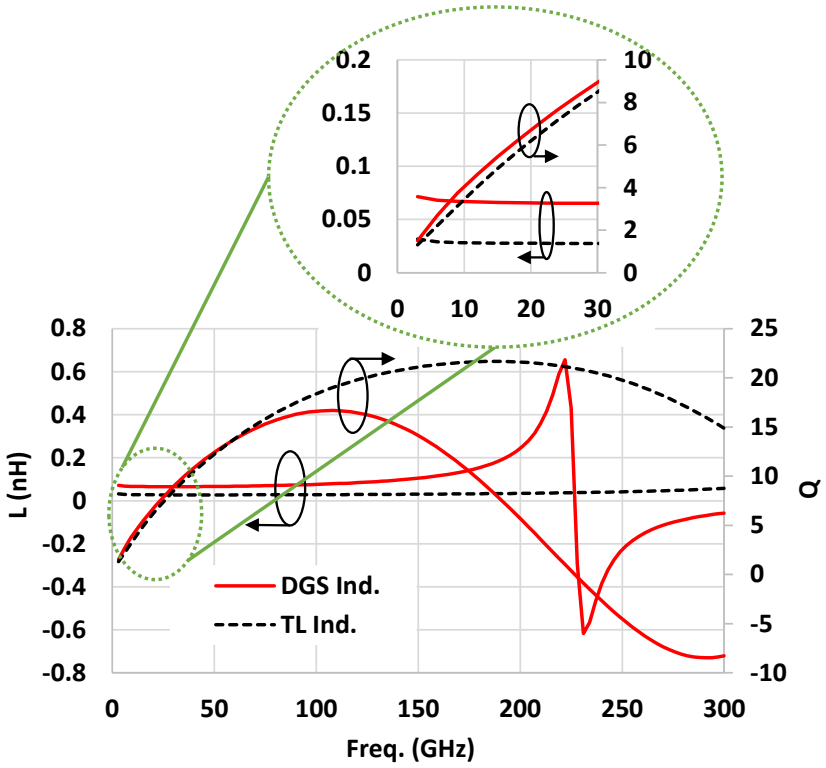


Fig. 3-9. Simulated inductance and unloaded Q-factor of both MSL inductance and DGS resonator.

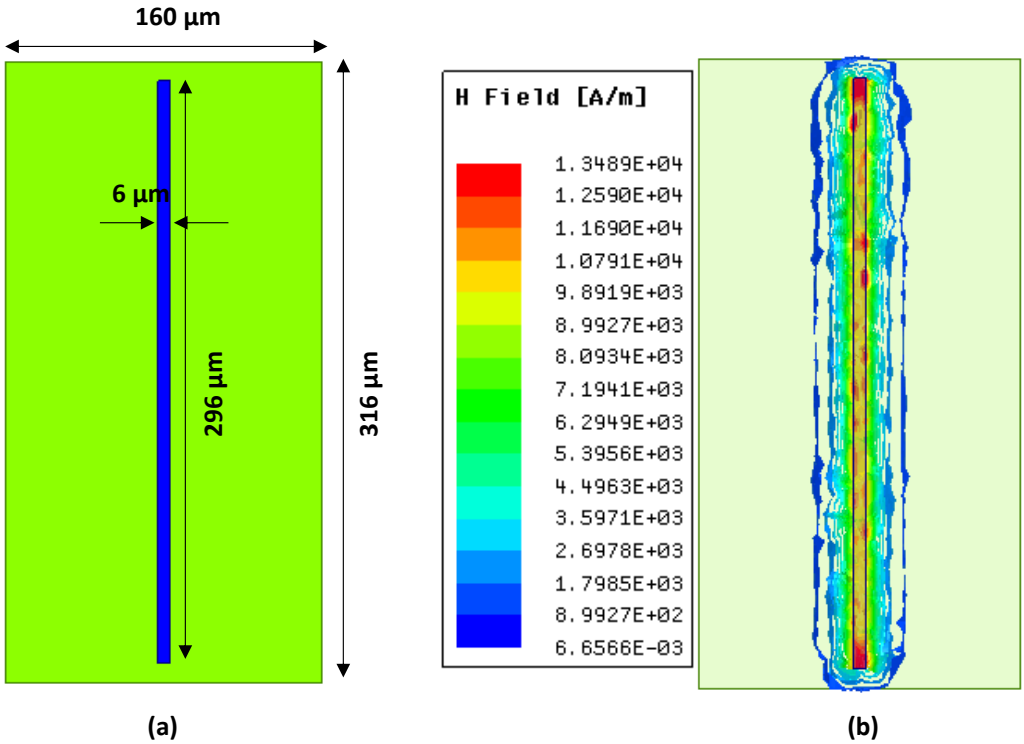


Fig. 3-10. Higher MSL inductance value (a) Two-dimension view (b) H-field distribution.

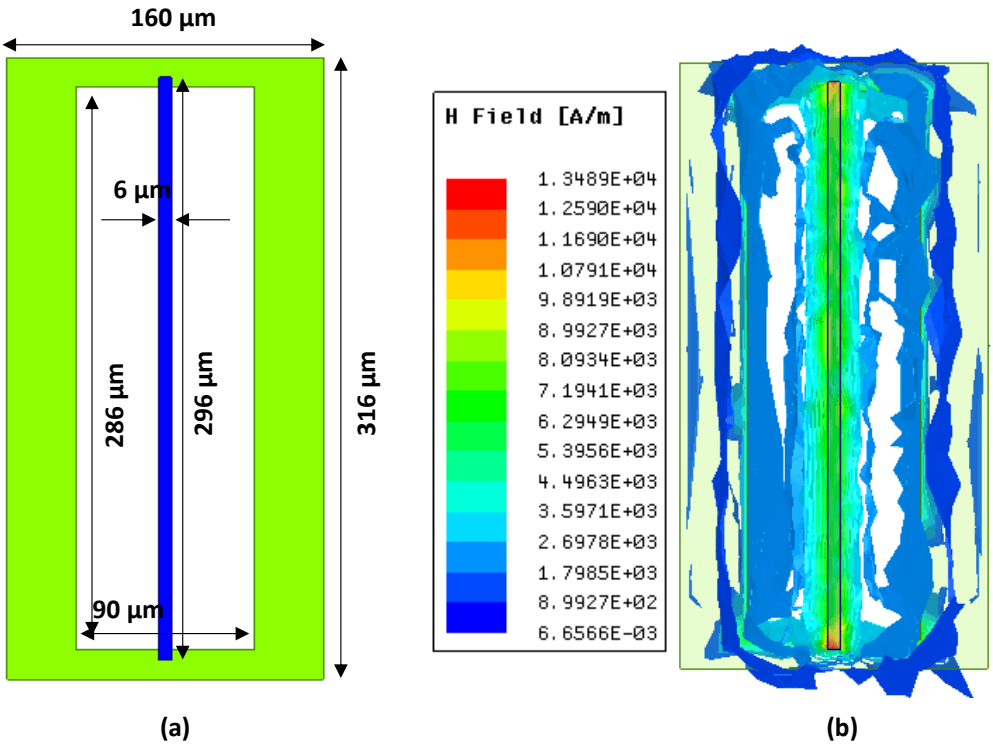


Fig. 3-11. Higher DGS inductor used in the implemented wideband CMOS PA (a) Two-dimension view (b) H-field distribution.

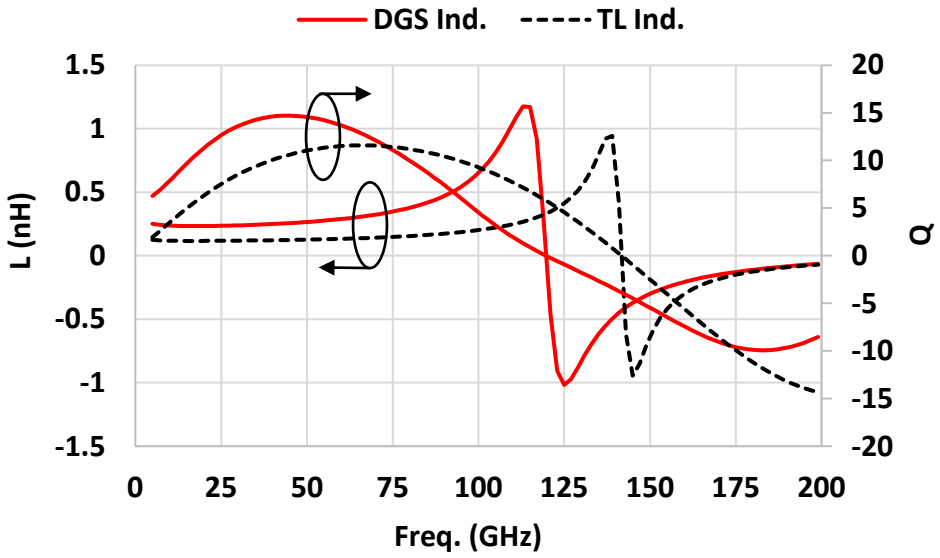
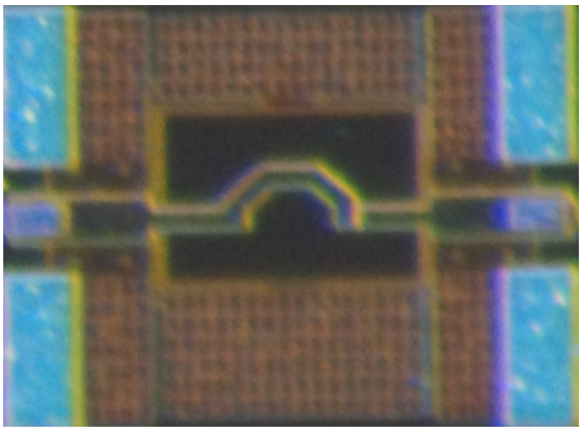


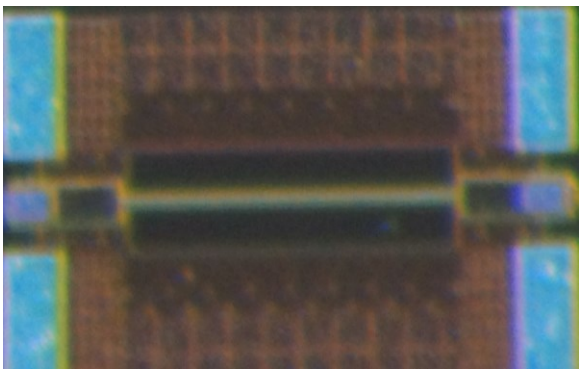
Fig. 3-12. Simulated inductance and unloaded Q-factor of higher inductances of both MSL inductance and DGS resonator.

The realized improvement in the Q-factors of the DGS inductors at lower frequencies compared with the ordinary MSL inductors will be augmented with implementing higher

inductance values, as illustrated in Fig. 3-10, Fig. 3-11, and Fig. 3-12. Where the achieved Q-factor of the DGS inductor is higher than the realized Q-factor of the ordinary MSL inductor at frequency bands lower than around 75 GHz which is more than enough to design our *K*-band wideband staggered CMOS PA. To the best of authors knowledge, this DGS technique has not been applied for fully fabricating a linear-mode CMOS PA. Therefore, DGS resonators have been utilized in implementing the designed wideband RF PA to get the optimum matching criteria and reducing the losses of the used matching networks compared with employing the foundry on-chip spiral inductors. Where utilizing the DGS topology, rather than using foundry spiral inductors, reduces the discontinuities in the current pass that achieve a uniform H-filed distribution. This uniformity decreases the resulting noise over the adjacent elements and diminishes the associated losses which enhances the unloaded Q-factors of the DGS inductors compared with the spiral counterparts.



(a)



(b)

Fig. 3-13. Chip photograph of the fabricated (a) foundry inductor (b) DGS resonator.

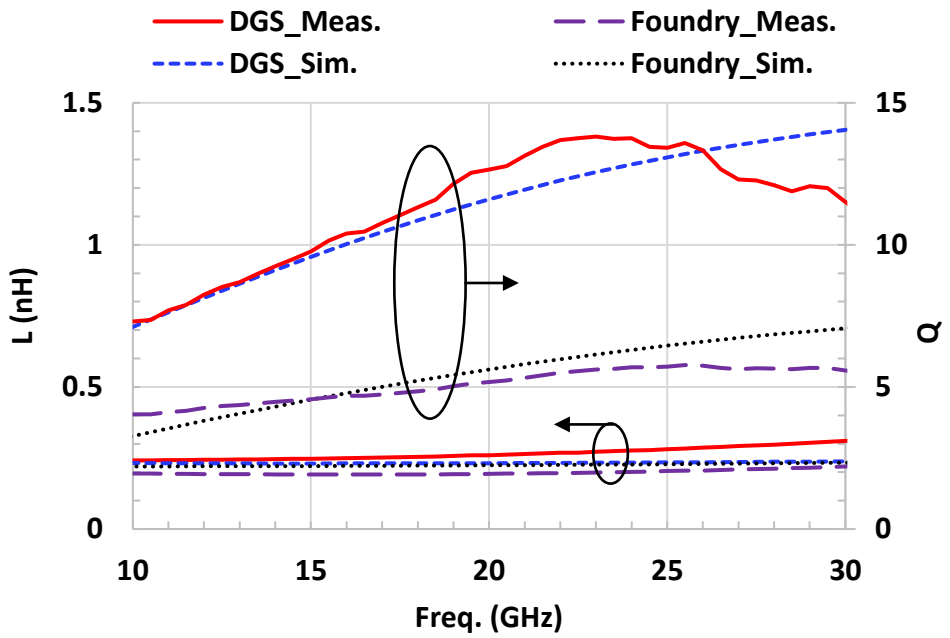


Fig. 3-14. Simulated and Measured inductance and unloaded Q-factor of both DGS resonator and foundry inductor. The measurements of inductors have been performed using Keysight's Vector Network Analyzer (PNA-E8361C).

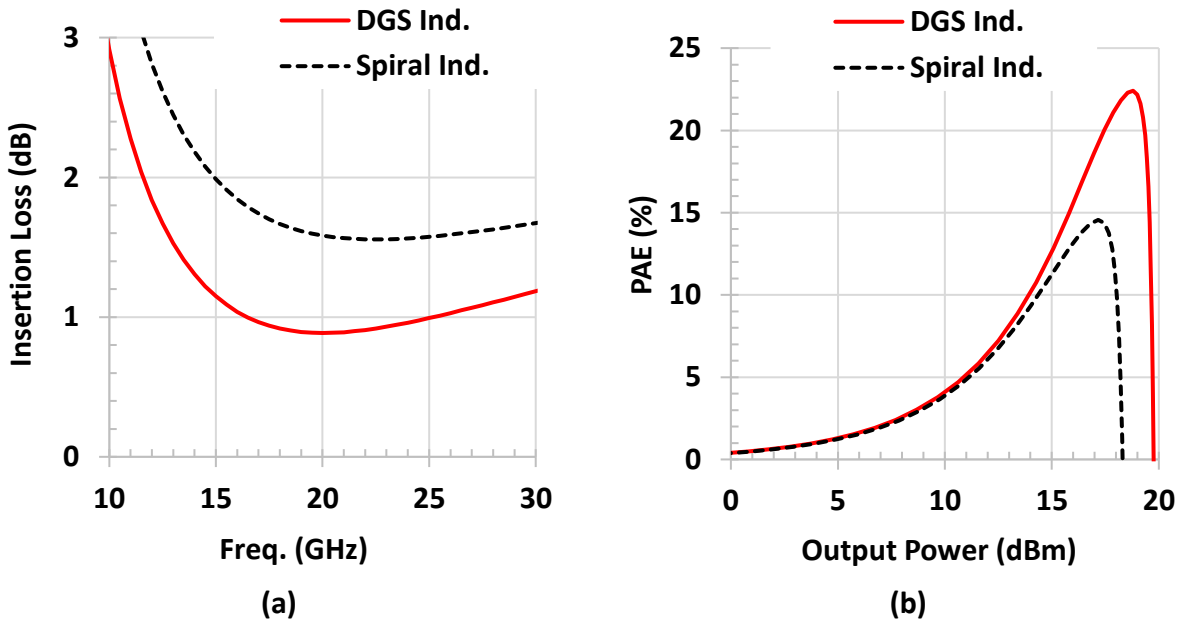


Fig. 3-15. Comparison between the simulated results for using DGS inductors versus spiral foundry inductors of the resulting (a) Insertion loss of the PA's utilized output matching circuit (b) PAE of the designed CMOS PA at the center frequency.

To investigate the realized enhancement in the simulated performance of the DGS inductors in realistic world, a DGS inductor used in designing the wideband CMOS PA is separately fabricated

to be compared with another spiral inductor provided by the foundry of approximately equal inductance, as demonstrated in Fig. 3-13. However, the fabricated DGS resonator requires relatively larger chip area (0.051 mm^2) for the same approximately similar inductance value level compared with the foundry inductor (0.036 mm^2) in this design. The measured performance of the deigned on-chip DGS resonator, after performing the de-embedding process, has achieved higher Q-factors compared with the spiral foundry inductor, as shown Fig. 3-14. Hence, the insertion losses of the utilized matching networks can be diminished by employing such DGS inductors. Fig. 3-15(a) illustrates that the PA's output network employing DGS inductors has realized lower insertion losses over the whole BW compared with using the foundry spiral inductors. Consequently, the reduction of the accumulated insertion loss of all utilized matching networks owing to employing DGS inductors will improve the simulated PAE of the CMOS PA, as demonstrated in Fig. 3-15(b).

3.4. Implementation and Results

3.4.1. Fabrication and Measurement Setup

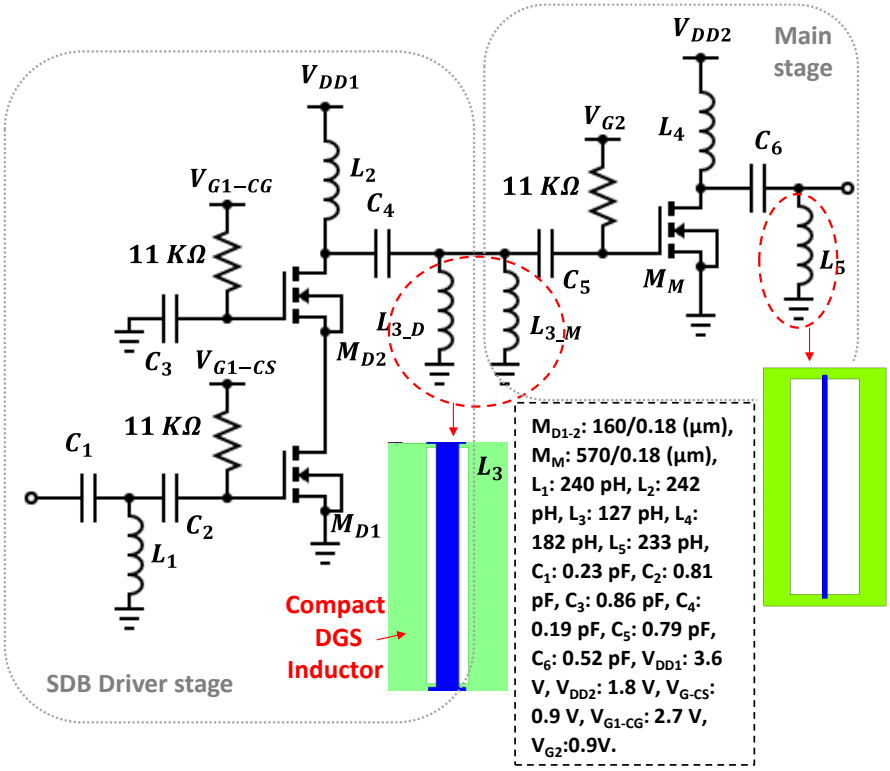


Fig. 3-16. Schematic view of the proposed two-sage wideband PA.

The proposed *K*-band wideband CMOS PA with employing the DGS topology and the proposed superimposed staggering technique was manufactured using 0.18-µm CMOS technology, as illustrated in Fig. 3-16. The PA has a SDB driver stage that consists of a 2-ST configuration connected to supply voltage equals 3.6 V while a CS transistor with a dc supply voltage of 1.8 V represents the main stage. Where Fig. 3-16 illustrates that the parallel combination of L_{3_D} and L_{3_M} can be fabricated using a single compact DGS inductor (L_3) to reduce the subsequent mutual effects and enhance the chip area utilization.

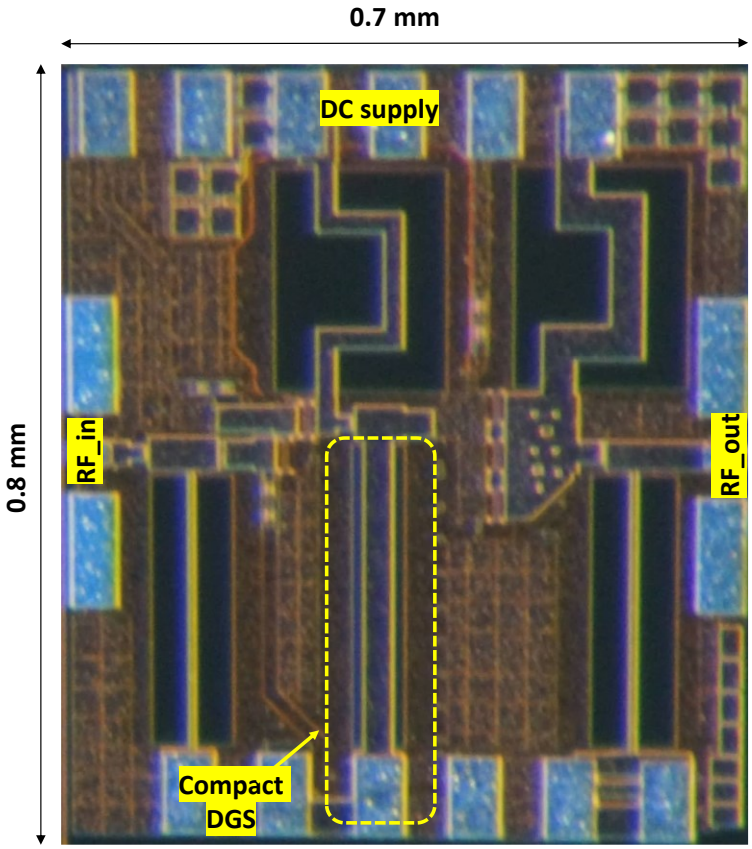


Fig. 3-17. Chip photograph of the designed Wideband PA.

The chip, as shown in Fig. 3-17, consumes around 0.564 mm^2 with the pads, that is measured on a probe station (CASCADE MICROTECH Summit 11000 M) and using *mm*-wave ground-signal-ground infinity probes connected with N5222A Keysight PNA vector network analyzer. For additional characterizing the implemented wideband CMOS PA for proper utilization in recent wireless communication systems, a high PAPR fifth generation-new radio (5G-NR) Downlink baseband signal is produced by a Keysight M9505A arbitrary waveform generator and a raised-cosine shaped filter with 0.35 roll-off factor. The baseband modulated signal is upconverted to

different frequencies in the BW of interest using E8267D Keysight PSG vector signal generator and applied to the input port of the CMOS PA. The output of the manufactured PA is connected to a N9030B Keysight PXA signal analyzer equipped with 89600 VSA software and necessary RF applications including EVM optimization tools, which are used to analyze and measure the amplified 5G-NR modulated signal.

3.4.2. S-Parameters and Power Measurement Results

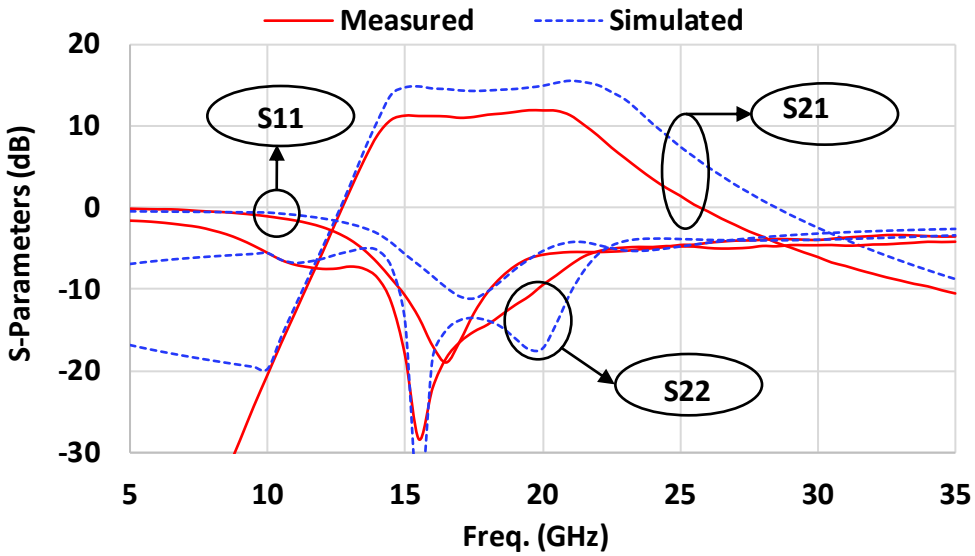


Fig. 3-18. Measured and Post-layout simulated S-Parameters of the implemented wideband CMOS PA.

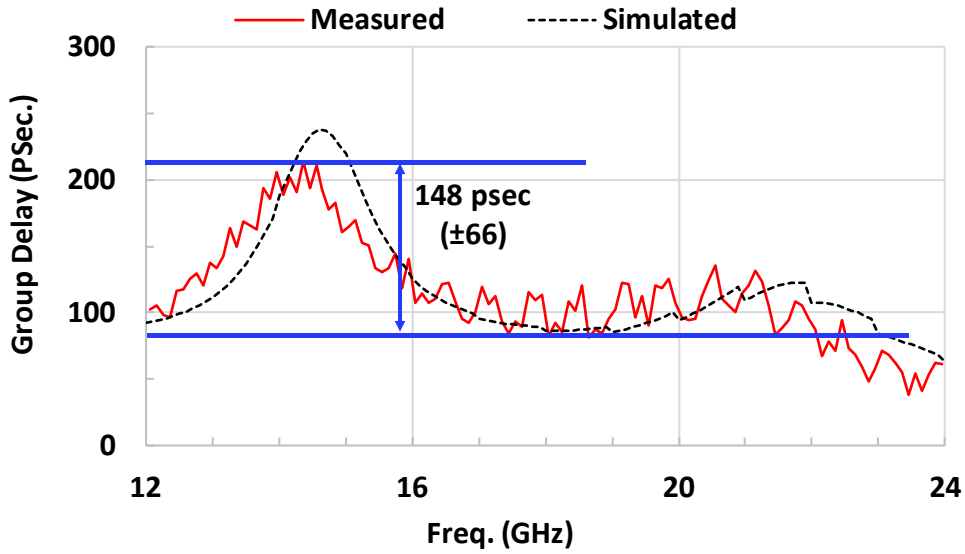


Fig. 3-19. Measured and Post-layout simulated GD variations of the designed wideband PA.

The measured S-parameters are shown in Fig. 3-18 where the maximum power gain of 12 dB was realized at 20 GHz. Also, the implemented CMOS PA has a measured 44.4% FBW (14-22 GHz) which is among the highest reported FBWs, as described in Table 3-1.

Table 3-1. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART WIDEBAND POWER AMPLIFIERS

Ref.	CMOS Tech. (nm)	FBW / BW_{3dB} (GHz)	Gain (dB)	Freq. (GHz)	P_{sat} (dBm)	OP_{1dB} (dBm)	Peak PAE (%)	GD (psec.)	EVM (dB) for 64-QAM, BW, P_{out}	Area (mm^2)
This Work	**180**	**(44.4 %) / (14-22)**	**12.0**	**18**	**16.6**	**12.3**	**18.7**	**148 (±66)**	**-25, 400 MHz/s, 9.3 dBm**	**0.564**
[37]		(18.2 %) / (20-24)	16.3	22	16.8	14.3	10.7	NR	NR	0.35
[38]		(58.8 %) / (18-33)	15.2	26	19.5	16	10.2	NR	NR	0.86
[39]	65	(33.8%) / (13.5-19)	20.6	15.5	13.9	11.6	20	167 **(±85)**	NR	0.62
[40]	28	(13.2 %) / (27.4-31.2)	15.7	30	14	13.2	35.5	NR	-25, 250 MHz/s, 4.2 dBm	0.16 (Active)
[41]		(31.7 %) / (21.8-30)	21.2	24	19.7	18.2	34.5	NR	-25, 200 MHz/s, 9.8 dBm	0.82

Fig. 3-19 shows the GD variations over the whole BW_{3dB}. Where the implemented wideband PA based on the proposed staggered dual-band configuration gives small GD variations of 148 (±66) psec. The large-signal continuous wave measurements in terms of gain and PAE related to the output power of the designed CMOS PA is presented in Fig. 3-20 for only 16, 18, and 20 GHz. While Fig. 3-21 shows the summary of full large-signal CW results of the designed PA over the whole BW_{3dB}. The PA gives, at the center frequency, a P_{sat} of 16.6 dBm, and an OP_{1dB} of 12.3 dBm. Where employing the proposed staggered technique, depending on selecting different optimum source and load impedances over the BW of interest, has contributed to flattening the maximum measured PAE over almost the BW of interest, as described in Fig. 3-21.

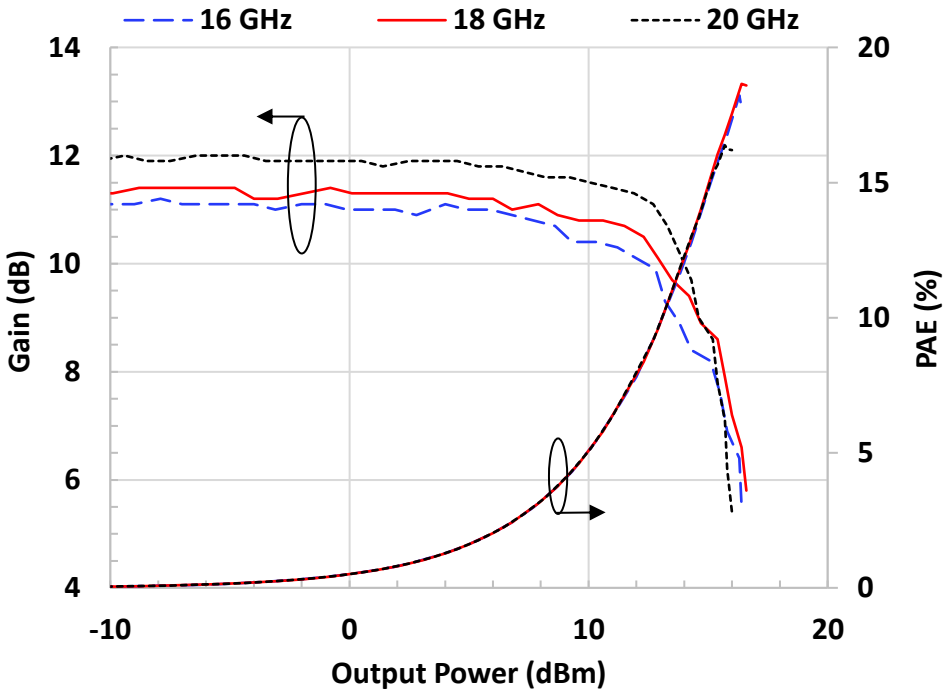


Fig. 3-20. Measured overall Gain and PAE of the wideband PA versus output power levels.

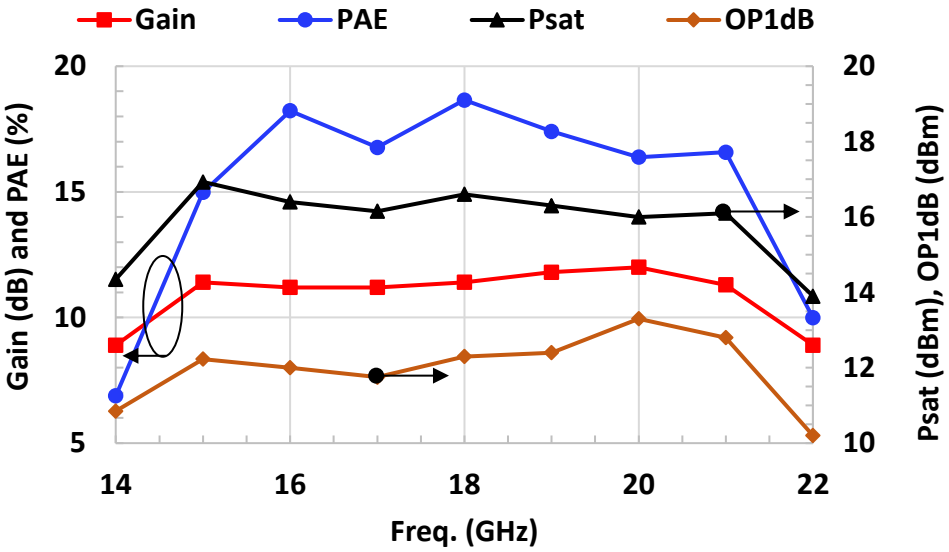


Fig. 3-21. Variations of measured gain, PAE, P_{sat}, and OP1dB over the BW of interest.

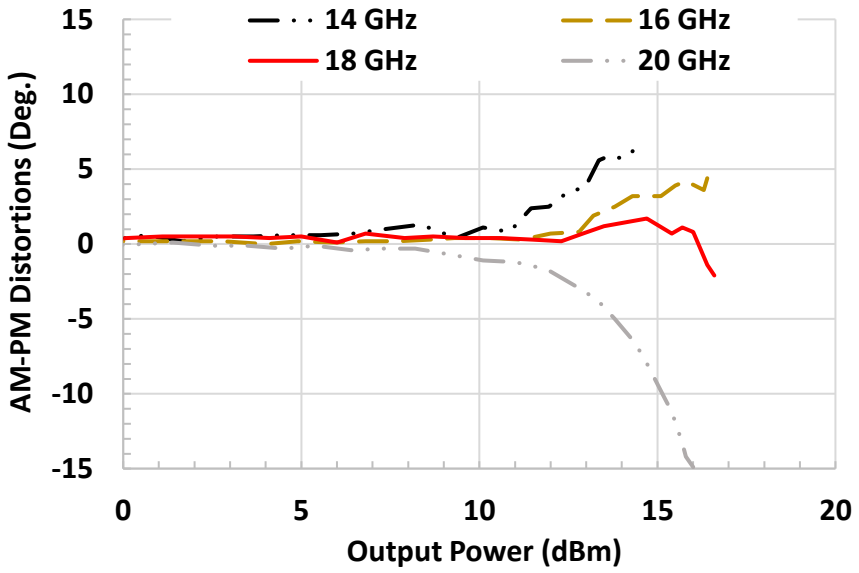


Fig. 3-22. Variations of AM-PM distortions related to the changes of both operating frequency and output power levels.

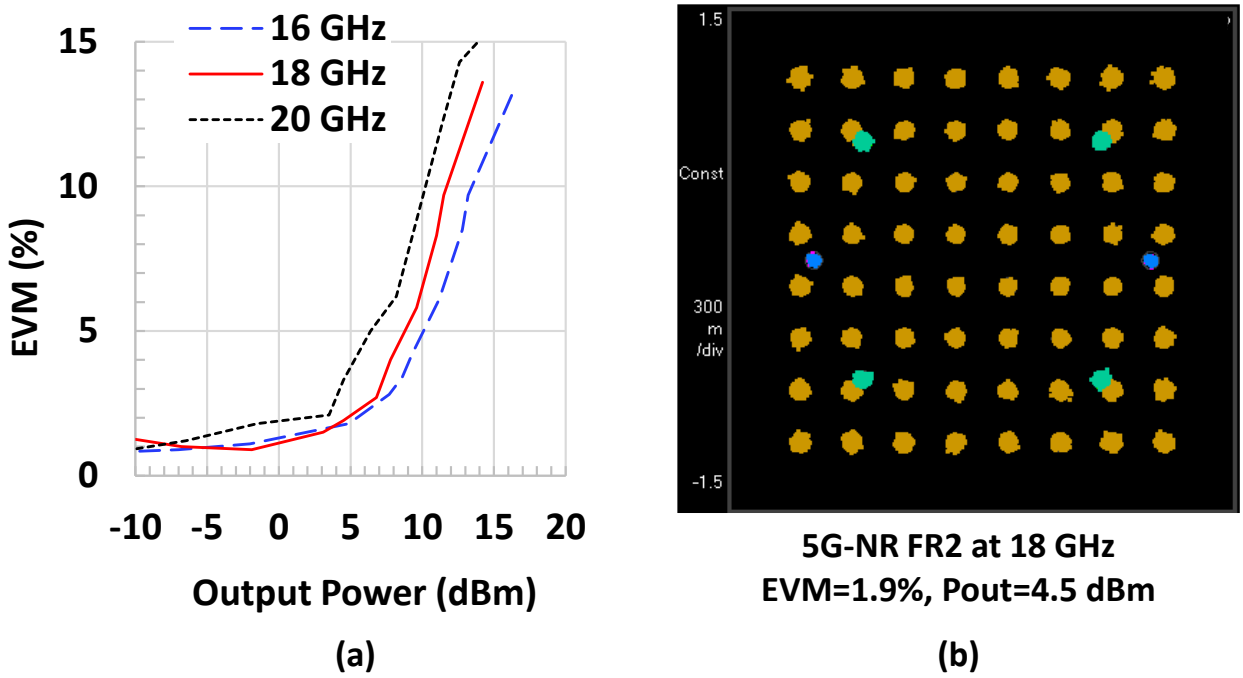


Fig. 3-23. EVM distortions of a 64-QAM 5G-NR Downlink signal including (a) Measured EVM in relation to the output power (b) Diagram of signal's constellation.

Fig. 3-22 illustrates the AM-PM distortions over the BW_{3dB} of the proposed wideband PA. Where the fabricated PA gives, at the center frequency, a small AM-PM distortion of 0.7° at OP_{1dB}

while it is a 2.1º at P_{sat}. It is worthy to mention that these distortions seem to increase by moving towards both frequency band edges, as shown in Fig. 3-22. Also, the wideband CMOS PA is used with a 400 MHz 64-QAM OFDM of 5G-NR FR2 modulated signal at 16, 18, and 20 GHz, as demonstrated in Fig. 3-23(a). It meets the 3GPP specifications and achieves, at the center freqeuncy, an EVM of -34.5 dB (1.9%) and -25 dB (5.6%) at output power of 4.5 dBm and 9.3 dBm, respectively, as demonstrated in Fig. 3-23(b) and Table 3-1.

3.5. Conclusion

This chapter has introduced an RF CMOS PA with 44.4% FBW where:

- A wideband CMOS PA with a frequency range of 14-22 GHz is proposed, using a SDB configuration, and DGS inductors, in order to achieve a flat gain response and improve the realized PAE.
- The designed wideband CMOS PA produces a flat gain response and high PAE. The resulting PA has low AM-PM distortions at maximum output power and minimal group delay variations. Additionally, it has a wide FBW of 44.4%, high PAE of 18.7%, and small EVM distortions that make it suitable for use in modern wireless communication systems at quasi-mm-wave frequency bands. The chip size for the implemented PA is 0.564 mm^2 including all the employed pads.

CHAPTER 4: DESIGN OF HIGH PAE STACKED *K*-BAND POWER AMPLIFIER

4.1. Introduction and Literature Review

Most of recent fabricated monolithic microwave integrated circuit (MMIC) designs deal with high data rates applications that use higher frequency bands. Automotive radars and other satellite communication systems, between these today's trends, use *K*-band frequencies (18-27 GHz). PAs, at such applications, are one of the most important parts that should be wisely designed [42]–[44]. These RF PAs should accommodate complex modulated techniques with high PAPR signals [45]–[47]. Moreover, the difficulty comes with the low breakdown voltage of the employed scaled down CMOS transistors, the inaccuracies in modeling of both active and passive components at high RF bands which is close to their transit and maximum frequencies (f_t and f_{max}, respectively), the isolation and noise cancellation between the implemented PA and the surrounding elements, and the burden of substrate loss. All these mentioned problems and others definitely pose additional constraints in designing CMOS RF PAs [24], [48]–[50].

STCs are commonly utilized to solve low breakdown voltages of the used nano-scaled CMOS transistors for increasing the output voltage headroom for high power applications. This presented solution, however, is usually accompanied with the phase shift problem at the intermediate nodes of these stacked configurations, particularly at higher RF bands, which decrease the realized PAE of the implemented CMOS PA [4].

To mitigate this phase shift problem, three commonly used reactive phase compensation techniques; series-inductive tuning technique (S-ITT), shunt capacitance tuning technique (Sh-CTT), and shunt-inductive tuning techniques (Sh-ITT) [4], [51]–[53] were employed with several STCs, as illustrated in Fig. 4-1(a–c), respectively. Nevertheless, the effectiveness of commonly used classical techniques can vary depending on the technology node used. These techniques may not take into account certain parasitic elements that can have a significant impact with the utilized CMOS technology.

In this chapter, A three-tunable low-pass π-phase compensator (π-PC) technique, as demonstrated in Fig. 4-1(d), is proposed and utilized in designing a CMOS RF PA to mitigate the

phase shift problem occurred at the intermediate nodes of the STCs. Additionally, it decreases the effects of high harmonic signals which in turns, improves the achieved PAE of the designed k-band PA. The implemented CMOS PA has two stages; driver and main stages, fabricated using two-STCs in 0.18-µm CMOS technology.

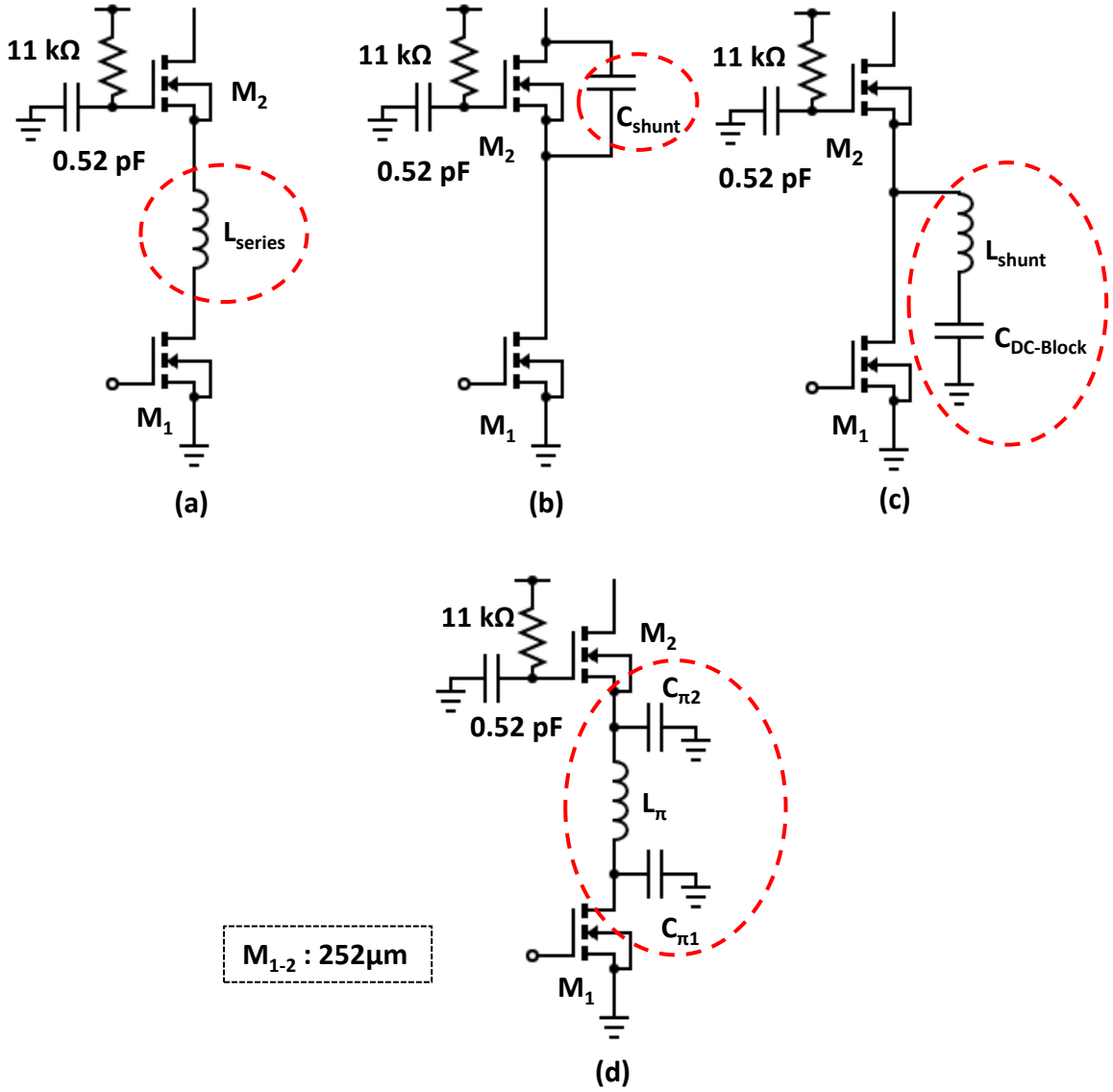


Fig. 4-1. Intermediate node tuning techniques utilized for designing the PA's main stage (a) Series inductive [51]. *(b) Shunt capacitance* [52]. *(c) Shunt inductive* [53]. *(d) proposed π-PC.*

This chapter explains, in section 4.2, the proposed three-tunable π-PC design. The measured results are demonstrated and evaluated with some of recently published results, as explained in section 4.3. Finally, section 4.4 concludes the main points of this chapter.

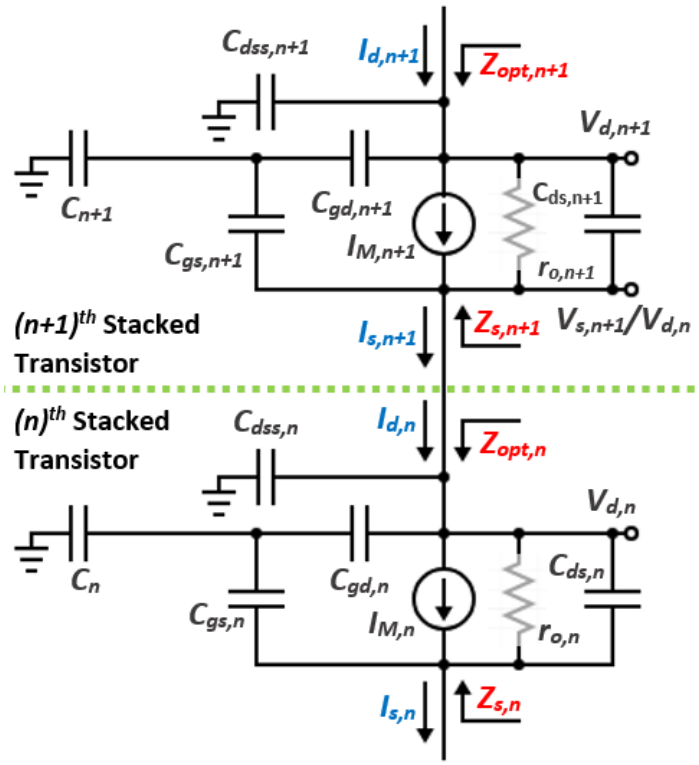


Fig. 4-2. Small-signal model of the STC.

4.2. Proposed Three-Tunable π-PC Design

The full K-band PA is manufactured using 0.18-µm CMOS technology which has two stages (driver and main stages) to enhance the overall power gain and the saturated output power of the implemented RF PA at the operating frequency band. As a consequence of employing STC for designing RF PAs at sub *mm*-wave frequency bands, the differences resulted in reactive parts of both output and input impedances of the stacked transistors cause the phase shift problem at these intermediate nodes. This problem reduces the maximum attainable PAE (PAE_{max}) of the stacked configurations.

Various techniques have been introduced in the literature to address the problem of phase shift in STs used in designing RF PAs. These techniques include adding a series inductor between STs [51], using an external shunt capacitor between the drain terminal and the source terminal of common gate STs [52], and connecting a shunt inductor at the intermediate nodes to ground with a dc blocking capacitor [53], as demonstrated in Fig. 4-1(a), Fig. 4-1(b), and Fig. 4-1(c), respectively. The values of the employed reactive elements are determined based on the difference

between the optimum drain output impedance of the n^{th} stacked transistor ($Z_{opt,n}$) and the source impedance of the $(n+1)^{th}$ stacked transistor ($Z_{S,n+1}$), as illustrated in Fig. 4-2.

Under the assumption of linear operation and do not take into account the small-signal output resistance of the n^{th} transistor ($r_{o,n}$), the optimal drain output admittance of the n^{th}stacked transistor ($Y_{opt,n}$) and the source admittance of $(n+1)^{th}$ stacked transistor ($Y_{S,n+1}$) can be derived as follows [54]:

$$\frac{V_{d,n+1}}{V_{d,n}} = \frac{n+1}{n}, \qquad n = 1, 2, \dots, N-1 \tag{4.2.1}$$

$$V_{ds,n} = V_{d,1} = V_{opt}, \qquad n = 1, 2, \dots, N \tag{4.2.2}$$

$$Y_{opt,n} = \frac{g_{m,n}V_{gs,n}}{nV_{opt}} + \frac{sC_{ds,n}}{n} + +sC_{dss,n} + \frac{sC_{gd,n}V_{gd,n}}{nV_{opt}}, \qquad n = 1, 2, \dots, N \tag{4.2.3}$$

$$V_{gs,n} = \frac{C_{gd,n}-(n-1)C_n}{C_{gs,n}+C_n+C_{gd,n}}V_{opt} \simeq \frac{V_{opt}}{g_{m,n}R_{opt}}, \qquad n = 2, 1, \dots, N \tag{4.2.4}$$

$$V_{gd,n} = -\frac{nC_n+C_{gs,n}}{C_{gs,n}+C_n+C_{gd,n}}V_{opt} \simeq -\frac{(1+g_{m,n}R_{opt})V_{opt}}{g_{m,n}R_{opt}}, \qquad n = 1, 2, \dots, N \tag{4.2.5}$$

$$\begin{aligned} Y_{opt,n} &\simeq \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{DS,n} + nC_{DSS,n}\right) - \frac{s}{n}\left(1 + \frac{1}{g_{m,n}R_{opt}}\right)C_{GD,n} \\ &= \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{EQV,n}\right), \quad n = 1, 2, \dots, N \end{aligned} \tag{4.2.6}$$

$$Y_{opt,n} \simeq \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{ds,n} + nC_{dss,n} + C_{gd,n}\right) = \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{EQV,n}\right), \quad n = 1, 2, \dots, N \tag{4.2.7}$$

$$I_{S,n+1} = \left(g_{m,n+1} + sC_{gs,n+1}\right)V_{gs,n+1} + s_{ds,n+1}V_{opt}, \qquad n = 1, 2, \dots, N-1 \tag{4.2.8}$$

$$Y_{S,n+1} = -\frac{g_{m,n+1}V_{gs,n+1}+sC_{ds,n+1}V_{opt}}{nV_{opt}} - \frac{sC_{gs,n+1}V_{gs,n+1}}{nV_{opt}}, \qquad n = 1, 2, \dots, N-1 \tag{4.2.9}$$

$$Y_{S,n+1} \simeq \frac{1}{nR_{opt}} - \frac{sC_{ds,n+1}}{n} + \frac{sC_{gs,n+1}}{ng_{m,n+1}R_{opt}}, \quad n = 1, 2, \dots, N-1 \tag{4.2.10}$$

As described (4.2.6) and (4.2.10), the resulting phase deviation ($\Delta\Phi_{ph}$) can be estimated as [54]:

$$\begin{aligned} \Delta\Phi_{ph} &= \Phi_{S,n+1} - \Phi_{opt,n} \\ &\simeq tan^{-1}\left(\omega\left(\frac{C_{gs,n+1}}{g_{m,n+1}} - C_{ds,n+1}R_{opt}\right)\right) \\ &\quad - tan^{-1}\left(-\omega C_{EQV,n}R_{opt}\right), \quad n = 1, 2, \dots, N-1 \end{aligned} \tag{4.2.11}$$

Where V_{opt} is the drain-source optimal voltage of each stacked transistor. For seeking to reduce the phase deviation at the intermediate nodes of the utilized STC, the three common classical phase compensation techniques are optimized and investigated in 0.18-µm CMOS technology for increasing the PAE_{max} extracted from employing the load-pull simulations for the two-STC of the proposed PA's main stage, as demonstrated in Fig. 4-3.

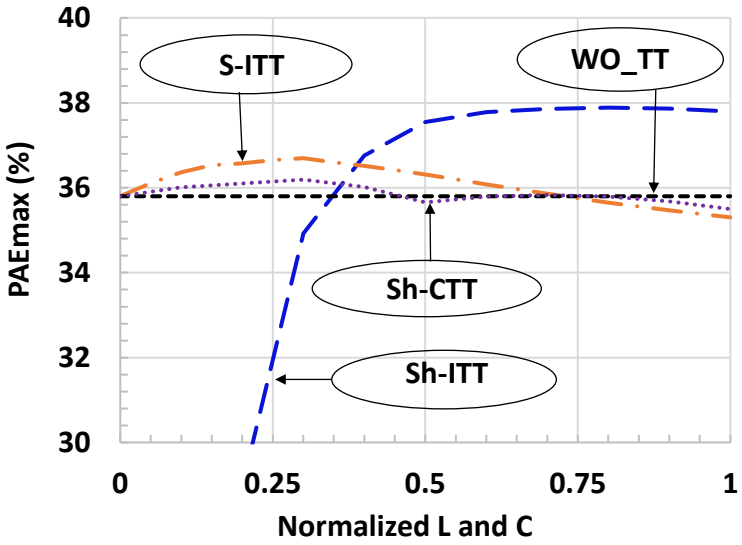


Fig. 4-3. Maximum simulated PAE for the two-stacked transistor main stage configuration, obtained through load-pull simulations utilizing classical techniques such as a series inductor normalized to a value of 100 pH, a shunt inductor normalized to 500 pH, and a shunt capacitor

normalized to 100 fF. The reference level is the PAE without using any tuning technique (WO_TT).

Employing these classical tuning methods particularly in case of using S-ITT and Sh-CTT, results in moderate improvements of the achieved PAE in 0.18-µm CMOS technology. These low realized performances of the three classical techniques would be from the engaged CMOS technology's limitations and other practical non-idealities at on- and off-states for the used class AB amplifiers, in particular in these high RF bands (approximately 0.5 f_t and 0.5 f_{max}).

Furthermore, some ignored terms are excluded from the analysis to simplify the mathematical analysis and reduce the resulting complexity of the derived (4.2.6), (4.2.10), and (4.2.11) equations. The neglected parasitics such as assuming full linear operation mode and ignoring the effect of $r_{o,n}$, especially at high-swing signals, may not be entirely valid. Additionally, the drain-source parasitic capacitance ($C_{ds,n}$) value in the employed triple-well CMOS technology is larger than both gate-source and gate-drain parasitic capacitances ($C_{gs,n}$ and $C_{gd,n}$, respectively) (about $1.5 * C_{gs,n}$ and $2.5 * C_{gd,n}$), which is the opposite case for some of the other recent CMOS technology nodes where their average value of $C_{ds,n}$ is much smaller than the $C_{gs,n}$ (about $0.1 * C_{gs,n}$ and $0.5 * C_{gs,n}$) [54]. Hence, the actual realistic values of both $Y_{S,n+1}$ and $Y_{opt,n}$ would vary corresponding to the explained limits and imposes a considerable responsibility in estimating the final $\Delta\Phi_{ph}$ at intermediate nodes of the used STCs.

In this regard, employing only one reactive passive element at these intermediate nodes may not be satisfactory for compensating these performance degradations and decreasing the mismatching criteria in both resistive and reactive components. Therefore, the proposed π-PC, as shown in Fig. 4-1(d), is designed utilizing three tunable reactive elements (L_π, $C_{\pi1}$ and $C_{\pi2}$) to modify the $Y_{S,n+1}$ to approximately equal the optimum load admittance of the n^{th} stacked transistor to maximize the PAE_{max} of the main stage's two-STC.

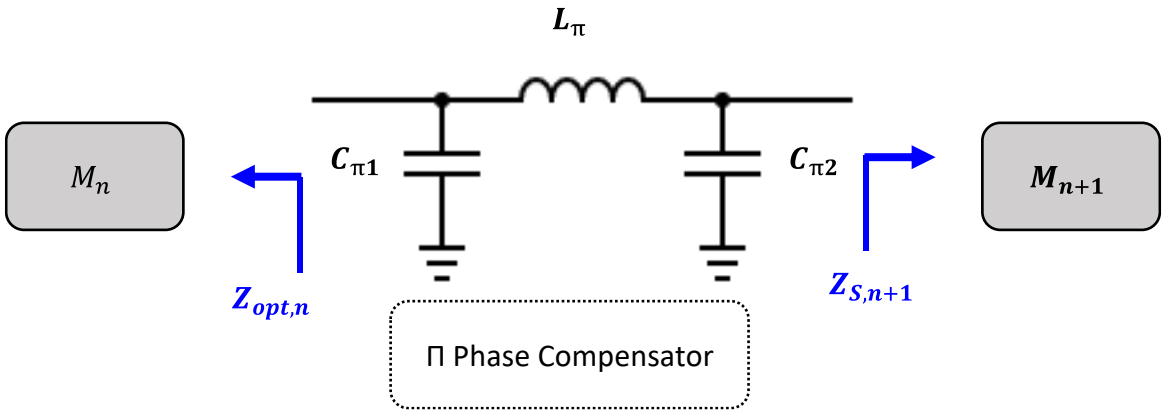


Fig. 4-4. Simple structure for employing the π-PC.

As shown in Fig. 4-4, the Y-parameters of the π-PC (Y_π) is given by:

$$Y_\pi = \begin{bmatrix} sC_{\pi1} + \frac{1}{sL_\pi} & -\frac{1}{sL_\pi} \\ -\frac{1}{sL_\pi} & sC_{\pi2} + \frac{1}{sL_\pi} \end{bmatrix} \tag{4.2.12}$$

$$|Y_\pi| = \frac{sC_{\pi1} * sL_\pi + 1}{sL_\pi} \times \frac{sC_{\pi2} * sL_\pi + 1}{sL_\pi} - \frac{1}{sL_\pi * sL_\pi} \tag{4.2.13}$$

$$|Y_\pi| = \frac{1}{s^2 L_\pi^2} \times \{(s^2 L_\pi C_{\pi1} + 1) \times (s^2 L_\pi C_{\pi2} + 1) - 1\} = B \tag{4.2.14}$$

Also, the Z-parameters of the π-PC (Z_π) is given by:

$$Z_\pi = \frac{1}{B} \begin{bmatrix} sC_{\pi2} + \frac{1}{sL_\pi} & \frac{1}{sL_\pi} \\ \frac{1}{sL_\pi} & sC_{\pi1} + \frac{1}{sL_\pi} \end{bmatrix} \tag{4.2.15}$$

$$Z_\pi = \frac{1}{sBL_\pi} \begin{bmatrix} 1 + s^2 L_\pi C_{\pi2} & 1 \\ 1 & 1 + s^2 L_\pi C_{\pi1} \end{bmatrix} \tag{4.2.16}$$

Where the modified load impedance ($Z^*_{opt,n}$) of the n^{th} transistor after employing the proposed π-PC can be determined as follows:

$$Z^*_{opt,n} = \frac{1}{sBL_\pi} \{1 + s^2 L_\pi C_{\pi2} - \frac{1}{1 + s^2 L_\pi C_{\pi1} + Z_{s,n+1}}\} \tag{4.2.17}$$

$$Z^*_{opt,n} = \frac{1}{sBL_\pi} \times \{A_2 - \frac{1}{A_1 + Z_{s,n+1}}\} \tag{4.2.18}$$

$$A_n = 1 + s^2 L_\pi C_{\pi n}, \quad n = 1,2$$

$$Z^*_{opt,n} = \frac{A_2A_1 + A_2Z_{s,n+1} - 1}{s(A_1 + Z_{s,n+1})BL_\pi} \tag{4.2.19}$$

The modified load admittance ($Y^*_{opt,n}$) of the n^{th} transistor after employing the proposed π-PC can be determined as follows:

$$Y^*_{opt,n} = \frac{s(A_2 + Z_{s,n+1})BL_\pi}{A_1A_2 + A_1Z_{s,n+1} - 1} \tag{4.2.20}$$

$$Y^*_{opt,n} = \frac{(s^2 \times \Im\{Z_{s,n+1}\}BL_\pi + s[A_2BL_\pi + \Re\{Z_{s,n+1}\}BL_\pi]}{A_1A_2 - 1 + A_1\Re\{Z_{s,n+1}\}] + s \times A_1\Im\{Z_{s,n+1}\}}$$
$$Z_{S,n+1} = \frac{1}{Y_{S,n+1}} = \Re\{Z_{S,n+1}\} + s\Im\{Z_{S,n+1}\} \tag{4.2.21}$$

Finally, the optimum values of L_π, $C_{\pi1}$ and $C_{\pi2}$, that minimize the phase shift problem at the intermediate nodes of the STC, can be calculated as follows:

$$\begin{aligned} &Y_{opt,n}(\omega) \\ &= \frac{\omega^2([A_1BL_\pi + \Re\{Z_{S,n+1}\}BL_\pi])(A_2\Im\{Z_{S,n+1}\}) - (\omega^2\Im\{Z_{S,n+1}\}BL_\pi)([A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}])}{[A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]^2 + (\omega A_2\Im\{Z_{S,n+1}\})^2} \\ &- j\omega\frac{([A_1BL_\pi + \Re\{Z_{S,n+1}\}BL_\pi])([A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]) + \omega^2(\Im\{Z_{S,n+1}\}BL_\pi)(A_2\Im\{Z_{S,n+1}\})}{[A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]^2 + (\omega A_2\Im\{Z_{S,n+1}\})^2} \end{aligned} \tag{4.2.22}$$

$$A_n(\omega) = 1 - \omega^2 L_\pi C_{\pi n}, \ \ n = 1,2$$
$$B(\omega) = \frac{1}{\omega^2 L_\pi^2}(1 - A_1A_2)$$
$$Z_{S,n+1} = \frac{1}{Y_{S,n+1}} = \Re\{Z_{S,n+1}\} + j\omega\,\Im\{Z_{S,n+1}\}$$

The process of mathematically finding the best values for the three reactive elements of the proposed π-PC in the used two-STC configuration of the PA's main stage would be a complex task due to the high frequencies involved. Thus, the three reactive elements of the π-PC, as shown in Fig. 4-5, are adjusted through load-pull simulation to determine the PAE_{max} of the two-STC of the PA's main stage after employing the proposed technique. Fig. 4-3 and Fig. 4-5 show the comparison between the performances of the proposed π-PC and the other classical techniques using reactive components with realistic characteristics according to the employed 0.18-µm CMOS technology. The use of the proposed tunable π-PC, as depicted in Fig. 4-3 and Fig. 4-5,

results in the highest PAE_{max} when compared to other commonly classical used compensation techniques. The improvement is primarily due to the compensation of both resistive and reactive components as described in (4.2.22). This results in the lowest $\Delta\Phi_{ph}$ at the operating frequency, as shown in Fig. 4-6.

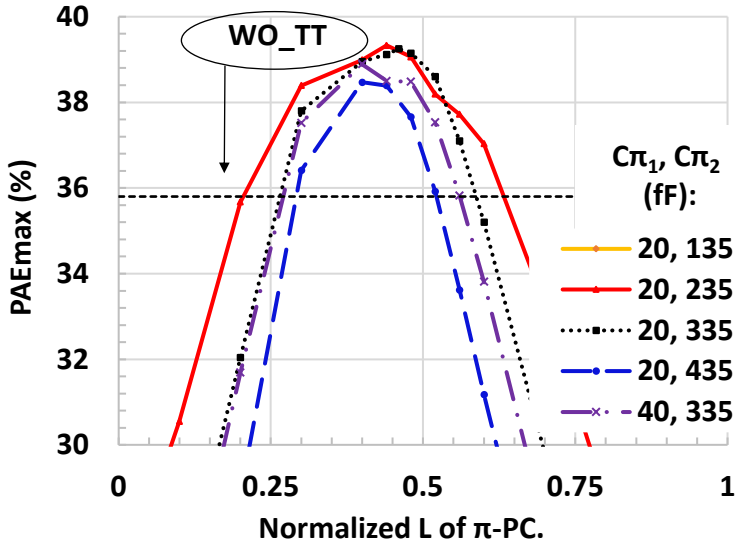


Fig. 4-5. Maximum simulated PAE for the two-stacked transistor main stage configuration, obtained through load-pull simulations utilizing classical techniques applying the suggested technique: Inductance of π-PC normalized to 500 pH with different values of $C_{\pi 1}$ and $C_{\pi 2}$.

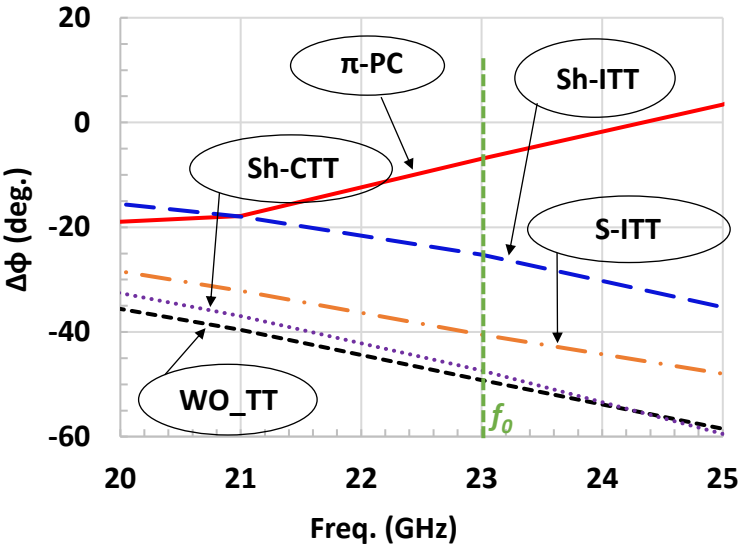


Fig. 4-6. Phase deviation between the source impedance of M_2 and the optimal output impedance of M_1 in the two-ST configuration of the main stage with and without using optimized phase compensation techniques. f_0 is the operating frequency.

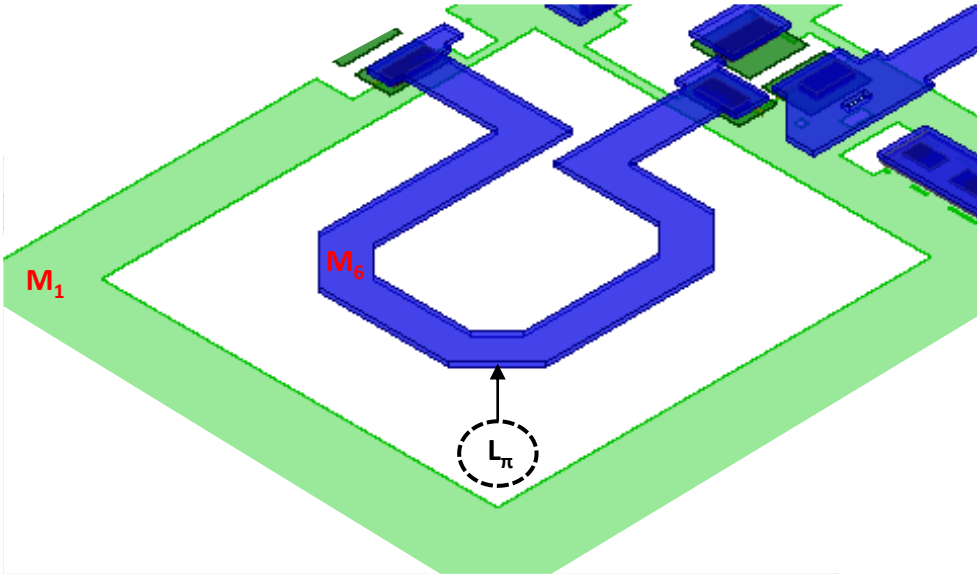


Fig. 4-7. Three-dimensional representation of the electromagnetic model of the designed π-PC.

Also, the third order low-pass filtering characteristic of the designed π-PC would contribute to lessening the effect of high harmonic signals. Despite S-ITT and Sh-CTT can behave as first order high harmonic traps, they do not substantially boost the PAE_{max}.

However, the suggested technique is sensitive to the values of the reactive elements used, as demonstrated in Fig. 4-5. Therefore, it must be constructed and optimized accurately using electromagnetic simulation tools that take into account the parasitics and the mutual effects of other used elements in the design, as illustrated in Fig. 4-7.

It must be constructed and optimized accurately using electromagnetic simulation tools that take into account the parasitics and the mutual effects of other used elements in the design, as shown in figure 4 7.

4.3. Implementation and Results

4.3.1. Fabrication and Measurement Setup

The proposed two-stage CMOS RF PA was manufactured engaging 0.18-µm CMOS bulk technology, as described in Fig. 4-8. The chip, as shown in Fig. 4-9, occupies around 0.74 × 0.82 mm^2 including the used pads. The fabricated chip was measured on a probe station (CASCADE

MICROTECH Summit 11000 M) by using *mm*-wave ground-signal-ground infinity probes connected with N5222A PNA Keysight network analyzer.

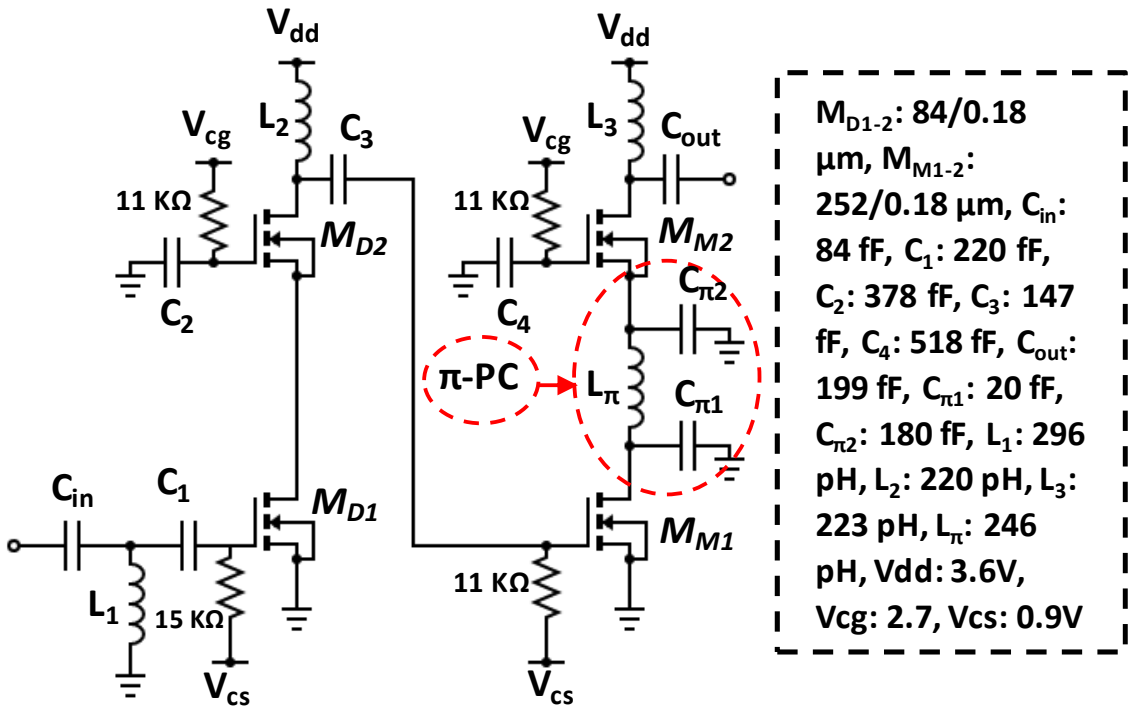


Fig. 4-8. Schematic view of the full fabricated K-band CMOS PA.

4.3.2. S-Parameters and Power Measurement Results

Fig. 4-10 shows the small-signal measured and simulated S-parameters of the designed RF PA. The PA achieves a measured power gain of 12.8 dB at 23 GHz. The BW_{3dB} is approximately 3 GHz (21 GHz -24 GHz), where its peak occurs at 23 GHz. The discrepancy in the measured results is attributable to the modeling errors and other foundry imperfections of active and passive components, particularly beyond the recommended frequencies (20 GHz).

Fig. 4-11 illustrates the performance of the large-signal continuous-wave power measurements of the proposed PA at different input power levels. The PA gives a P_{sat} of 16.0 dBm, an OP_{1dB} of 14.1 dBm, and an overall peak PAE of 18.3%. Additionally, the key points of the performance of the fabricated RF PA are compared with the literature CMOS RF PAs, as explained in Table 4-1. Where the measured power gain and peak PAE of the implemented PA is the highest among the reported *K*-band CMOS PAs using the same CMOS technology.

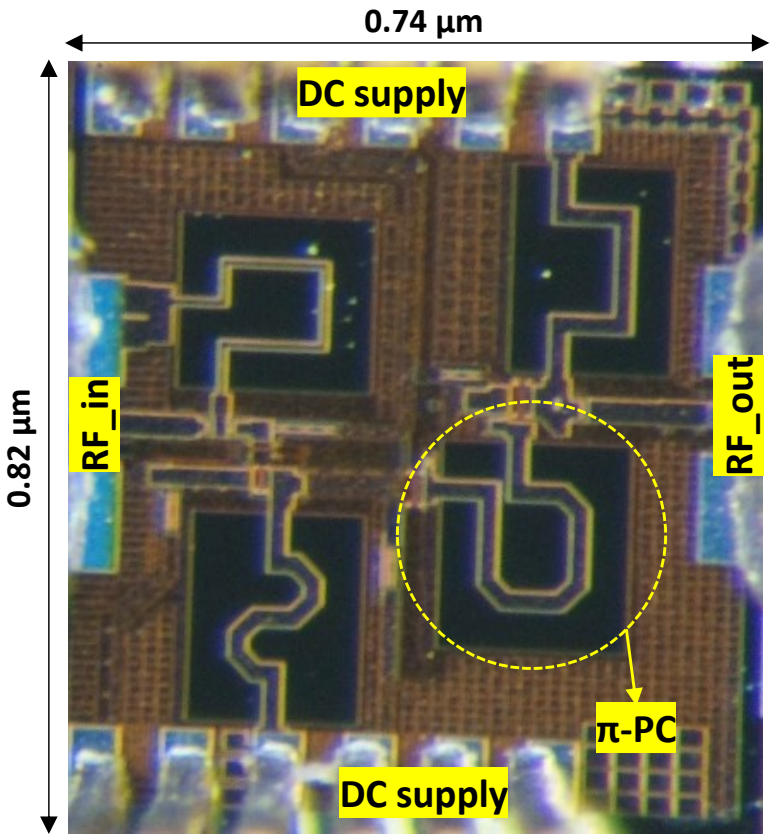


Fig. 4-9. Chip photograph of the manufactured K-band CMOS PA.

Table 4-1. COMPARING THE MEASURED RESULTS OF RECENT SUB-mm-WAVE CMOS PA DESIGNS

References	**This Work**	[55]	[56]	[57]	[58]
CMOS Tech. (nm)	**180**	180	180	180	65
Freq. (GHz)	**23**	24	23	23	28
Gain (dB)	**12.8**	8	10.2	12.8	18
P_{sat} (dBm)	**16.0**	16.6	19.8	18	18.5
OP_{1dB} (dBm	**14.1**	14.6	17.5	15.8	17
Peak PAE (%)	**18.3**	14	17.5	15	27.3
Total Area (mm^2)	**0.604**	0.37 (Active)	0.566	0.45	0.46

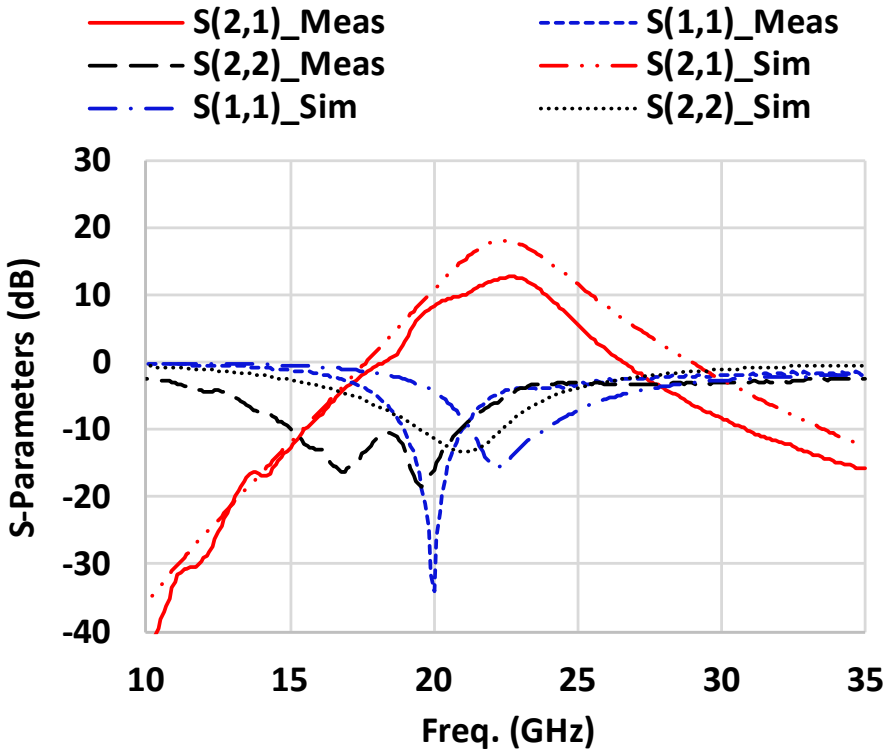


Fig. 4-10. Measured and post-layout simulated S-parameters of the PA.

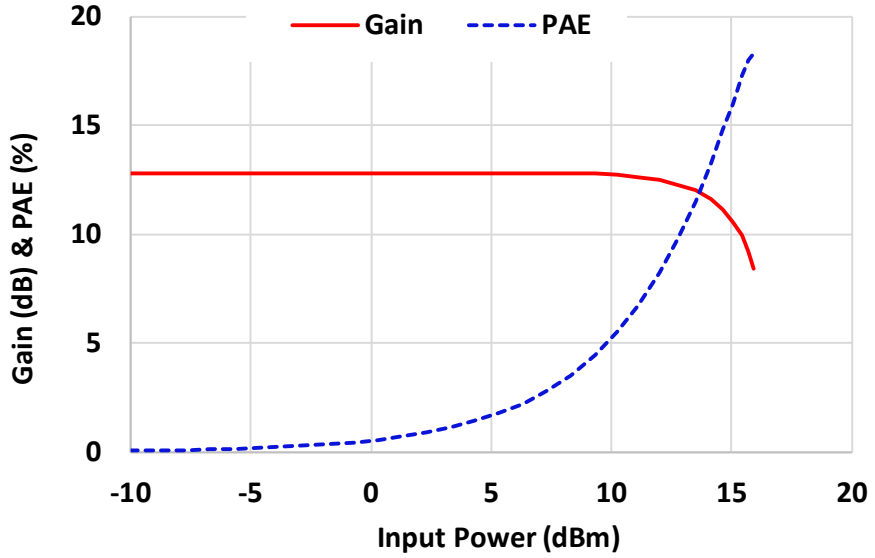


Fig. 4-11. Measured gain, output power, and PAE of the designed PA.

4.4. Conclusion

This chapter has introduced a high PAE stacked CMOS *K*-band PA where:

- A two-stage *K*-band PA with a proposed π-PC technique was fabricated in 0.18-µm CMOS technology node. The introduced π-PC has a simple structure which is behaving as a third-order harmonic trap that is utilized for reducing the distortions caused by high harmonic RF signals.
- The suggested π-PC is also using for minimizing the intermediate phase shift problem of STCs to enhance the PAE of the proposed RF PA.
- The fabricated PA realized a power gain of 12.8 dB at 23 GHz, a maximum PAE of 18.3%, an OP_{1dB} of 14.1 dBm, and a P_{sat} of 16.0 dBm. The fabricated RF PA consumes overall chip area of 0.604 mm^2.

CHAPTER 5: DESIGN OF HIGHLY LINEAR CMOS POWER AMPLIFIER

5.1. Introduction and Literature Review

As a result of increasing the necessity of the role of wireless applications in today's life, that require high transmitted and received data rates as stated in previous chapters. Most realized MMICs involve the use of higher frequency bands to fulfill these demands. The use of such high frequency bands, such as those found in satellite communication systems and automotive radars, has become a modern trend. PAs are crucial components in these systems. However, designing them for these high frequency bands using CMOS technologies poses several challenges. These include low breakdown voltages in transistors, difficulties in accurately modeling both active and passive on-chip elements at RF frequencies, the need for isolation and noise cancellation between the employed PAs and surrounding components, substrate loss, and the impact of the body effect of on-chip used transistors, which all impose strict limitations on the implementation of CMOS RF PAs [24], [50], [59]. Additionally, other problems, which take account of the on-chip parasitic effects and the non-linearity of the designed CMOS PAs, become more serious, particularly when accommodating advanced modulated waves having high PAPRs [60]–[62]. Lessening these accompanying non-linearity lets CMOS PAs to be used effectively in modern-day communication systems [63]–[65].

Given the limitations previously mentioned, one common technique for improving the linearity of RF PAs is to add a pre-distorter before the fabricated RF PAs. [22], [66]–[71]. The pre-distorter should have a non-linear characteristic that complements the gain compression behavior of the employed PA, as demonstrated in Fig. 2-19. However, the high data throughput, multi-user accessibility, power consumption and the use of higher-order modulations in modern high-frequency wireless applications, particularly those with wider bandwidth specifications, pose additional limitations to using digital pre-distorters [72]–[74].

One common method for achieving high gain expansion in RF PAs is to use a zero drain-to-source voltage field-effect-transistor (cold-FET) as an analog-pre-distorter, as it has smaller insertion loss and does not consume any dc power. However, increasing the size of the employed

cold-FET or applying a certain forward body biasing technique for achieving higher gain expansion can lead to lower insertion loss and reducing overall realized PAE [75], [76]. Furthermore, an adaptive built-in linearizer can be used to adjust the gate biases of the cold-FET based on the input power, that would improve the behavior of the pre-distorter [77], as demonstrated in Fig. 5-1. However, this presented adaptive pre-distortion linearizer needed an envelope detector that is a challenging to design an effective adaptive bias control circuit while operating with wide bandwidth envelope signals [78].

Also, the resulting performance of the RF CMOS linearizer could be evolved by utilizing an anti-phase signal at the gate terminal of the cold-FET with respect to its drain signal [56]. However, the necessary phase-delayed networks are normally implemented by transformers or transmission lines at higher frequencies consuming more chip area, as demonstrated in Fig. 5-2, and having further insertion losses which sequentially lead to decreasing the realized PAE of the fabricated CMOS PA. Accordingly, a 90° phase-delayed linearizer is employed instead of utilizing 180° phase-delay network to avoid using larger chip area at V-frequency band, however a large portion of the total fabricated chip is still consumed in fabricating such phase-delayed passive circuit, as shown in Fig. 5-2.

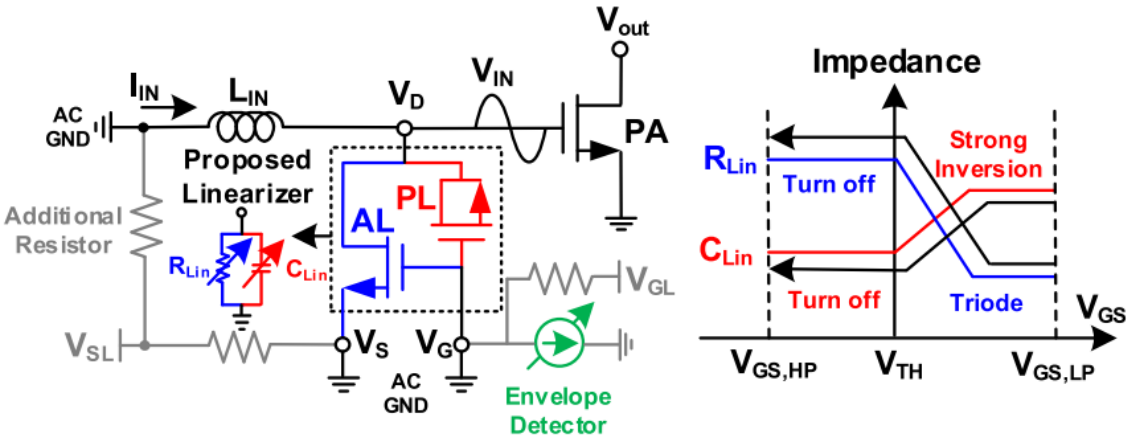


Fig. 5-1. Schematic of the introduced linearizer with the envelope detector [77].

Furthermore, Most of RF PAs use STCs to boost the isolation behavior and increase the output voltage headroom for high today's power applications [79]. This solution, however, is associated with an accurate adjustment to the voltage biasing of the STs to move away from the breakpoint of each used transistor. Besides, the phase shift problem between the intermediate nodes at stacked configurations, especially at high RF bands, diminishes the realized PAE of RF CMOS PAs, as

mentioned in the previous chapter. It is notable that this reduction of the CMOS PA performance would accumulate with the decrease of both of the power gain and the attained PAE coming from applying the pre-distortion linearizers. it is worthy to improve the overall realized PAE of the CMOS PA for satisfying the stringent requirement of the large-scale integration market.

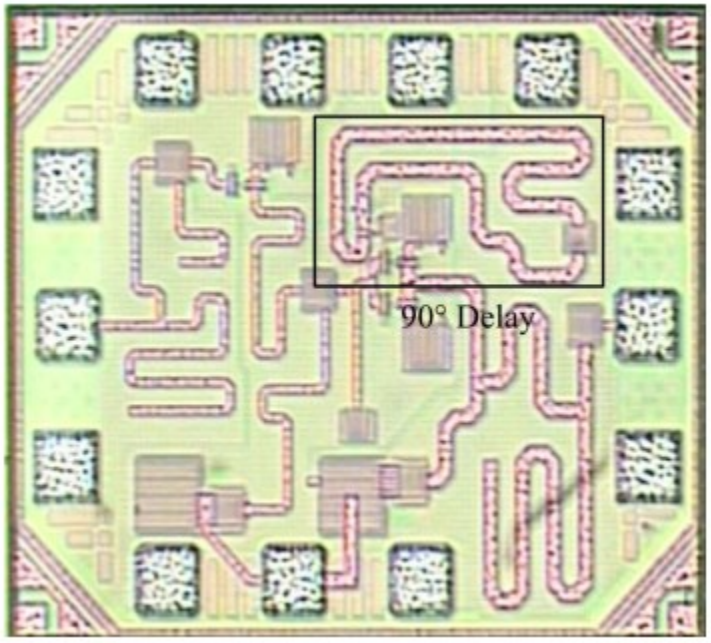


Fig. 5-2. Chip photograph of the introduced linear V-band PA using phase-delayed technique [56].

This chapter presents a new approach for enhancing the linearity of a CMOS PA by utilizing a capacitive feedbacked cold-FET APD. Additionally, an interstage two-tunable inductive and capacitive-phase compensator (LC-PC) designed circuit is introduced to improve the attainable PAE of the implemented PA. The proposed capacitive feedbacked APD and LC-PC are explained in this chapter at sections 5.2, and 5.3, respectively. The measured performance of the proposed approach is evaluated and compared to recently published results in section 5.4. The chapter also includes a design of an RF CMOS PA for Sub-6-GHz 5G applications using the proposed capacitive feedbacked linearizer, discussed in section 5.5. Ultimately, the main points are summarized in section 5.6.

5.2. Introduced Capacitive Feedbacked Cold APD

The full designed RF PA is implemented utilizing 0.18-µm CMOS technology as a two-stage PA (driver stage and main stage). The implemented two stages are utilized to boost the overall

power gain of the designed RF PA. An APD linearizer based on the cold-FET is designed to develop the linearity of the implemented CMOS PA, as explained in next sub-sections.

5.2.1. Classical Cold-FET APD

One of the key challenges in implementing RF PAs is the gain compression that occurs when the transistor is operated close to its saturation point, which leads to increased signal distortion. A passive APD can be utilized to mitigate this issue by introducing loss at low input power (P_{in}) levels and reducing these losses at higher input power levels, as illustrated in Fig. 5-3. While the use of an APD can increase the OP_{1dB}, it can also negatively impact other trade-off parameters of the designed PA such as gain and achievable PAE as a result of the insertion loss introduced by the APD. One efficient way to design that APD is by using a cold-FET, connected in parallel with the gate terminal of the RF CMOS PA, as demonstrated in Fig. 5-4.

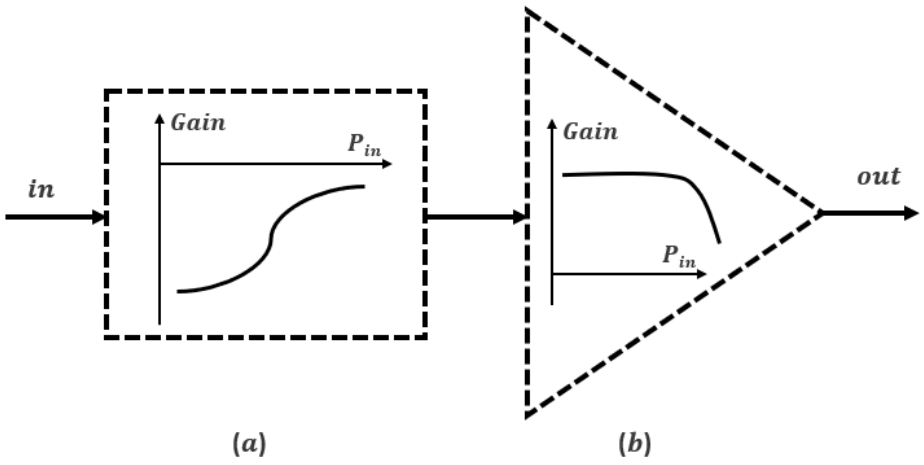


Fig. 5-3. Analog pre-distortion linearization technique (a) APD's characteristics (b) Gain compression behavior of the practical PAs.

The cold-FET's available power ($P_{av-Cold}$) is separated into the power supplied to the PA's gate terminal (P_{G-PA}) and the power used for the cold-(P_{Cold}). These two divided power levels are controlled by the size of the transistor and the gate biasing voltage of the linearizer (V_{G-Cold}). The dc source biasing voltage of the used cold-FET (V_{S-Cold}) is set to guarantee that the drain-to-source voltage is zero, reducing power loss through the linearizer, as seen in Fig. 5-4. The cold-FET's current-voltage characteristics in the linear and saturation regions make it suitable for use as a

passive APD. The equivalent drain-source resistance of the cold-FET in the linear region (R_{DS-L}) is given by the square-law transistor model for simplicity, as described in (5.2.1).

$$R_{DS-L} = \frac{1}{2\pi}\oint_0^{2\pi} \frac{1}{2K_n(V_{ov} - v_{DS})} d(\omega t) \tag{5.2.1}$$

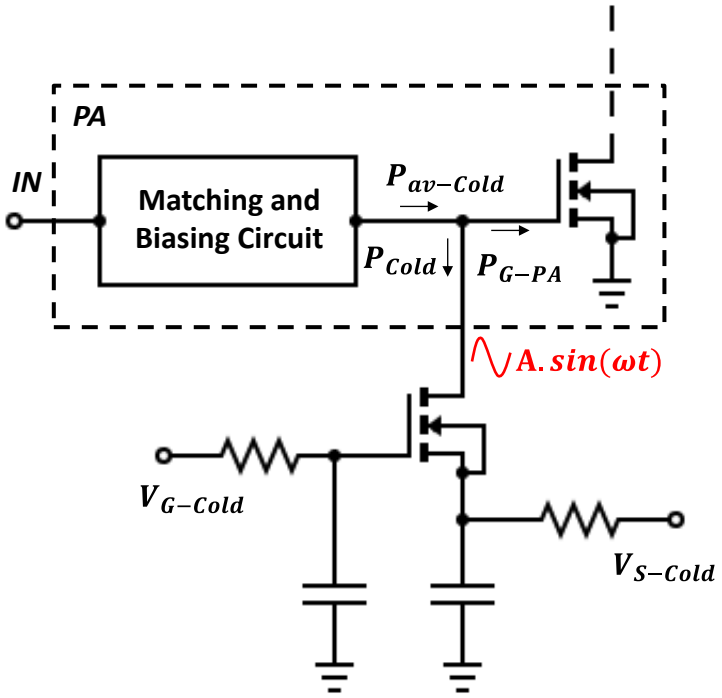


Fig. 5-4. Schematic view of the classical cold-FET linearizer.

Where: K_n and V_{ov} are the conduction parameter of the employed cold-FET and its over-drive voltage, respectively [56]. At very low input power levels, the V_{ov} of the cold-FET is considerably higher than the drain-to-source voltage ($v_{DS} = A.\sin(\omega t)$), making the used cold-FET acting approximately as a constant small shunt resistor at this deep triode operating region, as presented in (5.2.2). As a consequence of increasing the value of v_{DS} signal, that comes corresponding to increasing the input power level, the behavior of the employed cold-FET would be shifted to intermediate linear region raising its equivalent resistor until it gets its maximum value at its saturation region when the v_{DS} is equal to the V_{ov}. Consequently, the classical cold-FET shows a voltage-controlled parallel resistor that regularly grows with increasing input power level.

$$\frac{1}{2K_nV_{ov}} \tag{5.2.2}$$

In Fig. 5-5, the performance of a classical cold-FET linearizer is simulated by varying the input power and adjusting the employed transistor's width and gate bias voltage. The presented results show that the linearizer has lower losses at high input power levels than at low power levels. This is the key characteristic of the APD as demonstrated in Fig. 5-3(a). As mentioned in (5.2.1), increasing the gate dc bias voltage or employing wider transistors lessens the transistor's equivalent resistance, which improves the linearizer's compensation slope. However, it also leads to an increase in the transistor's insertion loss, as shown in Fig. 5-5.

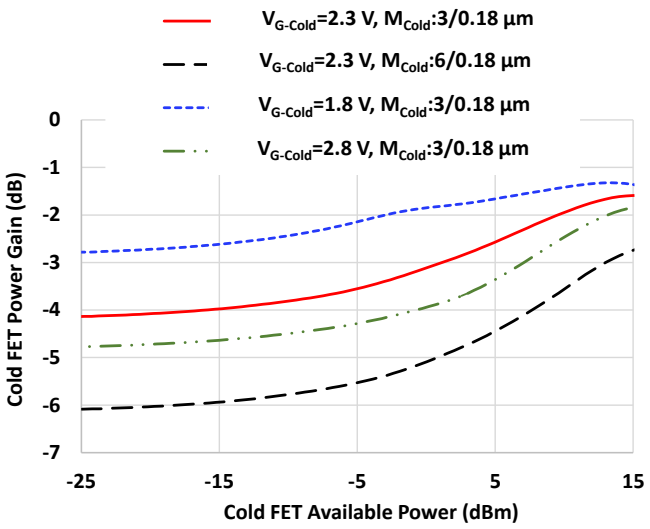


Fig. 5-5. Simulated power gain of the classical cold-FET with changing its size and its gate biasing voltage.

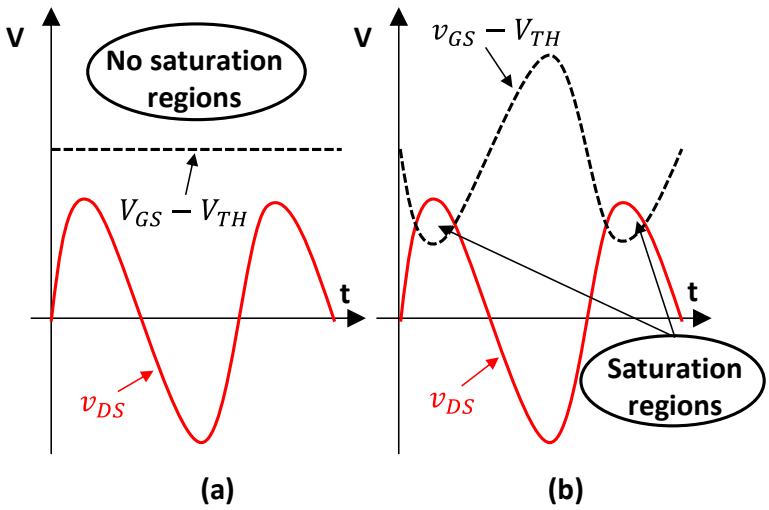


Fig. 5-6. Illustrative diagrams of v_{DS} and $(v_{GS} - V_{TH})$ waveforms with using (a) Classical technique (b) phase-delayed technique [56].

5.2.2. Phase-delayed cold-FET APD

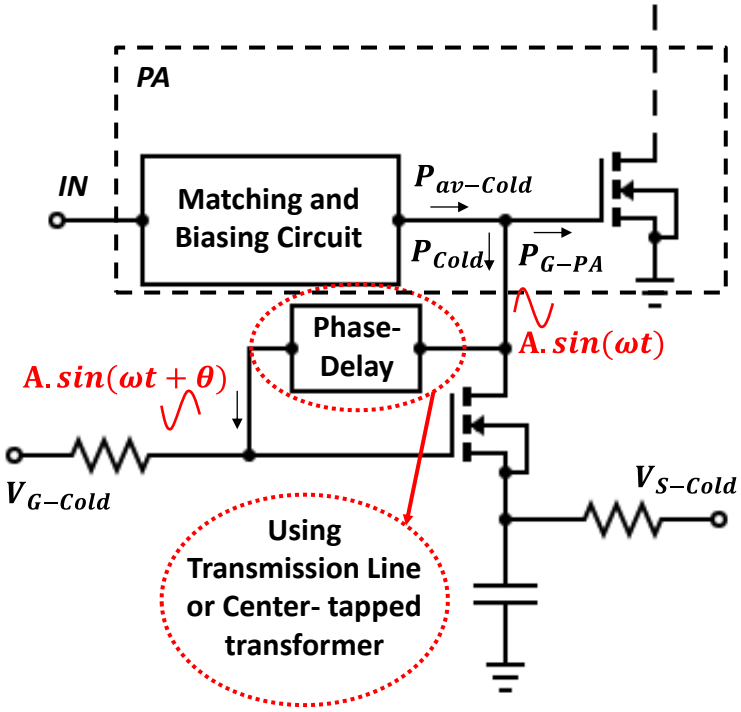


Fig. 5-7. Schematic diagram of the linearizer using a phase delayed cold-FET [56].

Because of the low classical APD's compensation slope, as explained in Fig. 5-5, that reduces its ability to compensate for the non-linearity of designed RF CMOS PAs, particularly near to the cut-off frequencies of the utilized CMOS technology. This modest compensation slope challenge comes as the only efficient source of modifying the used cold-FET's equivalent resistor at the linear region is v_{DS} , as illustrated in Fig. 5-6(a). However, an alternative method proposed by Kao et al. [56] is to use an anti-phase signal applied at the gate terminal of the cold transistor, as shown in Fig. 5-7. This improves the linearizer's compensation slope. With using this method where the V_{ov} of the cold-FET is pushed to decrease oppositely to the change of the v_{DS}, pushing the modified cold-FET into saturation earlier than the classical technique, as illustrated in Fig. 5-6(b). However, designing the necessary phase-delayed circuits using transmission lines or even utilizing center-tapped transformers is not recommended for on-chip designs at *K*-bands because of their larger chip area consumption and lower achievable Q-factors, which can worsen the APD's insertion loss, particularly with the CMOS technology used, which has a lower conductance compared to other

advanced CMOS technologies and limited metal stacking property. Therefore, the overall advantage of this phase-delayed method on the performance of the RF PA is likely to be reduced.

5.2.3. Proposed Capacitive Feedbacked Cold-FET APD

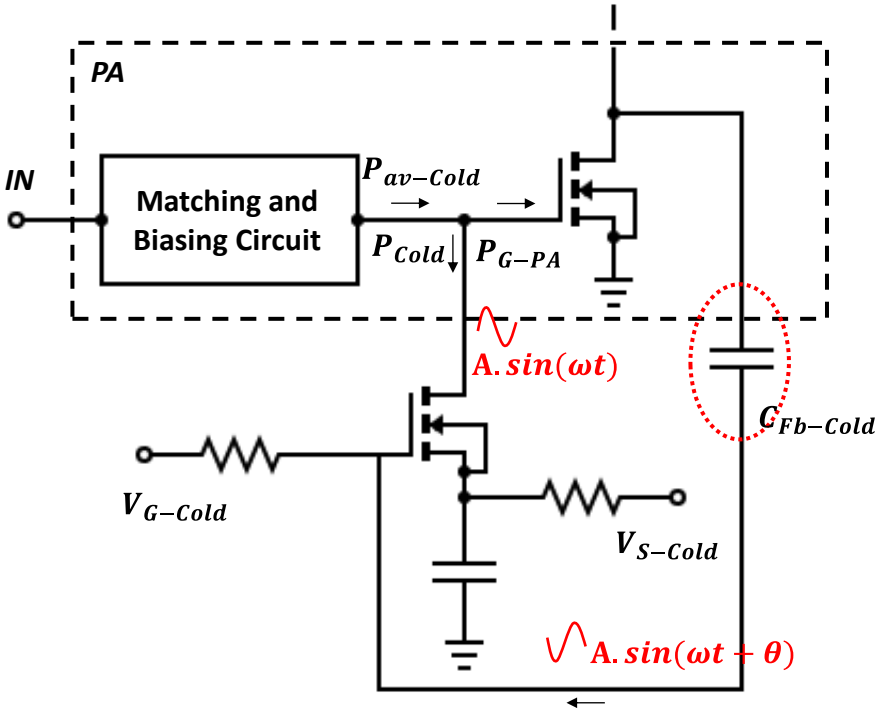


Fig. 5-8. Schematic view of the design concept for the capacitive feedback-enhanced cold-FET analog pre-distorter.

The proposed linearizer, shown in Fig. 5-8, utilizes an anti-phase concept rather than bulky used transmission lines and transformers [56] which negatively impact the performance of the fabricated PAs attributable to insertion losses. Instead, the anti-phase signal needed to adjust the V_{ov} of the employed cold-FET is generated by exploiting the natural anti-phase behavior between the gate voltage signal and the drain signal in the CS configurations. This is achieved by using a capacitor ($C_{Fb-Cold}$) between the input transistor of the driver stage and the cold-FET linearizer's gate terminal as a feedback path. This capacitor also serves as a dc-blocking capacitor between the amplifier's driver stage and the linearizer. The feedbacked capacitor has a minimal area and a better Q-factor compared to on-chip alternatives such as transmission lines and transformers. However, as a result of the parasitics of the utilized active and passive elements, the signal is not purely anti-phased with the input signal. Therefore, the value of $C_{Fb-Cold}$ is adjusted, as shown in

Fig. 5-9, to achieve optimal performance of the proposed linearizer. The voltage waveform at the gate terminal of the suggested cold-FET varies with the changes in the values of the utilized feedbacked capacitance, as shown in Fig. 5-10.

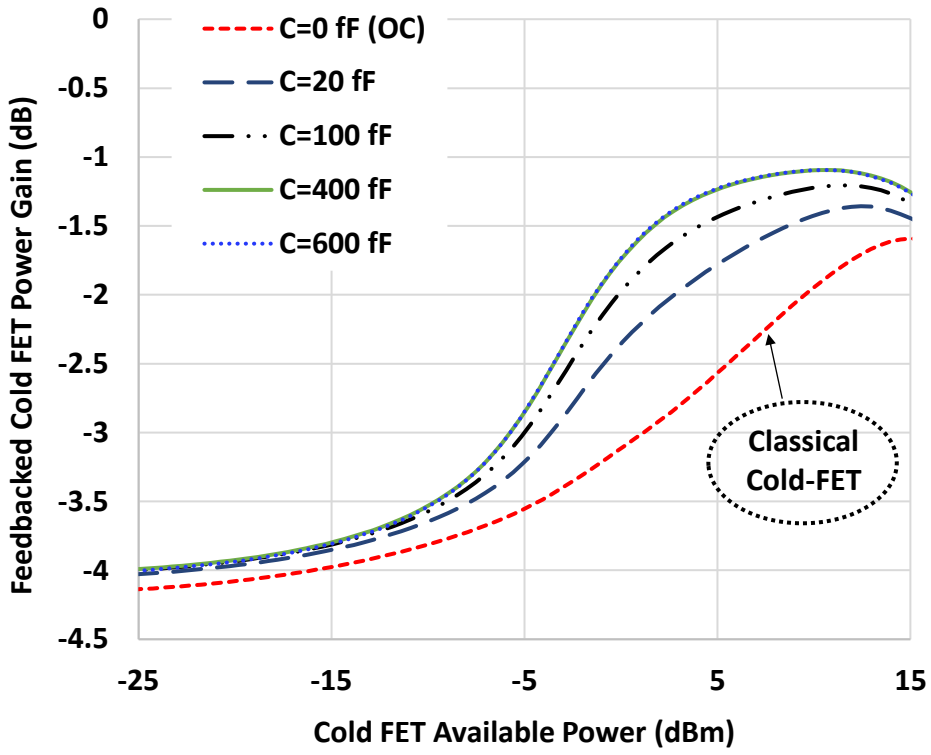


Fig. 5-9. power gain of the proposed capacitive feedbacked cold-FET APD, showing the results obtained using the same dimensions (3/0.18 µm) and bias voltage (2.3 V) for the feedbacked cold-FET, but with varying values of $C_{Fb-Cold}$.

Fig. 5-9 illustrates that utilizing the capacitive feedbacked proposed technique enhances the employed linearizer's compensation slope compared with utilizing classical APD that has the same size and dc-biasing voltage. Furthermore, the resulting compensation slope is developed by increasing the feedbacked capacitance until the compensation slope saturates with the value of 400 fF. In case of utilizing the classical cold-FET, the gate terminal has a constant dc signal, as shown in Fig. 5-10(a). Utilizing different values of the introduced feedbacked capacitance pushes the signal at the gate terminal of the employed cold-FET to be out-of-phase with different amplitude values, as demonstrated in Fig. 5-10(b)-(d), for enhancing the performance of the introduced linearizer. Therefore, utilizing only capacitor of 400 fF would achieve similar compensation slope of about 3 dB compared with the double-sized classical cold-FET (6/0.18 µm) by diminishing its insertion loss by about 58%, as shown in Fig. 5-5 and Fig. 5-9. This improvement happened in

both insertion loss and the resulting compensation slope, owing to the use of higher Q-factor feedback capacitor, will unquestionably be turned into enhancing the performance of the designed RF CMOS PA.

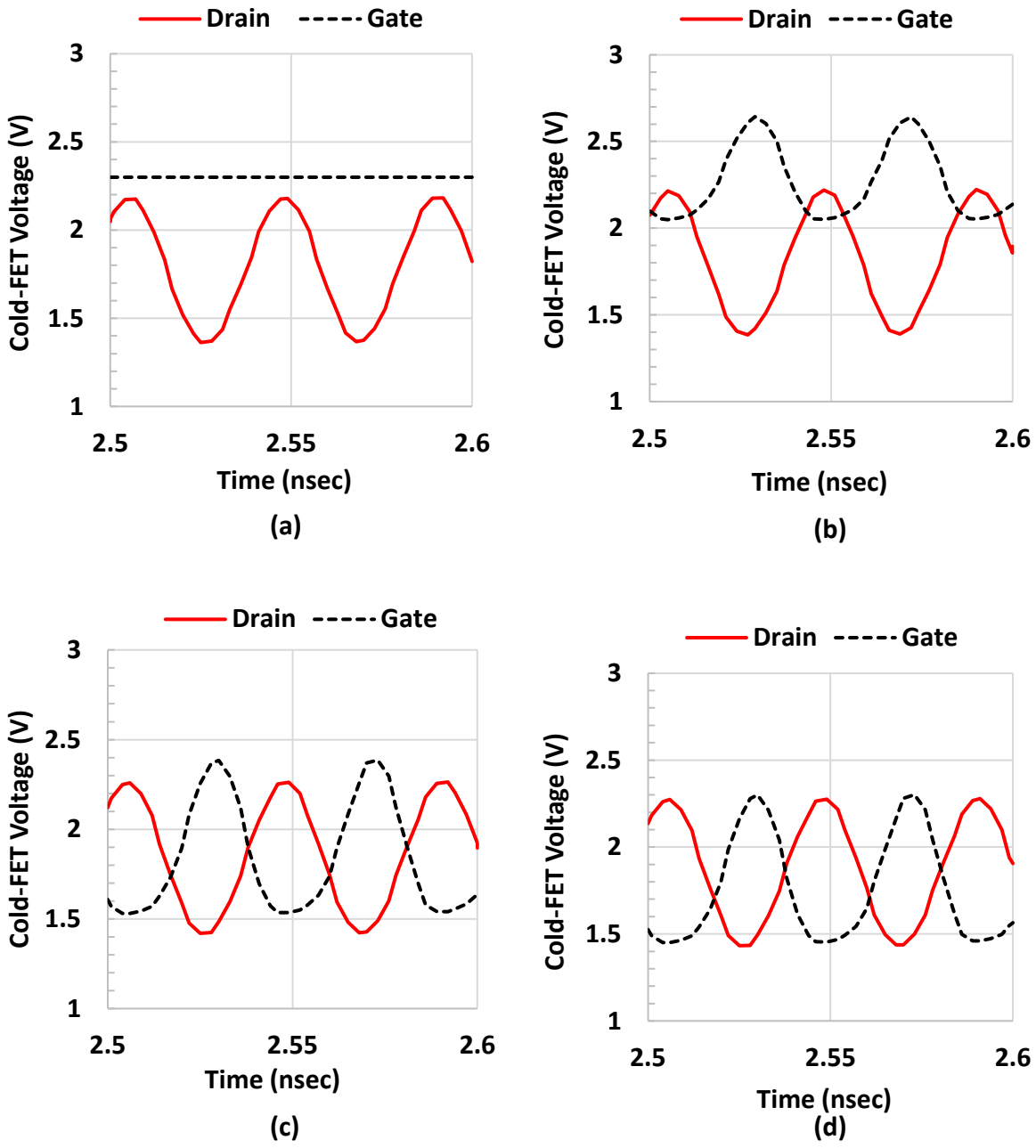


Fig. 5-10. Simulated changes in the drain and gate voltage waveforms of the cold-FET at a constant input power level of 0 dBm, as the value of the feedback capacitor is altered (a) Traditional method using 0 fF (b) 20 fF (c) 400 fF (d) 600 fF.

5.3. Proposed Two-Tunable LC-PC Design

5.3.1. Stacked Transistors Limitations

The driver stage of the design is composed of two-STC, and the main stage is a CS configuration. Theoretically, selecting the appropriate number and size of STs should lead to optimal performance, with an increase in the number of stacked transistors resulting in higher saturated output power, power gain, and reduced drain-gate and drain-source swings for the RF PA. However, in reality, these assumptions may not hold true due to limitations imposed by the CMOS technology used and its parasitics, phase shift, frequency of operation, and load mismatch, particularly at higher RF bands [32].

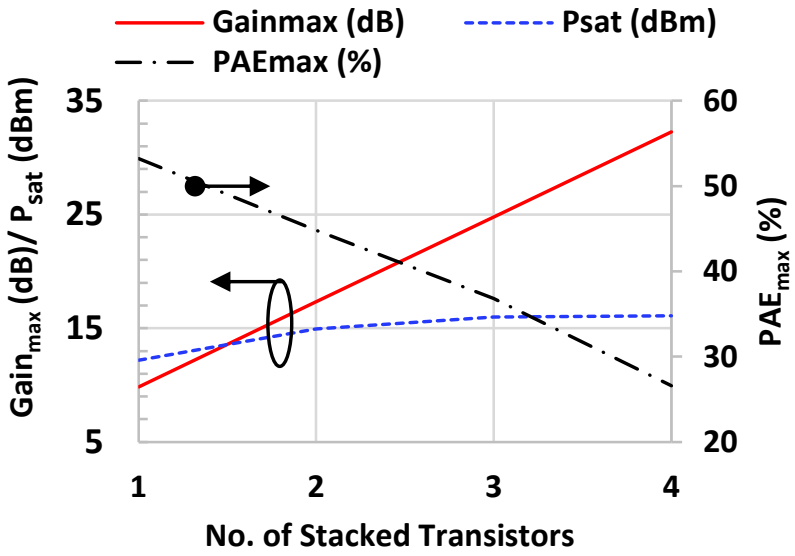


Fig. 5-11. The impact on maximum gain, PAE, and P_{sat} at 23.5 GHz of varying the number of the used transistors in the STCs as determined by S-parameter and load-pull simulations, with the drain-source voltage for every single transistor in the STCs held constant.

Therefore, The design of the driver and main stages of the CMOS PA must be done with care when it comes to selecting the number of stacked transistors. Amplifiers using one, two, three, and four stacked transistors with a size of 84/0.18 µm, as illustrated in Fig. 5-11, were designed and their performance was compared, apart from the effect of the introduced feedbacked pre-distortion linearizer. The four-STC, as shown in Fig. 5-11, achieved the highest maximum attainable gain and the smallest PAE. However, the CS configuration resulted in the largest realized PAE along

with the smallest maximum attainable gain. It's worth noting that the P_{sat} had only a modest change when using two, three, and four-STCs. Also, utilizing beyond 2-STs CMOS amplifiers can lead to phase shift problems at the intermediate nodes, which can increase the complexity of the final CMOS PA design, particularly at quasi-*mm*-wave frequencies. Employing a wider CS transistor configuration for the output stage can improve the delivered output power and the achieved PAE of the CMOS PA, while the use of a two-ST driver stage can increase the overall gain.

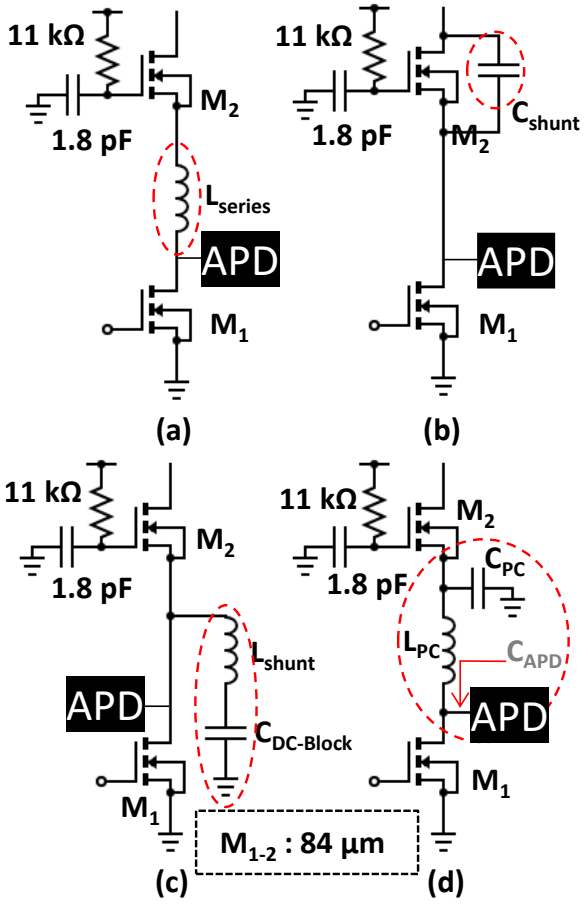


Fig. 5-12. Different methods used to adjust the intermediate node in the design of the PA's driver stage, taking into account the impact of the suggested Cold-FET linearizer (a) Series inductive technique (b) Shunt capacitance technique (c) Shunt inductive technique (d) Proposed two-tunable LC-PC.

5.3.2. Proposed LC-PC Design with Two-Tunable Reactive Elements

Due to employing STCs in designing of CMOS PAs at *K*-bands, the differences in reactive parts of both output and input impedances of the used stacked transistors cause a phase shift

problem occurred at the intermediate nodes. This problem reduces the achieved PAE_{max} of the used stacked configurations. Also, evolving the linearity of the implemented CMOS PAs by using the analog pre-distortion linearization technique primarily comes at the cost of diminishing the overall power gain along with the realized PAE of these PAs. So, an LC-PC is suggested for solving the phase shift problem at the intermediate nodes of the two-STC of the driver stage in addition with the formerly presented capacitive feedbacked cold-FET linearizer.

As previously illustrated, there are three frequently reported improved techniques, S-ITT, Sh-CTT, and Sh-ITT, employed to reduce the disadvantage of the resulting phase shift problem, as demonstrated in Fig. 4-1(a), Fig. 4-1(b), and Fig. 4-1(c), respectively. The values of these reactive elements should be estimated depending on the mismatching between $Z_{opt,n}$ and $Z_{S,n+1}$, as shown in Fig. 4-2. With assuming linear operation mode and ignoring the effect of $r_{o,n}$, as described in before, $Y_{opt,n}$ and $Y_{S,n+1}$ and the resulting $\Delta\Phi_{ph}$ can be given as follows [54]:

$$Y_{opt,n} \simeq \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{ds,n} + nC_{dss,n} + C_{gd,n}\right) = \frac{1}{nR_{opt}} - \frac{s}{n}\left(C_{EQV,n}\right), \quad n = 1, 2, \dots, N \tag{5.3.1}$$

$$Y_{S,n+1} = -\frac{g_{m,n+1}V_{gs,n+1} + sC_{ds,n+1}V_{opt}}{nV_{opt}} - \frac{sC_{gs,n+1}V_{gs,n+1}}{nV_{opt}}, \quad n = 1, 2, \dots, N-1 \tag{5.3.2}$$

$$\begin{aligned}\Delta\Phi_{ph} &= \Phi_{S,n+1} - \Phi_{opt,n} \\ &\simeq tan^{-1}\left(\omega\left(\frac{C_{gs,n+1}}{g_{m,n+1}} - C_{ds,n+1}R_{opt}\right)\right) \\ &\quad - tan^{-1}\left(-\omega C_{EQV,n}R_{opt}\right), \quad n = 1, 2, \dots, N-1\end{aligned} \tag{5.3.3}$$

In accordance with the above-mentioned equations, the proposed method for diminishing the value of $\Delta\Phi_{ph}$ in the two-stacked configuration of the driver stage involves testing the three commonly used tuning techniques. However, it should be noted that these methods assume full linear operation, do not take into account the effect of $r_{o,n}$ in (5.3.1) to (5.3.3), and neglect other practical factors such as parasitics and non-idealities in class AB operations, which may not be entirely accurate when using the utilized CMOS technology. Additionally, the evaluation of intermediate mismatching becomes more complex when taking into account the effect of the

utilized capacitive feedbacked APD, as illustrated in Fig. 5-12. As it affects the optimal load impedance of the two-STC in both its resistance and reactance components, as illustrated in Fig. 5-13. As a result, the actual values of $Y_{opt,n}$ and $Y_{S,n+1}$ will deviate from the simplified formulas presented in (5.3.1) and (5.3.2) at both the real and imaginary parts.

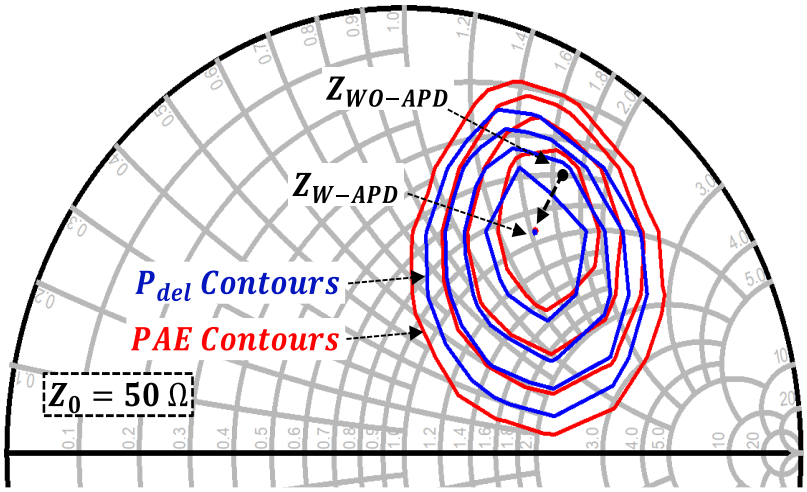


Fig. 5-13. Changes in the optimal load impedance of the two-stage driver configuration resulting from the influence of the capacitive feedbacked APD.

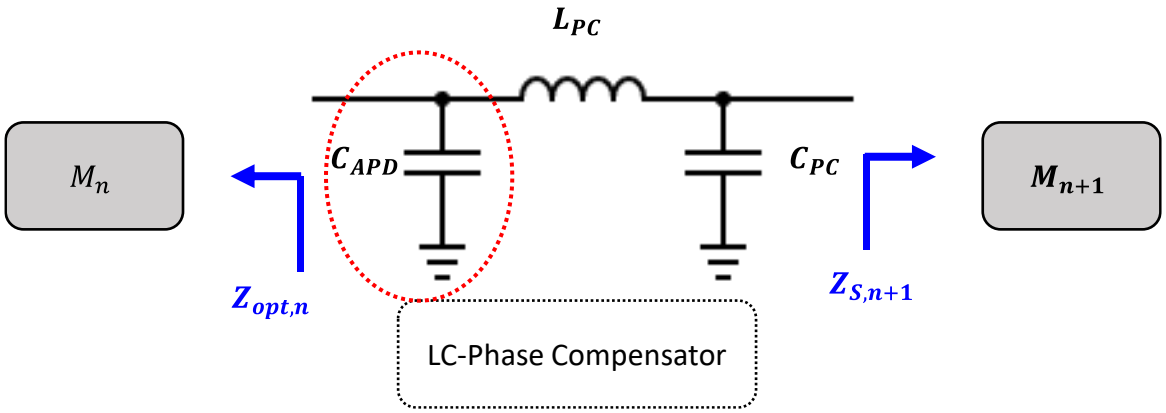


Fig. 5-14. Simple structure for employing the LC-PC considering the feedbacked APD's loading effect.

In this regard, adding merely one reactive component in the intermediate node is no longer enough to compensate for both resistive and reactive mismatching, as illustrated in Fig. 5-12(a), Fig. 5-12(b), and Fig. 5-12(c). Hence, an introduced LC-PC, as demonstrated in Fig. 5-12(d), is designed using two-tunable reactive components (L_{PC} and C_{PC}) without neglecting the capacitive loading effect of the feedbacked APD (C_{APD}).

As similar to the derivation of (4.2.22), the modified $Y_{opt,n}$ can be derived as expressed in (5.3.4). Where the optimal values of L_{PC} and C_{PC} can be estimated for improving the PAE_{max} of the used stacked configuration by compensating both resistive and reactive mismatching components considering the APD's loading effect, as illustrated in Fig. 5-14.

$$\begin{aligned}
&\boldsymbol{Y_{opt,n}}(\omega) \\
&= \frac{\omega^2\left([A_1 BL_{PC} + \Re\{Z_{S,n+1}\}BL_{PC}]\right)\left(A_2\Im\{Z_{S,n+1}\}\right) - \left(\omega^2\Im\{Z_{S,n+1}\}BL_{PC}\right)\left([A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]\right)}{[A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]^2 + \left(\omega A_2\Im\{Z_{S,n+1}\}\right)^2} \\
&- j\omega\frac{\left([A_1 BL_{PC} + \Re\{Z_{S,n+1}\}BL_{PC}]\right)\left([A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]\right) + \omega^2\left(\Im\{Z_{S,n+1}\}BL_{PC}\right)\left(A_2\Im\{Z_{S,n+1}\}\right)}{[A_2A_1 - 1 + A_2\Re\{Z_{S,n+1}\}]^2 + (\omega A_2\Im\{Z_{S,n+1}\})^2}
\end{aligned} \tag{5.3.4}$$

$$A_1(\omega) = 1 - \omega^2 L_{PC}C_{APD},\ A_2(\omega) = 1 - \omega^2 L_{PC}C_{PC},\ B(\omega) = \frac{1}{\omega^2 L_{PC}^2}(1 - A_1A_2)$$

$$Z_{S,n+1} = \frac{1}{Y_{S,n+1}} = \Re\{Z_{S,n+1}\} + j\omega\,\Im\{Z_{S,n+1}\}$$

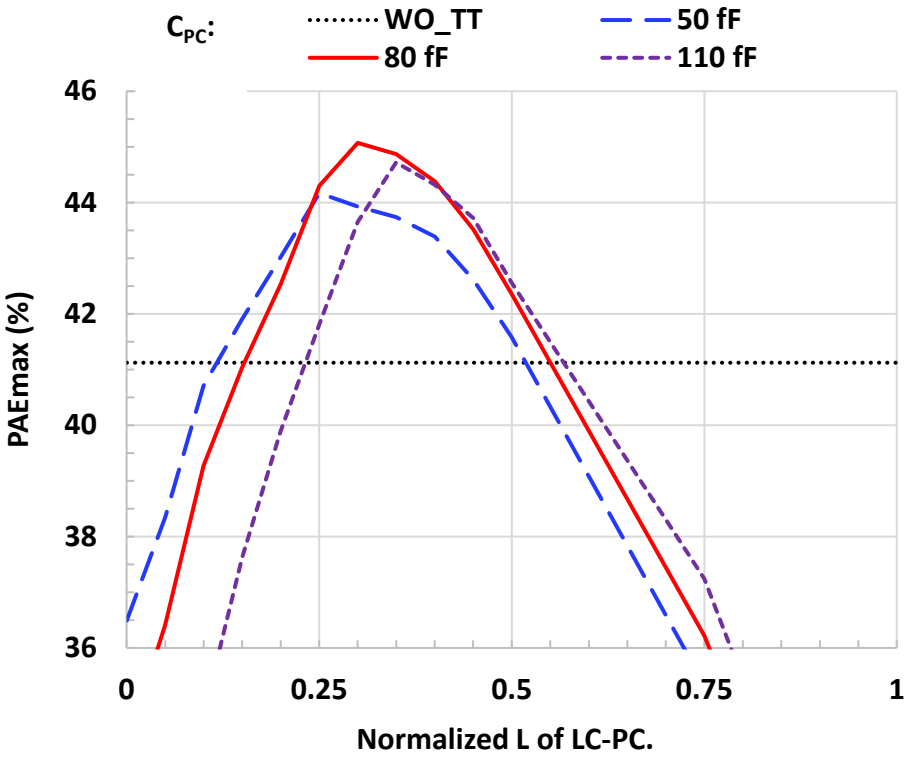


Fig. 5-15. Maximum PAE of the two-stage driver configuration achieved by optimizing the inductive and capacitive elements of the proposed LC-PC. The inductance values are normalized to 1 nH. The reference level is the performance without using any tuning technique (WO_TT).

Still, mathematically estimating the introduced LC-PC's optimal values, using these non-linear equations, would be actually a difficult task, particularly at *K*-band frequencies. Hence, L_{PC} and C_{PC} of the LC-PC are optimized utilizing load-pull simulations, as illustrated in Fig. 5-15, to

evaluate their best values that realize the highest PAE_{max} of the two-STC of the driver stage. The optimization process is performed with using lumped reactive components with realistic characteristics according to the employed 0.18-µm CMOS technology. Additionally, as shown in Fig. 5-16, the three commonly classical used compensation techniques, illustrated in Fig. 5-12, are optimized to compare their attained performances with the proposed technique.

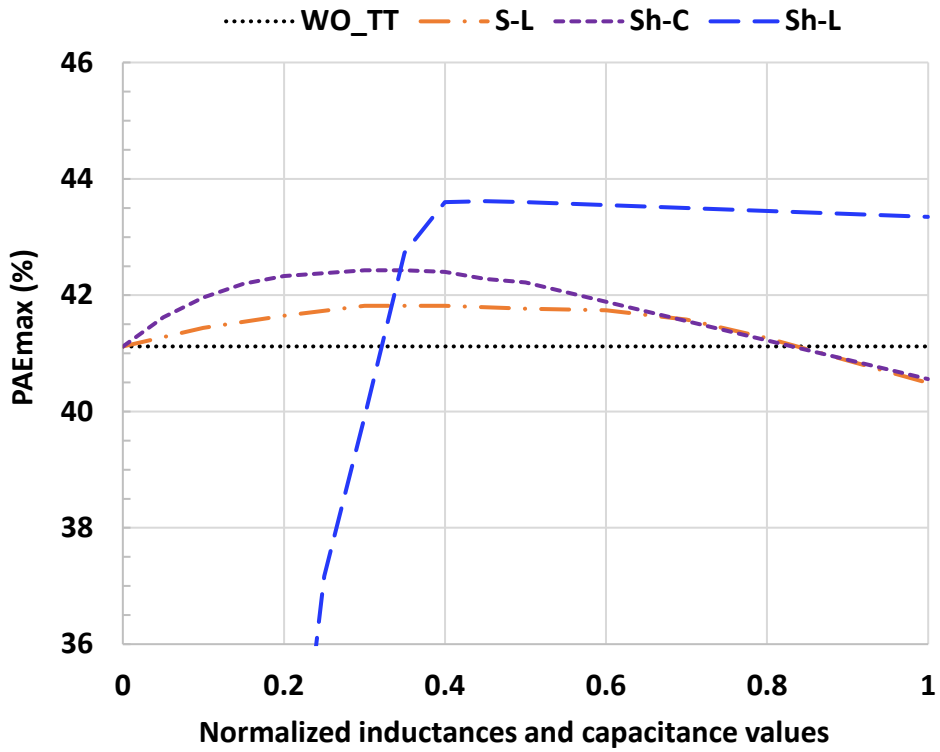


Fig. 5-16. Maximum PAE of the two-stage driver configuration achieved through optimization of the traditional techniques, including series inductance (normalized to 0.2 nH), shunt inductance (normalized to 1 nH), and shunt capacitance (normalized to 0.2 pF).

The suggested two-tunable LC-PC technique was found to be the most effective in improving the performance of the driver stage's two-STC, as shown in Fig. 5-15 and Fig. 5-16, when taking into account the impact of the capacitive feedbacked linearizer on the operating frequency. The superior performance of the LC-PC is attributed to its ability to compensate for both resistive and reactive mismatches, which results in the lowest simulated $\Delta\Phi_{ph}$, as illustrated in Fig. 5-17.

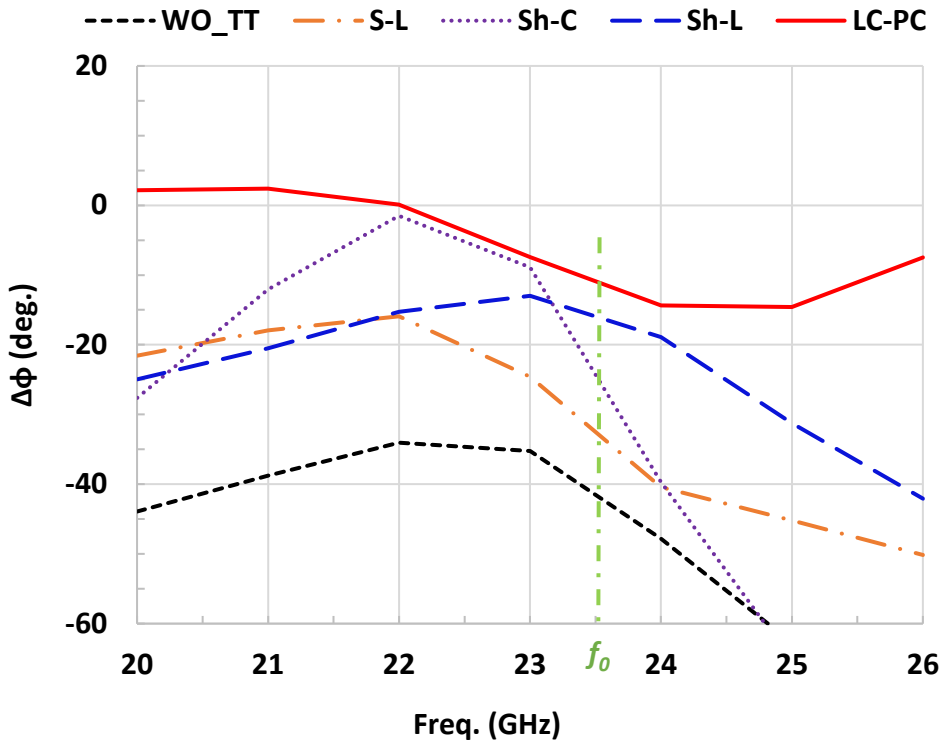


Fig. 5-17. Phase deviation between the source impedance of M_2 and the optimal output impedance of M_1 in the two-ST configuration of the driver stage with and without using optimized phase compensation techniques, as a function of operating frequency (f_0).

Instead of using the classical first-order techniques, the proposed LC-PC has a second-order low-pass filtering approach to improve its harmonic termination capability and reduce total harmonic distortions in the amplified transmitted signal, as illustrated in Fig. 5-18. The Sh-CTT method also requires higher inductance at the top drain node to compensate for capacitance loading, especially for a large number of stacked units. However, the proposed LC-PC technique is more sensitive to the values of the tuned reactive elements and is frequency-dependent, as demonstrated in Fig. 5-15. Therefore, it is crucial to correctly implement and optimize the designed cold-PC using an EM simulator to account for the mutual effects of surrounding components, as shown in Fig. 5-19.

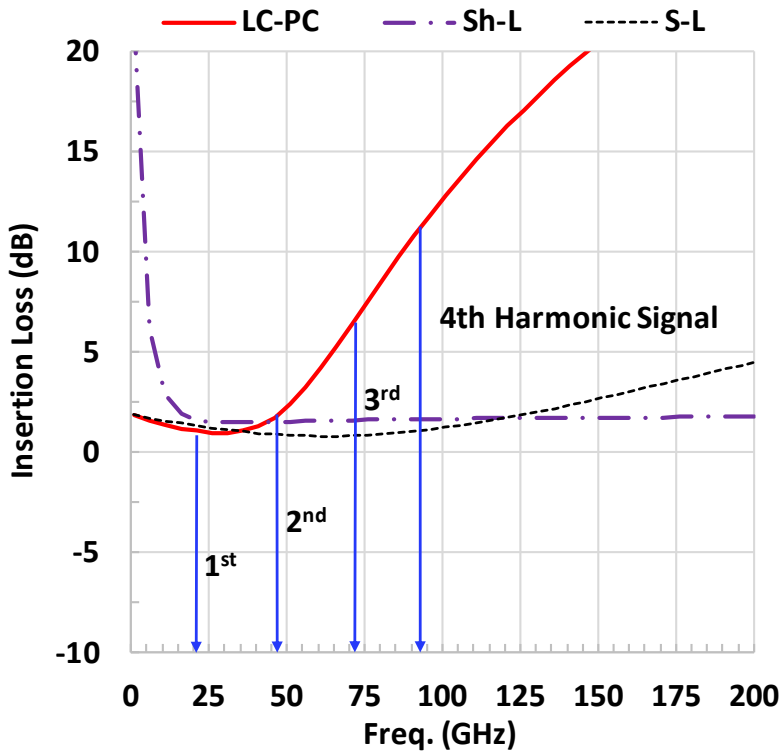


Fig. 5-18. Comparison between the harmonic termination behavior of the classical tunning techniques and the proposed one. The results are accomplished using the S-parameters test to calculate the insertion loss of the optimized circuits.

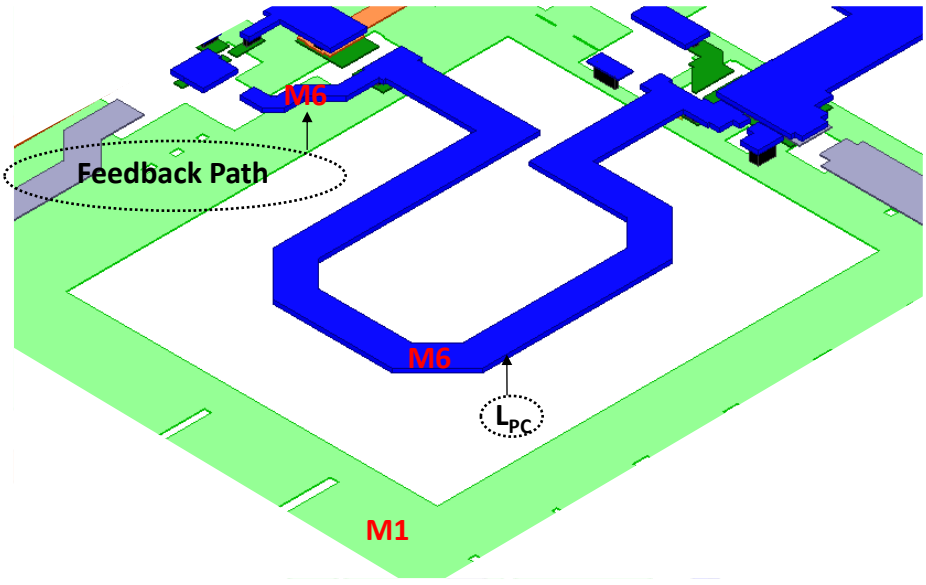


Fig. 5-19. Three-dimensional representation of the electromagnetic model of the feedbacked Cold-PC.

5.4. Implementation and Results

5.4.1. Fabrication and Measurement Setup

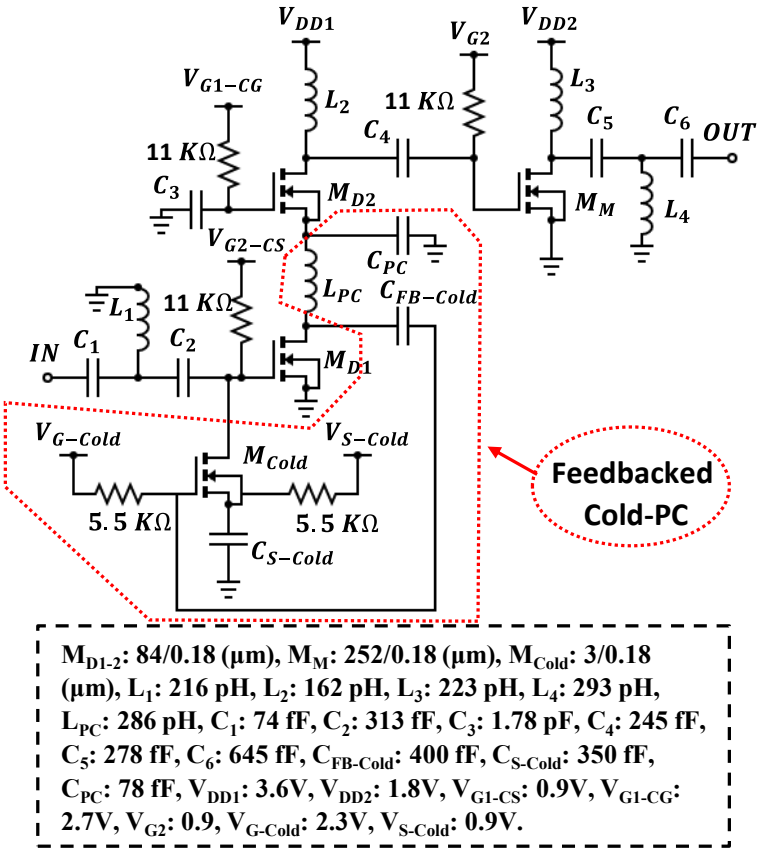


Fig. 5-20. Simplified schematic of the full designed PA with the feedbacked Cold-PC.

The implemented RF CMOS PA with the proposed capacitive feedbacked cold-PC linearizer and PAE enhancer was manufactured utilizing 0.18-µm CMOS technology, as illustrated in Fig. 5-20. The CMOS PA has a driver stage which consists of a two-STC with the designed feedbacked cold-PC that is connected to a supply dc voltage of 3.6 V while a CS wider transistor with a dc supply voltage of 1.8 V represents the PA's main stage. The fabricated chip, as shown in Fig. 5-21, consumes area around 0.582 mm^2 including the used RF and dc pads, which is measured on a probe station (CASCADE MICROTECH Summit 11000 M) with using *mm*-wave ground-signal-ground infinity probes connected with N5222A Keysight PNA network analyzer. For additional characterizing the improvement in the linearity of the fabricated K-band CMOS PA with modern and high PAPR modulated signals, the power amplifier is tested with a 64-QAM OFDM 5G-NR Downlink signal that usually has (9 – 12 dB) PAPR. The used modulated baseband 5G-NR signal

is generated by a Keysight M9505A arbitrary waveform generator and a raised-cosine shaped filter with 0.35 roll-off factor. Then, the baseband signal is upconverted to 23.5 GHz utilizing E8267D Keysight PSG vector signal generator and applied to the input port of the designed CMOS PA. The output of the manufactured PA is connected to a N9030B Keysight PXA signal analyzer equipped with 89600 VSA software and necessary RF applications including EVM optimization tools, which are used to analyze and measure the amplified 5G-NR modulated signal.

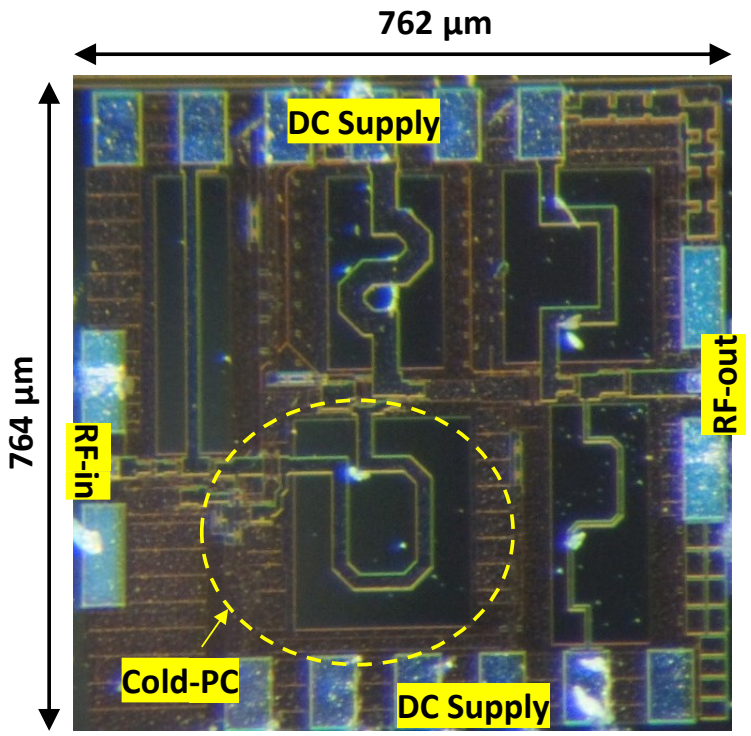


Fig. 5-21. Physical chip photograph of the PA design that utilizes a feedbacked Cold-PC.

5.4.2. S-Parameters and Power Measurement Results

The measured and post-layout simulated S-parameters, while the linearizer is turned on and turned off, are shown in Fig. 5-22. Where the BW_{3dB} of the manufactured PA is almost 3 GHz centered at 23.5 GHz. The measured AM-PM distortions of the implemented CMOS PA while the APD is in OFF-state and ON-state with changing the dc biasing voltages are shown in Fig. 5-23. Where tunning the biasing voltage of the gate terminal of the suggested used linearizer (V_{G-Cold}) would adjust the AM-PM distortion of the designed PA.

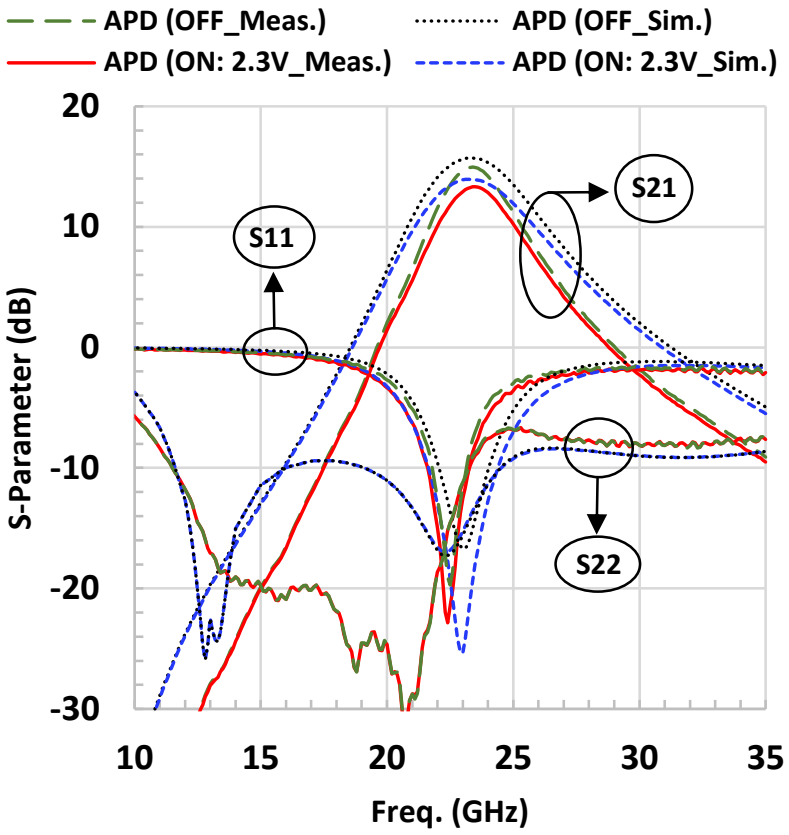


Fig. 5-22. Measured and post-layout simulated S-parameters of the fabricated PA.

However, the 2.8V case gives the smallest AM-PM distortions, it comes at the expense of maximizing the insertion loss of the linearizer and decreasing the achieved measured power gain. Hence, employing the linearizer biased by 2.3V gives the optimum trade-off performance in both AM-PM distortions and compression characteristics of the implemented RF PA compared with the case without utilizing the APD, as demonstrated in Fig. 5-23 and Fig. 5-24, respectively. The fabricated PA with the linearizer realizes an expansion of the measured OP_{1dB} by 2.5 dB (improvement by 78% from the original case), and an increase of its PAE by 7% (improvement by 72% from the original case) which is the highest improvement among the reported CMOS PAs. Also, almost a 1.5 dB difference between the OP_{1dB} and the output power point where the peak PAE occurs which are counted to be among the best reported performances of the *K*-band CMOS PAs.

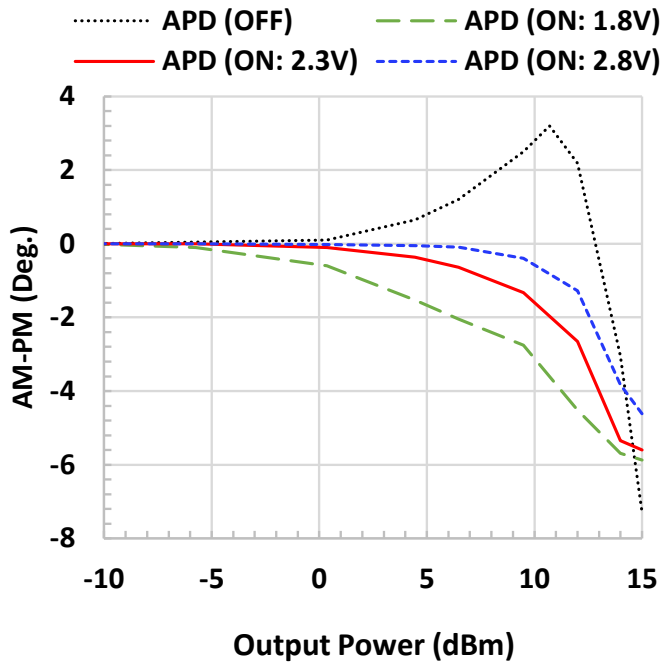


Fig. 5-23. Change in measured AM-PM distortion of the manufactured PA when the feedbacked Cold-PC is activated or deactivated at different bias voltages at the operating frequency of 23.5 GHz.

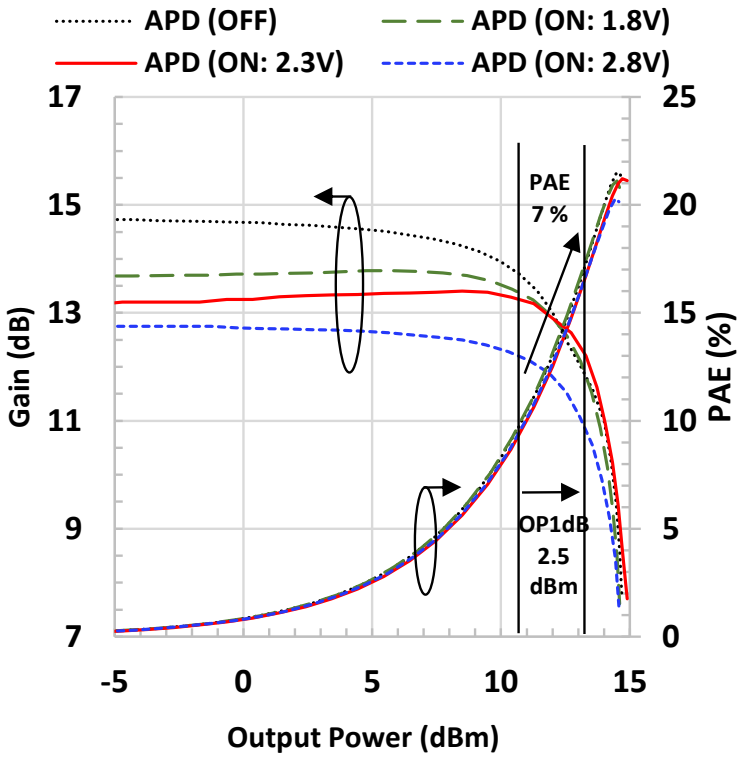


Fig. 5-24. Measured power gain and PAE of the manufactured CMOS PA while the APD is turned OFF and ON with various biasing voltages at the operating frequency of 23.5 GHz.

Table 5-1. COMPARISON OF RECENT K-BAND CMOS PA DESIGNS

Ref.	CMOS Tech. (nm)	Freq. (GHz)	VDD (V)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	OP_{1dB} Expansion (dB)	Peak PAE (%)	EVM (dB) for 64-QAM, BW, P_{out}	Total Area (mm^2)
[58]	65	28	2.2	18	18.5	17	-	27.3	-25, 800 MHz/s, 7.5 dBm	0.456
[53]		31	2.2	18.9	17.1	15*	1.8*	38.2	-25, 400 MHz/s, 9.6 dBm	0.47
[56]	**180**	23	1.8	10.2	19.8	17.5	1.5	17.5	-36, 8 MHz/s, 9.6 dBm	0.566
[80]		22	3.6	11.9	17.4	15.4	-	12	NR	0.4
[55]		24	3.6	9.3	16.6	14.6	1*	14	-36*, 1 MHz/s, 2.5 dBm	0.37+
[48]		20	3.6	12	16*	13.3*	-	16.4*	-25*, 400 MHz/s, 7.1* dBm	0.564
This Work		**23.5**	**3.6**	**13.4**	**15**	**13.4**	**2.5**	**21.2**	**-25, 400 MHz/s, 9.2 dBm** **-25, 400 MHz/s, 5.1 dBm**	**0.582 (0.38+)**

(-): There is no linearizer at the design, (*): graphically estimated, (+): active area without pads.

The results of the designed CMOS PA are compared with other *K*-band PAs that have been recently published and were also created using the same CMOS technology node, as presented in Table 5-1. The proposed capacitive feedbacked Cold-PC linearizer and PAE enhancer were used, which resulted in the highest reported PAE. Additionally, the performance of recently published

mm-wave CMOS PAs made with more advanced CMOS technology nodes are also included in the comparison.

5.4.3. Measured EVM and Linearity Improvement

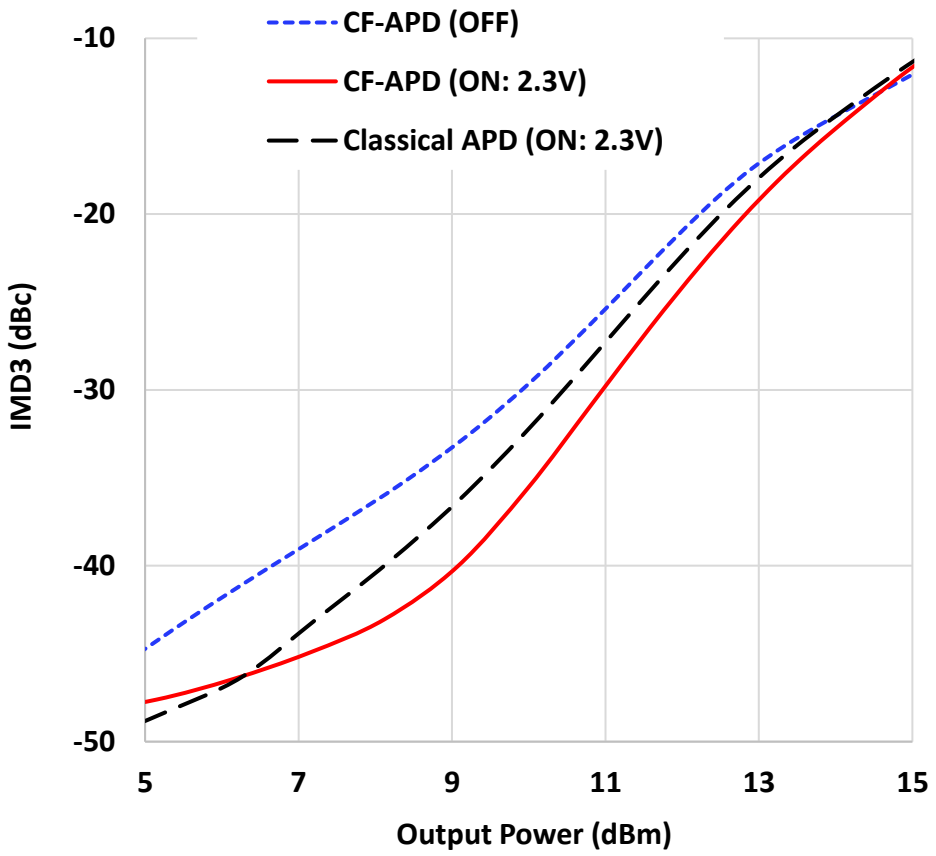


Fig. 5-25. Comparison of the post-layout simulated third-order intermodulation distortion between the proposed and classical APDs at a frequency spacing of 20 MHz.

Utilizing the suggested capacitive feedbacked APD decreases IMD3 and gives improved results compared with employing the classical APD, as illustrated in Fig. 5-25. Also, The linearity of a implemented RF PA can be measured using EVM, which takes into account both the magnitude and phase distortions of the amplified modulated signals. This is particularly important for RF implemented PAs that deal with high PAPR signals and complex modulation techniques, as they need to have higher linearity and lower signal distortions. As such, modern specifications like 3GPP-5G have strict EVM values to ensure proper signal delivery. The implemented CMOS PA was tested with a Downlink FR2 64-QAM OFDM 5G-NR modulated signal, that has a PAPR of about 10.5 dB and a bandwidth of 400 MHz, as shown in Fig. 5-26.

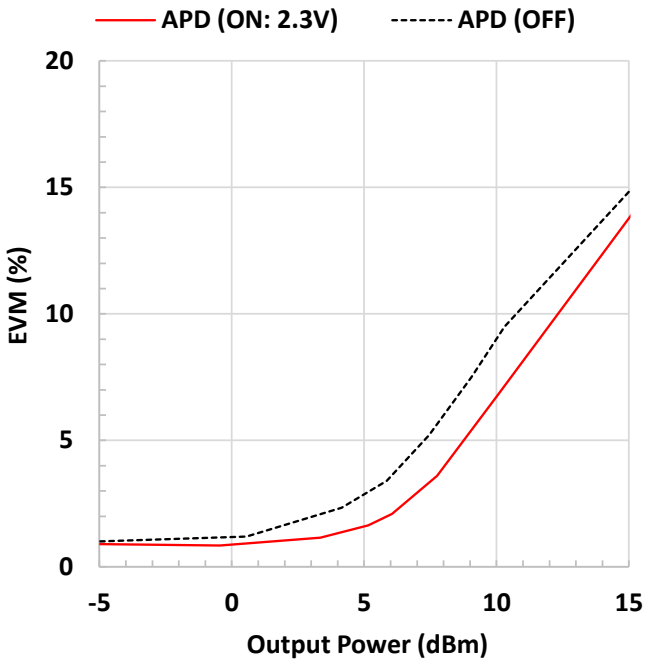


Fig. 5-26. EVM results of the 400 MHz 64-QAM 5G-NR Downlink FR2 signal at 23.5 GHz were measured in both the ON and OFF states of the APD.

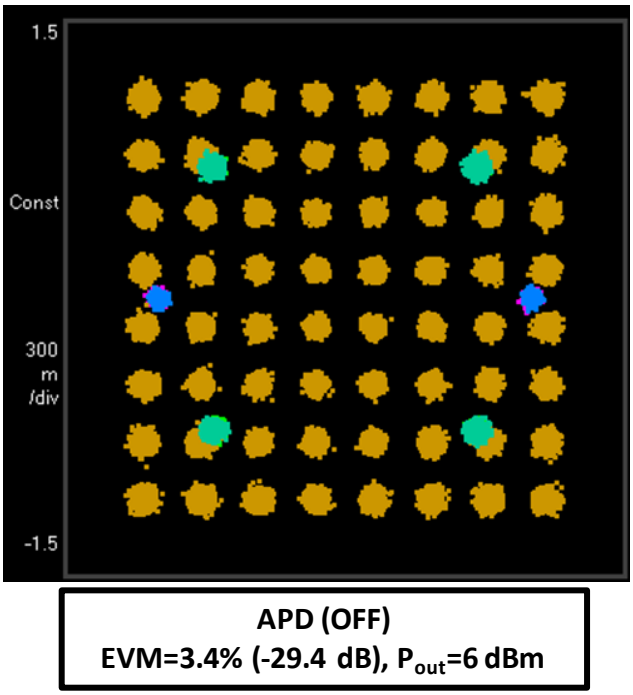


Fig. 5-27. Measured constellation diagram of the K-band PA when the APD is OFF.

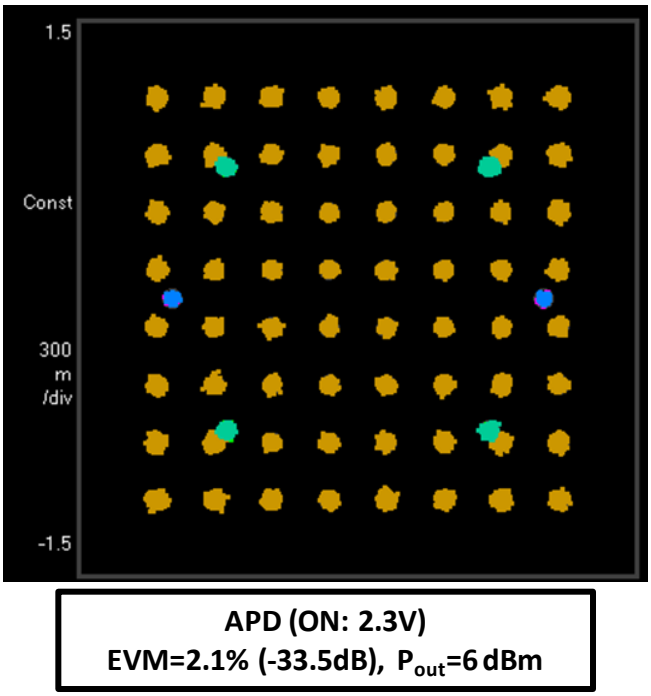


Fig. 5-28. Measured constellation diagram of the K-band PA when the APD is ON.

Using the introduced capacitive feedbacked APD, as illustrated in Fig. 5-26, reduces distortions of the amplified 5G-NR signal in terms of EVM and extends the linear output power. This is additionally demonstrated by the smaller signal distortions and lower EVM value (2.1%) in the output signal's constellation diagram when compared to not using the proposed linearizer (3.4%) at a similar output power level of around 6 dBm, as seen in Fig. 5-27 and Fig. 5-28. The implemented CMOS PA based on the capacitive feedbacked cold-PC also performs well compared to other reported *K*-band RF PAs and meets the requirements of 3GPP-5G wireless standards, as stated in Table 5-1.

5.5. Sub-6-GHz 5G High Linear Power Amplifier with the proposed Capacitive Feedbacked APD

In this section, the previously illustrated capacitive feedbacked APD is used for improving the linearity of the implemented RF CMOS PA, studying the effect of the cold-FET transistor width on its linear behavior in terms of the IMD at sub-6-GHz 5G applications. The fabricated PA with the cold-FET linearizer achieves at 5 GHz a power gain of 10.1 dB, a PAE of 31.9%, OP_{1dB} of 13.2 dBm, and saturated output power of 15.3 dBm while consumes chip area of 0.67 mm^2, including the pads. The proposed linearizer improves the measured OP_{1dB} and its PAE. Moreover,

the PA is tested with 5G-NR uplink 64-QAM signal. It achieves output power of 6.4 dBm at -25 dB of the measured error vector magnitude.

5.5.1. Circuit Implementation

The designed one-stage 5 GHz CMOS PA is implemented using two-stacked transistor configuration which achieves a good trade-off among the three compared parameters demonstrated in Fig. 5-29. Corresponding to the square-law transistor model, the cold-FET without employing any feedback criteria can be utilized as a voltage-controlled resistance, as illustrated in (5.2.1).

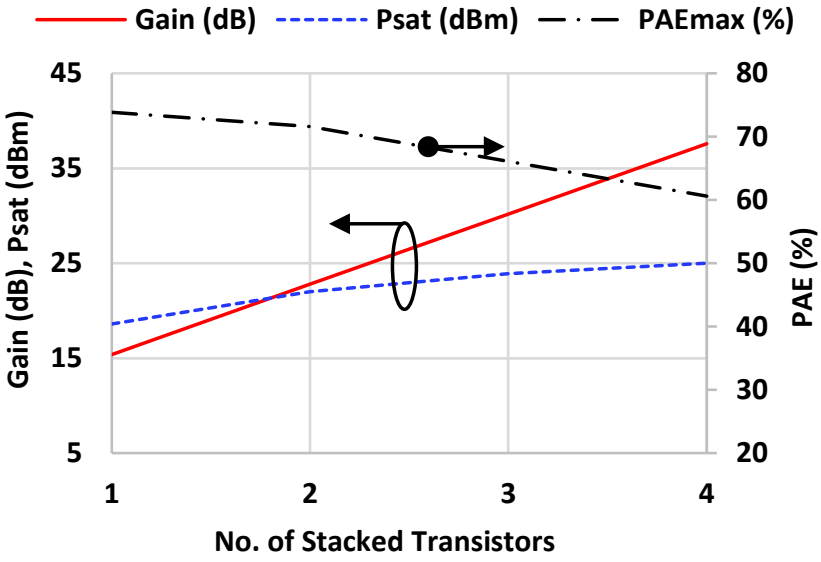


Fig. 5-29. The impact on maximum gain, PAE, and P_{sat} at 5 GHz of varying the number of the used transistors in the STCs as determined by S-parameter and load-pull simulations, with the drain-source voltage for every used transistor in the STCs held constant.

It is expected that, the performance of the designed APD would vary according to the width of the used cold FET and the accompanying parasitics alongside with the frequency of operation. One of the main parameters of studying the linearity of the designed RF PAs is the IMD3 and IMD5. Thus, the simulated performance of the IMD3 and IMD5 of the designed *C*-band PA is illustrated and compared according to the changes in the feedbacked cold FET width, as shown in Fig. 5-30. The used feedbacked cold-FET in the designed CMOS PA is selected to be 120/0.18 µm that realizes the best trade-off performance in terms of IMD3 and IMD5, as demonstrated in Fig. 5-30(a), Fig. 5-30(b), and Fig. 5-30(c).

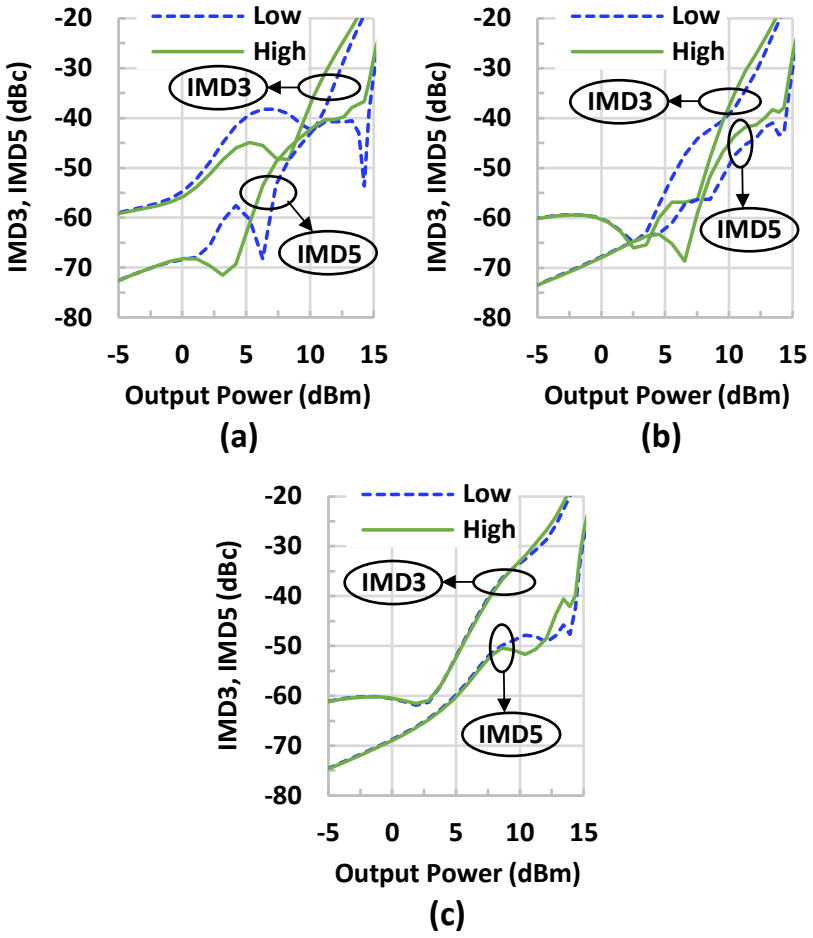


Fig. 5-30. Trade-offs variations of simulated IMD3 and IMD5 of the designed RF PA according to change of the feedbacked cold-FET width where the frequency spacing equals 5 MHz (a) 60 µm (b) 120µm (c) 240µm.

5.5.2. Implementation and Measured Results

The schematic view of the fabricated sub-6-GHz CMOS PA with utilizing the capacitive feedbacked APD (CF-APD) linearizer is illustrated in Fig. 5-31. The chip of the manufactured *C*-band RF PA using 0.18-µm CMOS bulk technology consumes chip area of 0.86*0.78 μm^2 including the pads, as shown in Fig. 5-32. The chip was measured on a probe station (CASCADE MICROTECH Summit 11000 M) with *mm*-wave ground-signal-ground infinity probes connected with N5222A Keysight PNA network analyzer. Then, for further characterizing the improvement in the linearity of the fabricated CMOS PA, as a result of utilizing the proposed linearizer, a high PAPR 5G-NR Uplink modulated baseband signal is used. This test signal is generated and

upconverted to the operating frequency by utilizing R&S SMCV100B vector signal generator with a raised-cosine shaped filter with 0.35 roll-off factor. The output port of the designed CMOS PA with the proposed APD is connected to R&S FSVA3030 signal and spectrum analyzer to measure the amplified modulated 5G-NR Uplink signal.

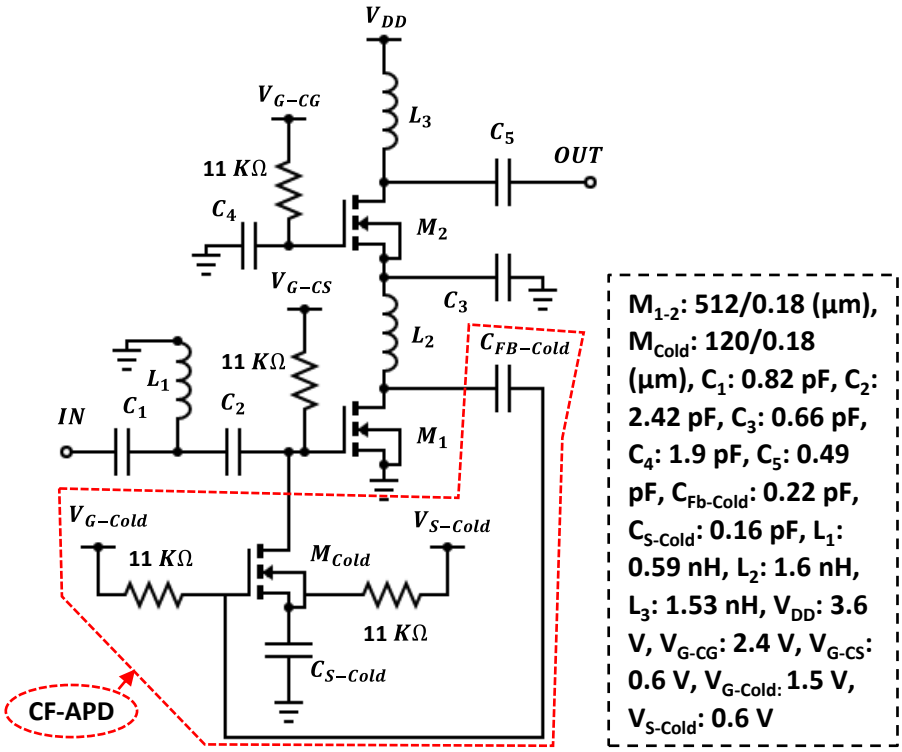


Fig. 5-31. Schematic of the implemented C-band PA with the CF-APD.

Fig. 5-33 demonstrates the simulated and the measured S-parameters while the introduced linearizer is in ON and OFF states. Where the BW_{3dB} of the proposed RF PA is approximately 1.4 GHz (4.2 GHz-5.6 GHz) that can be used for 5G's FR1 frequency band. The fabricated *C*-band CMOS PA with the CF-APD achieves a power gain of 10.1 dB at 5 GHz and a maximum PAE of 31.9%. Also, the designed RF PA with the linearizer extends the OP_{1dB} by approximately 1.5 dB and the PAE at the 1-dB compression point is increased by 6%, as shown in Fig. 5-34. For further investigating the enhancement occurred in the linear behavior of the PA, the EVM of a 100 MHz 64-QAM OFDM 5G-NR Uplink signal is measured in case of the APD is in ON and OFF states, as illustrated in Fig. 5-35. Where employing the CF-APD reduces the distortions of the measured output signal in terms of EVM distortions. Fig. 5-36 and Fig. 5-37 demonstrate that the constellation diagram of the amplified signal of about 5.5 dBm, in case of using the suggested

capacitive feedbacked linearizer, has low signal distortions and small EVM value (3.9%) compared with the case of without using any linearizer (6.2%).

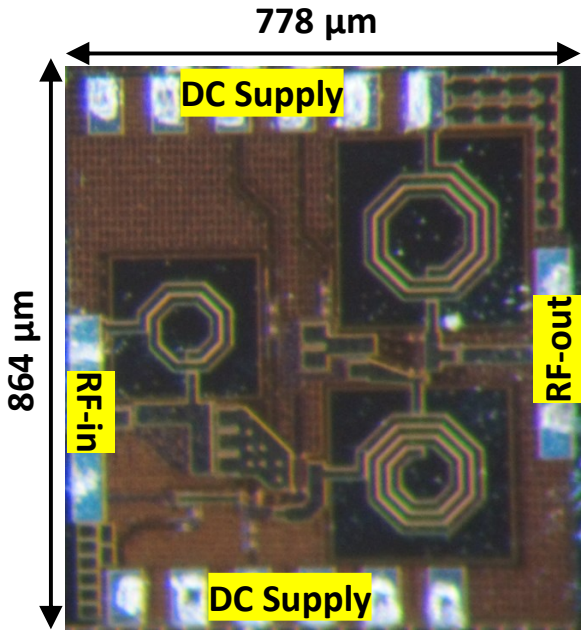


Fig. 5-32. Photograph of the fabricated chip of the designed C-band PA.

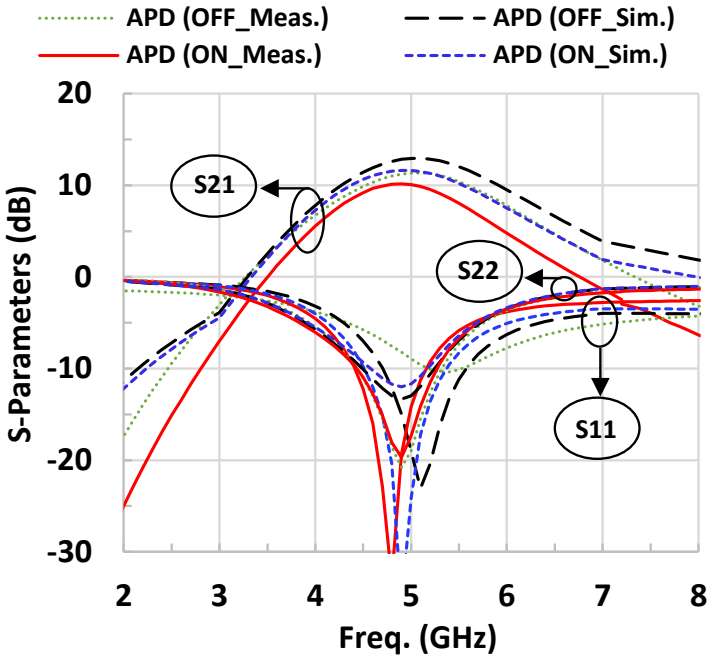


Fig. 5-33. Measured and post-layout simulated S-parameters of the designed PA.

The designed PA with the CF-APD, as shown in Table 5-2, achieves the highest PAE compared with the reported *C*-band PAs using the same technology node and satisfies the stringent requirements of the 3GPP-5G wireless standards. Moreover, the gain and the saturated output power can be improved, as reported in Table 5-2, by employing advanced CMOS technologies or using multi-stage or parallel designs that will consume additional chip areas.

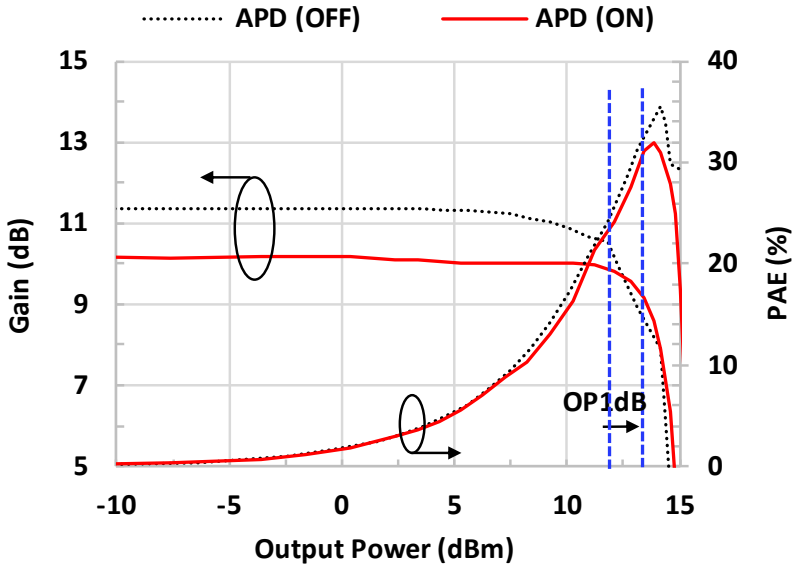


Fig. 5-34. Measured gain and PAE while the APD cold FET is in OFF and ON states.

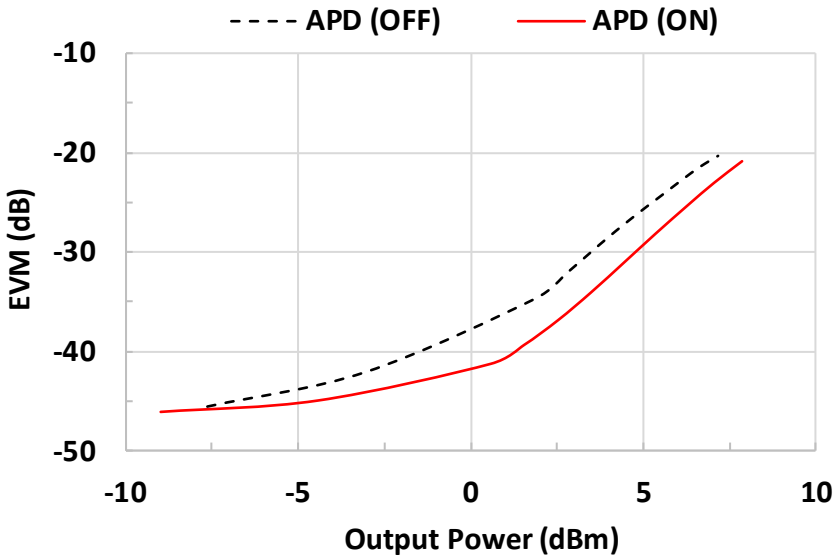
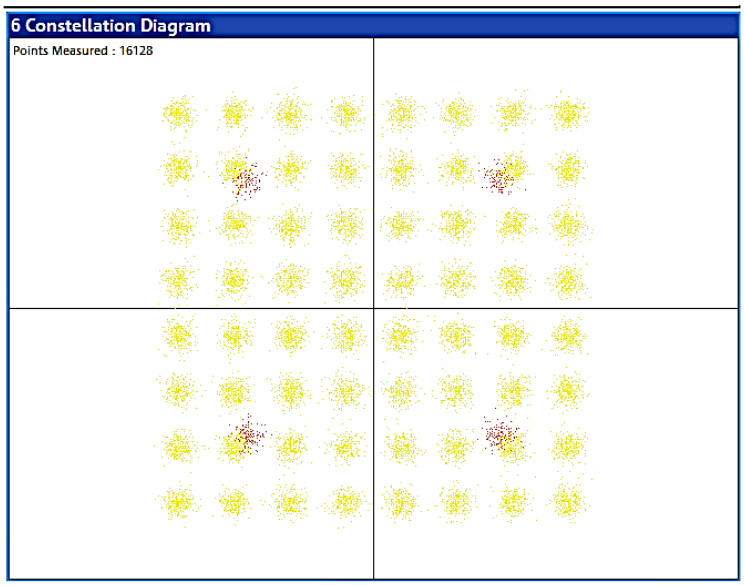
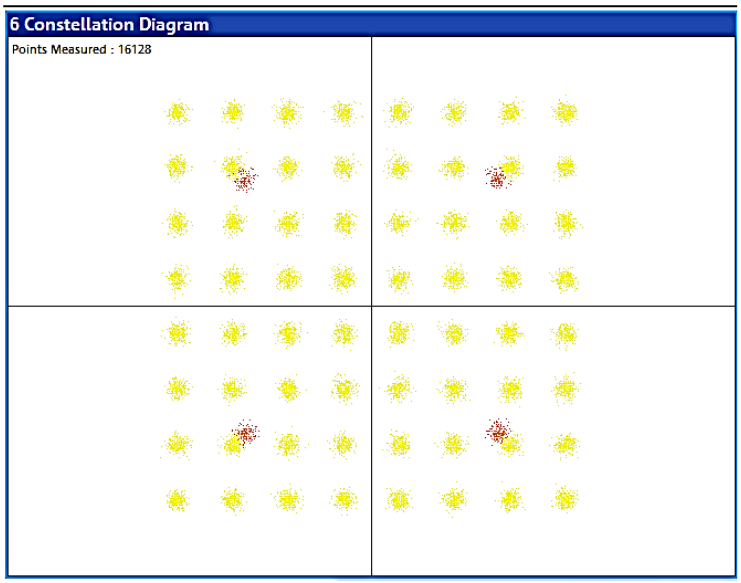


Fig. 5-35. EVM results of the 100 MHz 64-QAM 5G-NR Uplink signal at 5 GHz were measured in both the ON and OFF states of the APD.



APD (OFF)
EVM =6.2% (-24.2 dB), Pout=5.5 dBm

Fig. 5-36. Measured constellation diagram of the C-band PA when the APD is OFF.



APD (ON)
EVM =3.9% (-28.2 dB), Pout=5.3 dBm

Fig. 5-37. Measured constellation diagram of the C-band PA when the APD is ON.

Table 5-2. COMPARISON BETWEEN RECENT C-BAND REPORTED PA DESIGNS

Ref.	**This Work**	[81]	[82]	[83]
CMOS Tech (nm)	**180**	180	180	180
Freq. (GHz)	**5**	5.2	5.2	6
No. of Stages	**1-Stage + APD**	2-Stage + P. Com.	1-Stage + P. Com.	2-Stage
Gain (dB)	**10.1**	30.8	13.4	14
P_{sat} (dBm)	**15.3**	30.1	27.6	4
P_{1dB} (dBm)	**13.2**	24.3	23.5	2
Peak PAE (%)	**31.9**	22.2	19.2	10
EVM (dB) for 64-QAM, BW, P_{out}	**-25, 100 MHz/s, 6.4 dBm**	-25, 20 MHz/s, 19.8 dBm	-25, 20 MHz/s, 16.6 dBm	NR
Total Area (mm^2)	**0.67**	2.83	1.2	0.77

5.6. Conclusion

This chapter has introduced an effective way to enhance the linear behavior of the CMOS RF PAs where:

- The proposed capacitive feedback cold-PC technique improves linearity and PAE while minimizing chip area overhead. The simple structure avoids low Q-factor on-chip transformers. The two-stage K-band CMOS PA with the APD linearizer has been tested with a 400 MHz 5G-NR 64-QAM OFDM Downlink signal and achieved improved EVM compared to the OFF-state of the APD, meeting 3GPP-5G specifications. The proposed linearizer also resulted in a 2.5 dB increase in OP_{1dB} and 7% increase in PAE, which are the highest reported improvements in K-band RF PAs, to the best of authors' knowledge. The total chip area used for the manufactured K-band PA is 0.58 mm^2 with RF and DC pads included.
- Additionally, the designed one-stage *C*-band CMSO PA with the feedbacked linearizer has enhanced both the OP_{1dB} and its PAE by around 1.5 dB and 6%. Also, when the fabricated PA has been tested with a 100 MHz 5G-NR 64-QAM OFDM Uplink signal, the PA has achieved an enhancement in the measured EVM distortions in case of using the proposed capacitive feedbacked linearizer compared with the case while the

linearizer was OFF. The fabricated C-band CMOS PA consumes a total chip area of 0.67 mm^2 including the pads.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

The thesis has introduced different techniques for enhancing some of the trade-offs parameters of RF CMOS PAs such as efficiency, operating bandwidth, linearity that can be used in modern wireless communication systems. It is worthy to mention that the required specifications can vary depending on the specific application and system requirements. The designed PAs, in this work, are implemented using 0.18-µm CMOS technology and meet the frequency specifications for working in K-band radar systems and C-band 5G applications. The designed CMOS PAs give competitive performances compared with the reported published papers, especially which use the same technology node.

6.1. Conclusions

Main contributions of this dissertation are summarized as follows:

- A two-stage wideband RF PA using an introduced superimposed staggered technique and DGS inductors is presented in 0.18-µm CMOS technology. The main stage is designed to have a wideband peaking response at the center frequency, while a superimposed dual-band driver stage is designed to achieve a flat gain response of the designed PA across the entire bandwidth. DGS inductors are used to improve the overall PAE by minimizing the insertion losses of the matching circuits. The resulting PA has a power gain of 12 dB and occupies a chip area of 0.564 mm2. Additionally, it has a P_{sat} of 16.6 dBm at the center frequency. The proposed wideband RF PA that uses the superimposed staggered technique and DGS inductors has low group delay variations, a wide fractional bandwidth of 44.4%, and a high PAE of 18.7%. Additionally, it has minimal EVM distortion, making it suitable for use in current wireless applications.
- A new method that utilizes a three-adjustable low-pass π-phase compensator is proposed for a K-band CMOS PA to address the phase shift problem at intermediate nodes of STCs and reduce the impact of high harmonic signals, resulting in an increase in overall PAE of the PA. The PA is designed with two stages, including a driver stage and main stage using

2-STCs in 0.18-µm CMOS technology. The resulting PA achieved a power gain of 12.8 dB at 23 GHz, a maximum PAE of 18.3%, an OP_{1dB} of 14.1 dBm, and a P_{sat} of 16.0 dBm using a chip area of 0.604 mm2 including the utilized pads.

- A two-stage PA that operates in the K-band frequency range and uses 0.18-µm CMOS technology is presented. The PA includes a capacitive-feedbacked Cold-PC linearizer and PAE enhancer. The Cold-PC has two parts: a cold-FET analog-pre-distorter (APD) with a new capacitive feedback technique that improves the linearity of the PA and reduces insertion loss while minimizing chip area, and a low-pass two-tunable LC-PC that addresses the phase shift problem at intermediate nodes, resulting in an enhancement of the PAE. The implemented PA has a maximum measured PAE of 21.2%, an OP_{1dB} of 13.4 dBm, and P_{sat} of 15 dBm at 23.5 GHz, consuming an overall chip area of 0.58 mm^2. Using the proposed Cold-PC led to a decrease in the measured EVM distortions of a 400-MHz 5G-NR 64-QAM amplified modulated signal and an increase in the OP_{1dB} and PAE by 2.5 dB and 7%, respectively (78% and 72% enhancement from the original case, respectively), which is the highest reported enhancement of linearizers of K-band PAs to the best of the authors' knowledge.
- A *C*-band CMOS PA with a CF-APD, designed in 0.18-µm CMOS technology, is proposed. The effect of changing the width of the employed Cold-FET on the PA's linear behavior is introduced at 5 GHz frequency band. The fabricated PA with the cold-FET linearizer achieves at 5 GHz a power gain of 10.1 dB, a maximum PAE of 31.9%, an OP_{1dB} of 13.2 dBm, and P_{sat} of 15.3 dBm while consumes chip area of 0.67 mm^2, including the pads. The proposed CF-APD improves the measured OP_{1dB} and its PAE. Moreover, the PA has achieved smaller EVM distortions, when it is tested with 100 MHz bandwidth of 5G-NR 64-QAM signal, to be utilized in sub-6-GHz 5G applications.

6.2. Future Work

Future work may include the possible following points:

- Demanding of enhancing the efficiency at deeper back-off power levels are significantly increased to satisfy the today's market requirements. Topologies like Doherty and out-phasing PAs are usually employed in such application. Designing such topologies and

optimizing the trade-offs between them is an interesting and challenging research point to work with especially at *mm*-wave bands using advanced CMOS technology nodes for 5G and beyond 5G applications.

- Using CMOS technologies usually have limited output power capability compared with some of the modern utilized market technologies such as GaN PAs that would limit the use of these designed PAs for targeting higher distances especially in radar and other communication systems. Thus, working for designing such off-chip GaN PAs that delivers high output power levels will be challenging and interesting at higher RF frequency bands.

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LIST OF PUBLICATIONS

- **Journals/Transactions/Letters**

[1] **O. Z. Alngar**, A. Barakat, R. K. Pokharel, "High PAE CMOS Power Amplifier with 44.4% FBW Using Superimposed Dual-Band Configuration and DGS Inductors," *IEEE Microwave Wireless Components Letters, vol. 32, no. 12, pp. 1423–1426, Dec. 2022.*

[2] **O. Z. Alngar**, A. Barakat, and R. K. Pokharel, "Capacitive Feedbacked Cold-Phase Compensator Analog Pre-Distorter and PAE Enhancer for K-Band CMOS PAs," *IEEE Transactions on Circuits and Systems I (Regular Paper), vol. 69, no. 12, pp. 4969–4980, Dec. 2022.*

- **Conferences/Proceedings**

[3] **O. Z. Alngar**, A. Barakat, R. K. Pokharel, " A High PAE Stacked K-band Power Amplifier Using π-Phase Compensation Technique," in *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pp. 42-44, 2022.

[4] **O. Z. Alngar**, A. Barakat, R. K. Pokharel, " A Highly Linear CMOS Power Amplifier with Feedbacked Analog Pre-Distorter for Sub-6-GHz 5G Communications," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, (Submitted), 2023.