Thermal Deformation Analysis of Flip-Chip Packages by Moiré Interferometry and FEA

Morita, Yasuyuki
Graduate School, Kyushu University

新川, 和夫
Research Institute for Applied Mechanics Kyushu University

TODO, Mitsugu
Research Institute for Applied Mechanics Kyushu University

UENO, Yoichi
Graduate School, Kyushu University

他

https://doi.org/10.15017/6768412

出版情報：九州大学応用力学研究所所報. 121, pp.111-114, 2001-09. Research Institute for Applied Mechanics, Kyushu University
バージョン：
権利関係：

Thermal Deformation Analysis of Flip-Chip Packages by Moiré Interferometry and FEA

Yasuyuki MORITA*1, Kazuo ARAKAWA*2, Mitsugu TODO*2,
Yoichi UENO*1, Kiyoshi TAKAHASHI*2 and Masayuki KANETO*3
E-mail of corresponding author: *morita@riam.kyushu-u.ac.jp*

(Received July 30, 2001)

Abstract

Moiré interferometry technique was applied to the thermo-mechanical analysis of flip-chip packages. Thermal deformations of two kinds of flip-chip structures, no-underfill and underfill flip-chip packages, were studied to understand the macroscopic effect of underfill. The experimental results showed that there was no big difference in the global thermal deformations between the two kinds of flip-chip structures except microscopic deformations around the edges of silicon chip. The thermal deformations of the flip-chip packages were also simulated by finite element analysis (FEA) to compare with the experimental results. The FEA results gave a good agreement with the u displacement field experimentally obtained, but a big difference with the v displacement field.

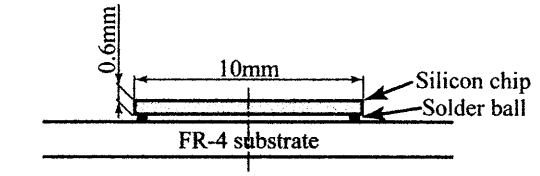
Key words : *Electronic Device, Thermal Deformation, Optical Measurement, Moiré Interferometry, Flip-Chip, Underfill, Coefficient of Thermal Expansion (CTE), Finite Element Analysis (FEA)*

1. Introduction

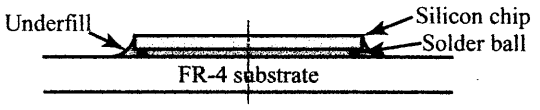
With the increasing demand for high mount density in electronic products and systems, flip-chip packages (see Fig.1) are drawing attention in microelectronics industries because of their simplicity, smallness, lightness and so on. Reliability of flip-chip packages is directly related to the degree of thermal stresses caused by the mismatch of coefficients of thermal expansion (CTE) between the different materials that construct the flip-chip package and assemblies. Therefore, it is important to evaluate the thermally induced stresses in controlling the structural reliability of flip-chip packages. Thermal deformations of conventional electronic packages, such as QFPs (Quad Flat Packages) and CSPs (Chip Size Packages), have been studied well from experimental and numerical points of view[1)~6)]. However, thermal deformation of flip-chip packages has not been studied thoroughly yet.

In most cases, underfill is usually introduced into a gap between the silicon chip and the substrate. It has been reported that the role of underfill is to adhere the chip to the substrate and to encapsulate the gap. Another role is to relax the CTE mismatch between them. However, it has not yet been fully verified experimentally how the underfill influences the thermal deformations of the package.

The aim of this study is to understand the macroscopic effect of underfill on the thermal deformations of flip-chip packages. A thermal loading was applied by cooling the packages from an elevated temperature 100℃ to room temperature 25℃. The thermal deformations were measured by using moiré interferometry, which is a high-sensitivity whole-field method for in-plane displacement measurements[7)]. Finite element analysis (FEA) was also performed to simulate the thermal deformations of the flip-chip packages, and the results were compared with the experimental results.



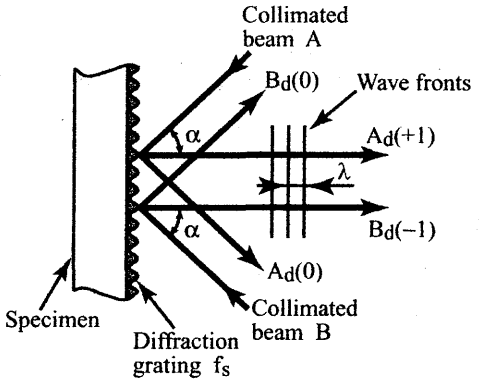
(a) No-underfill flip-chip



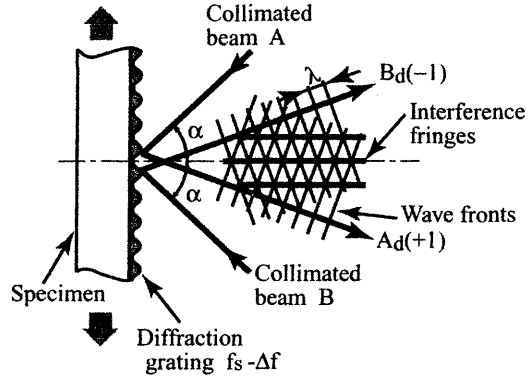
(b) Underfill flip-chip

Fig.1 Cross sections of flip-chip packages

*1 Graduate School, Kyushu University
*2 Research Institute for Applied Mechanics, Kyushu University
*3 Nitto Denko Corporation



(a) Before deformation of specimen



(b) After deformation of specimen

Fig.2 Principle of moiré interferometry

2. Experimental Method

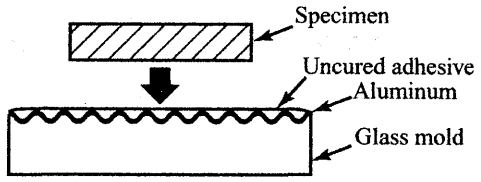
2. 1 Moiré Interferometry

The principle of moiré interferometry is shown schematically in Fig.2, where (a) and (b) illustrate the optics before and after specimen deformation, respectively. A fine diffraction grating is replicated on a specimen surface at the testing area. This grating, called specimen grating, is usually orthogonal cross-lined grating. If collimated coherent beams A and B are incident at an angle α given by

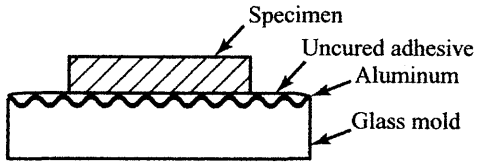
$$\alpha = sin^{-1}(f_s \lambda) \qquad (1)$$

where f_s is the spatial frequency of the specimen grating and λ is the wavelength of the laser beam, 1st-order diffracted beams A_d and B_d are generated perpendicular to the specimen surface. The wave fronts of these diffracted beams are parallel to the specimen surface, so that the beams do not interfere each other.

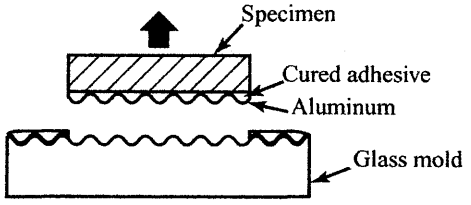
The specimen grating is deformed together with the specimen under an applied mechanical or thermal loading (see Fig.2 (b)). Therefore, the deformation of the grating represents the deformation of the specimen. Due to the specimen deformation, the spatial frequency of the grating changes. Thus, the directions of the two diffracted beams A_d and B_d change respectively, so that



(a) Spread of adhesive at 100 ℃



(b) Cast at 100 ℃



(c) Separation at room temperature

Fig.3 Cast of diffraction grating on specimen

the beams interfere with each other and produce moiré fringes. The *m-th* order moiré fringe indicates equi-displacement line. The displacement u is determined by the following equation:

$$u = m/2f_s \qquad (2)$$

2. 2 Specimens and Experimental Procedure

Figure 1 shows the cross sections of two kinds of flip-chip packages, no-underfill and underfill, where the silicon chip is connected with the FR-4 substrate by solder balls electrically. The size of the silicon chip is $10 \times 15 \times 0.6$mm. The diameter of the solder balls is 0.1mm. To ensure a two-dimensional deformation, specimens of 2mm thickness were made by slicing the flip-chip packages in the direction of the thickness.

The procedure shown in Fig.3 was used to replicate a cross-lined grating of 1200 lines/mm on the specimen at an elevated temperature 100℃. First, a ULE (Ultra Low Expansion) glass grating mold coated with thin aluminum layer was prepared. Second, Epoxy adhesive was spread thinly on the mold surface (see Fig.3 (a)). Third, the specimen and the mold were pressed together and maintained at 100℃ until the adhesive was cured (see Fig.3 (b)). Finally, the specimen was separated from the mold at room temperature 25℃ (see Fig.3 (c)). Since the specimen was cooled from 100℃ to 25℃, the grating profile on the specimen surface had the information of the thermal difference $\Delta T = -75$℃.

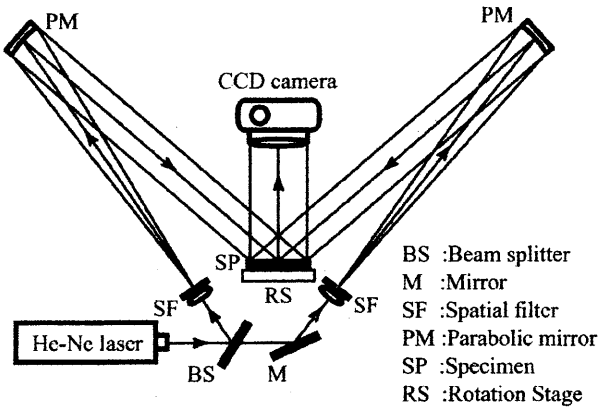


Fig.4 Optical arrangement for moiré interferometry

The optical arrangement for moiré interferometry is shown in Fig.4. Two-beam moiré setup was used to determine u displacement field. v displacement field was observed by rotating the specimen at an angle of 90 deg.

3. Experimental Results

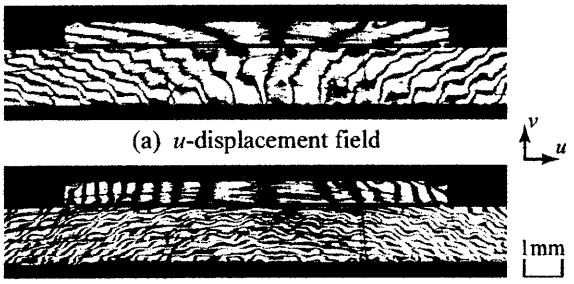
Moiré fringe patterns of the no-underfill and underfill flip-chip packages are shown in Figs.5 and 6, respectively. Each moiré interference fringe represents a constant displacement with a sensitivity of 417 nm/fringe.

The symmetric moiré patterns in Figs.5 and 6 suggest that the flip-chip packages deformed symmetrically. In the silicon chip with low CTE, coarse fringe patterns, i.e. small displacements, were obtained. Different numbers of fringes can be seen at the upper and lower surface of the silicon chip, indicating that the deformation of the silicon chip is influenced by the substrate with high CTE. In the substrate, on the other hand, dense fringe patterns can be seen. This indicates the displacement of the substrate was much larger. Zigzag fringe patterns in the substrate were not caused by optical noise. This is caused by the natures of FR-4 substrate, layered composites of glass-fiber/epoxy with different CTEs.

No big difference can be seen in the global fringe patterns between the no-underfill and underfill flip-chip packages. To study the effect of the underfill precisely, microscopic deformations around the solder balls have to be examined.

4. FEA Results

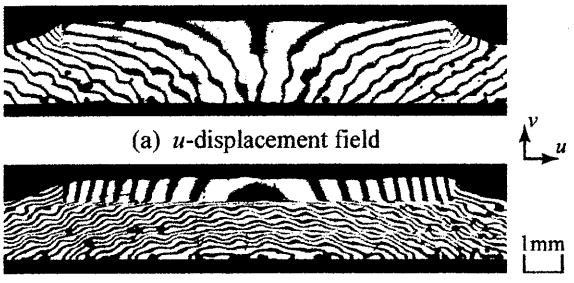
Finite element analysis (FEA) was performed to simulate the thermal deformations of the flip-chip packages. For simplicity, two dimensional stress condition and linear elastic material properties were assumed for the structures of the packages. The structures were divided into 6 nodes and triangular elements, and the material properties are shown in Table 1[1),8)~10)]. The FEA results are shown in Figs.7 and 8. To



(a) u-displacement field

(b) v-displacement field

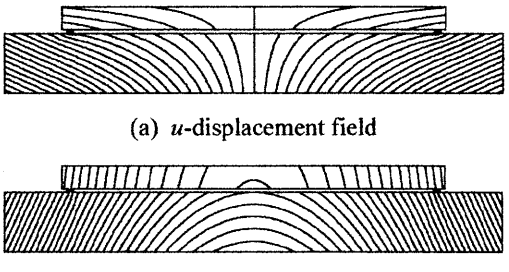
Fig.5 Moiré fringe patterns of no-undefill flip-chip package



(a) u-displacement field

(b) v-displacement field

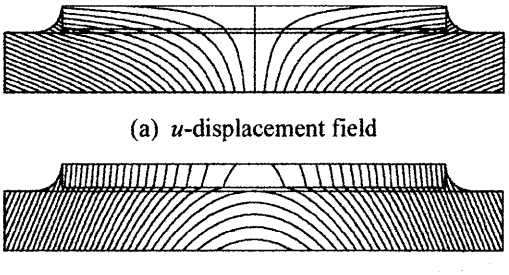
Fig.6 Moiré fringe patterns of underfill flip-chip package



(a) u-displacement field

(b) v-displacement field

Fig.7 Displacement fields of no-undefill flip-chip package by FEA



(a) u-displacement field

(b) v-displacement field

Fig.8 Displacement fields of underfill flip-chip package by FEA

Table 1 Material properties in FEA

	CTE [ppm/℃]	Young's modulus [GPa]	Poisson's ratio
Silicon chip	3.50	130	0.280
FR-4	17.0	12.0	0.165
Solder ball	24.7	37.4	0.410
Underfill	22.0	10.5	0.261

make a comparison with the experimental results, the displacements are represented by lines with the intervals 417nm.

Figure 9 exaggeratedly shows the difference of the macroscopic thermal deformations between the two flip-chip packages. Different curvatures can be seen in the silicon chip and the substrate without underfill. The similar curvatures are illustrated when the silicon chip is underfilled.

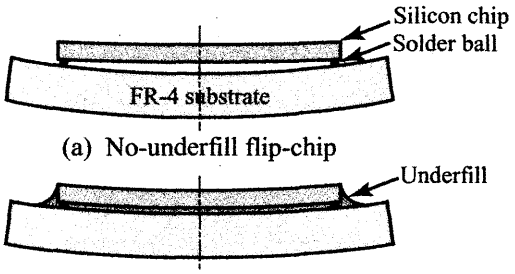
5. Discussion

The FEA results were compared with the experimental results to examine its validity. A good agreement was obtained for the u displacement fields as shown in Figs.5－8. The assumptions employed in the FEA are validated for the u displacements. However, there was a big discrepancy in the v displacement fields especially in the substrate. This may be primarily due to the anisotropic and heterogeneous natures of FR-4. Therefore, these natures should be included to analyze the deformation of the substrate quantitatively.

The FEA results suggested that there existed a difference in the curvatures of the silicon chip and the substrate without underfill. However, such difference was not obtained in the experimental results. This reason can be ascribable to the assumptions employed in the FEA especially for the material property of FR-4. Hence, to analyze the thermal deformations of flip-chip packages and the effect of underfill precisely, the material property of the FR-4 substrate has to be determined from microscopic viewpoint.

6. Conclusions

The thermal deformations of two kinds of the flip-chip packages, without underfill and with underfill, were studied by moiré interferometry. A thermal loading was applied by cooling the specimens from an elevated temperature 100℃ to room temperature 25℃. Moiré fringes were obtained to determine the u and v displacement fields. The macroscopic effect of underfill was examined. FEA was also conducted and the



(a) No-underfill flip-chip

(b) Underfill flip-chip

Fig.9 Schematic thermal deformations of flip-chip packages by FEA

following conclusions were obtained:

(1) A big difference cannot be observed in the global thermal deformations of the no-underfill and underfill flip-chip packages. The microscopic effect of underfill should be examined more precisely by measuring the fringe patterns around the edges of the silicon chip.

(2) The FEA results agreed well with the u displacement fields experimentally obtained in the no-underfill and underfill flip-chip packages. However, there was a discrepancy in the v displacement fields experimentally obtained, especially in the area of the FR-4 substrate. To predict the v displacement field, material property of FR-4 substrate should be determined more accurately.

References

1) Morita, Y., Arakawa, K., Todo, M., Yamada, S., Ueno, Y. and Takahashi, K., *Proc. of the First Ann. Meet. of JSEM*, No.1, (2001), 191-194.(in Japanese)
2) Arakawa, K., Todo, M., Morita, Y. and Yamada, S., *Proc. of the First Ann. Meet. of JSEM*, No.1, (2001), 113-116.(in Japanese)
3) Arakawa, K., Todo, M., Yamada, S., Morita, Y. and Takahashi, K., *Proc. of the Ann. Meet. of JSME / MMD*, No.**00**-19,(2000), 537-538.(in Japanese)
4) Ham, S. J. and Lee, S. B., *Proc. of the SEM IX Int. Cong. on Exp. Mech.*, (2000), 738-739.
5) Zou, D., Lu, M. and Liu, S., *Adv. In Electronic Packaging*, ASME, **19**-1, (1997), 1191-1196.
6) Han, B. and Guo, Y., *J. of Electronic Packaging*, **117**, (1995), 185-191.
7) Post, D., Han, B. and Ifju, P., *High Sensitivity Moiré*, (1994), Springer-Verlag, New York.
8) Nakamura, K., Inoue, Y., Nagasawa, M., Okeyui, K., Miyake, K. and Sugimoto, M., *6th Symposium on Microjoining and Assembly Technology in Electronics*, (2000), 23-28.(in Japanese)
9) Miller, M. R. and Ho, P. S., *Proc. of the SEM IX Int. Cong. on Exp. Mech.*, (2000), 523-525.
10) Yu, Q., Shiratori, M. and Sakairi, M., *Proc. of the Ann. Meet. of JSME / MMD*, No.**00**-19, (2000), 521-522.(in Japanese)