

SystemMorph: AnSoC Framework for Adaptive Dynamic Optimization Systems

Noori, Hamid
Department of Informatics, Kyushu University

Eshima, Kazuhito
Department of Informatics, Kyushu University

Fujii, Yousuke
Department of Informatics, Kyushu University

Yoshida, Makoto
Fukuoka Industry, Science & Technology Foundation

他

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Hamid Noori †, Kazuhito Eshima†, Yousuke Fujii†, Makoto
Yoshida††, Takeshi Soga††, Norifumi Yoshimatsu††, Takanori
Hayashida† & Kazuaki Murakami†

†Department of Informatics, Kyushu University
††Fukuoka Industry, Science & Technology Foundation
E-mail: †arch-systemorph@c.csce.kyushu-u.ac.jp,
††ngarch@fleets.jp

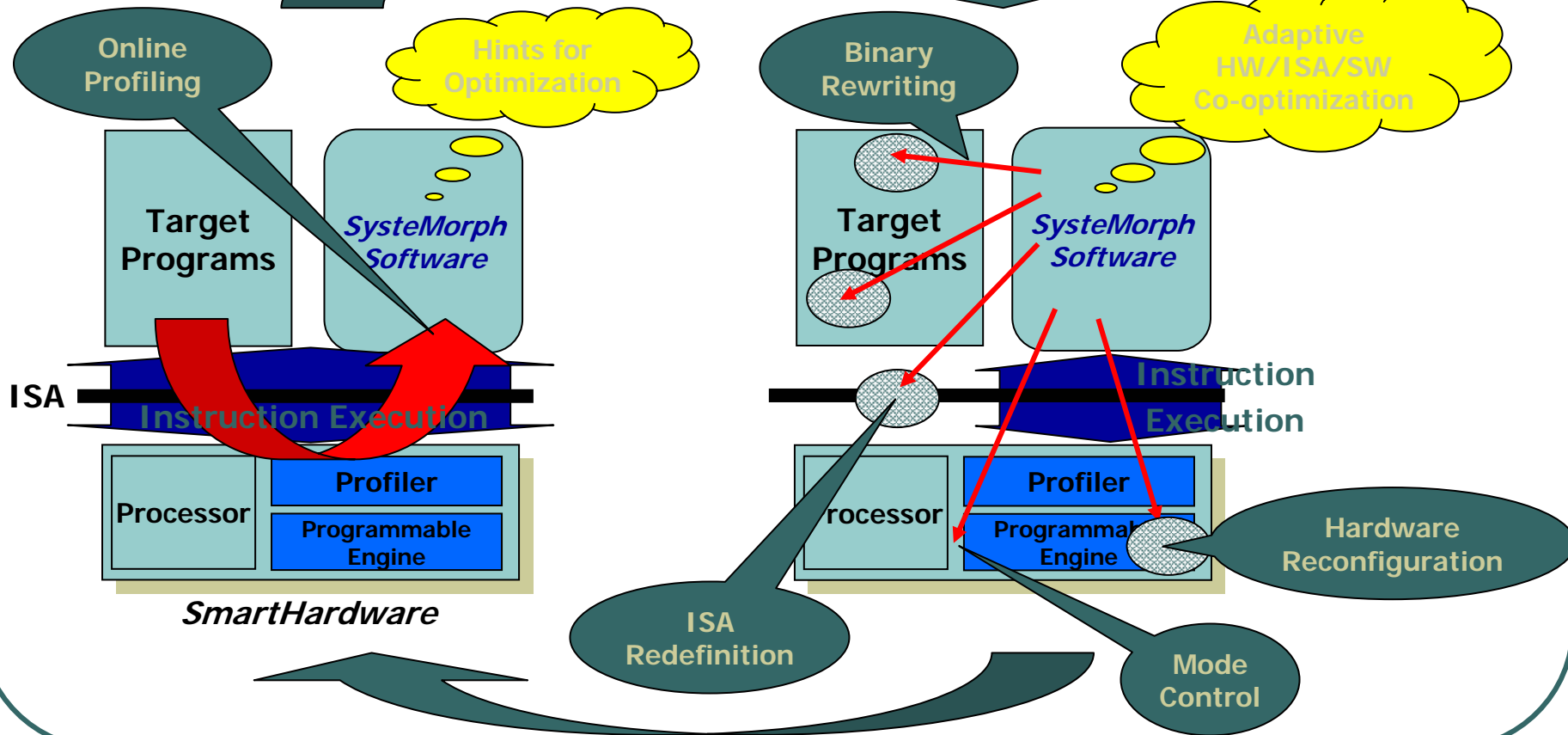
Abstract

- This research investigates a possible architecture to adaptive dynamic optimization systems. In this architecture, the running application is monitored and high frequently executed parts of the code are detected. Then, these parts of code are optimized, according to the architecture of embedded hardware accelerator. To be able to use the hardware accelerator, the new binary code is rewritten. IPFlex DAP/DNA-HP was the target of our prototyping to validate the concept. The proposed architecture for SoC implementation utilizes dynamic software pipelining technique for optimization and a simplified 8-way VLIW as the accelerator. Some preliminary performance evaluations show speedup.

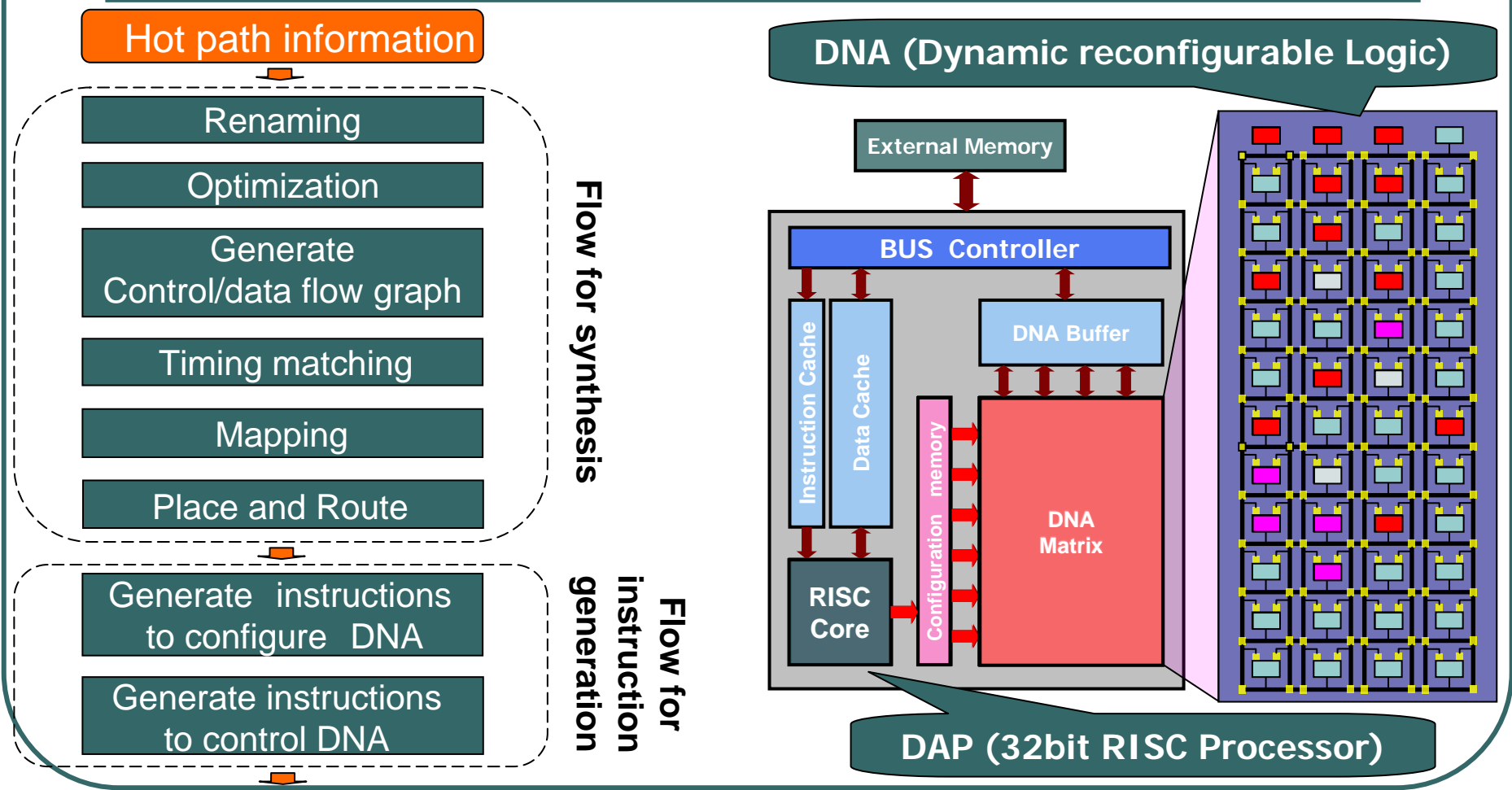
Concept of SystemMorph

Before Optimization

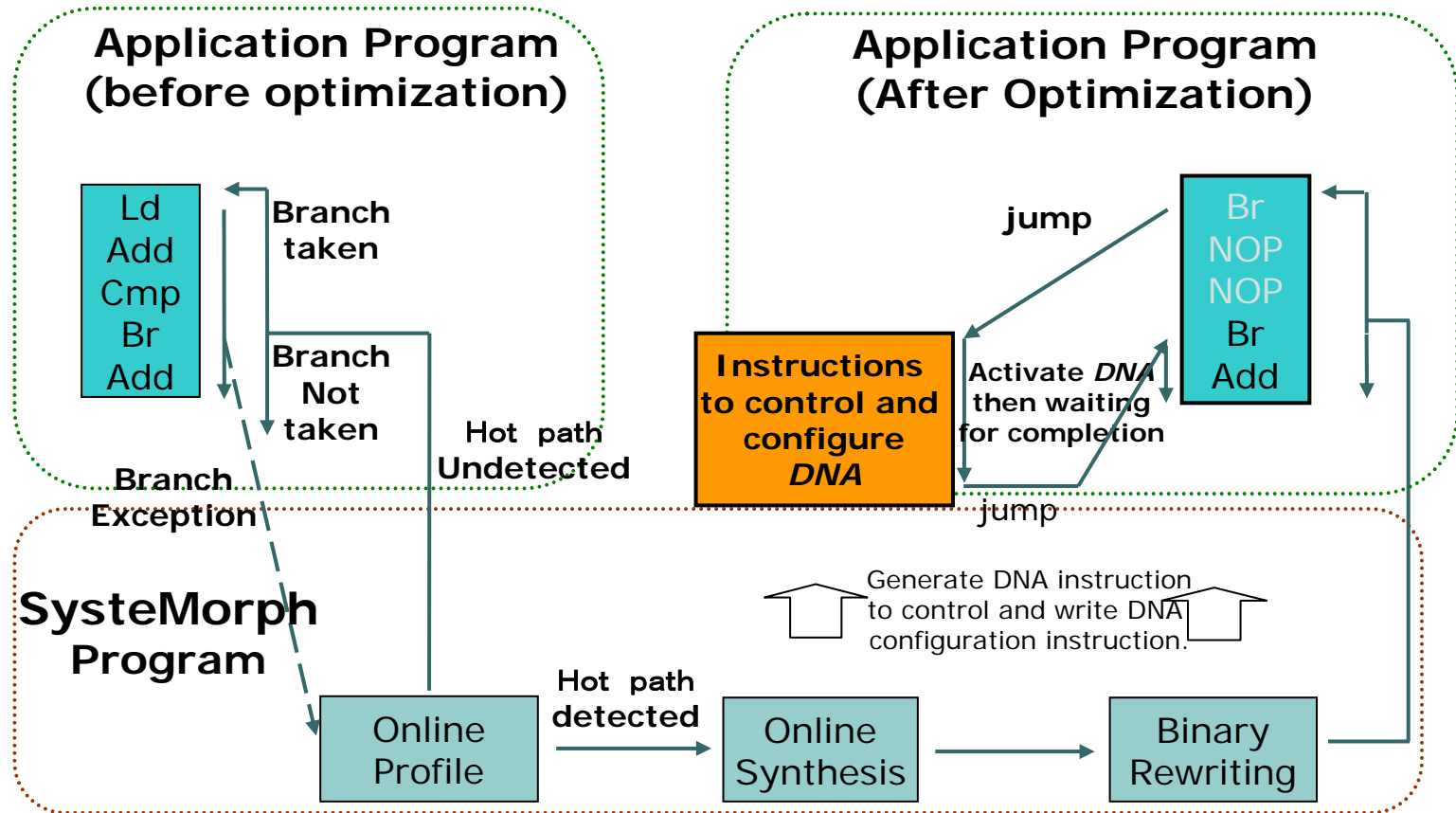
After Optimization



SystemMorph Synthesis Flow on DAP/DNA-HP



Execution Flow on DAP/DNA-HP



Branch History Method

■ Branch History Table

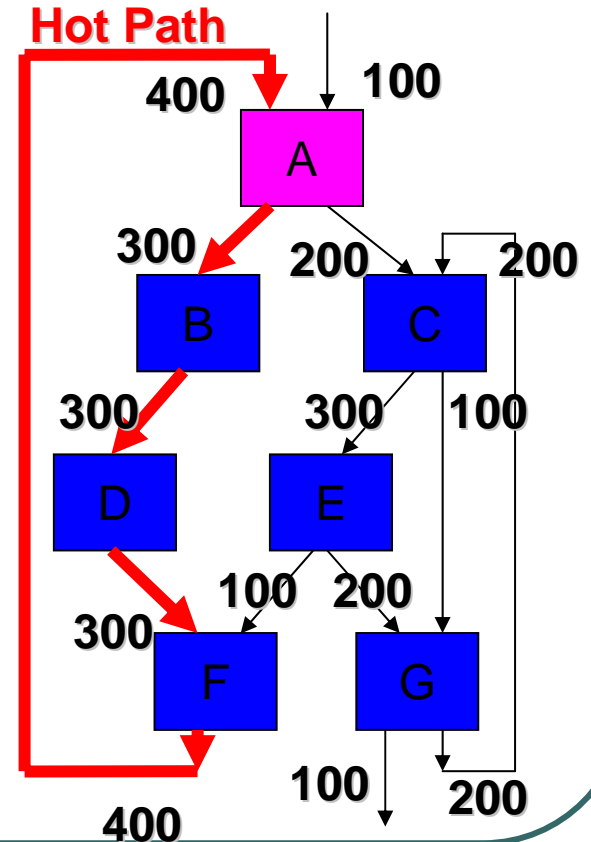
A_{top} : Head Address of Basic Block A
 A_{bottom}:End Address of Basic Block A

Branch Address	Branch Target Address	Number of Branch
A _{bottom}	B _{top}	300
A _{bottom}	C _{top}	200
...

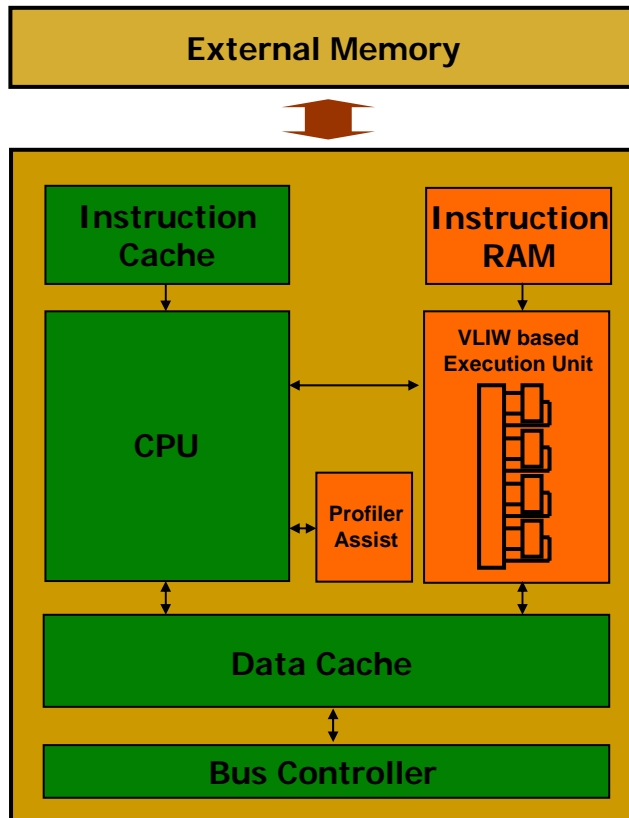
Number of Backward Branch > Threshold

■ Find Hot Path

A path which has more frequently taken is chosen as a Hot Path.

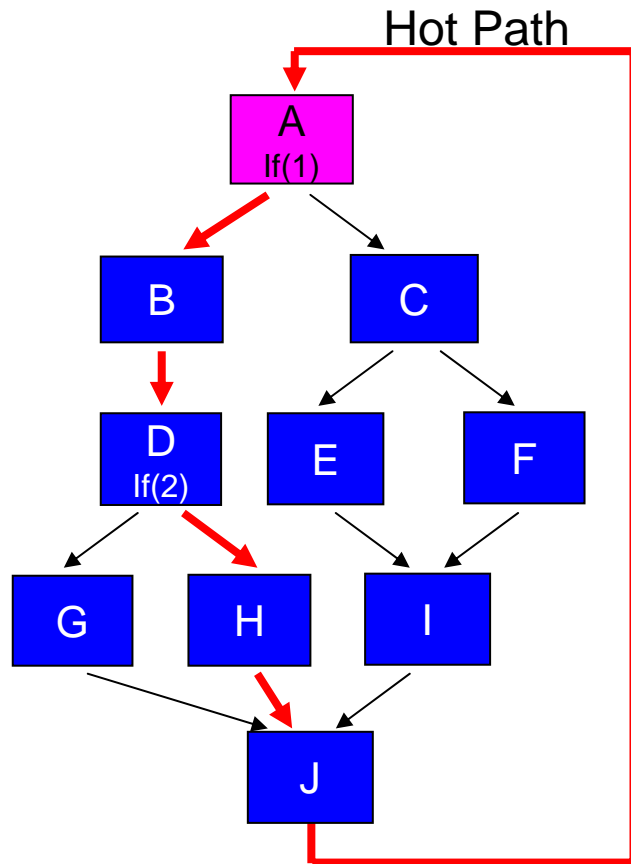


SystemMorph with VLIW accelerator

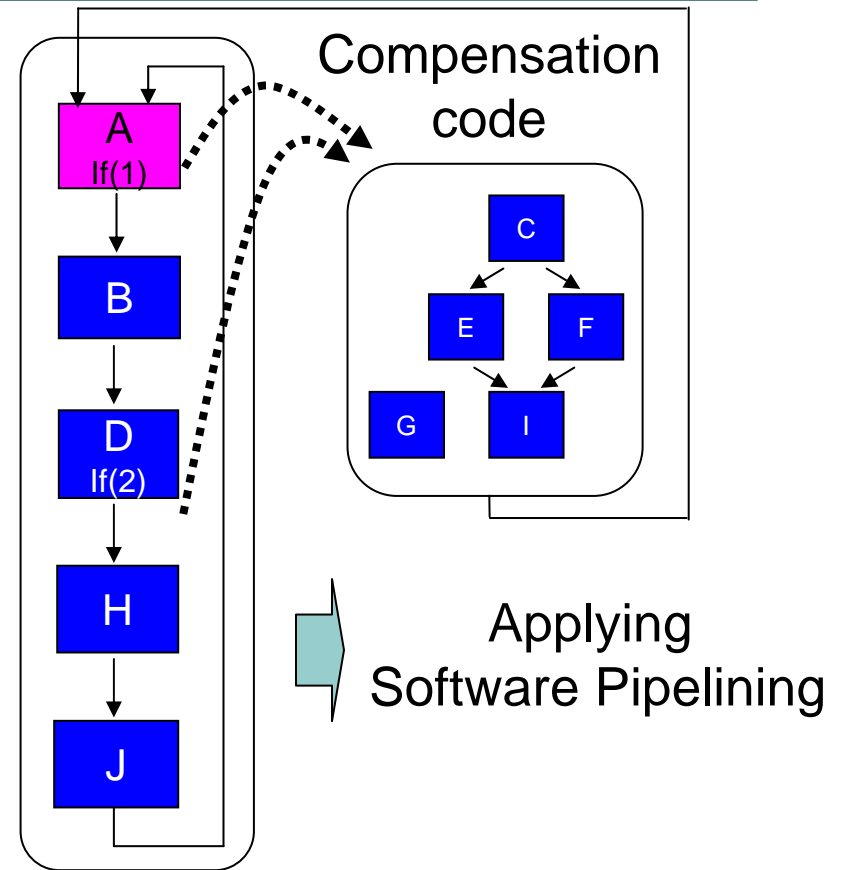


- **CPU**
 - Simple RISC processor
- **VLIW based accelerator**
 - Instruction RAM
 - Compute intensive execution unit
- **H/W profiler assist**
 - Store Branch history information
 - Branch Target Address
 - Branch Instruction Address
 - Number of Taken/Not Taken

Dynamic Trace Based Software Pipelining

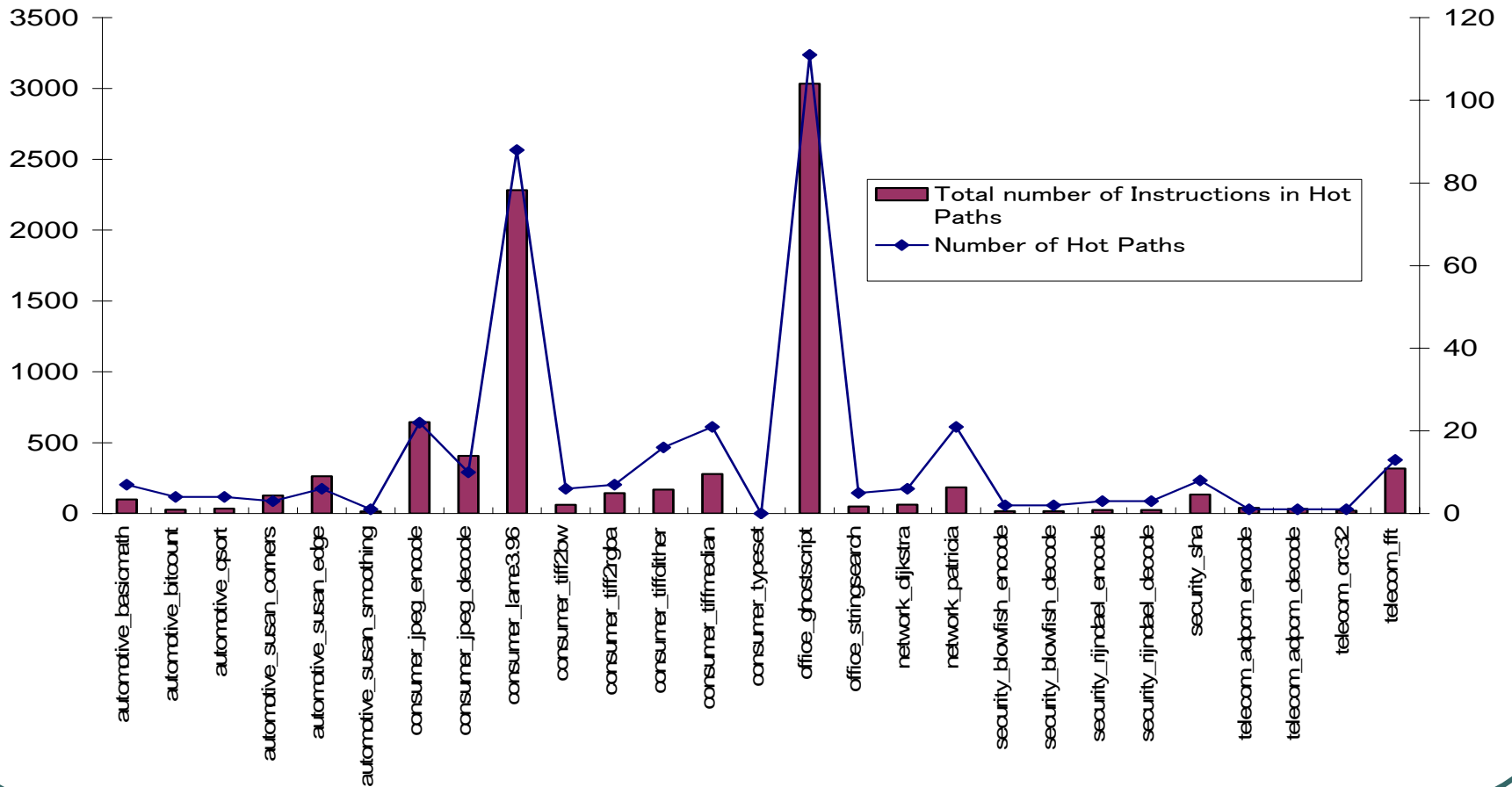


Original loop

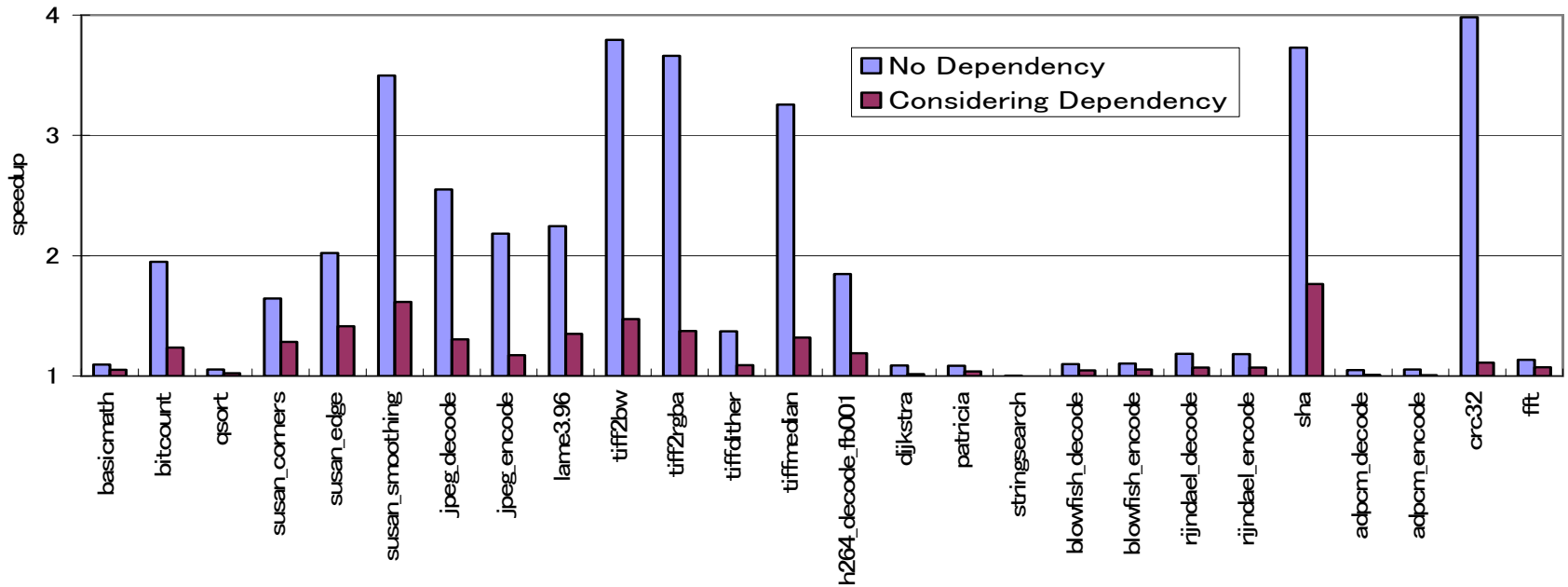


After applying dynamic software pipelining

Hot Paths



Preliminary Performance Evaluation



	N (way)	Int	FP	Ld/St	Br
Exp. 1	4	3		1	
Exp. 2	8	3	1	3	1
Exp. 2	12	5	1	5	1

