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A Design Method for a Low Power Equalization Circuit by Adaptive Bitwidth Control

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Abstract—In this paper, we propose a new design method for a low power equalization circuit using adaptive bitwidth control. It can reduce the amount of necessary calculation to control the bitwidth of the equalization circuit. We show that our new method is effective for a low power equalization circuit by experimental simulation while keeping the required calculation accuracy.

I. INTRODUCTION

Recently, digital wireless communication technologies have gained in popularity and are now used in various devices such as cellular phones, wireless LAN (local area network) cards, PDAs, digital TVs, RF ID tags, IC cards, and so on. The design methodology of LSIs for digital wireless communication systems places emphasis on low power and low energy system requirements, because of the growing need for longer battery lifetime and a restriction of power supply. For example, microsensor nodes are expected to operate in 5-10 years[1], [2], [3], [4]. The design methods for low power digital wireless communication systems constantly attract a great deal of researchers' attention.

In wireless LAN systems, a digital baseband processor includes a lot of operations, such as modulation, demodulation, noise elimination, timing adjustment, error detections and corrections and control operations. Due to the increased number of operations, the power consumption and the area of circuit requirements for digital baseband processing have increased rapidly. Hence, it is more important to develop a design methodology which minimizes the power consumption of digital baseband processing circuits. Some of the design techniques for low power digital baseband processors in digital wireless communication systems proposed[1], [2], [3], [4].

In addition, higher data rate systems are required. Many researchers have proposed new communication protocols for high data rate. These protocols have very complex modulation/demodulation schemes. These schemes need higher SNR because each modulated symbol contains a large amount of information. For higher SNR, digital wireless communication systems need equalization circuits. The goal of the equalization circuits is to restore the originally transmitted symbols by having a transfer function the reciprocal of the channel function. Equalization circuits can eliminate noise signals and

delayed signals added during propagation in wireless channels which is modeled by frequency selective fading[5], [6], [8].

However, an equalization circuit has a lot of arithmetic circuits such as multipliers, adders, and so on. In general, arithmetic circuits consume high power and have large circuit area. It is thus very important to reduce the power consumption and circuit area of equalization circuits. Some design techniques for low power equalization circuits have been proposed[7], [8]. In [7], many design methods for the low power equalization circuits are explained, such as fractionally spaced taps equalization techniques and simplifications of the tap updating algorithm using a power-of-two. The paper [8] extends the prior work that concerned real samples, to include a formulation of the update equation when the filter uses complex samples and coefficients.

In this paper, we propose a new power reduction method for an equalization circuit using adaptive bitwidth control. The rest of this paper is organized as follows: in section II, we discuss the adaptive equalization circuit and a power consumption model of a circuit designed in CMOS process. In section III, we describe our proposed method for a low power equalization circuit. In section IV, we show our experimental simulations and results. We present our conclusions in section V.

II. PRELIMINARY

A. Equalization circuit architecture

An example of architectures of equalization circuits is shown in Fig. 1 [5]. It consists of 3 parts listed below.

- Transversal filter
- Error evaluation
- Adaptive weight-control

The output signals of the equalization circuits are calculated in the transversal filter. This operation can be described in (1) [5].

$$y[n] = \sum_{k=0}^{M-1} h_n[k] \cdot x[n-k] \quad (1)$$

where $x[n]$, $y[n]$ and $h_n[k]$ represent the data input of the filter, output of the filter, and k -th coefficient of the filter at time step n respectively. M is the number of taps of filter.

This digital FIR filter consists of $M - 1$ unit-delay elements, M multipliers, and $M - 1$ adders.

The error evaluation part calculates the error signal which is the difference between output signal and desired signal. This operation can be expressed in (2).

$$e[n] = d[n] - y[n] \quad (2)$$

where $e[n]$ is the error signal at time step n , and $d[n]$ is the desired signal at time step n .

The adaptive weight-control part estimates the tap weight vector h_n by using the error signals $e[n]$ and the previous tap weight vectors. The Normalized Least Mean Square algorithm is often used as the algorithm for estimating the tap weight vectors.

The equalization circuit has two operation modes, such as the training mode and processing mode.

In the training mode, the equalization circuit estimates the tap weight vector to obtain the sufficiently performance. The equalization circuit operates in the training mode when training signals are received.

In the processing mode, the equalization circuit calculates the output signals using the tap weight vector estimated in the training mode. Therefore, signals with high SNR can be received.

B. Algorithm for estimating the tap weight vector

In this paper, we design the equalization circuit by using the Normalized Least Mean Square Algorithm as the algorithm for estimating the tap weight vector. The Normalized Least Mean Square algorithm is described in Fig. (2) [5].

C. The power consumption model

In this paper, we discuss only circuits which are designed using CMOS process. The total power dissipation of CMOS transistors, P_{CMOS} , can be obtained from the sum of the three dissipation components[9]. P_{CMOS} is expressed by (3).

$$P_{CMOS} = P_{dynamic} + P_{static} + P_{short} \quad (3)$$

where $P_{dynamic}$ is the dynamic power dissipation during the charging and discharging of the node capacitances. P_{static} is the static power dissipation caused by leakage current. P_{short} is the short-circuit power dissipation generated by the short-circuit current at the input rise and fall transition times.

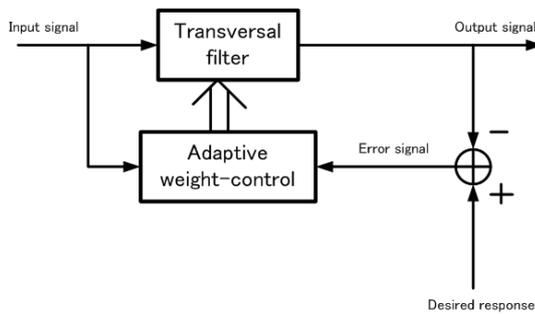


Fig. 1. Example of equalization circuit

Parameter:

M : number of taps
 μ : adaptation constant

Initialization:

If the prior tap weight vector \mathbf{h}_0 is known, use an appropriate value.
 Otherwise, set $\mathbf{h}_0 = \mathbf{0}$.

Data:

(a) given:

$\mathbf{u}(n) = M - by - 1$ tap input vector at time n

$$\mathbf{u}(n) = \begin{bmatrix} x[n] \\ \vdots \\ x[n - M + 1] \end{bmatrix}$$

(b) to be computed:

\mathbf{h}_{n+1} : estimation of tap weight vector at time step $n + 1$

$$\mathbf{h}_{n+1} = \begin{bmatrix} h_{n+1}[0] \\ \vdots \\ h_{n+1}[M - 1] \end{bmatrix}$$

Computation:

for $n = 0, 1, 2, \dots$,

$$y[n] = \mathbf{h}_n^t \cdot \mathbf{u}(n)$$

$$e[n] = d[n] - y[n]$$

$$\mathbf{h}_{n+1} = \mathbf{h}_n + \frac{\mu \cdot e^*[n] \cdot \mathbf{u}(n)}{\|\mathbf{u}(n)\|^2}$$

Fig. 2. Normalized Least Mean Square algorithm

The dominant source of power dissipation in CMOS circuits is the dynamic power dissipation expressed in (4),

$$P_{dynamic} = \sum_k Swit_k \cdot CL_k \cdot V_{DD_k}^2 \cdot freq_k \quad (4)$$

where CL_k is the load capacitance of a gate g_k , $Swit_k$ is the switching ratio of g_k in one clock cycle, V_{DD_k} is the supply voltage, and $freq_k$ is the operating frequency.

In this paper, we only consider the case when CL_k , V_{DD_k} and $freq_k$ are fixed. Our new design method can reduce the $Swit_k$ by controlling the effective bitwidth of calculations in the equalization circuit adaptively.

III. PROPOSED DESIGN METHOD FOR A LOW POWER EQUALIZATION CIRCUIT

A. Overview

We propose a new design method for a low power equalization circuit using adaptive bitwidth control.

In general, the amount of calculation in an equalization circuit depends on the received signals corrupted with noise signals or multipath delayed signals propagated in the wireless channels. For example, equalization circuits need high processing requirements to eliminate the unnecessary signals when the received signals pass through by noisy channels with a large number of multipath channels. On the other hand, less processing is needed to eliminate the unnecessary signals when the propagated signals pass through a less noisy channel. Hence, the amount of calculation required depends on the wireless channel environment.

In the compensation step, rough estimation in equalization will be held in the lower bitwidth when the error signals are big. On the other hand, detailed estimation will be held in the higher bitwidth when the error signals are small. Hence, the power consumption of equalization circuits can be reduced because they have a small amount of calculation. In short, the number of redundant operations in the variable coefficient digital filter can be reduced by using adaptive bitwidth control according to the magnitude of the error signals during the equalization process.

B. Assumptions

We assume the following to consider the problem simply.

- The calculation in the equalization circuit is performed in fixed-point, and 2's complement.
- The received packet consists of two kind of signals such as the training signal and the data signal. The training signals are received first.
- The equalization circuit calculates in the training mode when the training signals are received. On the other hand, the equalization circuit calculates in the processing mode when the data signals are received.
- The bitwidth of calculations in the equalization circuit is changed during the training mode only. In the processing mode, the bitwidth is fixed.
- The necessary bitwidth in the equalization circuit is determined by the magnitude of the error signal.
- The desired signals can be calculated by using the transmitted signals.

C. Notation

We define the parameters as follows.

- T : the number of training signals in the received packet
- D : the number of data signals in the received packet
- $bitwidth_n$: the bitwidth of calculations in the equalization circuit at time step n
- bit_{min}, bit_{max} : the minimum of the $bitwidth_n$ and the maximum of the $bitwidth_n$.

D. Motivational example

We show the motivational example in this section. First, we examine the relation between the bitwidth of the calculations in equalization circuit and the SNR of the received signal. We evaluated the necessary number of steps to converge the error in the equalization circuit and the power consumption of the

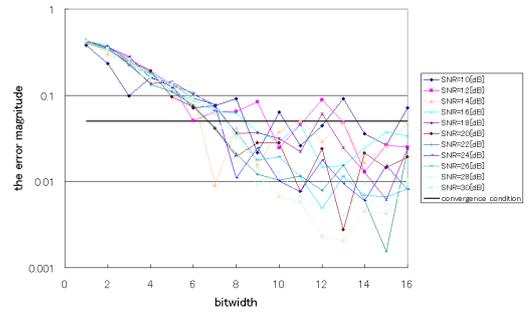


Fig. 3. The result of the error magnitude

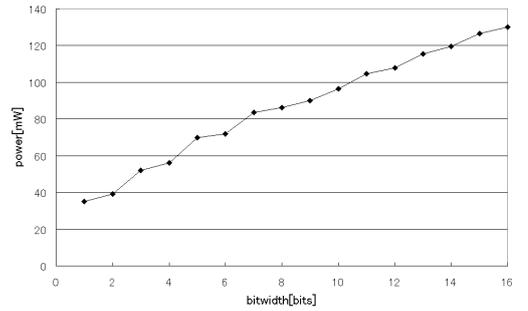


Fig. 4. The result of the power consumption

equalization circuit by using sine waves as the input signals into the equalization circuit. We evaluated the number of steps and the power consumption with the bitwidth and SNR as the variable parameter by computer simulations. In this evaluation, the convergence condition is that the magnitude of the error signals is less than 0.05. The ranges of the parameters, the bitwidth and the SNR, are listed below.

- bitwidth : 1 - 16 bit
- SNR : 10 - 30 dB (2dB step)

Fig. 3 shows the result of the error magnitude when the calculation of the 100th signal is finished. Fig. 4 shows the result of the power consumption. Fig. 5 shows the result of the number of steps to converge the error.

In Fig. 3, we can find that the some case are satisfied with the convergence condition. If the convergence condition is that the magnitude of the error signals is less than 0.05 when

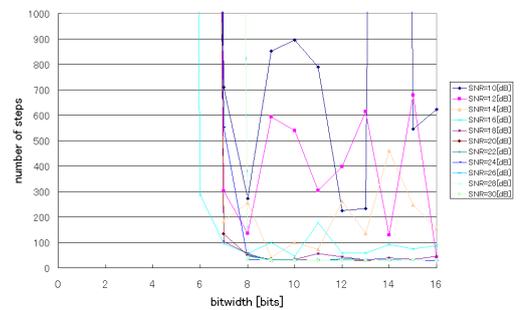


Fig. 5. The result of the number of steps to converge the error

the 100-th training signal is received, some bitwidth will be satisfied with the convergence condition. In Fig. 5, we can find that the error magnitude converge quickly when the bitwidth is big. However, the convergence of the error magnitude is not most rapid at the case of the biggest bitwidth. In Fig. 4, the more power consume at the case of the bigger bitwidth. Hence, it is not necessary to use the biggest bitwidth. So, the bitwidth control is very important for low power.

SNR is changeable by the communication environment. The power consumption of the equalization circuit can be reduced by the adaptive bitwidth control. The receiver cannot observe the SNR. The bitwidth of the calculations is controled adaptively by the magnitude of the error signal.

E. Procedure of adaptive bitwidth control

Fig. 6 shows the procedure for the calculations of the equalization circuit using adaptive bitwidth control.

The desired signals, the maximum and minimum bitwidth of the calculations in the equalization circuit are given to calculate the output signals. At first, the equalization circuit initialize the tap weight vector and the bitwidth register.

The equalization circuit calculates the output signals, the error signals, and the tap weight vectors by using the Normalized Least Mean Square Algorithm during the training mode. These signals are calculated in $bitwidth_n$ -bits. The equalization circuit estimates the necessary bitwidth of the calculations with the magnitude of the error signals. The variable, $bitwidth_n$ is estimated at every clock cycle in only the training mode. This estimation can be expressed by using the function for estimating the necessary bitwidth, f_{bit} .

On the other hand, the equalization circuit calculates only the output signals in the processing mode. The bitwidth of the calculations are fixed in the processing mode.

F. Implementation

Fig. 7 shows the block chart of the equalization circuit which is designed using our proposed design method. The bitwidth control module and the mask module are added into the equalization circuit in Fig. 7 compared with the equalization circuit in Fig. 1. This equalization circuit can control the bitwidth of the calculation adaptively by these modules.

We explained the operations of the transversal filter part, the error evaluation part, and the adaptive weight-control part in section II-A. The adaptive weight-control part in Fig. 7 has additional function for changing the bitwidth of the tap weight vector calculation using the bitwidth control signal. We further explain the function of the bitwidth control module and the mask module as follows.

The bitwidth control module controls the necessary bitwidth of the calculations in the equalization circuit. Less bits are used for estimation when the error signal is relatively large in magnitude. On the other hand, the bitwidth of the calculations is higher to estimate in detail when the error signals are small. The bitwidth control module models the detection of the effective bitwidth of the signals.

Procedure adaptive bitwidth control:

Function:

f_{bit} : the function of the necessary bitwidth estimation

Initialization:

$\mathbf{h}_0 = \mathbf{0}$

$bitwidth_0 = bit_{min}$

Data:

(a) given:

$\cdot bit_{min}$

$\cdot bit_{max}$

$\cdot d[n]$

(b) to be computed:

$\cdot y[n]$

$\cdot bitwidth_{n+1}$

Computation:

for $n = 0, 1, 2, \dots$

If (training mode)

calculate the signals masked as the $bitwidth_n$ -bits signals.

(see Fig. 2)

$\cdot y[n]$

$\cdot e[n]$

$\cdot \mathbf{h}_{n+1}$

estimate the necessary bitwidth of the calculations.

$bitwidth_{n+1} = f_{bit}(e[n])$

else if (processing mode)

calculate $y[n]$.

$bitwidth_{n+1} = bitwidth_n$

endif

Fig. 6. The procedure for the calculations in the equalization circuit using adaptive bitwidth control

The mask module controls the bitwidth of the signals using the bitwidth control signals from the bitwidth control module.

IV. EXPERIMENTAL RESULTS

A. Assumptions

We assumed the following for the experiment.

- The calculations in the equalization circuit were held in 2-16 bits.
- The overhead of the equalization circuit was ignored.
- The power consumption of the equalization circuit was known when the bitwidth of the equalization circuit was given.
- The bitwidth of the input and output signals were fixed as 16-bits.
- Noise signals were modeled by using white Gaussian noise.
- SNR was 15, 20, 25[dB].
- Some delayed signals were added in the received signals, which is modeled as (5) [10].

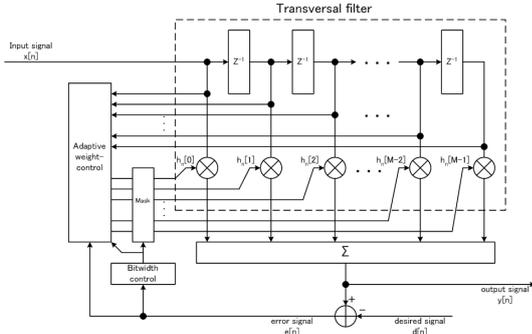


Fig. 7. Block chart of the implementation of the equalization circuit

$$S_r(t) = h_f(\tau, t) * S_t(t)$$

$$h_f(\tau, t) = \sum_{i=1}^L \beta_i \cdot \delta(t - \tau_i) \cdot e^{j\phi_i} \quad (5)$$

where $S_r(t)$ is the receive signal at time t , $S_t(t)$ is the transmit signal at time t , $h_f(\tau, t)$ is the mathematical model of multipath fading in the channel. L is the number of multipaths. β_i , τ_i , and ϕ_i represent the magnitude, arrival delay, and phase of the i th path. $*$ is the convolution operation expressed as (6).

$$a(t) * b(t) = \int_{-\infty}^{\infty} a(\tau) \cdot b(t - \tau) d\tau$$

$$= \int_{-\infty}^{\infty} a(t - \tau) \cdot b(\tau) d\tau \quad (6)$$

B. Experimental results

We evaluated our design method for the low power equalization circuit. We designed two kinds of equalization circuits as listed below.

- 1) The equalization circuit which was designed in the fixed bitwidth (16 bits) of the variable coefficient filter.
- 2) The equalization circuit which was designed in the controllable bitwidth of the variable coefficient filter.

In this paper, we call the first equalization circuit a fixed bitwidth equalization circuit and the second equalization circuit an adaptive bitwidth equalization circuit. We evaluated the power consumption and the error magnitude using MATLAB [11].

We considered two kinds of the input vectors for the equalization circuit listed below.

- Case 1. :
the sine waves sampled at 8 times more than the one cycle time
- Case 2. :
the packet signals modulated by DBPSK(Differential Binary Phase Shift Keying) which have the training signals and the data signals

The reason why the sine waves were used for the input signals is the simple example is to show the effectiveness of our proposed design method. The DBPSK modulated signals

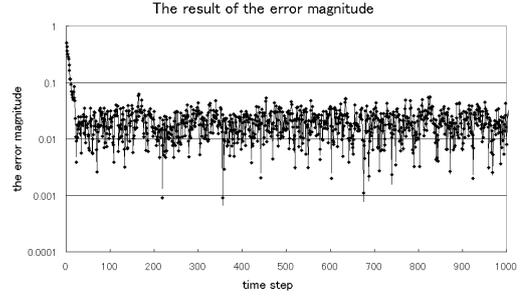


Fig. 8. The result of the error magnitude (Case 1. SNR=20[dB])

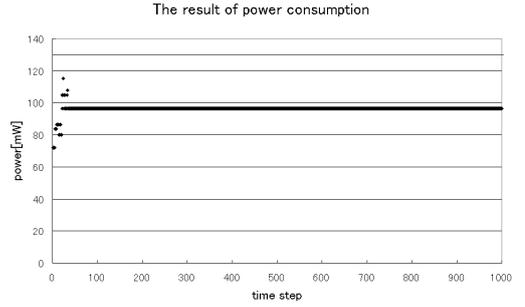


Fig. 9. The result of the power consumption (Case 1. SNR=20[dB])

were used for the input signals as they are the simple example of the real applications.

In case 1, the equalization was terminated when the magnitude of the error signal is less than 0.05. In case 2, the equalization was held during the training signals were received.

Fig. 8 shows the result of the error magnitude between output signals and desired signals when SNR is 20[dB]. Fig. 9 shows that the result of the power consumption at each time step when SNR is 20[dB]. In these figures, the solid lines show the results of the fixed bitwidth equalization circuit and the dotted lines show the results of adaptive bitwidth equalization circuit. Fig. 8 shows the error magnitude of the adaptive bitwidth equalization circuit are almost the same as the error magnitude in the fixed bitwidth equalization circuit. Fig. 9 shows the reduced power consumption.

Table I, II, and III show the result of the average power consumption of two kinds of equalization circuits at the Case 1, when SNR is 15[dB], 20[dB], and 25[dB] respectively. Table IV, V, and VI show the result of the average power consumption of two kinds of equalization circuits at the Case 2, when SNR is 15[dB], 20[dB], and 25[dB] respectively. The percentage numbers in round brackets in Table I, II, III, IV, V and VI show the reduction ratio compared with the fixed bitwidth equalization circuit.

V. CONCLUSIONS

In this paper, we proposed a new method for a low power equalization circuit using adaptive bitwidth control. The experimental results showed that our method can reduce the power consumption. Our design method can reduce power

TABLE I
AVERAGE POWER CONSUMPTION RESULTS (CASE 1. SNR=15[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	94.87 (27.1%)

TABLE II
AVERAGE POWER CONSUMPTION RESULTS (CASE 1. SNR=20[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	107.02 (17.7%)

consumption of the equalization circuits at architectural level. The equalization circuits can consume much less power with other proposed design method at circuit level and device level. The static power dissipation caused by leakage current cannot be ignored in the deep submicron CMOS circuits. We will consider the design method for the reduction of the leakage current.

Estimating the bitwidth of the calculatinos is the overhead occured in our proposed design method. However, controlling the bitwidth of the calculatinos adaptively is an effective method to reduce the power consumption of the equalization circuit. This is because the noise signals and the delayed signals by multipath phenomenon are varied in the different places, temperature, and environment for comunicatinos. Our proposed design method which is controlling the bitwidth of the calculations adaptively is very effective for reducing the power consumption.

In the experiment, we ignored that the overhead of the equalization circuit and assumed that the power consumption is in proportion to the bitwidth of the equalization circuit. However, the input sequences are more important parameters for the power consumption than the bitwidth of the equalization circuit.

Our future works are listed below:

- To consider the overhead of the adaptive bitwidth control scheme in the evaluation of power consumption
- To consider the input sequence for low power methods of the equalization circuits

TABLE III
AVERAGE POWER CONSUMPTION RESULTS (CASE 1. SNR=25[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	104.25 (19.9%)

TABLE IV
AVERAGE POWER CONSUMPTION RESULTS (CASE 2. SNR=15[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	72.11 (44.6%)

TABLE V
AVERAGE POWER CONSUMPTION RESULTS (CASE 2. SNR=20[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	72.21 (44.5%)

TABLE VI
AVERAGE POWER CONSUMPTION RESULTS (CASE 2. SNR=25[DB])

Type of equalization circuit	Average power[mW]
Fixed bandwidth	130.01
Adaptive bandwidth	72.19 (44.5%)

- To develop the algorithm of the adaptive bitwidth control
- To evaluate the error convergence mathematically
- To apply our method to the real applications of digital wireless communication systems.

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REFERENCES

- [1] Andrew Y. Wang, Seong-Hwan Cho, Charles G. Sodini, Anantha P. Chandrakasan, "Energy Efficient Modulation and MAC for Asymmetric RF Microsensor Systems," Proceedings of International Symposium on Low Power Electronics and Design 2001 (ISLPED '01), pp.106-111, August 2001.
- [2] Rex Min, Anantha Chandrakasan, "A Framework for Energy-Scalable Communication in High-Density Wireless Networks," Proceedings of International Symposium on Low Power Electronics and Design (ISLPED) 2002, August 2002.
- [3] Eugene Shih, Seong-Hwan Cho, Nathan Ickes, Rex Min, Amit Sinha, Alice Wang, Anantha Chandrakasan, "Physical Layer Driven Protocol and Algorithm Design for Energy-Efficient Wireless Sensor Networks," ACM SIGMOBILE, July 2001.
- [4] Curt Schurgers, Olivier Aberthorne, Mani B. Srivastava, "Modulation Scaling for Energy Aware Communication Systems," Proceedings of International Symposium on Low Power Electronics and Design (ISLPED) 2001, pp.96-99, August 2001.
- [5] Simon Haykin, "Adaptive Filter Theory, fourth edition," Prentice Hall, 2001.
- [6] Sergio Benedetto, and Ezio Biglieri, "Principles of Digital Transmission With Wireless Applications," Kluwer Academic/Plenum Publishers, 1999.
- [7] Chris J. Nicol, Patrik Larsson, Kamran Azadet, Jay H. O'Neill, "A Low Power 128-Tap Digital Adaptive Equalizer for Broadband Modems," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997.
- [8] David Garrett, Chris Nicol, Andrew Blanksby, Chris Howland, "A Low Power Normalized-LMS Decision Feedback Equalizer for a Wireless Packet Modem," Proceedings of Internatinoal Symposium on Low Power Electronics and Design 2002 (ISLPED '02), 11.2, August 2002.
- [9] Neil H.E. Weste, and Kamran Eshraghian, "Principles of CMOS VLSI Design -A Systems Perspective, second edition," Addison-Wesley Publishing Company, 1994.
- [10] Kaveh Pahlavan, Allen H. Levesque, "Wireless Information Networks," John Wiley & Sons Inc., 1995.
- [11] MATLAB, The MathWorks Inc. <http://www.mathworks.com/>