Wire Sizing Considering Skin Effect for High Frequency Circuits

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Abstract

This paper proposes Wire Sizing considering skin effect. Previous work on Wire Sizing usually uses RC model which is independent of frequency. However, as increasing operating frequency, frequency-dependence of interconnect characteristics is becoming significant. Therefore, in interconnect design and analysis, frequency-dependence must be considered. By Wire Sizing considering frequency-dependence, the experimental results show about 50% $\sim$ 80% reduction of effective upper-bound wire width compared with previous work.

1. Introduction

In the present LSI design, interconnect RC model which is independent of frequency is widely used. But, as increasing operating frequency, frequency-dependence of interconnect characteristics is becoming significant. In 2008, maximum operating frequency will reach 10GHz[1]. Resistance and inductance depend on frequency because of skin effect. Especially, as the inductance effect is becoming significant, we need consider signal overshoot, undershoot and crosstalk noise by inductance effect[2][3][4][5][6]. Therefore, in interconnect design and analysis, frequency-dependence must be considered.

This paper proposes a new Wire Sizing approach considering skin effect. We focus on global interconnects such as clock wires and signal buses. Previous work on Wire Sizing usually uses RC model which is independent of frequency[7][8][9]. By using this model, wire width is optimized to transmit signal within arrival time the designer sets and to reduce clock skew. So, global interconnects such as clock wires and signal buses are designed using wider lines(about $2\mu m \sim 5\mu m$) to reduce resistance. In this method, as wire width is becoming wider, delay is reduced. However, when skin effect is significant by increasing operating frequency, current only flows near the surface of conductor. Therefore, current doesn't flow in the center of conductor even if wire width is becoming wider. So, wire width is too wide in this condition.

We propose Wire Sizing considering skin effect to solve the problem in previous method. There are some advantages if wire width is reduced. 1)Wire area can be reduced. 2)Crosstalk noise is reduced. Because the designer can widen wire space if wire width is reduced. And, the designer uses the rest of wire resources as ground lines when he can reduce wire width. Crosstalk noise can be reduced due to shielding effect of ground lines[5]. 3)Power can be reduced because wire capacitance is reduced.

Therefore, our proposed Wire Sizing approach is more effective than previous method. We experimentally evaluate this. In this experiments, we do Wire Sizing by a field-solver[10][11] considering frequency-dependence. And, we do previous Wire Sizing by RC model which is independent of frequency. We compare these experimental results.

The rest of this paper proceeds as follows. Section 2 discusses related work on Wire Sizing. Section 3 describes skin effect and our proposed Wire Sizing approach. Section 4 concludes this paper.

2. Related Work

Previous Wire Sizing usually uses RC model which is independent of frequency[7][8][9]. Resistance and capacitance are calculated, based on width, thickness, length, and space of wires. Then, the wire model such as Figure 1 is constructed. Delay is calculated based on this model. Then, wire width is optimized to transmit signal within arrival time the designer sets and to reduce clock skew. Apparently, this model is independent of frequency. For, it is considered that current flows equally through the conductor. Therefore, as wire width is becoming wider, it is considered that delay is reduced. However, when skin effect is significant by increasing operating frequency, current only flows near the surface of conductor. So, current doesn't flow in the center of conductor even if wire width is becoming wider. And, because of increasing operating frequency and wider wires, the inductance

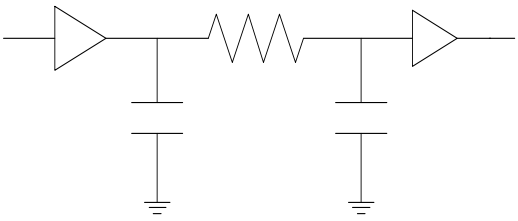

Figure 1 RC model

effect is becoming significant. Therefore, in previous Wire Sizing by RC model, wire width is inaccurate and too wide.

3. Wire Sizing Considering Skin Effect

This section first describes skin effect. Next, describes a new Wire Sizing approach considering skin effect.

3.1 Skin Effect

Skin effect[2] is the phenomenon such that current concentrates on the surface of conductor because of increasing frequency, conductivity, and permeability(Figure 2). When skin effect is significant, resistance is increases. The parameter to express skin effect is skin depth. Skin depth is the distance from the surface of conductor to the point such that current density reaches 37%$(1/e)$ of the surface. Skin depth "δ" is defined as follows:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{1}$$

where μ and σ are permeability and conductivity respectively, and f is the frequency of current which flows through the conductor. Skin effect is significant as frequency increases.

3.2 A New Approach for Wire Sizing

We propose Wire Sizing considering skin effect. We focus on global interconnects such as clock wires and signal buses. Long interconnects such as this need to be transmission lines. The main transmission line of the present LSI is co-planar line, which places parallel ground lines in the same layer as signal lines, such as Figure 2[2][3]. Because co-planar line is only one layer and can adjust the space between signal line and ground line. In the interconnect structure such as this, current concentrates near the side of conductor. This phenomenon is called for proximity effect[2]. Therefore, skin depth δ in co-planar line is expressed as the horizontal depth.

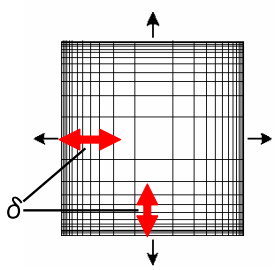

Figure 2 skin effect

Such as Figure 2, in low frequency, 2δ is wider than wire width. So, current flows equally through the conductor. But, in high frequency, 2δ is narrower than wire width because skin effect is significant. In this situation, current doesn't flow in the center of conductor. For, delay isn't reduced even if wire width is becoming wider. Then, in high frequency circuits such as this, effective upper-bound wire width(we define as "$Weub$") can be expressed as follows:

$$Weub = 2\delta = \frac{2}{\sqrt{\pi f \mu \sigma}} \tag{2}$$

To find $Weub$, we must find frequency of current which flows through the conductor. In digital circuits, common input waveform of interconnects are trapezoidal pulses. A trapezoidal pulse contains frequency components from DC to ∞. From these frequency components, we use significant frequency "$fsig$"[2] as the frequency to find $Weub$. Significant frequency $fsig$ is defined such that signal energy from DC to $fsig$ becomes 85% of all signal energy. When pulse width is Tw and signal transition time is tr, in the range $7 \leq Tw/tr \leq 13$, $fsig$ is expressed as follows:

$$fsig = \frac{0.34}{tr} \tag{3}$$

When (3) is substituted for (2), $Weub$ is expressed as follows:

$$Wopt = 2\delta = \frac{2}{\sqrt{\pi fsig \mu \sigma}} = \frac{2}{\sqrt{\pi \frac{0.34}{tr} \mu \sigma}} \tag{4}$$

3.3 Experiment

We experimentally evaluate our proposed approach. In this experiments, we use the model of Ref.[10]

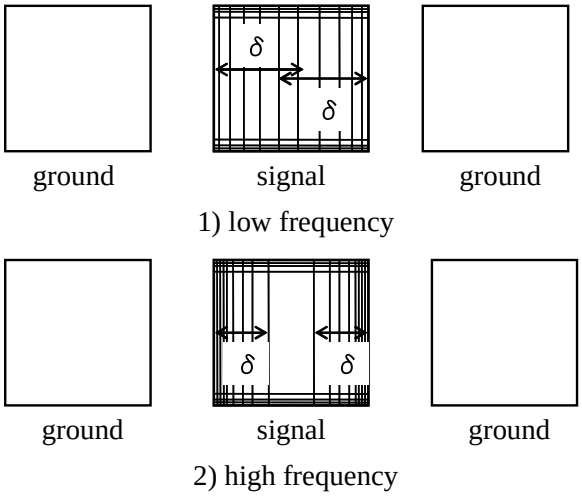

Figure 3 co-planar line and skin effect

as frequency-dependent model. It is implemented in HSPICE[11] as w-element model.

The interconnect structure in this experiments is co-planar line contains 15 signal lines between 2 ground lines, such as Figure 3. The material of interconnects is Cu, dielectric constant between interconnects is 2.0[1]. The reason uses as many as 15 signal lines is to analyze considering the inductance effect because inductance affects the far interconnects[2][4][5]. Inductance by orthogonal interconnects isn't affected. Because the direction of magnetic flux is different and eddy current doesn't occur in the narrow interconnects such that are used in LSI[2]. Therefore, in this experiments, we don't consider orthogonal interconnects. The output impedance of the driver is 100Ω. The input capacitance of the receiver is $50fF$. The input waveforms are clock $1GHz \sim 10GHz$. The pulse voltage is $1.0V$. The signal transition time is 1/16 of clock period. We measure the signal transition time at the near-end of interconnect by simulation. Then, we find $Weub$ by Equation (4). We show $Weub$ in Table1. We vary wire width based on $Weub$, and measure 50%delay respectively. 50%delay is the time from 50% transition time of input signal to 50% transition time of output signal. Wire space is equal to wire width. And, wire thickness and length are constant, $1.2\mu m$, $1mm$ respectively. The signal in which we measure delay is the center signal in the situation 14 left signals switch in opposite transition directions. In this situation, the center signal line is victim line, on the other hand, 14 left signal lines are aggressor lines. At this moment, in victim line, crosstalk noise occurs by undershoots of aggressor lines. Then, delay of victim line is increased. In the condition the above, we do Wire Sizing by our proposed approach. And, we do previous Wire Sizing by RC model in the same condition. We compare these experimental results.

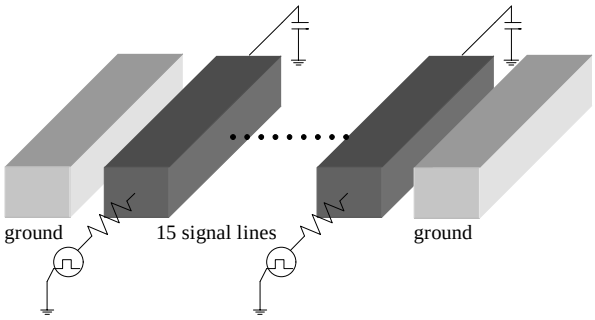

Figure 4 experimental circuit

3.4 Experimental Results

We arrange experimental results in Table 2. As you see, in all clock frequencies, $Weub$ by Equation (4) is effective upper-bound wire width. All $Weub$ are narrower than the general global wire width, $2\mu m \sim 5\mu m$. The reduction rate is about $50\% \sim 80\%$. Delay isn't reduced even if wire width is wider than $Weub$. It is inadequate because overshoot and undershoot by inductance effect are significant. On the other hand, in experimental results by previous RC model, delay is reduced as wire width is becoming wider. And, those by previous RC model are fewer delay($1/5 \sim 1/100$) than those by our proposed approach, and are independent of frequency. Because previous RC model is independent of frequency and can measure only the effect of capacitive crosstalk noise by adjacent wires because of shielding effect. Therefore, in high frequency and crowd routing area such as this experimental condition, Wire Sizing by previous method is inaccurate. On the other hand, we experimentally evaluate accuracy of our proposed approach.

4. Conclusion and Future Work

This paper proposes a new Wire Sizing approach considering skin effect. Our proposed approach is more accurate than previous Wire Sizing by RC model. Considering higher operating frequency in the future, proposed approach is the more effective.

In the future, we research wire delay calculation and timing constraint line algorithm based on Wire Sizing considering skin effect.

Table 2 experimental results

clock	delay time for wire width									
	$0.5\mu m$	$1.0\mu m$	$1.1\mu m$	$1.2\mu m$	$1.3\mu m$	$1.4\mu m$	$1.5\mu m$	$2.0\mu m$	$2.5\mu m$	$3.0\mu m$
$1GHz$		$21.7ps$					$21.6ps$	**21.3**ps	$21.6ps$	$21.9ps$
2	$18.3ps$	16.5				**15.8**ps		16.9	17.0	
3	18.6	16.3			**16.2**ps			16.4	16.4	
4	19.2			**16.5**ps			16.5	16.7	16.7	
5	19.8			**17.1**			17.1	17.2	17.3	
6	20.5		**17.7**ps				17.8	18.0	18.1	
7	21.0		**18.7**				18.7	19.0		
8	39.2		**38.5**				38.8	39.1		
9	35.2		**34.2**				34.4	34.8		
10	31.9		**30.7**				30.9	31.1		
RC model	$3.2ps$	$1.1ps$	$1.0ps$	$0.9ps$	$0.8ps$	$0.7ps$	$0.7ps$	$0.5ps$	$0.3ps$	$0.2ps$

Table 1 effective upper-bound wire width $Weub$

clock	tr	$fsig$	δ	$Weub$
$1GHz$	$84.0ps$	$4.05GHz$	$1.00\mu m$	$2.00\mu m$
2	38.9	8.74	0.70	1.40
3	30.6	11.1	0.63	1.26
4	28.0	12.1	0.60	1.20
5	26.0	13.1	0.58	1.16
6	24.7	13.8	0.56	1.12
7	23.8	14.3	0.55	1.10
8	23.1	14.7	0.55	1.10
9	22.6	15.0	0.54	1.08
10	22.5	15.1	0.54	1.08

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