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A Power Reduction Technique for an Equalization Circuit
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Abstract In this paper, we propose a new technique for a low power equalization circuit using adaptive bitwidth control. It can reduce the amount of necessary calculation to control the bitwidth of the equalization circuit. In the compensation step, estimation in equalizing will be held in the less bitwidth when the error signals are big. On the other hand, detailed calculation will be held in the more bitwidth when error signals are small. We show that our new technique is effective for a low power equalization circuit by experimental simulation while keeping the required calculation accuracy.

Keyword Low power, equalization circuit, adaptive bitwidth control

1. Introduction

Recently, digital wireless communication technologies have gained in popularity and are now used in various devices such as cellular phones, wireless LAN (local area network) cards, PDAs, digital TVs, RF ID tags, IC cards, and so on. The design methodology of LSIs for digital wireless communication systems places emphasis on low power and low energy system requirements, because of the growing need for longer battery lifetime and a restriction of power supply. For example, microsensor nodes are expected to operate in 5-10 years [1] - [4]. The design methods for low power digital wireless communication systems constantly attract a great deal of researchers' attention.

In wireless LAN systems, a digital baseband processor includes a lot of operations, such as modulation, demodulation, noise elimination, timing adjustment, error detections and corrections and control operations. Due to the increased number of operations, the power consumption and the area of circuit requirements for digital baseband processing have increased rapidly. Hence, it is more important to develop a design methodology which minimizes the power consumption of digital baseband processing circuits. Some of the design techniques for low power digital baseband processors in digital wireless communication systems proposed include techniques to adjust the dynamic range of digital baseband processors adequately to the SNR (Signal-to-Noise ratio) of received signals while satisfying the constraints of the transmission rate [5].

In addition, higher data rate systems are required. Many researchers have proposed new communication protocols for high data rate. These protocols have very complex modulation/demodulation schemes. These schemes need higher SNR because each modulated symbol contains a large amount of information. For higher SNR, digital wireless communication systems need equalization circuits. The goal of the equalization circuits is to restore the originally transmitted symbols by having a transfer function the reciprocal of the channel function. Equalization circuits can eliminate noise signals and delayed signals added during propagation in wireless channels which is modeled by frequency selective fading.

However, equalization circuit has a lot of arithmetic circuits such as multipliers, adders, and so on. In general, arithmetic circuits consume high power and have large circuit area. It is thus very important to reduce the power consumption and circuit area of equalization circuits. Some design techniques for low power equalization circuits have been proposed [9], [10]. In the paper [9], many design methods for the low power equalization circuits are explained such as fractionally spaced taps equalization techniques and simplifications of the tap updating algorithm using a power-of-two. The paper [10] extends the prior work that concerned real samples, to include a formulation of the update equation when the filter uses complex samples and coefficients.

In this paper, we propose a new power reduction technique for an equalization circuit using adaptive bitwidth control. The rest of this paper is organized as follows: in section 2, we discuss the adaptive equalization circuit. In section 3, we describe our proposed method for

a low power equalization circuit. In section 4, we show our experimental simulations and results. We present our conclusions in section 5.

2. Adaptive equalization circuit

2.1. Equalization circuit architecture

An example of architectures of equalization circuits is shown in Figure 1[7]. It consists of 3 parts listed below.

- Transversal filter
- Error evaluation
- Adaptive weight-control

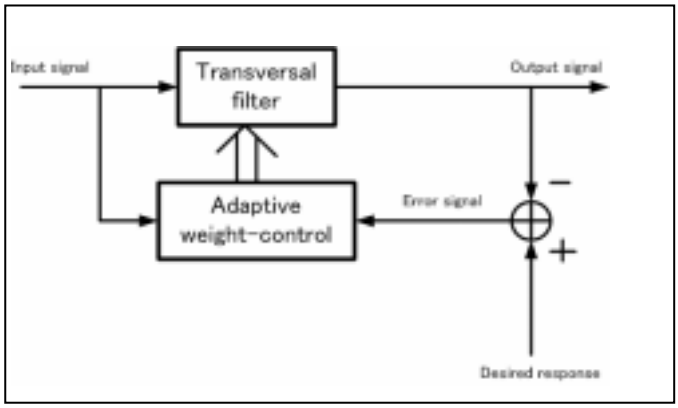

Figure 1: Architecture of equalization circuits

The output signals of the equalization circuits are calculated in the transversal filter. This operation can be described in Equation (1).

$$y(n) = \sum_{k=0}^{M-1} h_n(k) \cdot x(n-k) \qquad (1)$$

where $x(n)$, $y(n)$, and $h_n(k)$ represent data input of the filter, output of the filter, and k-th coefficient of the filter at time step n respectively. M is the number of taps of filter. This digital FIR filter consists of $M-1$ unit-delay elements, M multipliers, and $M-1$ adders.

The error evaluation part calculates the error signals which are the difference between output signals and desired signals.

The adaptive weight-control part calculates the tap weight vector. The Normalized Least Mean Square algorithm is often used as the filter coefficient updating algorithm.

2.2. Algorithms for equalizations

In this paper, we design the equalization circuit by using the Normalized Least Mean Square Algorithm. The Normalized Least Mean Square algorithm is described in Figure 2 [7].

・Parameter:

M = number of taps

μ = adaptation constant

・Initialization:

If the prior tap weight vector $\mathbf{h}_0$ is known, use an appropriate value. Otherwise, set $\mathbf{h}_0 = \mathbf{0}$.

・Data:

(a) given:

$\mathbf{u}(n)$ = M-by-1 tap input vector at time n

$$\mathbf{u}(n) = \begin{bmatrix} x(n) \\ \vdots \\ x(n-M+1) \end{bmatrix}$$

$d(n)$ = desired response at time step n

(b) to be computed:

$\mathbf{h}_{n+1}$ = estimation of tap weight vector at time step $n+1$

・Computation:

For $n = 0,1,2,\cdots$,

$$y(n) = \mathbf{h}_n^H \cdot \mathbf{u}(n)$$
$$e(n) = d(n) - y(n)$$
$$\mathbf{h}_{n+1} = \mathbf{h}_n + \frac{\mu \cdot e^*(n) \cdot \mathbf{u}(n)}{\|\mathbf{u}(n)\|^2}$$

Figure 2: Normalized Least Mean Square algorithm

3. Proposed technique for a low power equalization circuit

3.1. The power consumption model

In this paper, we discuss only circuits which are designed using CMOS process. The total power dissipation of CMOS transistors, P_{CMOS}, can be obtained from the sum of the three dissipation components[6]. P_{CMOS} is expressed by Equation (2).

$$P_{CMOS} = P_{dynamic} + P_{static} + P_{short} \quad (2)$$

where $P_{dynamic}$ is the dynamic power dissipation during the charging and discharging of the node capacitances. P_{static} is the static power dissipation caused by leakage current. P_{short} is the short-circuit power dissipation generated by the short-circuit current at the input rise and fall transition times.

The dominant source of power dissipation in CMOS circuits is the dynamic power dissipation expressed in Equation (3),

$$P_{dynamic} = \sum_{k} C_{load_k} \cdot Swit_k \cdot V_{DD_k}^2 \cdot freq_k \quad (3)$$

where C_{load_k} is the load capacitance of a gate g_k, $Swit_k$ is the switching ratio of g_k in one clock cycle, V_{DD_k} is the supply voltage, and $freq_k$ is the operating frequency.

In this paper, we only consider the case when C_{load_k}, V_{DD_k} and $freq_k$ are fixed. Our new technique can reduce the $Swit_k$ by controlling the bitwidth in the equalization circuit adaptively.

3.2. Our proposed technique

We propose a new technique for a low power equalization circuit using adaptive bitwidth control.

In general, the amount of calculation in an equalization circuit depends on the received signals which are with noise signals or multipath delayed signals propagated in the wireless channels. For example, equalization circuits need high processing requirements to eliminate the unnecessary signals when the received signals pass through by noisy channels with a large number of multipath channels. On the other hand, equalization circuits need less calculation to eliminate the unnecessary signals when the received signals pass through a less noisy channel. Hence, the amount of calculation required depends on the wireless channel environment.

In the compensation step, rough estimation in equalization will be held in the lower bitwidth when the error signals are big. On the other hand, detailed estimation will be held in the higher bitwidth when the error signals are small. Hence, the power consumption of equalization circuits can be reduced because they have a small amount of calculation. In short, the number of redundant operations in the variable coefficient digital filter can be reduced by using adaptive bitwidth control according to the magnitude of the error signals during equalization process.

4. Experimental results

4.1. Assumptions

We assume the following for the experiment.

- Noise signals are modeled by using white Gaussian noise.
- SNR is 20[dB].
- Some delayed signals are added in the received signals.
- The calculations in the equalization circuit are held in 2-16 bits.
- The overhead of the equalization circuit is ignored.
- The power consumption of the equalization circuit is known when the bitwidth of the equalization circuit is given.
- Input signals are expressed by sine waves.

4.2. Experimental results

We evaluated our technique for the low power equalization circuit. We designed two kinds of equalization circuits as listed below.

1. The equalization circuit which is designed in the fixed bitwidth (16 bits) of the variable coefficient filter.
2. The equalization circuit which is designed in the controllable bitwidth of the variable coefficient filter.

In this paper, we call the first equalization circuit a fixed bitwidth equalization circuit and the second equalization circuit an adaptive bitwidth equalization circuit. We evaluated the power consumption and the error magnitude using MATLAB [8].

Type of equalization circuit	Average power[mW]
Fixed bitwidth	130.10
Adaptive bitwidth	83.52 (34.5%)

Table 1: Average power consumption results

Figure 3 and figure 4 show the result of the error magnitude between output signals and desired signals. Especially, figure 4 shows the result of time step 1-100.

Figure 5 and figure 6 show the result of the power consumption at each time step. Figure 6 shows the result of time step 1-100. In these figures, the solid lines show the results of the fixed bitwidth equalization circuit and the dotted lines show the results of adaptive bitwidth equalization circuit. Table 1 shows the result of the average power consumption of two kinds of equalization circuits. The percentage number in round brackets in table 1 shows the reduction ratio compared with the fixed bitwidth equalization circuit.

Figure 3 and 4 show that the error magnitudes between the output signals and the desired signals in the fixed bitwidth equalization circuit and the adaptive bitwidth equalization circuit are almost the same. Figure 5 and 6 show the power consumption of the adaptive bitwidth equalization circuit can be reduced compared with that of the fixed bitwidth equalization circuit. The maximum reduction ratio of the power consumption in equalizing operations is about 69.8%. The average reduction ratio of the power consumption is about 34.5% as shown in table 1.

5. Conclusions

In this paper, we proposed a new technique for a low power equalization circuit using adaptive bitwidth control. The experimental results showed that our technique can reduce the power consumption by the experiment.

In the experiment, we ignored that the overhead of the equalization circuit and assumed that the power consumption is in proportion to the bitwidth of the equalization circuit. However, the input sequences are more important parameters for the power consumption than the bitwidth of the equalization circuit.

Our future works are listed below,

- To consider the overhead of the adaptive bitwidth control scheme in the evaluation of power consumption
- To consider the input sequence for low power techniques of the equalization circuits
- To apply our technique to the real applications of digital wireless communication systems.

6. Acknowledgements

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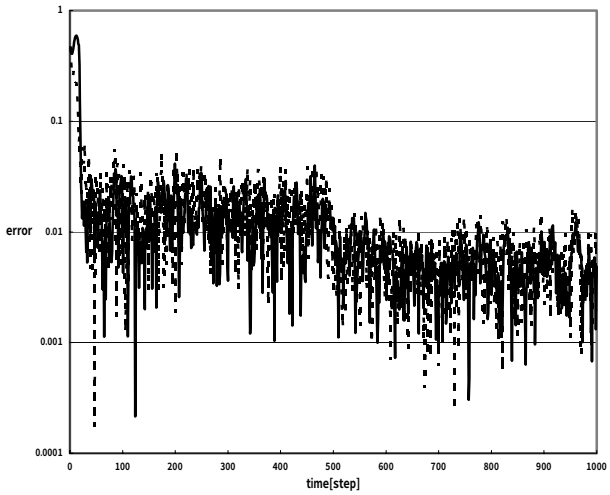

Figure 3, the result of the error magnitude

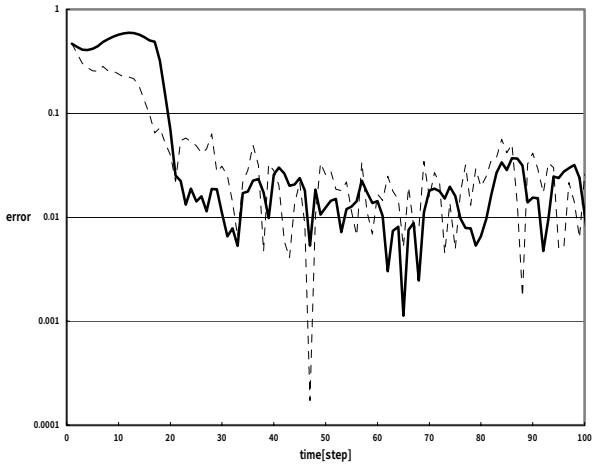

Figure 4, the result of the error magnitude
(from 1 to 100 time step)

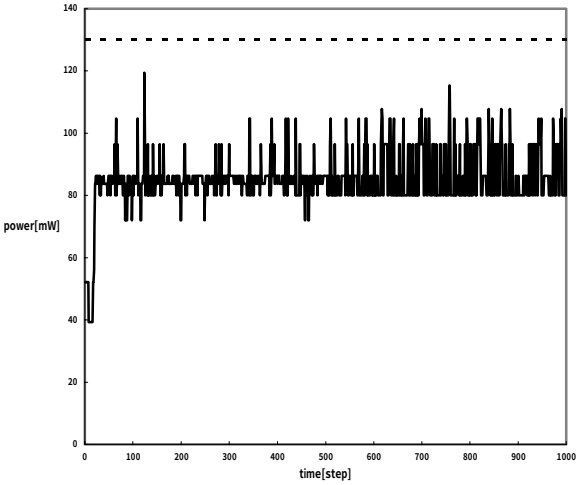

Figure 5, the result of the power consumption

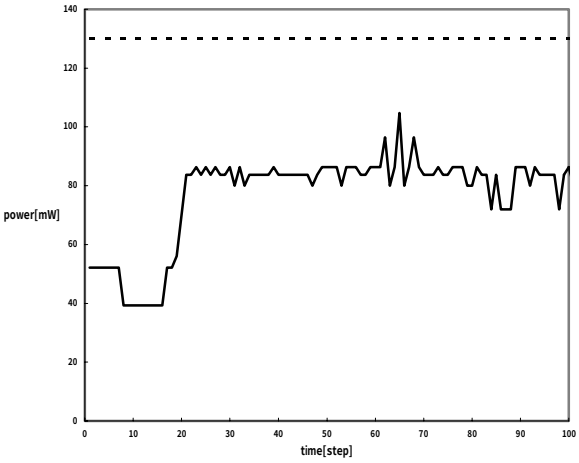

Figure 6, the result of the power consumption
(from 1 to 100 time step)