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A design method for a low power digital FIR filter in digital wireless communication systems

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1 Introduction

Recently, digital wireless communication technologies are very popular devices and used in various devices; cellular phones, wireless LAN (local area network) cards, PDAs, digital TVs, RF tags, IC cards, and so on. Design methodology of LSIs which contains digital wireless communication systems addresses to low power and low energy system implimentation, because of the growing need for longer battery lifetime and a restriction of power supply. For example, microsensor nodes are expected to operate from 5-10 year [1],[2],[3].

In wireless LAN systems, a digital baseband processor includes a lot of operations, such as modulate operations, demodulate operations, noise elimination operations, timing adjustment operations, error detections and corrections, and control operations. Due to incresing amount of operations, the power consumption and the area of circuit for digital baseband processing are increasing rapidly. Then, it is more important to develop design methodlogy which minimize power consumption of digiral baseband processing circuits.

Digital FIR filter should be designed to implement required accuracy of calculation specified by specification of communication system. High accurate calculations make digital FIR filters consuming a large power. Then, the demand of low power consumption digital FIR filter is increasing. A lot of design methods of low power digital FIR filters are proposed, for example, reducing multiple or add calculations [8],[9],[10], reducing the power consumption of adders and multipliers [11], reducing the amount of calculation using CSD expression [12], and so on.

The digital FIR filters are usually designed bit-serial in VLSI systems [13]. We observed that redundancy is included in the existing digital FIR filter circuits from experiments. Each operation does not use full size of bitwidth, and many parts of multipliers and adders are not actually used in the computation. So, we propose reduction of unused bits in the datapath and can minimize the area and power consumption of the digital FIR filter circuit.

The rest of this paper is organized as follows. In Section 2, we discuss the digital filter optimization. In Section 3, we describe the implimentation of low power digital filter. We conclude this paper in Section 4.

2 Digital filter optimization

2.1 Digital filter architecture

In general, a function of digital FIR filter is described by a simple convolution operation as the Equation(1) [4], [7],

$$y[n] = \sum_{k=0}^{N-1} h[k] \cdot x[n-k] \tag{1}$$

where $x[n]$, $y[n]$, and $h[n]$ represent data input of the filter, output of the filter, and a coefficient of the filter respectively. N is the number of taps of filter. This digital FIR filter consists of $N-1$ unit-delay elements, N multipliers, and $N-1$ adders. One example of digital FIR filters whose function is expressed by Equation(1) is depicted in Figure1 [4],[7].

A frequency response of this digital FIR filter is expressed by Equation(2)[4],[7],

$$H(f) \quad = \quad \sum_{k=0}^{N-1} h[k] \cdot e^{-j2\pi fTk} \tag{2}$$

where T is sampling time. In this digital FIR filter, input signals, output signals, and coefficient parameters of this filter are expressed by signed

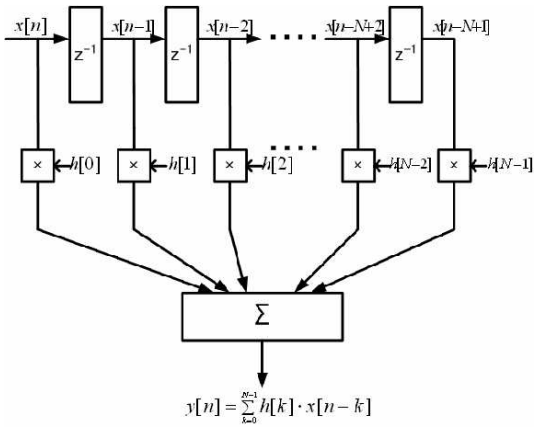

Figure 1: Example of digital FIR filter structure

digit, fixed point number and 2s-compliment. n-bit signed digit and fixed point number is expressed by Equation(3).

$$\begin{aligned} X &= [x_{n-1}, x_{n-2}, \cdots, x_1, x_0] \\ &= \frac{1}{2^{n-1}} \cdot (-2^{n-1} \cdot x_{n-1} + \sum_{i=0}^{n-2} 2^i \cdot x_i) \quad (3) \end{aligned}$$

$$x_i \in \{0, 1\}, i = 0, 1, ..., n-1$$

2.2 CMOS power dissipation model

In this paper, we discuss circuits which are designed in CMOS process. Total power dissipation of CMOS transisters, P_{CMOS}, can be obtained from the sum of the three dissipation components[5]. P_{CMOS} is expressed by Equation(4).

$$P_{CMOS} = P_{dynamic} + P_{static} + P_{short} \quad (4)$$

where $P_{dynamic}$ is the dynamic power dissipation produced during charging and discharging of the node capacitances. P_{static} is the static power dissipation caused by leakage current. P_{short} is the short-circuit power dissipation generated by the short-circuit current at the input rise and fall times.

The dominant source of power dissipation in CMOS circuits is the dynamic power dissipation expressed by Equation(5),

$$P_{dynamic} = \sum_k CL_k \cdot Swit_k \cdot V_{DD_k}^2 \cdot freq_k \quad (5)$$

where CL_k is the load capacitance of a gate g_k, $Swit_k$ is the switching ratio of g_k in one clock cycle, V_{DD_k} is the supply voltage, and $freq_k$ is the operating frequency.

2.3 Bitwidth optimization for a low power digital FIR filter

For Equation(1), digital FIR filter has a lot of arithmetic operations. In general, arithmetic operation modules, such as adder and multiplier module, consume much power, energy, and circuit area. Input bitwidth of the modules is quite important design parameter for low power. The number of adder and multiplier module is very important, too. The number of adder and multiplier module is proportional to the number of taps of digital FIR filter circuits. Bitwidth of input signal and filter coefficient is related to the scale of the circuit of adder and multiplier modules[5].

The power of digital FIR filter circuit is reduced by optimization of the taps and bitwidth of input signal and filter coefficients. The multiplier modules in digital FIR filter circuit must be designed for low power and small circuit area.

Until now, many digital filters are designed in the same bitwidth as all datapath modules. We can find out that internal operations of digital filter circuit have a lot of redundant operation. Those redundant operations can be reduced, as long as output value of digital filter has no fault. Our approach is to reduce bitwidth of input signal and filter coefficient as long as output specification of digital filter circuit is sufficient.

In short, we analysis sufficient bitwidth of each multiplier module and each adder module of digital filter circuit. Each bitwidth of digital filter internal operation is optimized using these analysis results[13].

2.3.1 Assumptions

We assume the following to simplify the optimization problem of degisning the low power digital FIR filter circuit.

- the filter calculation is held in fixed-point, and two-s complemental.
- the filter coefficients, $h[k]$ can be calculated in real numbers if a frequency response and a number of taps of a FIR filter are given.
- filter coefficients can be calculated if a bitwidth of $h[k]$ is given.
- input signal $x[n]$ has a characteristic listed below,

$$E(x[n]) = 0$$

$$E(x[n] \cdot x[m]) = \begin{cases} 0, & m \neq n \\ \sigma^2, & m = n \end{cases} \quad (6)$$

Here, $E(X)$ is an average of X.

2.3.2 Notation

We define the parameters of formulation as follows.

- $h_i[k]$, $x_i[k]$, $y_i[k]$: the approximate value of $h[k]$, $x[k]$, and $y[k]$ expressed by i-bit two-s complemental
- $\Delta h_i[k]$: an error generated by expressing $h[k]$ in i-bit two-s complemental, $\Delta h_i[k] = h[k] - h_i[k]$
- m_k : bitwidth of $h[k]$
- bit_{in} : bitwidth of input signal
- tap_{min}, tap_{max} : minimum length of taps, maximum length of taps
- bit_{min}, bit_{max} : minimum bitwidth, maximum bitwidth
- p_{ki} : a parameter of usage that $h[k]$ is expressed in i-bit two-s complemental number

$$\sum_{i=bit_{min}}^{bit_{max}} p_{ki} = 1, for\ \forall k \quad (7)$$

- $D(f)$: a frequency response of designed digital FIR filter
- $S(f)$: a frequency response specification of a digital FIR filter
- $\varepsilon(f)$: a relative error between $D(f)$ and $S(f)$ in frequency domain. $\varepsilon(f)$ is expressed in complex number.

$$\varepsilon(f) = \frac{D(f)}{S(f)}$$

- $A_\varepsilon(f), \phi_\varepsilon(f)$: a function of an amplitude characteristic and a phase characterristic of a frequency response,$\varepsilon(f)$.

$$\begin{aligned} A_\varepsilon(f) &= \mid \varepsilon(f) \mid \\ \phi_\varepsilon(f) &= \angle\varepsilon(f) \end{aligned}$$

- $\varepsilon_A^l(f), \varepsilon_A^u(f)$: a lower bound or an upper bound of a permissible error of an amplitude characterristic
- $\varepsilon_\phi^l(f), \varepsilon_\phi^u(f)$: a lower bound or an upper bound of a permissible error of a phase characteristic
- δ : a permissible error of output signal

2.3.3 Problem definition

We define the problem that is to find a set of bitwidth of each coefficient to minimize a total power consumption of the digital FIR filter with keeping accuracy of filter calculation. The accuracy of filter calculation is defined by using the relative error of the frequency response, $\varepsilon(f)$, and output error.

Here, constraints of keeping accuracy of the filter calculation are below,

- the relative error between the specification and designed filter, expressed by Equation(8)

$$\begin{aligned} \varepsilon_A^l(f) \leq &\ A_\varepsilon(f) \ \leq \varepsilon_A^u(f) \\ \varepsilon_\phi^l(f) \leq &\ \phi_\varepsilon(f) \ \leq \varepsilon_\phi^u(f) \end{aligned} \quad (8)$$

- the output error calculataing some sample input, expressed by Equation(9)

$$\mid y[n] - y_{ex}[n] \mid \leq \delta \quad (9)$$

Here, we discuss these constraints. $y[n]$ is approximated by Equation(10), and $y_{ex}[n]$, and $\Delta y[n]$ are defined below respectively,

$$\begin{aligned} y[n] &= \sum_{k=0}^{N-1} h[k] \cdot x[n-k] \\ &= y_{ex}[n] + \Delta y[n] \\ y_{ex}[n] &= \sum_{k=0}^{N-1} h_{ex}[k] \cdot x[n-k] \\ \Delta y[n] &= \sum_{k=0}^{N-1} \Delta h[k] \cdot x[n-k] \end{aligned} \quad (10)$$

$h[k]$ is expressed in Equation(11) using p_{ki}, $h_{ex}[k]$, and $\Delta h[k]$,

$$\begin{aligned} h[k] &= h_{ex}[k] + \Delta h[k] \\ h_{ex}[k] &= \sum_{i=bit_{min}}^{bit_{max}} (h_i[k] \cdot p_{ki}) \\ \Delta h[k] &= \sum_{i=bit_{min}}^{bit_{max}} (\Delta h_i[k] \cdot p_{ki}) \end{aligned} \quad (11)$$

In short, the constraints about amplitude characteristics and phase characteristics can be expressed

with the only p_{ki} parameter using Equation(6), (8), (9), (10) and (11). Equation(12), (13) and (14) are expressed as the constraint about the amplitude characteristic, the phase characteristic and the output error for any frequency value.

$$\sum_{k_1=0}^{N-1}\sum_{k_2=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}}\sum_{j=bit_{min}}^{bit_{max}} a_{ij}[k_1,k_2]\cdot p_{k_1i}\cdot p_{k_2j} \geq b^l$$
$$\sum_{k_1=0}^{N-1}\sum_{k_2=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}}\sum_{j=bit_{min}}^{bit_{max}} a_{ij}[k_1,k_2]\cdot p_{k_1i}\cdot p_{k_2j} \leq b^u \quad (12)$$

$$\sum_{k=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}} c_i^l[k]\cdot p_{ki} \leq 0$$
$$\sum_{k=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}} c_i^u[k]\cdot p_{ki} \geq 0 \quad (13)$$

$$\sum_{k=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}}\sum_{j=bit_{min}}^{bit_{max}} d_{ij}[k]\cdot p_{ki}\cdot p_{kj} \leq \delta^2 \quad (14)$$

where,

$$a_{ij}[k_1,k_2] = h_i[k_1]h_j[k_2]\cos 2\pi fT(k_1-k_2)$$

$$b^l = \varepsilon_A^l(f)\sum_{k_1=0}^{N-1}\sum_{k_2=0}^{N-1} h[k_1]h[k_2]\cos 2\pi fT(k_1-k_2)$$

$$b^u = \varepsilon_A^u(f)\sum_{k_1=0}^{N-1}\sum_{k_2=0}^{N-1} h[k_1]h[k_2]\cos 2\pi fT(k_1-k_2)$$

$$c_i^l[k] = h_i[k]\tan\varepsilon_\phi^l(f)\sum_{k_1=0}^{N-1} h[k_1]\cos 2\pi fT(k-k_1) - h_i[k]\sum_{k_1=0}^{N-1} h[k_1]\sin 2\pi fT(k-k_1)$$

$$c_i^u[k] = h_i[k]\tan\varepsilon_\phi^u(f)\sum_{k_1=0}^{N-1} h[k_1]\cos 2\pi fT(k-k_1) - h_i[k]\sum_{k_1=0}^{N-1} h[k_1]\sin 2\pi fT(k-k_1)$$

$$d_{ij}[k] = \sigma^2\Delta h_i[k]\Delta h_j[k]$$

The power consumption of digital FIR filter, P_{total}, can be estimated by Equation(15),

$$P_{total} = \sum_{k=0}^{N-1} P_{mult_k} + \sum_{k=1}^{N-1} P_{add_k} + \sum_{k=1}^{N-1} P_{sr_k} \quad (15)$$

where P_{mult_k} is power consumption of k-th multiplier, P_{add_k} is power consumption of k-th adder, P_{sr_k} is power consumption of k-th shift register, respectively. In this problem definition, we approximate the power consumption of a digital FIR filter as Equation(16) for simplicity, assuming that the power consumption of multipliers is dominant in the digital FIR filter. And the power consumption of multipliers is in proportion to the circuit area which is almost the same as the product of bitwidths of 2 input signals when supply voltage and operation frequency are fixed.

$$P_{total} \cong Const\cdot\sum_{k=0}^{N-1} m_k\cdot bit_{in} \quad (16)$$

A bitwidth of a filter coefficient can be approximated by using the parameter p_{ki}. It is expressed by Equation(17).

$$m_k = \sum_{i=bit_{min}}^{bit_{max}} i\cdot p_{ki} \quad (17)$$

p_{ki} is the only variable parameter in the target function and the constraint functions. The other parameters are constant parameters.

Then, we can define the problem to find bitwidth of each filter coefficient,

$$\begin{aligned} Minimize &: P_{total} = Const\cdot\sum_{k=0}^{N-1}\sum_{i=bit_{min}}^{bit_{max}} bit_{in}\cdot i\cdot p_{ki} \\ Subject\ to &: b^l \leq w^tAw \leq b^u \\ &\quad C^lw \leq 0 \\ &\quad C^uw \geq 0 \\ &\quad w^tDw \leq \delta^2 \end{aligned}$$

where A, C^l, C^u, and D are matrixes of constant parameters. And, the elements of A, C^l, C^u, and D are defined by Equation(12), (13), (14). w is a vector defined by using p_{ki} as follows,

$$w = \begin{bmatrix} p_{0bit_{min}} \\ \vdots \\ p_{ki} \\ \vdots \\ p_{(N-1)bit_{max}} \end{bmatrix} \quad (18)$$

For given the constant parameters, find the variable parameters, p_{ki}, to minimize the power consumption of digital FIR filters satisfying the constraints about keeping calculation accuracy of filtering.

Table 1: specification of digital FIR filter circuit

sampling rate	22MHz
cut off frequency	5.5MHz
stopband relative amplitude	-30dB
bitwidth of input signal	8-bit
bitwidth of output signal	8-bit
throughput	22Msample/sec
characteristic	root cosine roll off

3 Experimental result

3.1 Specification of a target digital filter

The specification of digital FIR filter circuit is represented in Table1.

Here, it shows what is cosine roll off spectrum filter. A cosine roll off filter is often used in digital wireless communication systems, because it is satisfied the Nyquist criterion. The Nyquit criterion is a criterion whether intersymbol interference is occured or not. A frequency response of cosine roll off filter is expressed by Equation(19) [4],[6].

$$H(f) = \begin{cases} 1, & |f| \leq \frac{1-\alpha}{2T} \\ \frac{1}{2}\{1 - \sin\frac{\pi T}{\alpha}(|f| - \frac{1}{2T})\}, & \frac{1-\alpha}{2T} \leq |f| \leq \frac{1+\alpha}{2T} \\ 0, & \text{otherwise} \end{cases} \tag{19}$$

3.2 Experimental result

We evaluate our approach for a low power digital baseband processing. In this evaluation, our target specification of the digital FIR filter is a cosine roll off filter. The tap length of the digital FIR filter is fixed. We evaluate the power consumption and the circuit area of those digital FIR filter circuits. Three kinds of digital FIR filters are designed and evaluated. First one, we call it 16-bits coefficient in Table2 and Table3, is designed as an example of a high accurate digital FIR filter that all datapath bitwidth of are the same as 16-bits. Second one, we call it 8-bits coefficient in Table2 and Table3, is designed as an example of a low accurate digital FIR filter that all datapath bitwidth of are the same as 8-bits. The bitwidth of this digital FIR filter, 8-bits, is the minimum bitwidth in the FIR filters whose all datapath bitwidth are the same. Third one, we call it optimized bitwidth in Table2 and Table3, is designed by using our approach. The bitwidth of each filter coefficient in this digital filter is optimized.

Table 2: power consumption of digital FIR filter circuit

digital filter	power consumption(mW)
16-bits coefficient	1248
8-bits coefficient	502
optimized bitwidth	450

Table 3: circuit area of digital FIR filter circuit

digital filter	circuit area(μm^2)
16-bits coefficient	494679
8-bits coefficient	261372
optimized bitwidth	230908

In the digital FIR filter optimized by using our approach, this digital filter has some kinds of bitwidths of filter coefficients. The maximum bitwidth of filter coefficients is 10-bits. The minimum bitwidth is 3-bits.

We search the optimized bitwidth of each digital FIR filter coefficient using MATLAB[15]. After the bitwidths of filter coefficients are decided, we design the digital FIR filter using verilog-HDL. Then we evaluate the power consumption and the circuit area of the digital FIR filter with all modules such as multipliers, adders, and shift registers. We estimate the power consumption at transistor level simulation using Nanosim (Synopsys Inc.). We estimate the circuit area using the report of Design-Compiler (Synopsys Inc.).

We show the result of the power consumption in Table2 and the circuit area in Table3 at the case that output bitwidth is 8-bits.

Table2 shows the power dissipation of digital FIR filter, which we design coefficients as 16-bits, 8-bits, and optimized bitwidth. Table3 shows the circuit area. Table2 shows that the power consumption of digital FIR filter optimized by our approach is about 63.8% reduction compared with the filter designed in 16-bits, about 10.0% reduction compared with the filter designed in 8-bits, respectively. Table3 shows that the circuit area of digital FIR filter optimized by our approach is about 53.3% reduction compared with the filter designed in 16-bits, about 11.7% reduction compared with the filter de-

signed in 8-bits, respectively. This results show that our approach is very effective for a low power design of digital FIR filters.

4 Conclusions

In this paper, we have proposed a novel approach for a design method of a low power digital baseband processing. In particular, we focus on a digital FIR filter that is a part of the digital baseband processing. Our approach is to optimize the bitwidth of each filter coefficient. We define the problem to find optimized bitwidth of each filter coefficient. It took long time to solve the problem which we define in this paper. We show effective results for low power and small circuit area by the experiment.

We have some future works. One is developing algorithms to solve the problem faster.

Our approach can be applied to not only the digital FIR filters of digital wireless communication systems but also general digital signal processing.

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