Test architecture exploration on reconfigurable scan chain network

Sugihara, Makoto
Institute of Systems & Information Technologies/KYUSHU

Murakami, Kazuaki
Department of Computer Science and Communication Engineering, Kyushu University

出版情報：IEEE International Symposium Pacific Rim Dependable Computing, pp.41-42, 2004-03.
IEEE Computer Society
バージョン：
権利関係：

Test Architecture Exploration on Reconfigurable Scan Chain Network

Makoto Sugihara
Institute of Systems &
Information Technologies/KYUSHU
sugihara@isit.or.jp

Kazuaki Murakami
Department of Computer Science &
Communication Engineering, Kyushu University
murakami@i.kyushu-u.ac.jp

Abstract

In this paper, a test architecture exploration on reconfigurable scan chain network is discussed. Reconfigurable scan chain network enables system integrators to optimize their test designs without modification and accelerates the reuse of cores. Our method can achieve both short turn-around-time and test design optimization without redesigning legacy cores.

1 Introduction

Recent significant advances in semiconductor technology have been increasing the number of transistors available on a chip dramatically. This increases the numbers of both faults to be tested and patterns to be applied. The testing cost is, consequently, increasing prohibitively.

The gap between functionality available on a chip and design productivity is growing up and the reuse of predesign and pre-verified cores is getting quite important. It is essential to avoid redesign circuits including DFT (Design For Testability) ones to achieve short turn-around-time (TAT).

In this paper, test architecture exploration on reconfigurable scan chain architecture (RSCA) is proposed which can achieve both short test time and short TAT. RSCA can avoid redesigning legacy cores by varying the lengths of scan chains and optimizing test designs. It can also reduce the computation to obtain optimal test architecture because the size of exploration space to be sought out can be reduced due to the structure of RSCA.

2 Reconfigurable Scan Chain Architecture

In this section, a reconfigurable scan chain architecture (RSCA) is discussed. RSCA can achieve both short TAT and short computation time by varying the lengths of scan chains. RSCA makes it possible that system integrators finish designing their SOCs without redesigning intellectual property because the test design for the SOCs can be optimized by reconfigurating the scan chain network instead of redesigning them. An example of RSCA is shown in Figure 1. A scan chain is split by multiplexers and multiple scan chains can be virtually used to reduce the testing time and cost for SOC without any redesign. Scan Chain Reconfiguration Controller (SCRC) can control how the total scan chain should be split and it can be implemented with programmable memory such as RAM. If RAM is adopted in a design, the design might be able to reconfigure the scan chain network dynamically in order to reduce testing time. This is out of this paper and should be a future work on this

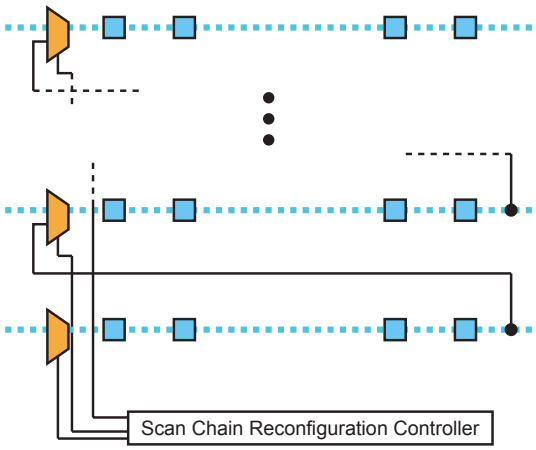

Figure 1. Reconfigurable scan chain arc.

architecture. In this paper, it is assumed that scan chains are reconfigured at the beginning of testing and SCRC is to keep the configuration until the testing is finished. Note that core designers should make a decision on how many and long scan chains are implemented by the SCRC. Multiplexer configuration depends on the implementation of SCRC. Let us examine an SCRC implementation for Module 5 on d695 of ITC '02 benchmark. Test design for the module is shown in Table 1. An example of the implementation of SCRC for Module 5 on d695 of ITC '02 benchmark is shown in Table 2.

Table 1. Test design for Module 5 on d695.

Patterns	110
Inputs	32
Outputs	304
Bidirs	0
Scan Chains	18 45-bit-long chains 14 44-bit-long chains

Table 2. A configuration for Module 5 of d695.

Configuration	1	2	3	4	5	6
TAM width (# Scan chains)	32	16	8	4	2	1
Max Length	55	109	217	433	865	1729
Test Time [cycles]	6215	12209	24197	48173	96125	192029

In this example, 2^n scan chains (the widths for TAM) are available for $0 \leq n \leq 5$ in compliance with the requirement of system integrators, though the other ways of implementation are also available. The whole scan chain is split into 18 45-bit-long chains and 14 44-bit-long chains by multiplexers in this example. 3 bit memory would be enough to control the multiplexers to realize the configurations of Table 2. In contrast with the RSCA shown in Figure 1, TAM width adaptation by redesign for Module 5 of d695 is shown

Table 3. TAM width adaptation by redesign for Module 5 of d695.

TAM width	1	2	3	4	5	6	7	8
Max Length	1730	865	577	433	346	289	248	217
Test Time [cycles]	191874	95992	64070	48106	38516	32167	27613	24163

9	10	11	12	13	14-15	16	17	18	19
193	177	158	145	134	133	109	102	97	92
21518	19757	17624	16194	14983	14873	12192	11420	10869	10319

20-24	25-31	32	33	34	35	36	37	38	39
89	88	55	53	51	50	49	47	46	45
9989	9878	6206	5985	5765	5655	5545	5325	5215	5105

in Table 3. Redesigning is so flexible to optimize the test design of the SOC but the flexibility might lead to impractical computation time to optimize the test design because it makes the optimization process more complex to solve.

3 Optimal Assignment of Cores to TAMs

In this section, test architecture exploration is discussed. First, let us define Problem $\mathcal{P}_{\mathrm{Raw}}$ to reduce testing time for SOC. We basically adopted the notation introduced in [1] except for R. R derives from Reconfigurable Scan Chain Architecture.

- $\mathcal{P}_{\mathrm{Raw}}$: Given an SOC having N_C cores, N_B TAMs of widths $w_1, w_2, \cdots, w_B$, and reconfigurable scan chains for all cores, determine an assignment of cores to TAMs, and configuration of SCRC such that the total testing time is minimized.

This problem is $\mathcal{NP}$-hard as well as in [1]. To model this problem, consider an SOC consisting of N_C cores, N_B TAMs of widths $w_1, w_2, \cdots, w_B$, and reconfigurable TAM architecture of widths $b_{i1}, b_{i2}, \cdots, b_{iB_i}$ for Core i, where B_i is the number of confiugration for Core i which is available to system designers. If Core i is assigned to TAM j, let the time taken to test Core i be given by $T_i(w_j)$ clock cycles. The testing time $T_i(w_j)$ is calculated as $T_i(w_j) = T_i(b)|_{b=\max_k b_{ik}, b_{ik} \le w_j} = (1+s) \cdot p_i + s$, where p_i is the number of test patterns for Core i and s is the length of the longest wrapper scan chain. Let introduce 0-1 variables x_{ij} (where $1 \le i \le N_C$ and $1 \le j \le N_B$), which are used to determine the assignment of cores to TAMs in the SOC.

$$x_{ij} = \begin{cases} 1 & \text{if Core } i \text{ is assigned to TAM } j, \\ 0 & \text{otherwise.} \end{cases} \quad (1)$$

The time needed to test all cores on TAM j is given by $T_{\mathrm{TAM}_j} = \sum_{i=1}^{N_C} T_i(w_j) \cdot x_{ij}$. The testing time for the SOC is given by $T_{\mathrm{SOC}} = \max_j T_{\mathrm{TAM}_j} = \max_j \sum_{i=1}^{N_C} T_i(w_j) \cdot x_{ij}$. A mathematical model for optimal core assignment to TAM is given as follows.

Objective: Minimize $\mathcal{T}$, subject to

1. $\mathcal{T} \ge \sum_{i=1}^{N_C} T_i(w_j) \cdot x_{ij}$, $1 \le j \le B$.
2. $\sum_{j=1}^{B} x_{ij} = 1$, $1 \le i \le N_C$.

The above 0-1 ILP can be easily solved within less a second.

4 Optimal Test Architecture

In this section, we discuss how to obtain the optimal test architecture. First, let us define Problem $\mathcal{P}_{\mathrm{Rnpaw}}$ to reduce testing time for SOC. We basically adopted the notation introduced in [1], except for R. R derives from Reconfigurable Scan Chain Architecture.

- $\mathcal{P}_{\mathrm{Rnpaw}}$: Given an SOC having N_C cores and a total TAM width W, obtain the number of TAMs, the widths of TAMs, an assignment of cores to TAMs such that the total testing time is minimized.

To solve this problem, all possible combinations for TAM widths and numbers are enumerated. A pseudo-code is shown in Figure 2. The most important part in this procedure is that there are many times of iteration skipped in the enumeration of partitioning the total TAM widths. This is quite probable because RSCA offers less resolution on varying w.

RSCA Optimization Algorithm

```
Procedure OptimizeRSCA
Input W_SOC: The total bits of all TAMs.
Input T_i(w): Test time for Core i when the width of TAM is w.
Output b: Optimal TAM bits distribution.
Output Optimal core assignment to TAMs.
begin
  forall partitions of TAM width W do
    if this formulation is different from the previous
      iteration then
        Solve P_Raw by an LP solver.
        if a better core assignment and TAM configuration
          are obtained then
            Record the core assignment
            and TAM configuration.
        endif
    endif
  endfor
end
```

Figure 2. Test architecture optimization algorithm.

5 Conclusion

We proposed a reconfigurable scan chain architecture (RSCA) which enables short design time and short computation time to obtain an optimal test architecture. RSCA accelerates design reuse because system designers can save the time for redesigning by reconfiguring the scan chain network. Moreover, RSCA can reduce the computation time to obtain the optimal test architecture because it achieves less search space, that is, less enumeration.

References

[1] V. Iyengar, K. Chakrabarty and E. J. Marinissen, "Test wrapper and test access mechanism co-optimization for system-on-a-chip," *Journal of Electronic Testing: Theory and Applications*, vol. 18, pp. 213–230, April 2002.

[2] Y. Zorian, E. J. Marinissen and S. Dey, "Testing embedded core based system chips," *IEEE International Test Conference*, pp. 130–143, 1998.

[3] IEEE P1500 Standard for Embedded Core Test. *http://grouper.ieee.org/groups/1500/*.