Development of CMOS Coplanar Waveguide Matching Circuit for RF Front-end

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DEVELOPMENT OF CMOS COPLANAR WAVEGUIDE MATCHING CIRCUIT FOR RF FRONT-END

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For realizing a single chip microwave front-end, we studied the new design theory of impedance matching circuits for a Si-CMOS low noise amplifier (LNA) or power amplifier (PA), which are composed of coplanar waveguide (CPW) meanderline resonators and impedance inverters. We also present the simulated performances of CMOS-LNA or PA connected with input and output matching circuits. Finally, we designed the trial chip for 2.4GHz wireless LAN (IEEE 802.11b) system.

1. Introduction

There are many location-free data translations, such as wireless LAN, bluetooth, IMT-2000 and satellite telecommunications. In order to make size reduction and cost performance, there are great expectations of a single chip RF-CMOS LSI, which is composed of low noise amplifier (LNA), power amplifier (PA), mixer, and so on [1]. Fig.1 shows the typical block diagram of RF section of the wireless terminal. Impedance matching circuit is necessary for interconnecting above devices. Although the lumped element circuits such as the spiral inductor and MIM capacitor are adopted for matching circuit [2], it cannot be used at high frequency range because of the self-resonance and stray impedances. On the other hand, distributed elements made of transmission lines are particularly effective because their size becomes smaller, as the frequency is higher. Moreover, coplanar waveguide (CPW) is easy to fabricate on the CMOS chip because the signal line and ground plane exist only on the same side, and also easy to realize desired characteristic impedance.

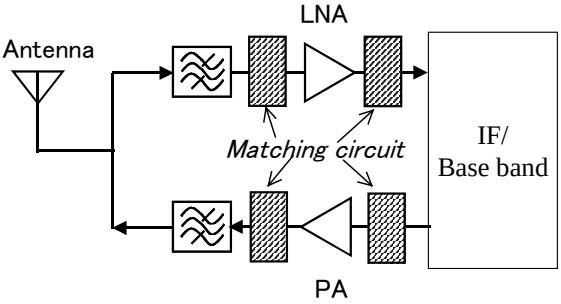


Fig.1. Brock diagram of the RF front-end.

In our previous papers [3,4], we proposed a new design method of the broadband impedance matching circuit for the small antenna. In this paper, we generalize the design method of the on-chip matching circuit connecting with the LNA or PA. The circuit simulator and electromagnetic field simulator studies provide the expected performances of the LNA or PA with the input and output impedance matching circuit.

2. Design of CMOS low noise amplifier (LNA)

Fig.2 shows the schematic diagram of low noise amplifier (LNA). The gate length is 0.25μm and VDD is 2.5V. The characteristics are simulated by the ADS (Agilent technologies).

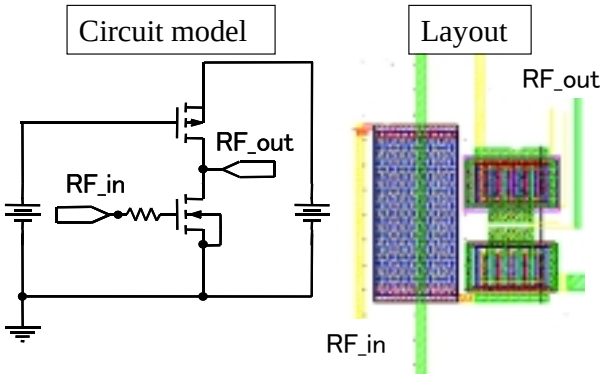


Fig.2. Circuit model and layout of LNA (0.25μm process).

The noise figure (F) is calculated as,

$$F = 1 + \frac{1}{G_S}\left(G_n + R_n\left|Y_S + Y_C\right|^2\right) = F_{\min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 \quad (1)$$

$$F_{\min} = 1 + 2R_n(G_c + G_{opt}) \quad (2)$$

where, $Y_{opt}=G_{opt}+jB_{opt}$, $G_{opt}=(G_c^{\,2}+G_n/R_n)^{1/2}$ and $B_{opt}=-B_c$. F_{min}, R_n and Y_s ($=G_s+jB_s$) are the

minimum noise figure, equivalent noise resistance and source admittance, respectively. In the noise simulation, we suppose that Y_c ($=G_c+jB_c$) (correlation admittance) is approximated to Y_{in} (input admitance) [5]. The simulated maximum available power gain ($G_{a(max)}$) and the noise circle of LNA are shown in Fig.3 and Fig.4, respectively. At 2.45GHz, we obtain Z_{opt}=390+j190 (Ω), where Z_{opt} ($=1/Y_{opt}$) is the impedance which minimize the noise figure. Also, the input and output impedances are Z_{in}=321–j871[Ω] and Z_{out}=133-j121[Ω], respectively.

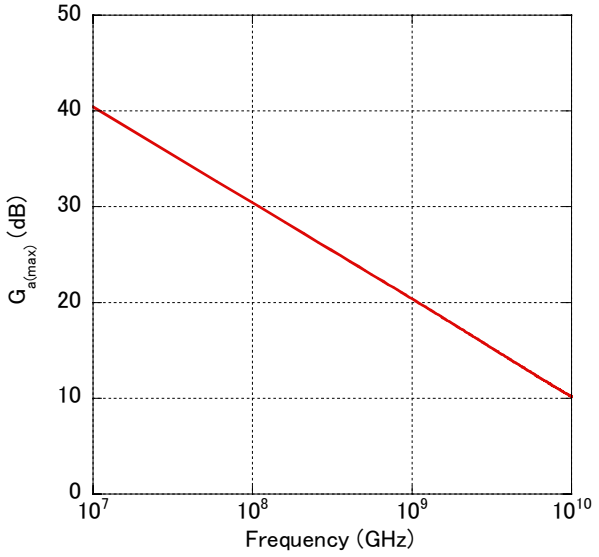


Fig.3. Frequency dependence of the maximum available power gain.

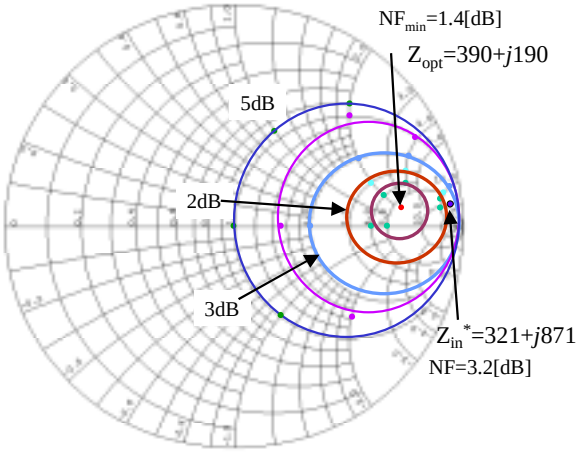


Fig.4. Noise circle at 2.45GHz.

3. Design theory of on chip impedance matching circuit

Fig.5(a) shows the circuit model of the 1-pole BPF. In this figure, Z_0, w and g_i are the characteristic impedance of the transmission line, normalized bandwidth and normalized filter element, respectively. The reactance (X) and the reactance slope parameter (x) are for the series resonance circuit. At the resonant frequency (ω_0), the impedance inverters (K-inverters) of the 1-pole BPF are given by [4],

$$K_{0,1}=\sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}},$$
$$K_{1,2}=\sqrt{w}\sqrt{\frac{x_1 Z_0}{g_1 g_2}},\quad X_1=x_1\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right) \qquad (3)$$

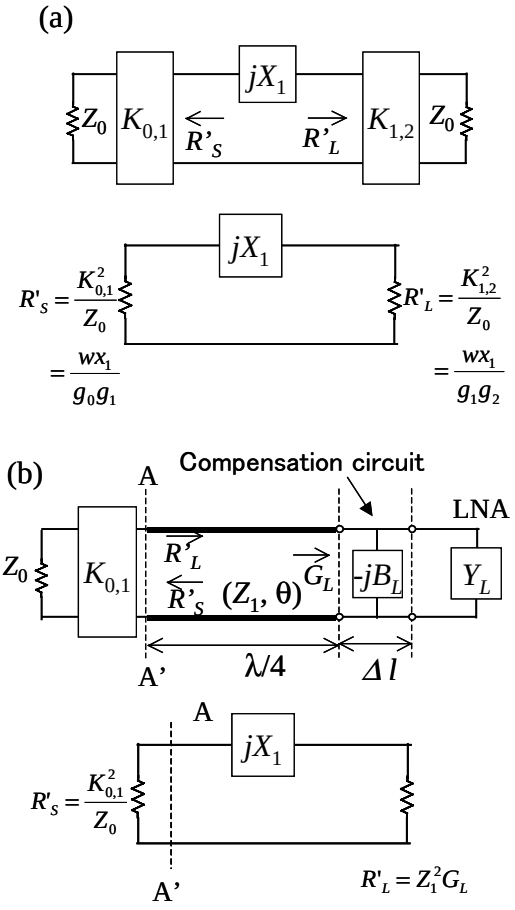


Fig.5. Circuit models of (a) 1-pole bandpass filter and (b) quarter wavelength matching circuit.

Fig.5(b) shows the circuit model of the quarter wavelength matching circuit. In the figure, Y_L ($=G_L+jB_L$) and Z_1 are the input impedance of the LNA and characteristic impedance of the quarter wavelength line, respectively. In order to compensate the jB_L, we adjust the length by $\Delta\ell$ as (see Fig.5(b)),

$$\Delta\ell = -\frac{B_L}{\omega_0 C}, \qquad (4)$$

where, C is the capacitance per unit length of the transmission line. Finally, by comparison of the R'_s and R'_L in the Fig.5(a) and (b), the proposed design values for the K-inverter and Z_1 are given by,

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4} Z_1\right), \quad Z_1 = \frac{\pi}{4}\frac{w}{g_1 g_2 G_L}. \quad (5)$$

In the case of noise matching, it is easy to show $Z_L = Z^*_{opt}$ in eqs. (4) and (5).

4. Layout of LNA connected with CPW input and output impedance matching circuit

Fig.6 shows the sectional views of the CPW structure and EM-simulated condition of the CMOS chip. This chip has a 5-metal layer structure. In order to avoid the loss in the Si, we covered the lowest metal (metal1), namely conductor backed CPW. For suppressing the conductor loss, metal4 and metal5 are connected with a large number of vias, where a conductance of the metal is 4.1×10^7 S/m in this simulation. The signal width and the interval between the slots of the 50Ω line are 5μm and 13μm, respectively. The EM simulated quality factor of the CPW straight resonator is Q_u=68 at 2.45GHz. For size reduction, the quarter wavelength line was bended into meander structure. The design parameters of the matching circuit are f_0=2.45GHz, w=100MHz (IEEE 802.11b). Fig. 7 shows the layout of the quarter wavelength impedance matching circuit on the Si substrate. K-inverter is fabricated by using shunt meander inductor. The chip aria of the input matching circuit is $0.2mm^2$, which is 40% as small as that of the spiral inductor (lumped element).

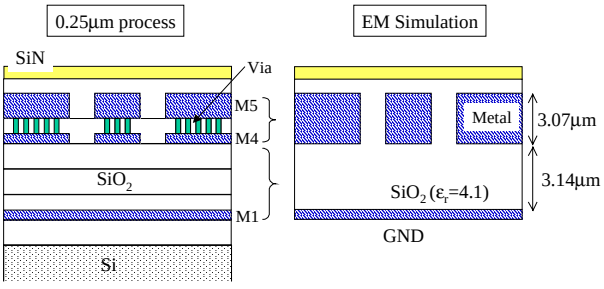


Fig.6. Sectional views of the real process and EM-simulated condition.

Fig. 8 shows the EM simulated input return loss and insertion loss of the matching circuit. Fig. 9 shows the frequency dependence of the input impedance. The return loss (S_{11}) and the input resistance are almost similar to the data calculated from eq. (5) (theoretical curve). Although, the insertion loss in the passband appears because of the metal loss, the R_{in} and X_{in} are matched to Z_0 (=50+j0Ω) at the center frequency.

Fig. 10 shows the chip layout of the LNA and PA with input and output impedance matching circuit, namely there are 4 matching sections. The chip size is 5mm x 5mm. The input and output port are connected with the CPW pads for measuring.

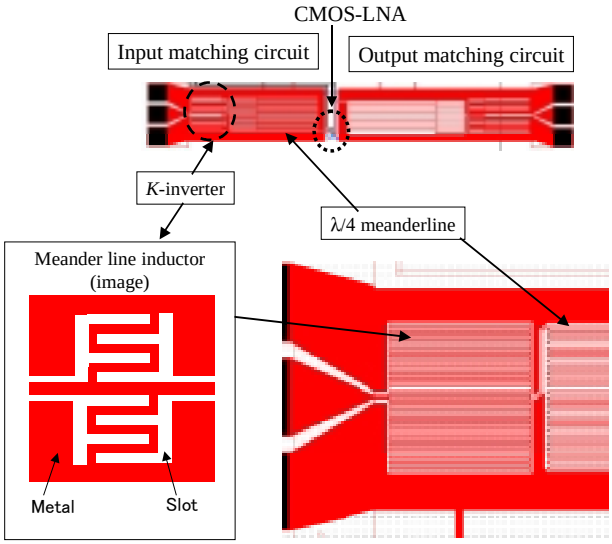


Fig.7. Layout of input and output matching circuit connected with LNA.

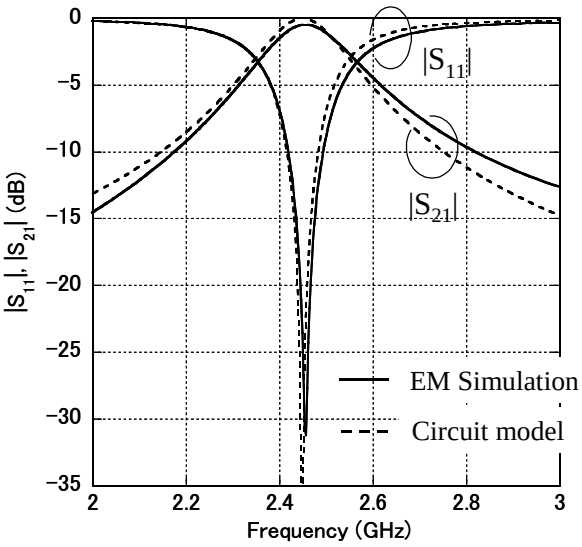


Fig.8. Simulation results of S parameters.

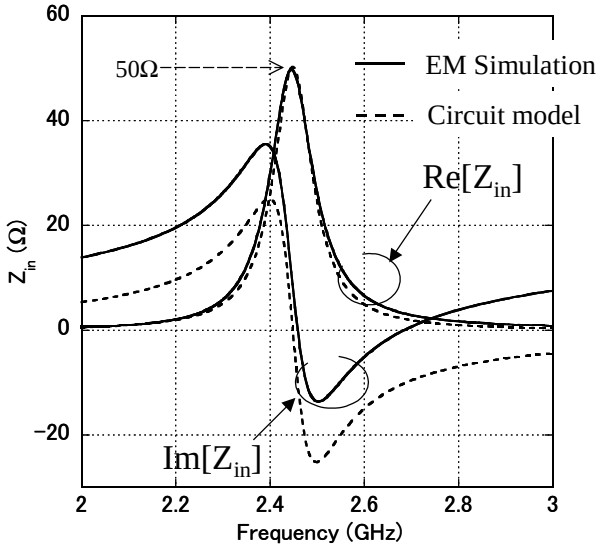
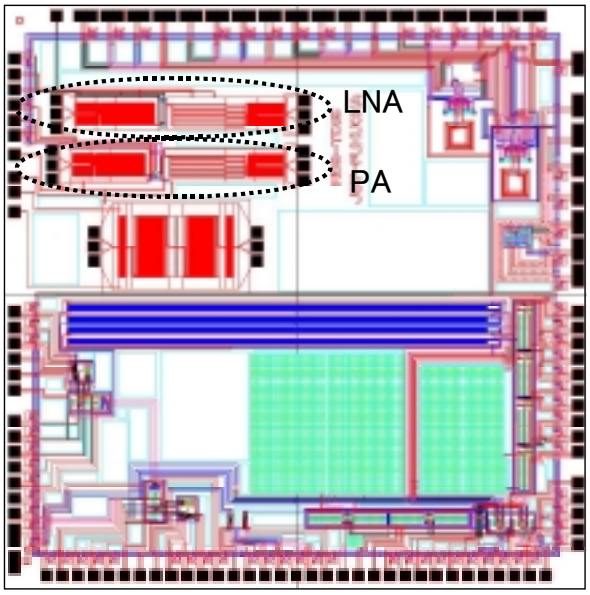


Fig.9. Frequency dependence of the input impedance.



Size: 5mm x 5mm

Fig.10. Chip layout of RF CMOS front-end.

5. Conclusion

We designed the LNA and PA connected with input and output impedance matching circuit on the CMOS chip, which is composed of quarter-wavelength resonator and *K*-inverter. Our new transmission-line-based matching circuit is not only of the small size but also we can design the bandwidth, which is superior to the lumped element matching circuit. Moreover, we can adjust the meander-line shape in order to fit the vacant place on the substrate. We will evaluate the microwave characteristics of the trial chip.

Acknowledgements

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