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Power Analysis Techniques for SoC with Improved Wiring Models

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ABSTRACT
This paper proposes two techniques for improving the accuracy of gate-level power analysis for system-on-a-chip (SoC).
(1) The creation of custom wire load models for clock nets
(2) The use of layout information (actual net capacitance and input signal transition time)
The analysis time is reduced to less than one three-hundredth of the transistor-level power analysis time. The error is within 5% of that of a real chip, (the same level in transistor-level power analysis) if technique (2) is used. The analytical error between technique (1) and (2) is within 1%.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids – S*imulation, Verification, Placement and routing, Layout.*

General Terms
Verification, Experimentation, Design

Keywords
SoC, power analysis, gate-level, custom wire load model

1. INTRODUCTION
The overall power consumption of a SoC, which consists of RISCs, memories, analog circuits, user logic and so on, is expected to continue increasing despite improvements in low power consumption technology. In this situation, the need for techniques that would enable us to determine the power consumption of a SoC with high accuracy is growing.

Although RT-level power analysis takes less time, its analytical accuracy varies, depending on the type of circuit. Transistor-level power analysis has a high degree of accuracy, but it takes several months to complete a full analysis of circuitry containing up to ten million transistors. In [8], the authors proposed an interconnect energy model with consideration of spatio-temporal coupling effects, and their approach is several orders of magnitude faster than HSPICE with error of less than 5%. Gate-level power analysis takes less than one day for the same circuitry [1][3][7][9]. The high accuracy level of gate-level power analysis prior to placement allows us to improve the architecture and behavior of a chip at the design level in a short period.

Gate-level logic simulations using the actual functional patterns of two SoCs are performed, and estimated their full-chip power consumption taking into consideration the results of the logic simulations. Errors in the analysis are checked against chip measurements on an LSI tester using the same patterns, and it is found that these could be as low as 5%. Using the net capacitance that is extracted based on the wire load models, errors in the analysis checked against analysis using actual net capacitance data are within 1%.

In this paper, we develop techniques that enable us to perform gate-level power analysis at a low level of error to within 10%. This is the same level as that achieved by transistor-level power analysis, and at the same time, we reduce the analysis time to less than one three-hundredth of the time needed for transistor-level analysis. We perform SPICE simulations of analog circuits and SRAMs and generate power consumption data for a full-chip power analysis. We verify the accuracy of the gate-level analysis by applying it to two SoCs.

Because the results of the power analysis show that the clock nets and the clock cells consume more than one quarter of the power for the whole chip, it is very important to improve the accuracy of the power consumption of the clock lines. In this research, we take the approach of designing wire load models exclusively for the clock nets and reduce the errors in the power estimate for the clock lines to less than one tenth of previous methods.

We also perform power analysis using additional wiring information relating to the actual layout, (that is, the input signal transition time), with aim of increasing the accuracy of the gate-level power analysis to the limit of the technique.

2. POWER ANALYSIS METHODS
In this paper, we apply three methods of gate-level power analysis (Figure 1).

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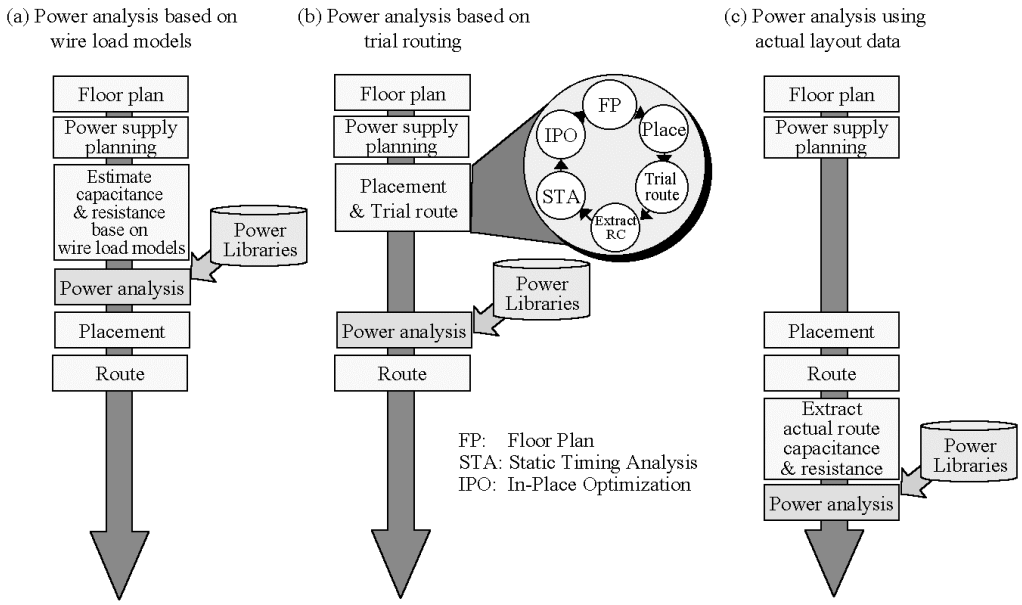


Figure 1. Flows of power analysis.

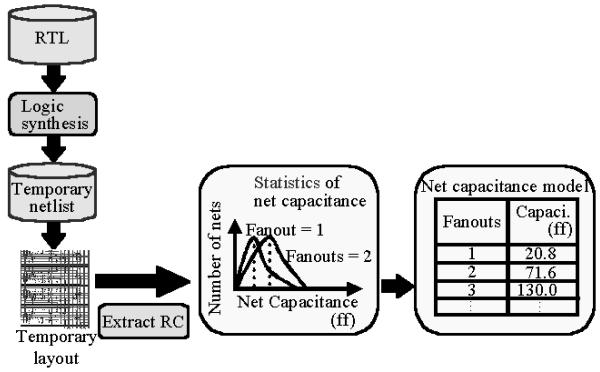


Figure 2. Flow of wire load model creation.

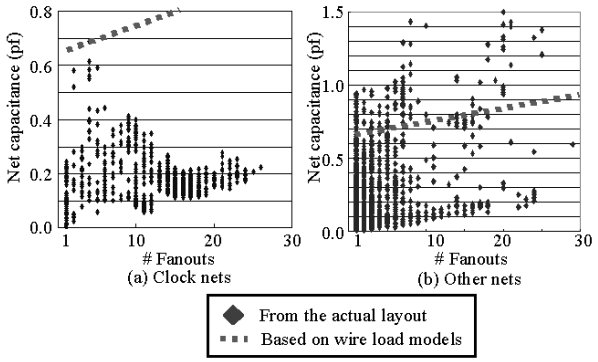


Figure 3. Number of fanouts and net capacitance.

(a) analysis prior to placement. In this technique, the net capacitance and resistance based on the wire load models are used in order to estimate the power consumption.

(b) analysis after carrying out trial routing in the placement stage. In this technique, values for the net capacitance based on trial routing are used.

(c) analysis following the routing stage. In this technique, the net capacitance and resistance extracted from the actual layout are used.

3. HIGH-ACCURACY POWER ANALYSIS TECHNIQUES

This section presents two approaches that can be used in order to increase the accuracy of gate-level power analysis.

3.1 Increasing the accuracy of the wire load models

When carrying out power analysis (a), while creating the wire load models, temporary layout data for the circuits to be designed are prepared, and the resistance and capacitance of each net are extracted. These resistance and capacitance data are statistically processed for each individual fanout, and the processed data are turned into mathematical expressions, as shown in Figure 2.

Because the clock synthesis is carried out prior to the routing in the actual LSI layout, the capacitance of the clock nets is different from that of the general signal nets at each individual fanout.

After the nets are classified into clock nets and general signal nets, the number of fanouts for each net is identified and the net capacitance is extracted from the actual layout. As shown in Figure 3, although the capacitance values of each general signal net vary widely, those given by the wire load models are the average values. However, the capacitance values for each clock net given by the wire load models differ markedly from those of the actual layout. This large difference plays a major role in the significant errors experienced in power analysis, and we need to improve the clock net capacitance values given by the wire load models. The routing data are processed statistically for each fanout, based on the capacitance of each clock net extracted from the actual layout, and a custom wire load model for the clock nets

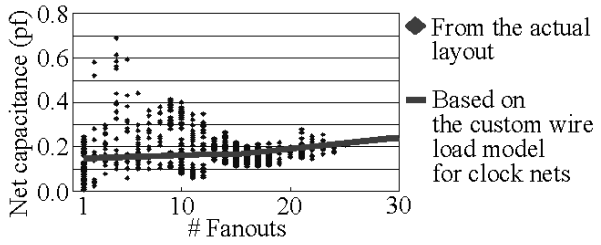


Figure 4. Custom wire load model for clock nets vs. actual net capacitance.

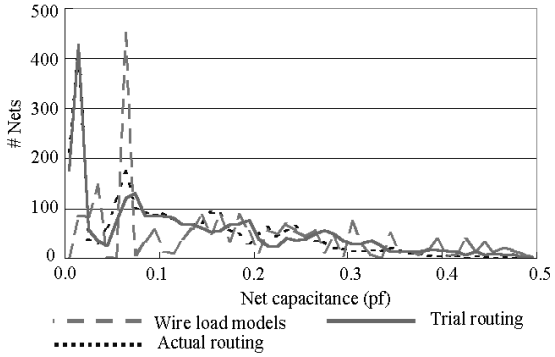


Figure 5. Comparison of net capacitance estimate.

is created. As shown in Figure 4, the values given by this custom wire load model for the clock nets are close to those of the actual layout, indicating the possibility that the accuracy of the power analysis that will be performed prior to placement can be increased. In order to achieve a more precise analysis, we should not only create custom wire load models for each functional block of the SoC, but also for the clock nets. Therefore, in this paper, we perform power analysis using a custom wire load model designed exclusively for the clock nets.

3.2 Using routing data to increase accuracy

In the placement stage, the errors in the net capacitance estimated using trial routing checked against that of the actual layout are 20% on average. It is found that the net capacitance estimated by carrying out trial routing is in much better agreement with the net capacitance of the actual layout than with the capacitance given by the wire load models (Figure 5). We perform power analysis using values for the net capacitance estimated using trial routing.

When performing power analysis using the net capacitance extracted from the actual layout, any signal skews or transition times of all the input signals are usually considered uniform if one net connects to many gates as an input signal. In this paper, in order to reduce the analytical error to 10%, both the net capacitance data and the transition time data of each input signal are extracted from the actual layout, and they are used in the power analysis.

4. POWER LIBRARY SPECIFICATIONS

This section describes the power library specifications on which the power analysis performed for each block of the SoC is based. These include the user logic, the RISCs, the I/O cells, the analog circuits and memories used for power analysis and IR drop analysis.

Table 1. Specifications of image processing LSI (1) and (2).

	LSI (1)	LSI (2)
Design rule	0.35μm, 3 layers	0.25μm, 5 layers
Supply voltage	3.3V	2.5V(internal)/3.3V(external)
Number of transistors	3.06 million	6.18 million
User logic	185 thousand gates	1.09 million gates
Embedded cores	RISC (I$: 4KB (2-way) D$: 4KB (2-way)), 40 SRAMs (Total 16KB), one 14bit A-D, one 8bit D-A, one 16bit D-A	RISC (I$: 4KB (2-way) D$: 4KB (2-way)), 61 SRAMs (Total 33KB), one 16bit A-D, one 8bit D-A, one 16bit D-A
Chip size	11.42mm x 10.98mm	9.90mm x 9.77mm
Package	324 pin FBGA	324 pin FBGA

The power consumption of the user logic, the RISCs and the I/O cells is calculated according to the power consumption categories shown below: [2][4][5][6]

i Dynamic cell internal power consumption
ii Net switching power consumption when a signal value changes
iii Cell leakage power consumption resulting from leakage current

The power consumption in these three categories is summated in order to determine the overall power consumption.

High precision SPICE simulations are performed to estimate the power consumption of the analog circuits, and the power consumption of the active analog circuits is determined to be constant.

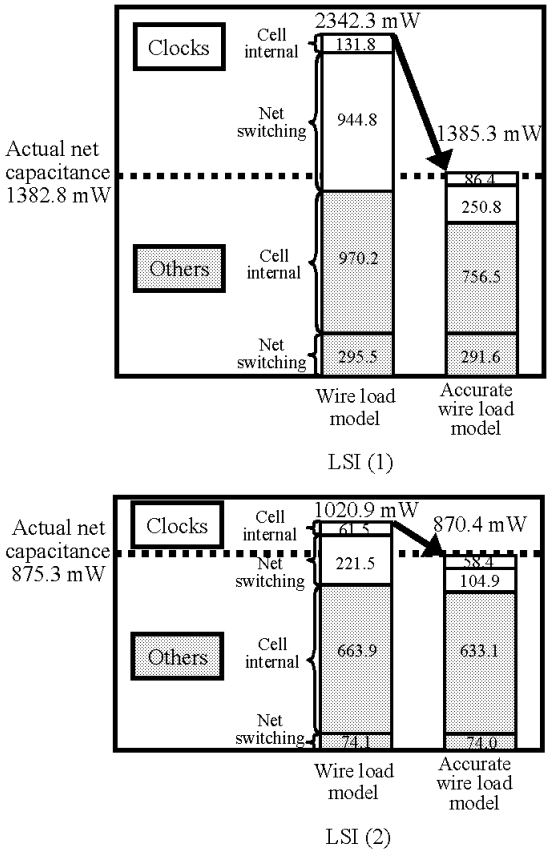
The data obtained from the circuit simulations for the SRAM are processed to calculate the SRAM power consumption.

5. RESULTS OF THE ANALYSIS

The specifications of the two SoCs on which the power analysis are performed in this paper are shown in Table 1. It takes about 12 hours and 14 hours respectively to perform power analysis on LSIs (1) and (2), – less than one three-hundredth of the estimated time that transistor-level full-chip power analysis performed using SPICE simulations with the same actual functional patterns would take to complete. It takes only a few hours in order to create custom wire load models for the clock nets or to extract transition time data of each of the input signals.

The improvements in the results of the power analysis made possible by the increased accuracy of the wire load models are shown in Figure 6. Errors in the analysis checked against analysis using actual net capacitance data decrease from 69.4% to 0.2% for LSI (1) and from 16.6% to 0.6% for LSI (2) due to the use of the custom wire load model for the clock nets. The power consumption of the clock nets in LSI (1) and LSI (2) decrease by 73% and 53%, respectively. This shows that the overall accuracy of the power analysis improves due to the increased accuracy of the clock net power consumption estimate.

The improvements in the results of the power analysis made possible by taking into account the high-precision net capacitance estimates that are made using trial routing are shown in Table 2. Errors in the analysis checked against analysis using actual net capacitance are 0.3% for LSI (1) and 2.5% for LSI (2).



accurate wire load models.

The improvements in the results of the power analysis that are made possible by high-precision power analysis using routing data are also shown in Table 2. Errors in the analysis checked against measurements of a real chip decrease from 14.7% to 11.8% for LSI (1) and from 9.4% to 4.7% for LSI (2) due to the use of the signal transition time of each input signal.

6. IR DROP ANALYSIS

The power analysis techniques described above are used to increase the accuracy of the IR drop analysis that is performed in the placement stage.

The results of the IR drop analysis performed on LSI (2) using both the average and the peak power data are shown in Table 3. After the power supply nets have been optimized, the maximum voltage drop is reduced.

7. CONCLUSION

The accuracy of gate-level SoC power analysis is increased by using two techniques:

(1) Creating custom wire load models for the clock nets
(2) Using layout information (actual net capacitance and input signal transition times)

By using technique (1), errors of 1% or less compared against analysis using the actual net capacitance data are achieved prior to placement using the wire load models. By using technique (2), errors of 5% or less, checked against chip measurements and comparable with the accuracy of transistor-level power analysis,

Table 2. Results of power analysis using trial routing and actual routing data

	LSI (1)	LSI (2)
Trial route	1378.2 mW	897.0 mW
Actual net capacitance	1382.8 mW	875.3 mW
Actual net capacitance + transition time	1348.0 mW	837.3 mW
Measure real chip	1205.7 mW	800 mW

Table 3. Results of IR drop analysis.

	Average	Peak
Power consumption	837.3 mW	2084 mW
Supply voltage (Vdd)	2.5 V	2.5 V
Maximum voltage drop (Vdrop)	39.4 mV → 24.9 mV	113.8 mV → 93.2 mV
(Reduction ratio)	(36.8%)	(18.1%)
Vdrop/Vdd	2% → 1%	5% → 4%

are achieved. The analysis time is less than one three-hundredth of that required for transistor-level power analysis. In addition, the accuracy of the IR drop analysis and the reliability of the power supply routing are increased by using these power analysis techniques.

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