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Fabrication of Oxide Passivated and Antireflective Thin Film Coated Emitter Layer in Two Steps for the Application in Photovoltaic

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Abstract: The gap between laboratory scale and commercial silicon solar cells is wider, as many processes are not being practiced in commercialization. In this work, we have investigated the silicon solar cell fabrication process followed by industries and proposed a simplified process. The fabrication process for the emitter layer, 100 nm thin film anti-reflection coating and wet oxide passivation in a single chamber diffusion furnace on 200 micron p-type mono crystalline silicon wafer was followed. The diffusion process was carried out in an atmospheric furnace using phosphorus oxychloride as dopant source, oxygen for anti-reflection coating and wet oxide surface passivation. Topographical, optical and electrical characterization were conducted to understand the properties of the above layers for application in solar cell fabrication. The reflectivity and average sheet resistivity data of the diffused wafer is in the range those published in literature. Following the procedure, number of process steps, instrument and cost of commercial solar cell fabrication can be optimized.

Keywords: oxide passivation, thin film, crystalline silicon, antireflection coating, emitter layer.

1. Introduction

Mono-crystalline silicon wafers are an interesting area for the research in the development of low cost commercial photovoltaic (PV) devices. Large industry scale PV cell fabrication is different from small laboratory scale cell fabrication. In practice many standard laboratories developed processes are not being transformed to large scale commercialization due to lack of commercial viability for turnkey-type establishment[1)]. Hence, development of a simplified process for industry scale silicon solar cell fabrication has become essential as the proof of concept especially in the case of developing countries as Bangladesh[2)].

The generalized structure of the industrial silicon wafer based solar cells is shown in figure-1. The basics steps involve in the fabrication of wafer based commercial silicon solar cell are, texturing of p-type silicon wafer, diffusion of n-type dopant and formation of metal contacts. Keeping these three basic steps any inclusion of process that enhances the performance of the solar cell will not contribute to the production cost significantly. The objective of the study is to develop a simplified process to enhance the electrical performance of the solar cell.

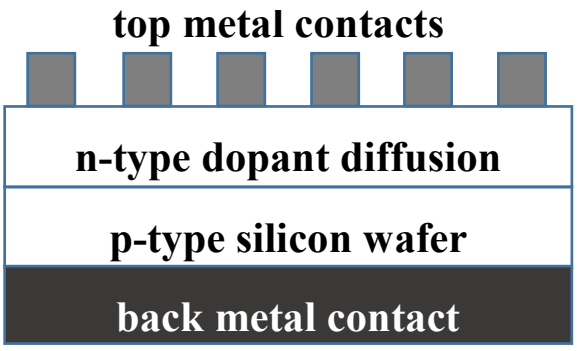


Fig 1. The schematic of the generalized structure of the industrial silicon wafer based solar cells.

At present, after the dopant diffusion in a furnace, the surface passivation and anti-reflection coating (ARC) is

executed using several techniques such as plasma enhanced chemical vapour deposition (PECVD), atomic layer deposition (ALD)[3], atmospheric pressure chemical vapor deposition (APCVD) which are separate instrument[4]. This requires transfer of under processing solar cells from one instrument to another, which introduces risk of contamination, additional cost and wafer handling procedure. The developed simplified process explained in the other literature incorporates phosphorus diffusion[5], ARC[6] and surface passivation[7] in a single step using the spin on dopant (SOD) process[8]. In commercial silicon solar cell fabrication process[9], diffusion furnaces are widely used for the formation of the n-type emitter layer[10]. Low cost anti-reflection layer can be formed using chemical solution[11], spray spin coated system[12] and sol-gel process[13]. Multi layered ARC performance for Silicon solar cell was modeled by Silvaco software[14]. An efficiency of 9.84% for a crystalline silicon solar cell without any ARC was observed and efficiencies of 14% and 14.25% are obtained using TiO_2 and Si_3N_4 ARC[15], respectively. The surface passivation is another aspect of improving the performance and degradation of solar cell. The surface passivation increases the open circuit voltage by reducing the surface recombination velocity[16]. Various methods[17] of surface passivation for the crystalline silicon solar cell is optimized using oxygen and nitrogen atmosphere at temperature range in 850°C -1000°C[18].

The other kind of low cost thin film solar cell is dye-sensitized solar cell (DSSC)[19),20]. It uses titanium dioxide (TiO_2) thin film as the photo anode[21),22]. The variation in the thickness of the TiO_2 thin film on glass shows an increase in optical band gap[23),24]. The tuning of optical band gap allows a larger spectrum of electromagnetic wave to be received by the DSSC solar cell which increases the performance of the thin film by enhancing the optical properties [25].

In the industry, the simplification of solar cell fabrication process is imperative to the economic output of the product. Other than the growth of thin film on the silicon wafer, there are few techniques that are used to enhance the performance of silicon solar cell without affecting the process. The light trapping technique is widely used to enhance the performance of the silicon solar cell. This technique uses texturing process[26] such as copper nano particle etching to produce light trapping pyramids[27]. The variation in the doping profile in silicon wafer enhances the electrical properties of silicon solar cell[28),29]. The contact resistance optimization is another technique that enhances the electrical performances of the silicon solar cell[30),31].

The application of multiple layers of thin film for the performance enhancement of silicon solar cell can be estimated using software[32]. The multiple layers consist of silicon dioxide and silicon nitride shows an increase in the light absorption which enhances the efficiency of the solar cell. This inclusion of another layer does not affect the industrial fabrication process rather act as a simplified step[33].

A theoretical study using PC1D simulation predicted that the efficiency of the solar cell made by following the simplified process can be 20.35% with optimizing effective parameters[34]. An SOD experimental process showed that a simplified process can be used to fabricate 15% efficient solar cells on c-Si wafers[6].

In this study, phosphorous diffusion process was carried on a p-type mono crystalline silicon wafer using a thermal diffusion furnace. This process is used to form the emitter layer followed by wet oxide passivation, silicon dioxide (SiO_2) ARC formation and annealing under nitrogen flow. All of these steps are performed using a thermal diffusion furnace in one process run. The topographical, optical and electrical characteristic of the processed wafer is evaluated using scanning electron microscope, reflectometer and four-probe setup respectively. The well passivated silicon dioxide (SiO_2) thin film is widely used by the various industries to produce photovoltaic cells[35], optoelectronics devices, electronic sensors and transistors[36].

2. Experimental

The experimental process followed in this research includes phosphorus diffusion, anti-reflection coating (ARC) and a surface passivation in two steps in a single chamber. In the thermal diffusion process, phosphorus oxychloride ($POCl_3$) served as the dopant source and the final incorporation of the oxygen gas, produced silicon dioxide (SiO_2) anti-reflection coating as well as surface passivation layer. The annealing of SiO_2 in the presence of N_2 was observed at 600°C using PECVD[37] which is comparable to the process shown in this study in Table-1. The N_2 purging also provides a contamination and moisture-free inert environment in the diffusion chamber for the entire process.

P type mono crystalline Cz-Si (thickness=180±20μm, resistivity = 1-3 Ω-cm, crystal orientation (100), dimension 125 × 125 mm^2) wafers were cleaned by standard Radio Corporation of America (RCA) cleaning process[38]. The saw damaged was removed using high concentration of sodium hydroxide (NaOH) (NaOH: H_2O=1:10) at 70°C temperature for 10 minutes for isotropic etching. The wafers were dipped into hydrofluoric (HF) acid solution (HF: H_2O=1:50) for 10 seconds followed by rinsing in de-ionized water (DIW) for 1 minute and then dried with nitrogen blow.

The texturing process was performed using potassium hydroxide (KOH) solution (KOH:IPA:DIW=1:5:125) at 70°C temperature for 10 minutes. After that the wafers were dipped into HF solution for 10 seconds, DIW for 1 minute and then dried with nitrogen blow. The recipe is used to produce pyramid shape surface morphology on silicon wafer[39].

The diffusion process was carried out by using atmospheric pressure chemical vapor deposition

(APCVD) technique in a horizontal tube thermal furnace from Sandvik Thermal Process Inc. CA, USA. The instrument covers an extensive range of temperatures for solar cell processing. It has three tubes, each 48 inches long with three thermal flat zones and compatible for 150 mm diameter substrate. The details of the process steps for the phosphorous diffusion, ARC and wet oxide passivation are given in the Table 1. The temperature profile is shown in Figure 2.

Table 1. The details of process steps for the phosphorous diffusion, anti-reflection coating (ARC) and oxide passivation in thermal diffusion furnace.

Temperature in °C	Duration in minutes	N_2 flow rate in liter/min	$POCl_3$ flow rate in liter/min	O_2 flow rate in liter/min	Name of Steps
200	20	10	off	off	N_2 purge
600	20	10	off	off	Textured wafer loaded
875	15	off	30	30	Phosphorus diffusion
875	10	30	off	off	
875	10	off	off	30	Surface passivation and SiO_2 ARC
875	20	30	off	off	N_2 purge annealing
600	05	10	off	off	Cooling
200	10	10	off	off	Wafer collection

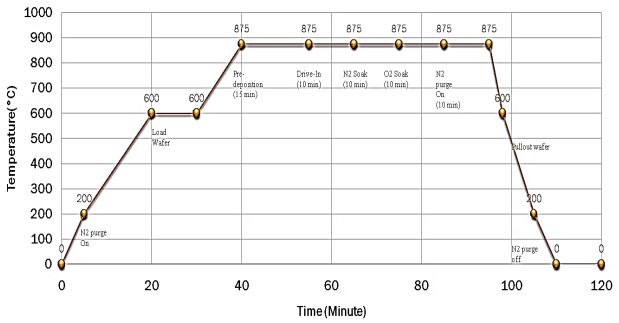


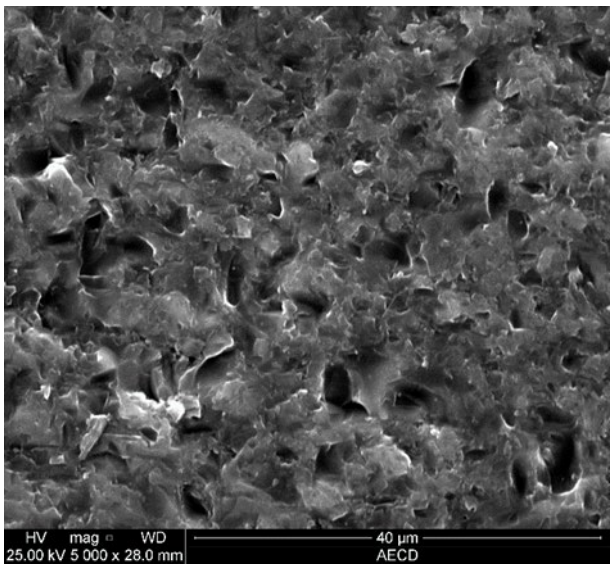
Fig 2. Temperature profile for the phosphorous diffusion, anti-reflection coating (ARC) and oxide passivation in thermal diffusion furnace.

3. Results and Discussion

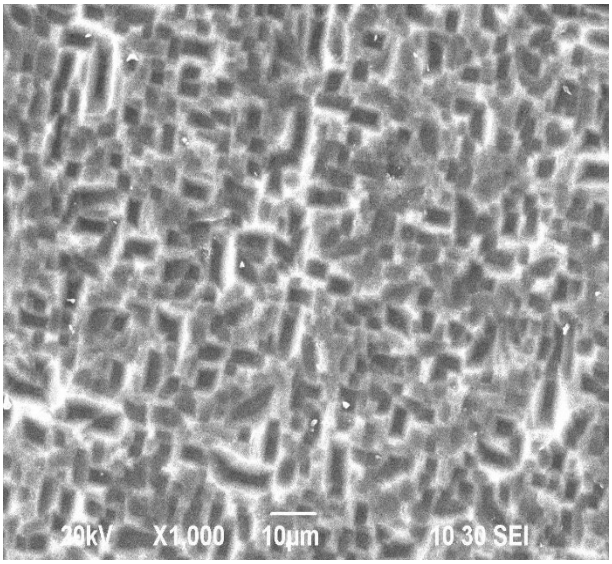
The silicon wafers with the layers were characterized for the evaluation of morphological, optical and electrical properties. The morphological aspects of raw, textured and phosphorus doped silicon wafers were investigated using scanning electron microscope. The reflectance in the visible and infrared range was measured for saw dust removed silicon wafer and phosphorus doped with SiO_2 anti-reflection coated silicon wafer. The thickness of the ARC layer was estimated using reflectometer. The sheet resistivity was calculated from the electrical measurement using collinear four point probe setup.

3.1 Surface morphology analysis

The scanning electron microscope (SEM) model JSM 7600F, from JEOL, Japan was used to observe the grains on raw, cleaned, textured and phosphorus doped silicon wafer which is shown in figure 3. The SEM image of commercial p-type silicon wafer as purchased from Renesola Yixing Co. Ltd. China, shown in figure 3(a), shows saw dust on top of the silicon wafer. After the RCA cleaning the dust is removed and sharp edge silicon grains are seen in figure 3(b). The chemical texturing causes significant changes in the wafer surface shown in figure 3(c). Figure 3(d) shows the wafer topography after the phosphorus diffusion process in the diffusion furnace at 875°C. The phosphorus diffusion along with the ARC layer covers the top of the pyramids, hence the bright spots which were seen in figure 3(c) become broad. Using Veeco Dektak-150 surface profiler for the chemically textured silicon wafer, for 10 minutes etching, the average pyramid height was measured 2.937 µm which is in the range (2-3 µm) suitable for light trapping in photovoltaic devices[40]. Larger pyramid size of 10-15 µm[41] was observed for etching time of 30-50 minutes[42].



(a)



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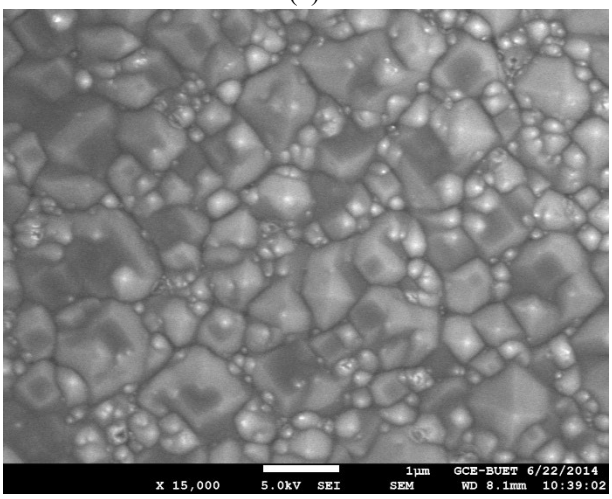

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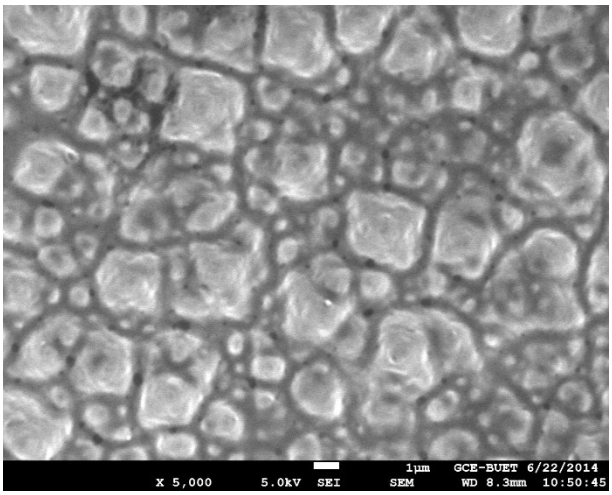
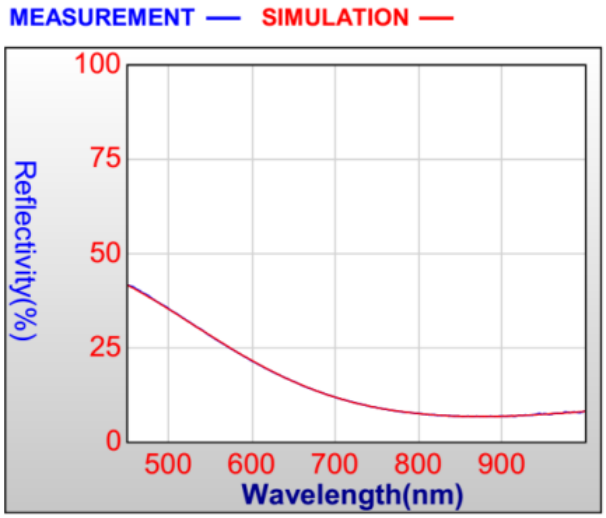


(d)

Fig 3. Surface topography images of p-type 200 micron silicon wafer taken by SEM (a) raw silicon wafer (b) saw dust removed silicon wafer (c) chemically textured silicon wafer (d) phosphorus doped, surface passivated and silicon dioxide (SiO_2) ARC layer on p-type silicon wafer.

3.2 Optical reflectance analysis

The optical reflectance study was conducted in the visible to near infrared range (400 nm – 1000 nm) using spectroscopic reflectometer from Radiation Technology Inc. Taiwan[43]. The reflectivity data of visible light from saw dust removed, phosphorus doped and anti-reflection coated silicon wafer was estimated for 400 nm – 1000 nm wavelength shown in Figure 4(a,c,e) and in Table-2.



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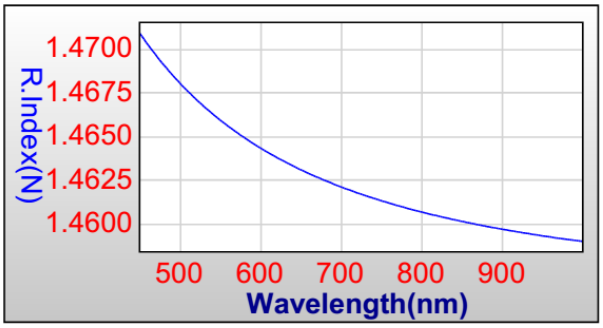

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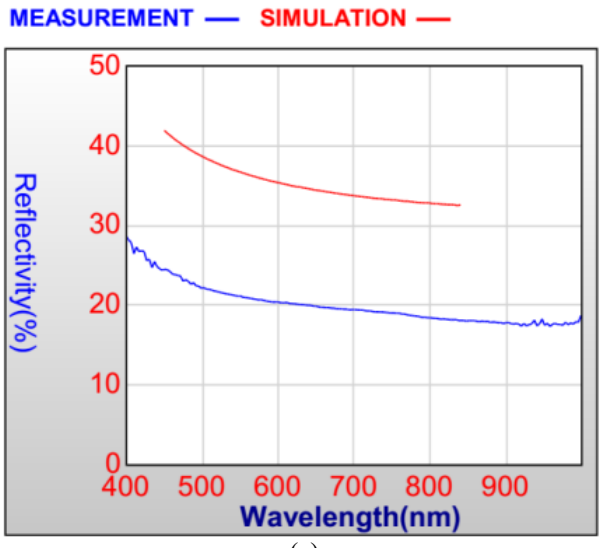

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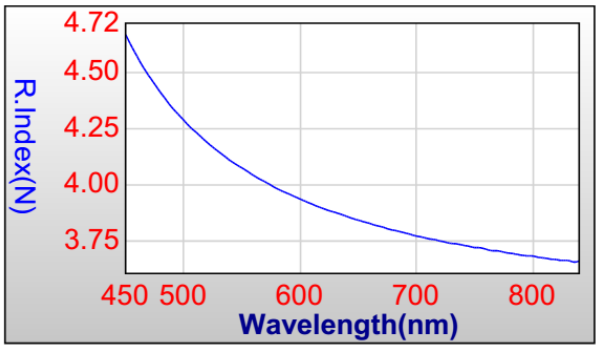

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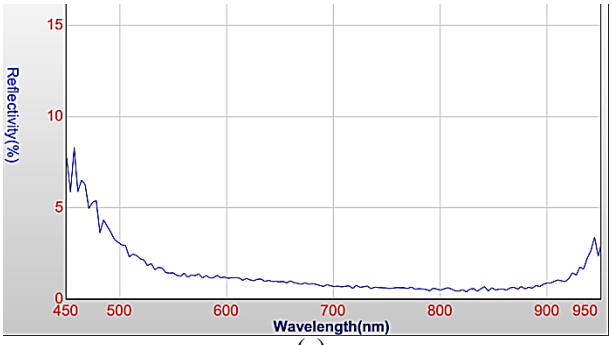
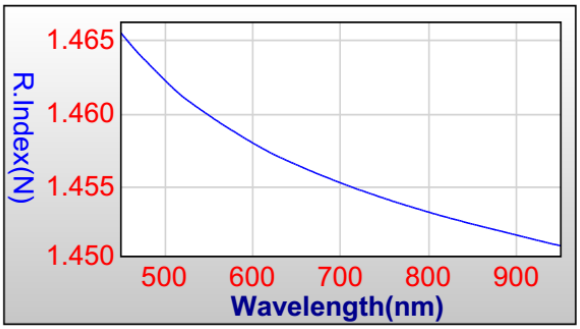


(e)



(f)

Fig 4. Optical Reflectivity in wavelength range 400 nm – 1000 nm, of (a) SiO_2 on SiCr substrate reference sample for reflectometer calibration (c) saw dust removed RCA cleaned silicon wafer (e) SiO_2 ARC layer on phosphorus doped textured silicon wafer, (b,d,f) corresponding refractive index-wavelength plot

The reflectivity-wavelength graphs in Figure-4(e) shows the reduced optical reflectivity for the phosphorus doped silicon wafer. The percentage of reflectivity is less than 1% in the near infrared region. Table-2 shows the spectroscopic reflectometer data of reference sample, RCA cleaned silicon wafer and phosphorous diffusion, anti-reflection coating (ARC) silicon wafer. The refractive index and thickness of the silicon dioxide (SiO_2) ARC layer was 1.455 and 101 nm respectively[44]. The reflectivity of the phosphorus doped silicon wafer is in the range similar to other published literatures[45),46)].

Table 2. The spectroscopic reflectometer data of reference sample, RCA cleaned silicon wafer and phosphorous diffusion, anti-reflection coating (ARC) silicon wafer.

Sample Name	Name of layers	Material	Thickness in nm	Refractive Index	Extinction co-efficient
Reference	Ambient	Void	-	1.000	0.000
	Layer-1	SiO_2	147	1.466	0.000
	Substrate	SiCr		4.086	0.040 at 550nm
RCA cleaned Si Wafer	Ambient	Void	-	1.000	0.000
	Substrate	Si100	-	3.871	0.016 at 633nm
Phosphorous diffused and ARC wafer	Ambient	Void	-	1.000	
	Layer-1	SiO_2	101	1.455	
	Substrate	Si100		3.759	0.010 at 710nm

3.3 Electrical properties analysis

The sheet resistance of phosphorus diffused silicon wafer was determined using four point probe setup. The setup consists of a i) manual tungsten probe station from Cascade Microtech, Germany, ii) Agilent 34401A voltmeter form Agilent Technology, Germany and iii) Keithley 6221 AC/DC source from Keithley Instruments, Inc. USA was used to record I-V data manually. The diffused wafers were dipped into hydrofluoric (HF) acid solution (HF49%: H_2O=1:5) for 1 minute followed by rinsing in de-ionized water (DIW) and dried with nitrogen blow to remove the ARC layer, before the sheet resistivity data was taken. The sheet resistance of raw and phosphorus doped wafer was 115 Ω/square and 60 Ω/square, respectively[47)], which is also in well agreement with the other literatures published earlier for high efficiency silicon solar cells[10)]. The solar cell fabricated in the same facility, was 9.63% efficient[48)] following the similar diffusion process with a variation in the texturing, duration of diffusion, gas flow rate and process steps.

4. Conclusion

In this research work, a simplified route was explored to incorporate phosphorus diffusion, SiO_2 antireflection coating and oxide passivated p-type silicon wafer in a diffusion furnace. As a result, apart from achieving less than 1% surface reflection from the silicon surface, the diffused wafer shows the sheet resistance of 60 Ω/square, which are in the most suited parametric ranges for crystalline silicon solar cell fabrication. The diffusion furnace can be further optimized for the silicon nitrite antireflection coating using nitrogen, the thickness of the antireflection coating and the annealing of the surface for better passivation in the presence of nitrogen or oxygen. Innovative fabrication process flow for commercial solar

cell is an ongoing field of research. This focuses on reducing the number of processing steps as well as less use of chemicals or ingredients. The process steps are directly related to the time, cost and human work hour where the use of chemicals directly impact the environment. In addition, the simplified process was carried out with the optimum amount of chemicals to reduce the effect on environment.

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Nomenclature

ARC	*anti-reflection coating*
PECVD	*plasma enhanced chemical vapour deposition*
ALD	*atomic layer deposition*
APCVD	*atmospheric pressure chemical vapor deposition*
HF	*Hydrofluoric*
SiO_2	*silicon dioxide*
IPA	*Isopropyl alcohol*
RCA	*Radio Corporation of America*
DIW	*De-ionized water*
AC/DC	*Alternating current/ Direct current*

Greek symbols

Ω	*Ohm*
℃	*Degree Celsius*
μ	*micrometer*

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