Development of the Compact Low Phase Noise Voltage Controlled Oscillator Using Integrated High-Q Resonator

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Development of the Compact Low Phase Noise Voltage Controlled Oscillator Using Integrated High-Q Resonator

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Contents

ABSTRACT

The recent exponential growth of wireless communication systems has promoted a great demand for compact, low cost, and low power consumption. Therefore, high-performance frequency generation technologies of quasi-millimeter and millimeter (mm-) wave have attracted increasing interest and developed rapidly. The main challenge in designing a low phase noise CMOS voltage-controlled oscillator (VCO) is to improve the low quality (Q-) factor of the conventional spiral inductor, which is due to the stringent size limitation of the metal layers and the lossy substrate.

This dissertation focuses on the analysis, design, and implementation of high-Q integrated CMOS resonators technology for quasi-mm-wave and mm-wave VCO applications. There are two main categories of high-Q resonators are proposed in this dissertation. The first category is the defected ground structure (DGS) resonator. This type of resonator is proposed to be implemented in the LC oscillator instead of the conventional LC tank resonator. A novel two-branch DGS resonator is designed and investigated. The proposed two-branches DGS resonator doesn't only have a higher Q-factor than the conventional spiral inductor but also performs better than the DGS resonator's predecessors. In the V band, the Q-factor of the proposed novel DGS resonator is around two times higher than those conventional resonators and is expected to improve the phase noise characteristic of mm-wave VCO applications.

The second resonator category discussed in this dissertation is called substrate integrated waveguide (SIW) resonator. This type of resonator is proposed as the post design of the DGS resonator. The SIW-based resonator is a "closed" structure compared with the DGS resonator thus less affected by adjacent circuit components. In the dissertation, a novel miniaturization method of SIW resonator is proposed to realize the implementation of SIW resonator in CMOS technology. The proposed miniaturization method is extremely effective and reduces the area of the SIW resonator to 0.3% compared with the full-mode SIW resonator. The proposed miniaturized SIW resonator is transformed to the bandpass filter (BPF) applications, which is a kind of two ports resonator, with low insertion loss. These two ports resonators are projected to be implemented in future W band (75-110 GHz) VCO designs. One of the proposed BPF is realized with an extremely compact size (99 μm × 99 μm, $0.054\lambda_g \times 0.054\ \lambda_g$). The measured insertion loss (|S21|) of 2.26 dB

at 84.4 GHz. A weak coupling coefficient problem between CMOS SIW resonators is figured out and analyzed as well. A novel coupling method that couples two SIW resonators through a DGS is proposed as the solution to this problem. The second W band BPF is designed using this novel coupling method and fabricated. The measured insertion loss is 3.15 dB at 85.5 GHz. To validate the feasibility of a SIW-base resonator working at a frequency beyond 100 GHz, a two ports bandpass resonator with two transmission zeros is implemented and measured. The active size of the proposed bandpass resonator without pads is 309μm × 275μm (~0.1λ_g×~0.09 λ_g), and the measured insertion loss (|S21|) is 2.06dB. This is the first time that a SIW resonator/BPF is implemented in a commercial Si-based technology successfully, which gives more choice in the future on-chip circuits design.

To evaluate the performance of proposed high Q resonators and verify our design concept of low phase noise VCO, VCO applications using the proposed resonators are designed, fabricated, and measured. The two-branch DGS resonator is implemented in the design of the V band (40-75 GHz) VCO, and the measured best phase noise is -102.58 dBc/Hz at a 1 MHz offset with a carrier frequency of 49 GHz. This is the first time that the DGS resonator is implemented in the VCO which works at a such high frequency. After this, the proposed two-branches DGS resonator is optimized and implemented in a K band (18-27 GHz) VCO to realize the wide tuning function. The K band VCO using optimized two-branches DGS resonator is possible to achieve a 19.8% tuning range and the best phase noise performance of -109.43dBc/Hz at 1 MHz offset with the carrier frequency of 18.51GHz. Finally, experimental research of the relationship between interconnects and phase noise of the K band VCO is given.

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LIST OF ABBREVIATIONS

1P6M	**O**ne-**P**oly-**Six**-**M**etal (radio frequency)
3-D	**T**hree **D**imensional
5G	**5**th **G**eneration mobile communication system
AC	**A**lternative **C**urrent
ADS	Keysight **A**dvanced **D**esign **S**ystem
BPF	**B**and **P**ass **F**ilter
CMOS	**C**omplementary **M**etal-**O**xide- **S**emiconductor
CPS	**C**oplanar **S**trip **L**ine
CPW	**C**oplanar **S**trip **W**aveguide
DC	**D**irect **C**urrent
DGS	**D**efected-**G**round **S**tructure
EM	**E**lectro**m**agnetic
FBW	**F**ractional **B**and**w**idth
FOM	**F**igure-**O**f-**M**erit
FOM$_T$	**F**igure-**O**f-**M**erit with **T**uning range
FTR	**F**requency **T**uning **R**ange
GSG	**G**round-**S**ignal-**G**round
HFSS	**H**igh **F**requency **S**tructure **S**imulator
IF	**I**ntermediate **F**requency
IL	**I**nsertion **L**oss
ISF	**I**mpulse **S**ensitivity **F**unction
LAN	**L**ocal **A**rea **N**etwork
LC	**I**nductor-**C**apacitor
LO	**L**ocal **O**scillator
LNA	**L**ow **N**oise **A**mplifier
MIMCAP	**M**etal-**I**nsulator-**M**etal **Cap**acitor
MM-wave	**M**illi**m**eter-wave
MSL	**M**icro-**S**trip **L**ine
PBG	**P**hotonic **B**and **G**ap
PCB	**P**rinted **C**ircuit **B**oard
PHY	**Ph**ysical **L**ayer
PLL	**P**hase-**L**ocked-**L**oop
Q(-factor)	**Q**uality Factor
QMSIW	**Q**uarter-**m**ode **SIW**
RF	**R**adio-**F**requencies
RFIC	**R**adio **F**requency **I**ntegrated **C**ircuit
RFID	**R**adio **F**requency **Id**entifier
SiO_2	**S**ilicon **O**xide
SIW	**S**ubstrate **I**ntegrated **W**aveguide

S-parameter	**S**cattering parameters
SSA	**S**ignal **S**ource **A**nalyzer
VCO	**V**oltage-**C**ontrolled **O**scillator
WPAN	**W**ireless **P**ersonal **A**rea **N**etwork
Z-parameter	Impedance parameters

CHAPTER 1: INTRODUCTION

1.1 Background

In 1887, Heinrich Hertz's experiments proved the existence of electromagnetic waves and their propagation through space as predicted by Maxwell's equations, which became the basis of wireless communication. Later, the transatlantic wireless communication experiment successfully conducted by Italian inventor Guglielmo Marconi in 1901, attracted attention from all over the world. Many pieces of research and applications of wireless communication technology developed very fast. At that time, wireless communication was mainly used for business purposes. But nowadays, various wireless communication systems, such as cell phones and Wi-Fi, are already familiar to us and have become indispensable in our life.

There are four main types of wireless communication systems: fixed terrestrial wireless communication, satellite communication, mobile communication, and broadcasting. Among them, mobile communication grows the fastest, and the number of cell phones used worldwide is expected to reach 40 billion by 2023. Therefore, problems such as rapidly increasing

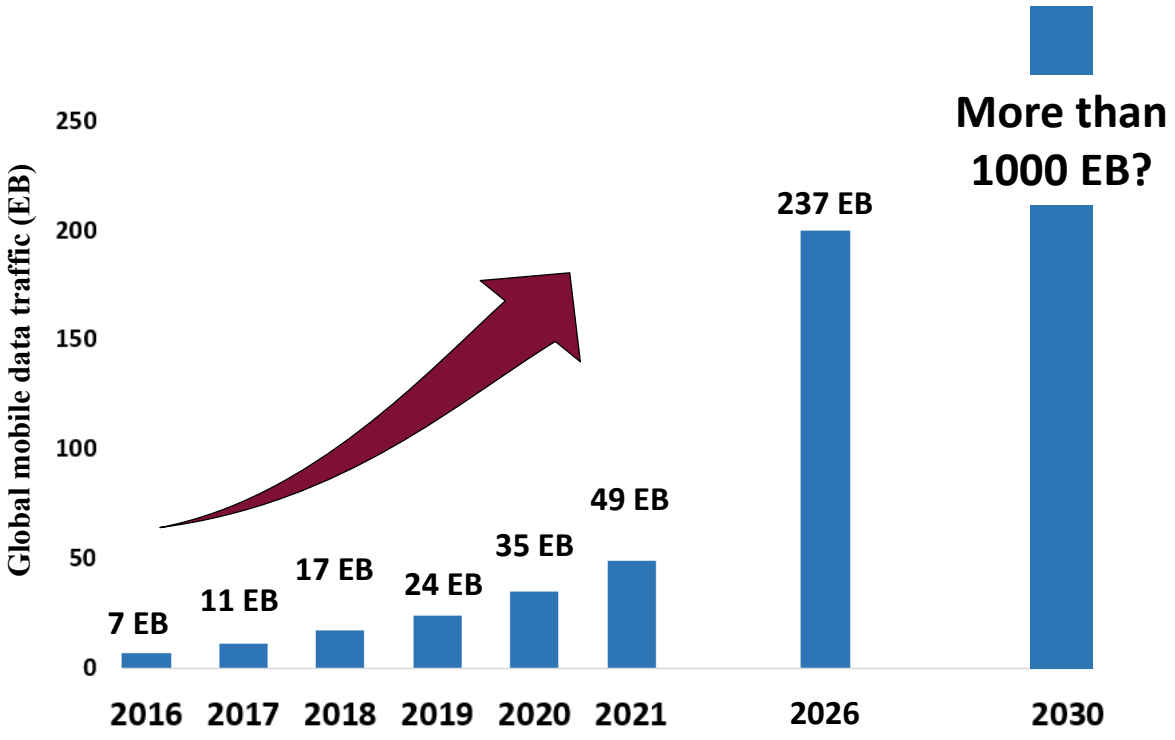


Fig. 1. 1 The growth of global mobile data traffic.

communication data traffic and the shortage of frequency bands are expected. Telefonaktiebolaget LM Ericsson, the major contributor to the development of the telecommunications industry, estimates that the total global mobile data traffic is projected to grow by a factor of close to 4.4 to reach 288 EB per month in 2027, and the total mobile network traffic is forecast to exceed 300 EB per month in 2026 [1].

In addition to the conventional ultra-short waves, the 5th generation mobile communication system (5G) uses quasi-millimeter waves, which is expected to have a communication speed of more than 10 Gbps, end-to-end latency as low as 1 millisecond, and reliability of 99.999%. This is expected to make our lives more convenient by enabling automated driving and remote surgery. However, affected by the epidemic and some political factors, the development of 5G was hampered. According to the forecast of Cisco Systems, Inc., the average 5G connection speed will reach 575 Mbps by 2023, which is half of the expected [2]. Therefore, the development of "Beyond 5G", the next generation of communication technology, is attracting more attention from the industry as a challenge to further develop the trend of higher communication speed, higher density and connectivity through multi-layers, and higher capacity data traffic. Beyond 5G technology is expected to bring a change in our lives to even higher quality, with the goal of meeting the demand a little further down the road, 5 or 10 years from now (around 2025-2030).

The standard IEEE 802.15.3c provides an unlicensed spectrum at around 60 GHz. It is quite suitable for high data-rate wireless communication applications. Firstly, it has an ultra-wide 7 GHz bandwidth with a maximum channel bandwidth of 2.16 GHz. Besides, there has been almost no interference around 60 GHz so far. It seems fairly promising to achieve multi-Gb/s data-rate communication through the 60 GHz frequency band. Since 2003, the IEEE 802.15.3 task group has investigated the use of the 60 GHz spectrum as the physical layer (PHY) for the high data-rate WPAN [3]. Up to now, the standard IEEE 802.15.3c has been granted about the millimeter-wave (mm-wave) wireless personal area network (WPAN) PHY at 60 GHz.

On the other hand, as communication technology evolves day by day, the process of manufacturing circuits is also changing at a tremendous pace over the past several decades. In the past, communication terminals were made up of surprisingly large components such as vacuum tubes, but with the continuous development of microelectronic technologies in the semiconductor process, transistors have almost replaced them. Now, more than 1,000 transistors are integrated on

a silicon chip in the area of a grain of rice. The complementary metal-oxide-semiconductor (CMOS) technology has the advantages of low power consumption, low manufacturing cost, compact size, and ease of fabrication. Therefore, CMOS technology has become the mainstream choice for the employment of wireless communication devices, which are required to be both small and diversified.

However, there is also some shortage of CMOS process. Firstly, the model of the CMOS transistor is always a problem because it is normally developed for digital design. The model is supposed to be optimized for high-frequency design. Besides, the resistivity of CMOS substrate is pretty low, normally $< 10\ \Omega$-cm. This would induce great coupling between circuits as well as losses in passive devices as well. So, it is hard to achieve passive components (such as the resonator) with a high quality (Q-) factor in CMOS technology. Thirdly, the stringent limitation of the thickness of each metal layer and the distance between each two metal layers also aggravate the losses. Therefore, on-chip design with the CMOS process is always challengeable, especially when your target is designing a low phase noise amplifier or a voltage-controlled oscillator (VCO) with low phase noise. In addition, the natural drawbacks of CMOS technology still exist, such as low break-down voltage and high noise. Theoretically, the CMOS transistor is unable to produce high power because of its low break-down voltage.

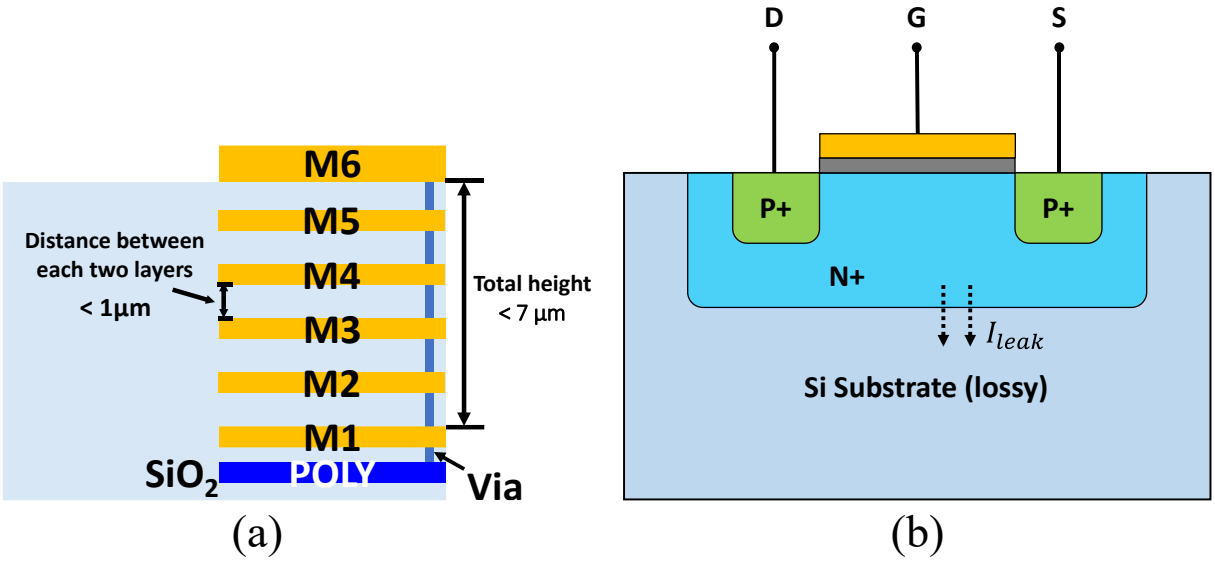


Fig. 1. 2 Structural reasons that make it hard to achieve passive components with a high Q-factor in CMOS technology. (a) The stringent limitation of the metal size. (b) The lossy substrate.

1.2 Research target

In recent years, the demand for mobile communications has been increasing rapidly, and the development of next-generation wireless communication technologies is urgently needed. Beyond 5G communication is expected to introduce millimeter waves, and we are aiming to realize even faster and more stable communication by realizing advanced technologies such as phased array and beamforming technologies in Beyond 5G systems. To realize beamforming technology, the development of a local oscillator with high phase accuracy is the most important issue. In general, the phase accuracy (phase noise) of an oscillator is determined by three factors: noise figure, output power, and Q-factor of its resonator. The realization of low noise performance normally requires the use of advanced processes. The realization of high output power is linked to the high power consumption of the system, which is undesirable for wireless communication systems. Therefore, designing a resonator with a high Q-factor is considered the best way to realize a millimeter-wave low phase noise oscillator. However, during designing the millimeter-wave oscillators, the effect of parasitic parameters on the circuit is significant, which is explained in the above section. It has been shown that the Q-factor of conventional resonators can be significantly reduced [4]. My research target is to design the mm-wave resonator structures with high Q-factor in CMOS process and utilize them in the development of low phase noise oscillators. In this dissertation, two types of high Q resonators are proposed. One is based on the defected ground structure (DGS) technology, and the other is based on the substrate integrated waveguide technology. With DGS resonators, low phase noise oscillators that work in the K band (18-27 GHz) and V band (40-75 GHz) will be designed and analyzed. The SIW based resonator is designed for W band (75-110 GHz) applications.

The dissertation will be organized as follows. Since the VCO is the key component and is widely used in electronic devices, its fundamentals will be presented first in chapter 2. Its theory of operation, basic architectures, the concept of the phase noise, and how to realize the low phase noise characteristic will be introduced in this chapter as well. Chapter 3 introduces the main research objects of two types of integrated high Q-factor resonators, which are DGS resonators and SIW resonators, in this dissertation. The design methods of these resonators are discussed, and an investigation of their characteristics is given. In addition, a miniaturization method on the SIW

resonator is discussed, which makes the SIW resonator available to be implemented in CMOS technology. Then, in chapter 4, the designs of K band and V band low phase noise VCO implementing DGS resonator are presented in 0.18 μm CMOS technology as the applications of integrated high Q-factor resonator introduced in chapter 3. Research of the relationship between interconnects and the phase noise characteristic of K band VCO is given in this chapter as well. A short conclusion will be made in chapter 5.

CHAPTER 2: OSCILLATOR

2.1 introduction

An oscillator is a device that converts the electrical energy of a DC power source into stable and sustained AC electrical energy of the target frequency. Among the electronic devices in our daily life, whether it's the calculator or the computer, the oscillators are implemented inside them. For the wireless communication system, the oscillator is as important as the power supply. Figure 2.1 shows a general example of a wireless communication system. The signal picked up by the antenna is firstly sent to a low noise amplifier (LNA), where it is amplified once while suppressing noise. And then, the signal is amplified to a sufficient level by the radio frequency amplifier through a bandstop filter. Next, the received signal is going to be restored. In order to attain the original information, the amplified signal is multiplied by the signal from the local oscillator (LO) through a mixer. After this, the original information can be extracted from the carrier wave.

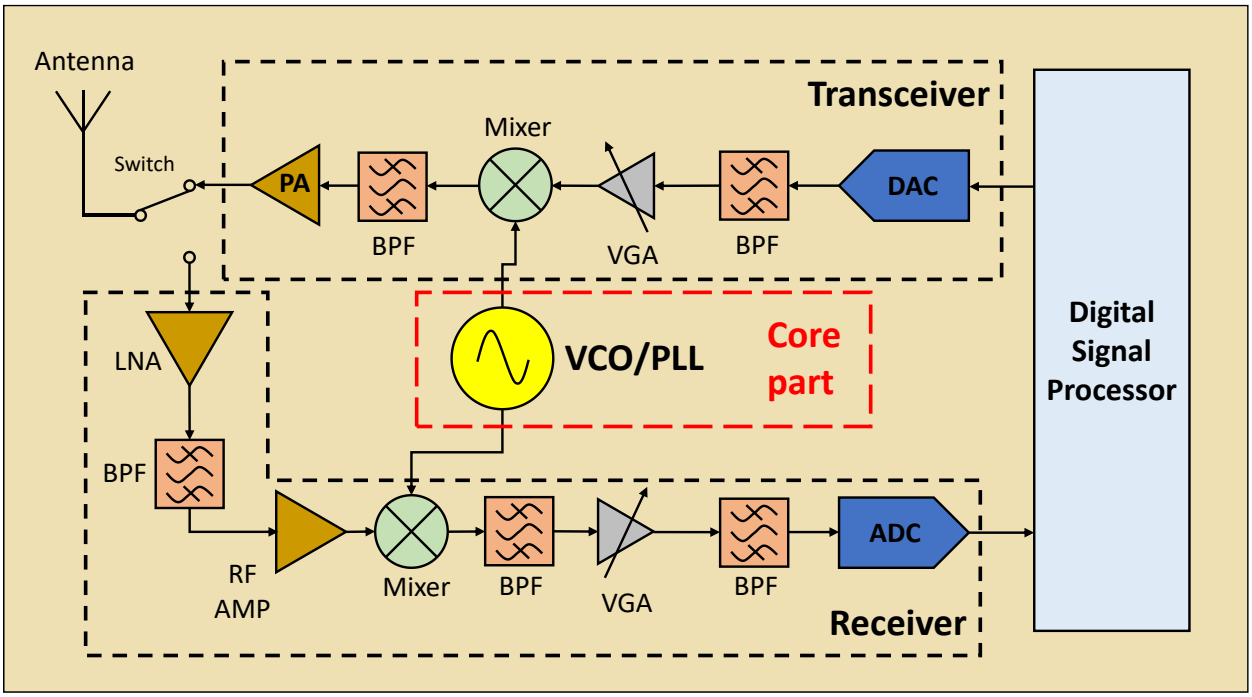


Fig. 2. 1 Diagram of the wireless communication system.

The local oscillator consists of a phase-locked loop (PLL) which normally consists of a phase detector, charge pump, lowpass filter, voltage-controlled oscillator (VCO), and a frequency divider. The PLL synchronizes the phase of the input signal and the output signal by comparing the phase

difference between them. The input signal is generally provided by a crystal oscillator with high reliability and high accuracy. The charge pump converts the information of the phase difference

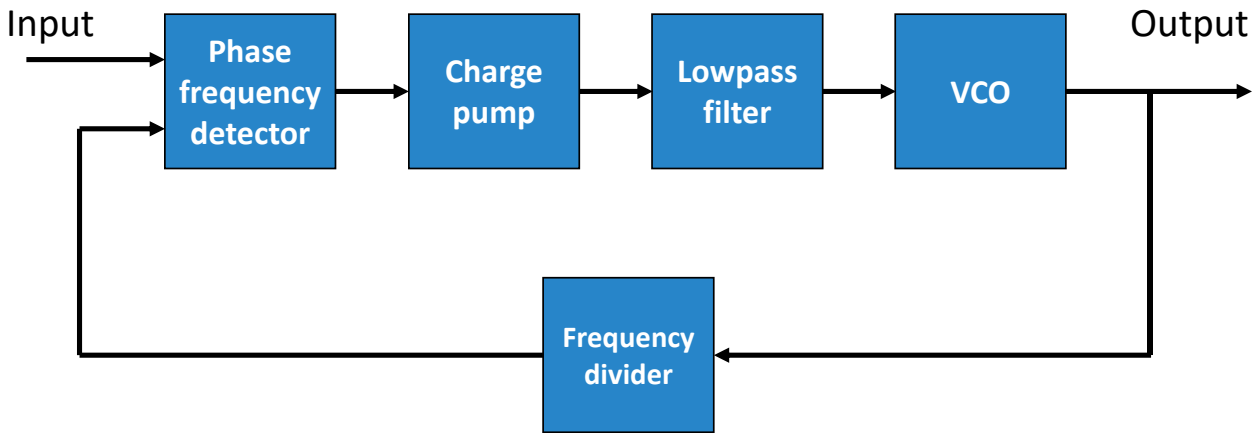


Fig. 2. 2 Diagram of the PLL circuit.

into the continuous voltage signals. This voltage signal enters the VCO, whose frequency varies depending on the input voltage, and the frequency of the output signal will be optimized and synchronized automatically. Thus, the PLL is possible to obtain a more stable output signal.

In the case of a transmitter, the baseband signal will be sent to the mixer, where it is multiplied by the local oscillator. Then, the modulated signal is filtered, amplified, and sent to the space, which performs the reverse function of a receiver. Hence, if the output frequency of the local oscillator goes wrong, it may lead to poor communication quality, interference, or even a complete system breakdown. In order to avoid such situations, it is important to select an appropriate oscillator and design an appropriate circuit.

2.2 Types of the oscillator

Various types of oscillators have been reported so far. According to the topology, they can be classified into two types: feedback type and relaxation type. The feedback type (harmonic oscillator) generates regular voltage fluctuations by returning a part of the output of the amplifier circuit to the input, while the relaxation type oscillator generates intermittent electrical signals by controlling the on/off timing of switches. The crystal oscillator, LC oscillator, and ring oscillator are the best-known feedback type oscillators. The famous 555 timer IC is one of the relaxation type oscillators.

When selecting which type of oscillator to implement or evaluating the performance of an oscillator, we often use the following parameters to help us to do the judge. I'd like to introduce some of them here.

(1) **Output frequency**: The oscillation frequency in Hz (1/s). Different target output frequency normally uses different types of the oscillator.

(2) **Phase noise or jitter**: One of the most important performances of the VCO, which is usually specified in dBc/Hz at a specific offset frequency from the output frequency of VCO. The lower phase noise means better performance. This will be explained in more detail in the latter section 2.3.

(3) **Frequency tunning range or Variable frequency range**: Defined as the ratio of the maximum/minimum frequency difference to the center frequency; a wide tuning range is preferred.

(4) **Power consumption**: The total power that is consumed from the DC source. Portable devices with batteries require low power consumption. The typical power consumption value of a CMOS VCO is around 10 mW.

(5) **Size or chip area**: Miniaturization is required.

(6) **Modulation linearity**: Mainly evaluated when VCOs are used as spread-spectrum clock oscillators.

(7) **Frequency stability with temperature**: It refers to the frequency drift of VCO with a temperature change and is usually expressed as $\mathrm{MHz/^{\circ}C}$.

(8) **Voltage sensitivity (K_{VCO})**: This is defined as the change in output frequency for input voltage change, which is specified as a positive real scalar with units in Hz/V.

In many cases, there is a discrepancy among the above characteristics, so it is difficult to design a circuit that performs well with all of the above parameters. For example, ring oscillators are known to have wide modulation width and compact chip size, but they always suffer from their poor phase noise performance.

In the next section, several types of oscillator circuits and their characteristics will be discussed, which are commonly used in high-frequency wireless communication systems.

2.2.1 Crystal oscillator

A crystal oscillator is a device that generates an accurate frequency by utilizing the piezoelectric phenomenon of quartz. Fig. 2. 3(a) shows the structure of the crystal unit. A typical crystal unit consists of a piezoelectric crystal blank sandwiched by two metal electrodes and is housed in a protective cage. When a voltage is applied to the metal electrodes in the opposite (applying an electric field to the piezoelectric crystal), deformation occurs in the piezoelectric

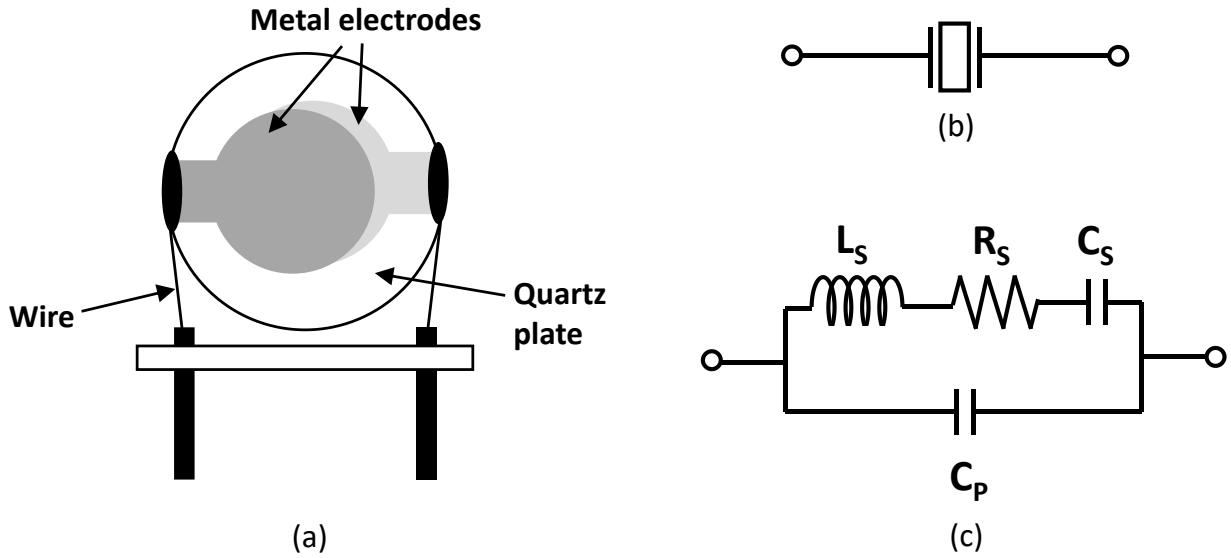


Fig. 2. 3 The crystal unit. (a) Its Internal construction. (b) Circuit symbol. (c) Equivalent circuit.

material. On the contrary, the piezoelectric crystal can also produce voltage when mechanical pressure is applied in a certain direction. Since the vibrations generated are mechanical vibrations, if the selected crystal is pure enough, very accurate and stable signals can be generated. The stability against environmental conditions, such as temperature, is also very excellent. Since the quartz crystal oscillator vibrates freely, the waveform is in the form of a sine wave.

In terms of electrical characteristics, the quartz crystal unit normally acts as a capacitor, but only in a certain frequency band close to its natural frequency, it will act as a coil with inductive admittance. Its equivalent circuit is shown in Fig. 2. 3(c).

Due to the big size of the crystal plate, most quartz crystal oscillators used in practical applications work around the range of 1 to 100 MHz. When a higher frequency is required, a frequency multiplier is normally required. However, the multiplier will worsen the phase noise

characteristics, so it will not be appropriately used as a signal source for mm-wave applications. Furthermore, because the oscillation frequency of the crystal unit itself is determined by the natural frequency of the crystal unit, this also makes it difficult to realize a wide frequency tuning range.

2.2.2 Ring oscillator

In a typical ring oscillator, the input and output ports of an odd number of NOT gates (inverters) are connected one after the other, and the last output is feedback to the first NOT gate's input. Fig. 2. 4 shows a three-stage ring oscillator. The gain of each inverter is designed as minus 1 (amplification factor is 1 and phase delay is 180 degrees). Because the time delay of each invert is the same, after three stages, the last inverter outputs the inverted value of the first stage's input, which is then input to the first inverter again. This kind of loop is repeated again and again, and then the square wave of constant frequency is generated.

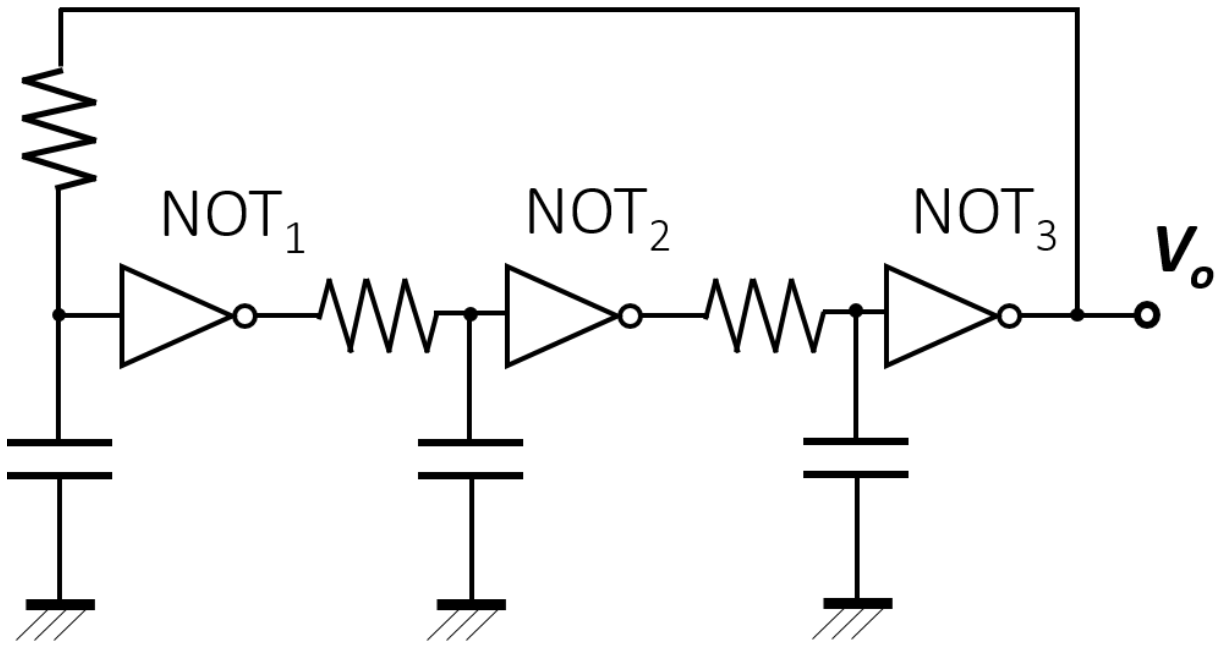


Fig. 2. 4 A 3-stage ring oscillator

Since the ring oscillator has a simple structure and can be realized with only NOT gates, it is ideally suited for integration into the chip. This makes it widely used in current electronic devices, especially those wearable devices. Another characteristic of the ring oscillator is that a relatively wide tuning range can be obtained by introducing resistors and capacitors between each NOT gate. However, because ring oscillators don't have a mechanism that can automatically compensate for

the phase shifts caused by external noise, the phase shifts will accumulate gradually. This is why the ring oscillator's phase noise characteristic is normally inferior to that of other types of oscillators. Although ring oscillators can produce a much higher output frequency than the crystal oscillator, it's difficult for them to generate signals higher than 10 GHz. In addition, multiple stages also bring a high power consumption. For these reasons, they are not suitable for the designs of mm-wave wireless communication systems.

2.2.3 LC oscillator

An LC oscillator is a type of resonant circuit that extracts a specific frequency signal by using the resonance effect of a capacitor and a coil. As an example, we can consider there is a parallel circuit that consists of a coil and a pre-charged capacitor. When the coil is connected to the capacitor which has stored the power, the capacitor begins to discharge, and the current flows to the coil, converting it into magnetic energy and lowering the voltage between the two ports of the capacitor. Eventually, all the power stored in the capacitor is released. However, the current will keep flowing. The current is gradually stored in the capacitor in the form of electrical energy, and

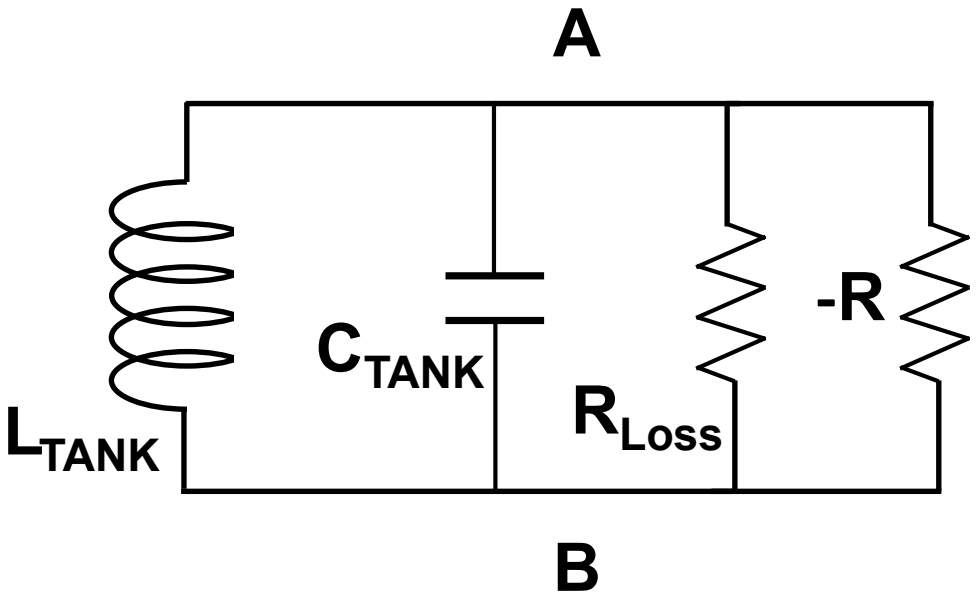


Fig. 2. 5 Simplified equivalent circuit of the LC oscillator.

the voltage is applied with the opposite polarity to the initial. When the magnetic energy in the coil

disappears, the current will stop this time, and the capacitor will become charged with a voltage in the opposite polarity, and it will discharge again, but this time the current will start flowing in the opposite direction.

The energy then goes back and forth again and again between the coil and the capacitor creating a sinewave. However, since both the actual coil and the capacitor have internal resistance, the sinewave decays rapidly. Therefore, in order to obtain a stable sinewave without decay, extra energy compensation is necessary. This concept is shown in Fig 2. 5. The outside energy compensation can be also recognized as a negative resistance that cancels the internal resistance of the LC resonator. Figure 2. 6 shows an example of an LC oscillation circuit, where the two transistors connected to the resonator perform the function of negative resistance.

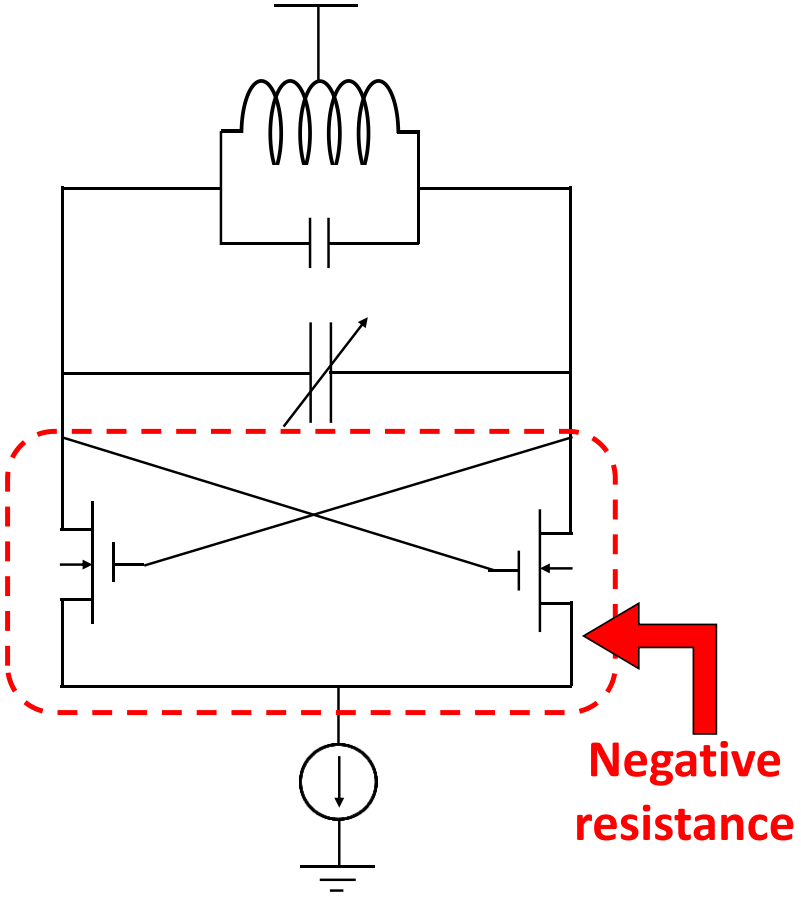


Fig. 2. 6 LC VCO.

The LC oscillator is known for characteristics such as simple configuration, high output frequency, and relatively wide frequency tuning range. Due to its positional in a frequency band higher than 10 GHz, research on it has been exceptionally popular recently [5]-[10]. However, in

order to satisfy the resonance condition, an inductor is required in the design of an LC oscillator, which normally occupies a big area in the chip. In addition, the circuit is susceptible to parasitic parameters at high frequencies, especially at the mm-wave band. It is always concerned about problems such as a significant drop in Q-factor and self-resonance. If we can overcome these problems, we can make progress in creating a mm-wave oscillator with good performance.

2.3 Phase noise characteristic of LC oscillator

In wireless communication systems, noise is an unwanted and random disturbance of the useful signal. It determines the quality of the communication and always trades with power dissipation, speed, and linearity of the communication system. Therefore, understanding the noise phenomenon and its effect on the circuit is very important. In the integrated circuits (such as receiver and transmitter), analog signals are normally corrupted by two different types of noise: device electronic noise and "environment" noise. The latter refers to random disturbances that a circuit experiences through the supply or ground lines or the substrate. As our target is to design the oscillator, I concentrate on the electronic noise in this section.

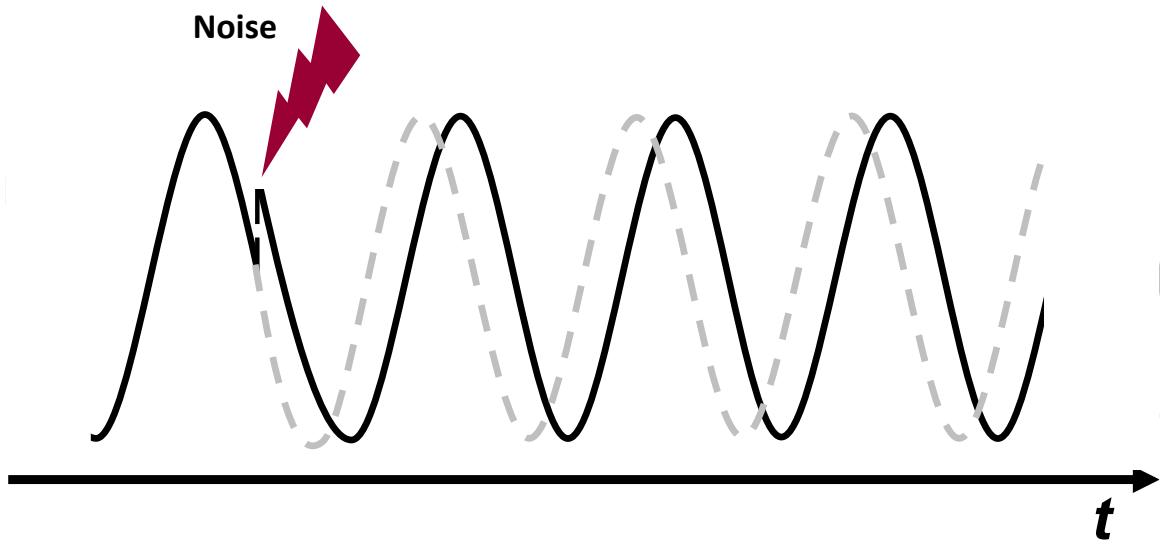


Fig. 2. 7 Origin of phase noise

2.3.1 What is the phase noise?

In recent years, communication technology has been developing rapidly, and the public demand for communication performance is increasing day by day. High speed, low latency, and stable communication systems are highly demanded. In order to evaluate the stability of a signal source, its phase noise characteristics are often investigated. Phase noise is explained by the fact that the amplitude and phase of an ideal sine wave are modulated by the inherent random noise of the device. As Figure 2. 7 shows, at a specific time, the overall phase of the signal is delayed or accelerated by thermal noise, flicker noise, shot noise, etc.

Due to this change, as shown in Fig. 2. 8, output spectrums generate in the neighbor frequency band of the original signal spectrum. One of the reasons why phase noise is important is that if the local oscillator of a communication system, which uses many frequency channels in close proximity, such as a cellular phone, has poor phase noise characteristics, the phase noise of a strong signal will bury those weak spectrums whose channel offset equals to the offset frequency of the phase noise. This is illustrated in Fig. 2. 9.

2.3.2 Phase noise models

Several models of phase noise have been proposed over these years for trying to explain how phase noise occurs and its characteristics. These models are extracted from the circuit models, so they also relate the phase noise to the oscillator design parameters like *Q-factor* and bias current. This may help the designer understand the oscillator from a different insight.

Those models introduced in the following sections have been presented in papers to predict the oscillator noise. In 1960 [11], Edson first projected the oscillator's noise model. In 1966, Leeson followed his work and described the noise distribution [12] in terms of the inductor-based oscillator. In 1996, Razavi studied the phase noise of inductor-less CMOS oscillators (ring oscillator and relaxation oscillator) and proposed linear models of them [13]. Then, Hajimiri and Lee improve Razavi's model by including nonlinear and long-delay effect [14]. Hajimiri and Lee also proposed a general theory of phase noise that can be used for all types of oscillators [15].

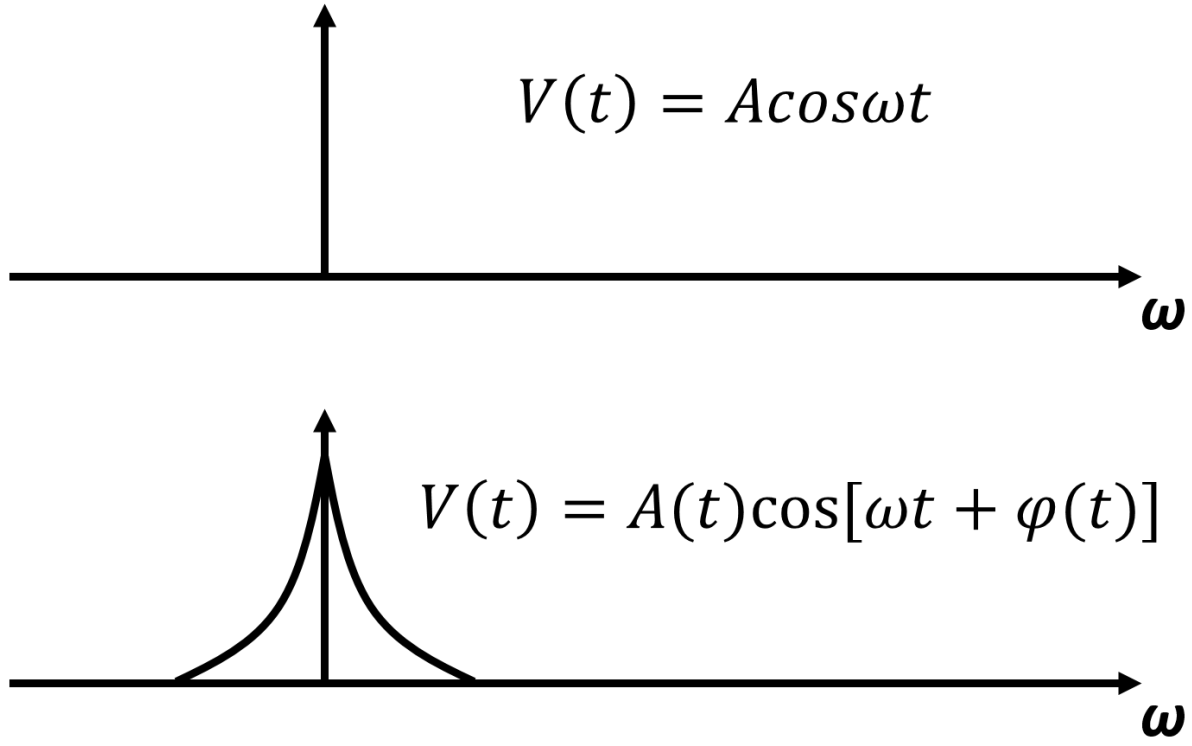


Fig. 2. 8 Ideal signal and practical signal.

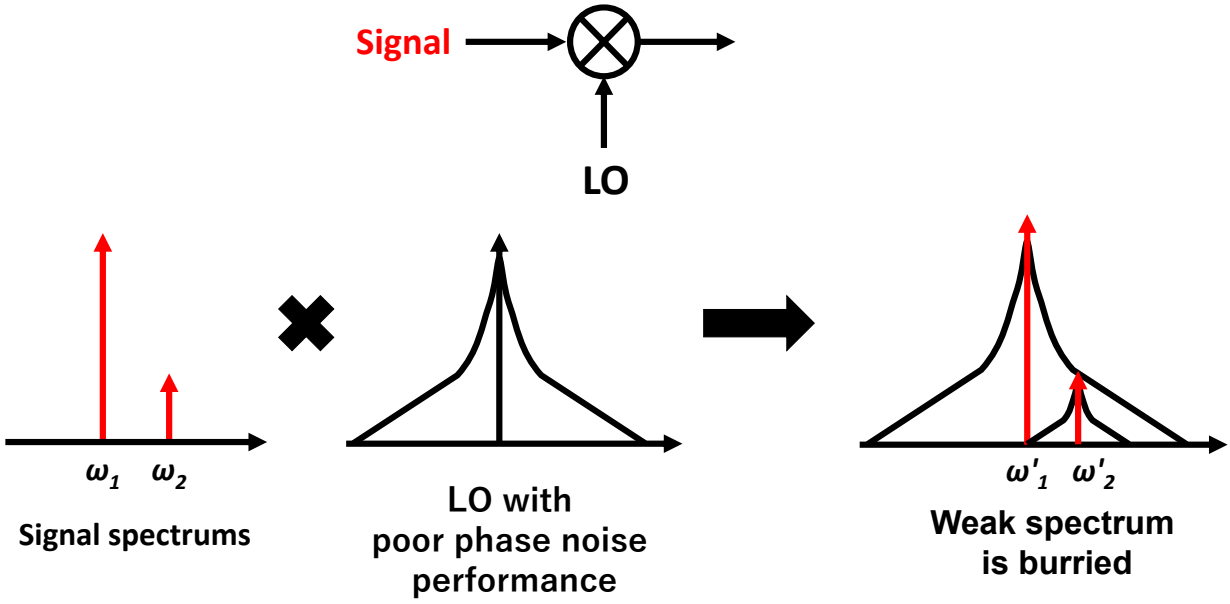


Fig. 2. 9 The hazards of phase noise

2.3.2.1 Lesson's model of the phase noise

The Lesson's phase noise model starts from an LC oscillator circuit shown in Fig. 2. 5. The impedance of the LC resonator can be expressed in a simpler form as equation (2.1).

$$Z_{tank} \approx \frac{j\omega L}{1-\omega^2 LC} \tag{2.1}$$

Here, the impedance of the resonator at frequency $\omega_0 + \omega_m$ can be calculated by the equations (2.2) and (2.3)., where the ω_m is the offset angular frequency from the central frequency ω_0,

$$Z_{tank}(\omega_0+\omega_m) \approx \frac{j(\omega_0+\omega_m)L}{1-(\omega_0+\omega_m)^2 LC}$$

$$= \frac{j\omega_0 L}{1-({\omega_0}^2+2\omega_0\omega_m)LC} = -\frac{j\omega_0 L}{2(\frac{\omega_m}{\omega_0})} \tag{2.2}$$

$$\therefore |Z_{tank}(\omega_0+\omega_m)| \approx \frac{\omega_0 L}{2(\frac{\omega_m}{\omega_0})} \tag{2.3}$$

while the Q-factor of the LC resonator tank circuit is calculated by the equation (2.4).

$$Q = \frac{R}{\sqrt{\frac{L}{C}}} = \frac{R}{\omega_0 L} = R\omega C \tag{2.4}$$

Using equation (2.4), the equation (2.3) can be transformed as shown in equation (2.5).

$$|Z_{tank}(\omega_0+\omega_m)| \approx \frac{\omega_0}{2\left(\frac{\omega_m}{\omega_0}\right)}\frac{R}{\omega_0 Q} = \frac{R\omega_0}{2Q\omega_m} \tag{2.5}$$

If we consider the thermal noise as the voltage form, the output noise will be the product of the current noise and the impedance of the resonator, which is shown in equation (2.6).

$$\overline{v_n^2} = \overline{i_n^2}|Z_{tank}(\omega_0+\omega_m)|^2 \tag{2.6}$$

The current noise $\overline{i_n^2}$ can be expressed by the equation (2.7), where k is the Boltzmann constant, T is the temperature, and Δf is the offset frequency.

$$\overline{i_n^2} = \frac{4kT}{R}\Delta f \tag{2.7}$$

Therefore, equation (2.8) can be derived from equations (2.5) to (2.7).

$$\overline{v_n^2} = \frac{4kT}{R}(\frac{R\omega_0}{2Q\omega_m})^2\Delta f = 4kTR(\frac{\omega_0}{2Q\omega_m})^2\Delta f \tag{2.8}$$

Since the phase noise is defined as the ratio of the noise power to the power of the carrier divided by the offset frequency, the phase noise $L(\omega_m)$ at an offset ω_m from the carrier frequency can be calculated by the equations (2.8) and (2.9).

$$L(\omega_m) = \frac{\frac{\overline{v_n^2}}{\Delta f}}{v_{out}^2} = \frac{4kTR}{v_{out}^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \tag{2.9}$$

Here, the relationship between the output power P_{osc} and output amplitude v_{out} of the oscillator can use equation (2.10) to express.

$$P_{osc} = \left(\frac{v_{out}}{\sqrt{2}}\right)^2 \frac{1}{Re(Z_{tank})} = \left(\frac{v_{out}}{\sqrt{2}}\right)^2 \frac{1}{R} \tag{2.10}$$

Then, the equation (2.11) can be obtained from equations (2.9) and (2.10).

$$L(\omega_m) = \frac{4kTR}{v_{out}^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 = \frac{2kTR}{P_{osc}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \tag{2.11}$$

If the noise factor of the active device is F, equation (2.11) can be transformed into equation (2.12).

$$L(\omega_m) = \frac{2kTF}{P_{osc}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \tag{2.12}$$

Since the LC resonator can be considered as a kind of bandstop filter, the phase noise of the oscillator becomes independent of the offset frequency from ω_m and finally becomes flat. Therefore, a constant is added to the equation (2.12) and the equation (2.13) is obtained.

$$L(\omega_m) = \frac{2kTF}{P_{osc}}\left\{1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\} \tag{2.13}$$

The noise factor of active devices is introduced in equation (2.14). The active devices don't only have the thermal noise, but also have the flicker noise in its low harmonic frequency region. If we consider the corner frequency of the thermal noise and flicker noise in the active device circuit is $\omega_{1/f}$, we can add that term and convert the angular frequency to frequency to obtain the equation (2.14).

$$L(\omega_m) = \frac{2kTF}{P_{osc}}\left\{1 + \left(\frac{f_0}{2Qf_m}\right)^2\right\}\left(1 + \frac{f_{1/f}}{f_m}\right) \tag{2.14}$$

This equation is called Leeson's equation [12] and it is proposed for feedback type oscillators. From equation (2.13), the phase noise of the LC oscillator is considered to have a slope of -9 dB/oct (-30 dB/dec.) in the low harmonic frequency region due to the superposition of flicker noise. A

slope of -6 dB/oct (-20 dB/dec.) is in the thermal noise region. Figure 2. 10 shows the relationship between the phase noise of the oscillator and the offset frequency.

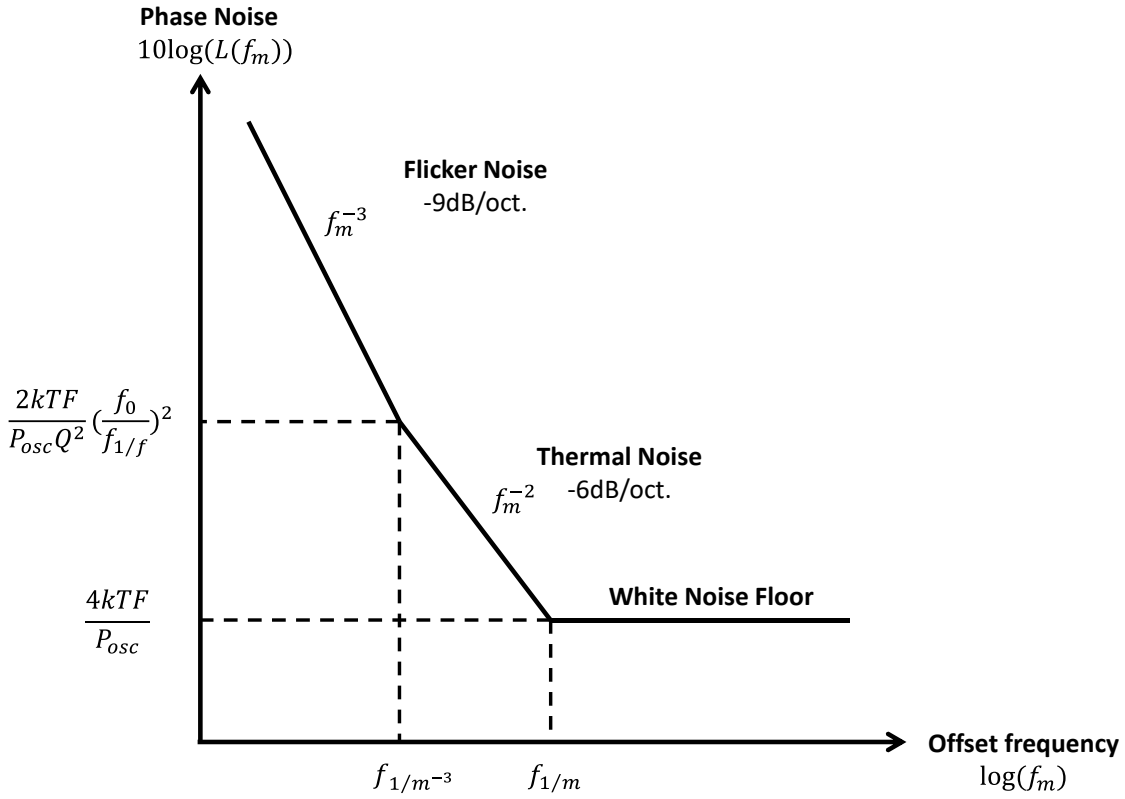


Fig. 2. 10 The spectrum of the phase noise.

2.3.2.2 Razavi's model of the phase noise

To obtain an estimate of the noise behavior of the ring oscillator and the relaxation oscillator, Razavi introduced a new definition of Q-factor for them. This makes it possible to use a similar analyzing way of Leeson's model which is based on the Q-factor of the LC resonator tank in a traditional LC oscillator [12]. He employed a linear model which identified and formulated three phase noise phenomenon called additive noise, high-frequency multiplicative noise, and low frequency multiplicative noise of CMOS ring oscillator [13]. The open loop Q-factor for the ring oscillator is defined as (2.15). This Q-factor, for ring oscillator, does not mean the ratio of active energy to energy loss per cycle.

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\phi}{d\omega}\right)^2} \tag{2.15}$$

where, A and ϕ are the gain and the phase of the open-loop transfer function in the linear model of an oscillator. In this model, Razavi described the trade-off between power dissipation and oscillator noise, by designing a four stage quadrature ring oscillator.

2.3.2.3 Hajimiri and Lee's model of the phase noise

All of the above phase noise models are based on the analysis of linear time-invariant systems, which make them inapplicable for all classes of oscillators. However, in reality, most of the oscillators are periodically time-varying systems. In order to solve this problem, Hajimiri and Lee proposed a new phase noise model which is based on the time-variant system. This extends the theoretical analysis of phase noise to all types of oscillators.

Hajimiri and Lee's model explains how electrical noise sources such as device noise up-converted into phase noise and the impact of the output waveform to flicker noise up-conversion. This model can predict phase noise from stationary and cyclo-stationary sources and shows that $1/f^3$ corner in the phase noise spectrum is not the same as $1/f$ corner in the device noise spectrum as assumed in previous models [12], whose factors depend on the symmetry property of the waveform. Their research shows that it's possible to suppress the flicker noise up-conversion with a good design.

In addition, Hajimiri and Lee also proposed a useful design metric called impulse sensitivity function (ISF) to describe how "sensitive" the circuit is from a perturbation at the specific time at time $t = \tau$ of the whole waveform. It is a dimensionless periodic function symbolized as $\Gamma(x)$ with a period of 2π, which is independent of frequency and amplitude, but the value is governed by the nonlinearity and topology of the oscillator [16]-[18].

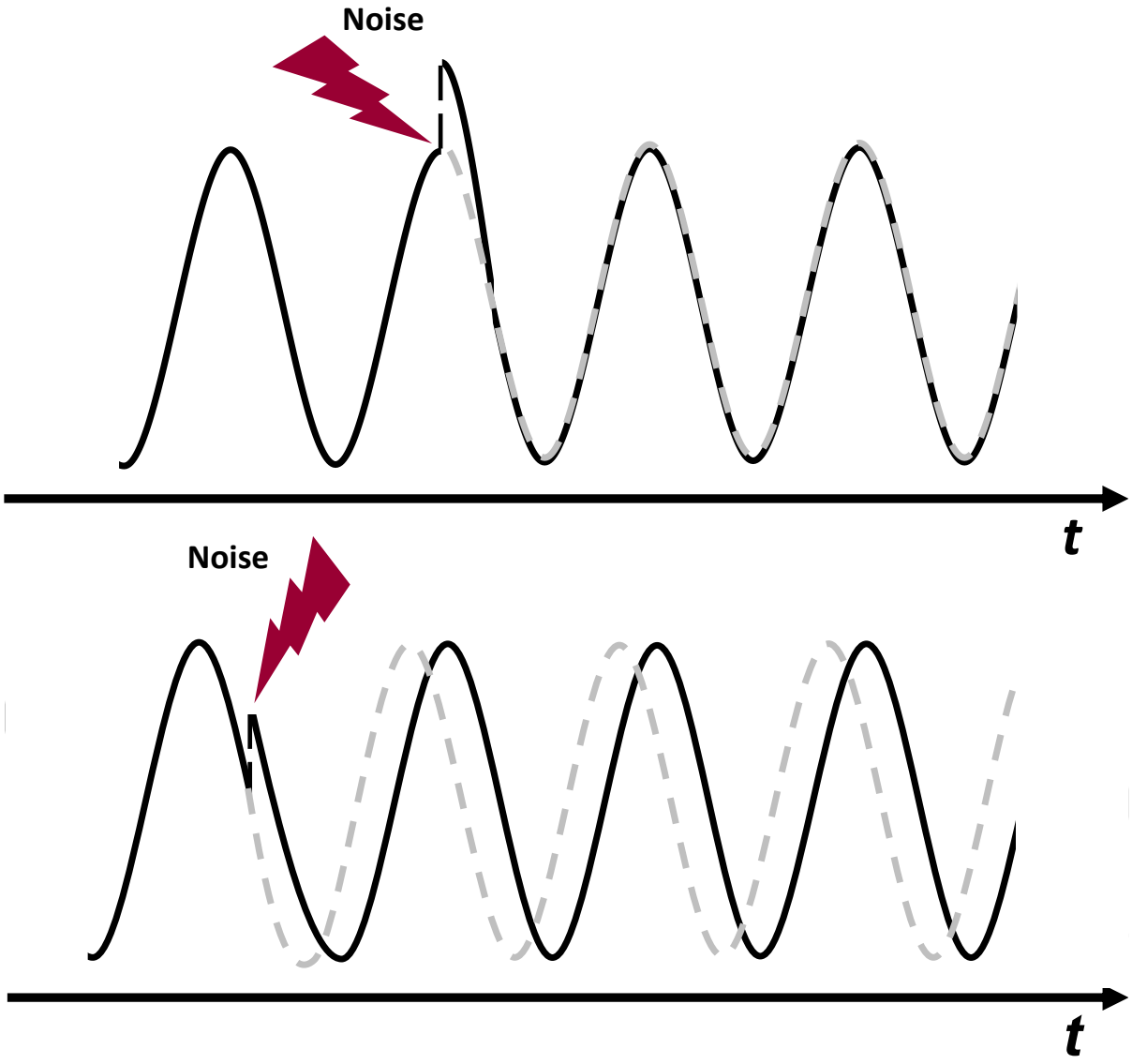


Fig. 2. 11 Time variant perturbation of the oscillator signal by an impulse produces different effects on the oscillation. (a) At peak crossing (b) At a position between the peak and valley.

The ISF theory points out that at different instants of the output signal, it has a different sensitivity to the noise. For example, as shown in Fig. 2. 11, if the impulse noise signal is injected while the oscillation amplitude is at its peak, the oscillation waveform will return to its original amplitude except enduring a small amplitude change (ΔV). However, if the same noise impulse is applied while the amplitude is between the peak and valley, the oscillation undergoes a noticeable phase shift ($\Delta\emptyset$). This is how the phase noise formed, and the impulse response may be written as (2.16).

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{2.16}$$

where, *u(t)* is the unit step function and $\Gamma(x)$is the impulse sensitivity function, and q_{max} is the maximum charge displacement across the capacitor. As a periodic function, ISF can be expanded in a Fourier series given by (2.17).

$$\Gamma(\omega_0) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n \cos(n\omega_0 + \theta_n) \tag{2.17}$$

where, C_n represents the amount of noise contributed around the frequency $n\omega_0$ and θ_n represents the phase shift at nth harmonics. Phase noise in the $1/f^2$ region can be expressed as (2.18).

$$\mathcal{L}(\Delta\omega) = 10\log[\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{i_n^2/\Delta f}{2\Delta\omega^2}] \tag{2.18}$$

Γ_{rms}^2 is the root mean square (RMS) value of the ISF. However, there are certain limitations of the linear time-variant theory when explaining the phase noise spectrum in oscillators especially the ω_{1/f^3} region.

According to the description above, it can be found that the calculation of ISF is complex and this makes it difficult to use. So, in the appendix of their paper, Hajimiri and Lee give an easy-to-use approximate method to calculate the ISF as shown in (2.19). This method is based on the first derivative and shows only little variation with the accurate result.

$$\Gamma_i(x) = \frac{f_i'(x)}{f_{max}'^2} \tag{2.19}$$

2.3.3 Phase noise reduction

After the discussion of the above phase noise models, we can find that there are three main directions in that we can improve our oscillator design in order to achieve an LC oscillator with low phase noise.

- Low noise figure, F
- High oscillation power, P_{osc}
- High Q-factor of the LC resonator

However, the realization of low noise figure F normally requires a redesign of the transistor or implementation of advanced processes. Therefore, the manufacturing cost will continue to increase

along with the complexity of the transistor structure and the change of materials. Then, although the output phase noise can be suppressed with high output power, the power consumption of the entire circuit increases at the meanwhile, which is undesirable for wireless communication systems. This research mainly focuses on the realization of LC resonator with high Q-factor in mm-wave, and two methods of implementing high Q resonator is proposed and discussed in the following sections.

CHAPTER 3: Integrated High-Q Resonators in CMOS Process

According to the discussion in the above chapter, designing a resonator with a high Q-factor is the most effective way to realize a low phase noise VCO for the wireless communication system. However, due to the stringent size limitation of the metal layers of the CMOS process, the implementation of the high-Q integrated resonator becomes very challenging.

During the doctoral course, my research focused on the analysis, design, and implementation of high-Q integrated CMOS resonators. There are two main categories of high-Q resonators utilized in my research. They are defected ground structure (DGS) resonators and substrate integrated waveguide (SIW) resonators. In this chapter, the implementation method and characteristics of these types of resonators will be investigated and introduced respectively.

3.1 DGS Resonators

DGS is a technology that controls the electromagnetic characteristics of a transmission line by defecting a hole of a specific shape in the ground. DGS was proposed by Jong-Im Park and his colleagues in 1999 to solve the problems of the Photonic Band Gap (PBG) structure, which works as a band stop filter but has difficulty in fabrication and radiations [19]. One of the features of DGS is that it does need practical capacitors and inductors to realize the resonance, which makes it possible to design in a compact size. Hence, there has been a lot of research into DGS over recent years [20]-[35]. So far, DGS has been used as antennas and filters, but there are still few reports of its application in CMOS process.

In this section, the DGS is used to realize the high Q-factor resonator for improving the phase noise performance of VCO designs. The limitations of the conventional DGS resonators are introduced at first. Then, to solve these problems, a novel two-branch DGS resonator is proposed and its characteristic is investigated.

3.1.1 Limitations of the Conventional DGS Resonator

A DGS resonator is a technology realized by etching a specific pattern on the ground plane of the transmission line. This pattern will interrupt the electromagnetic (EM) fields of the transmission line and realize a resonator with a high Q-factor [26]. Fig. 3. 1 shows two types of the conventional

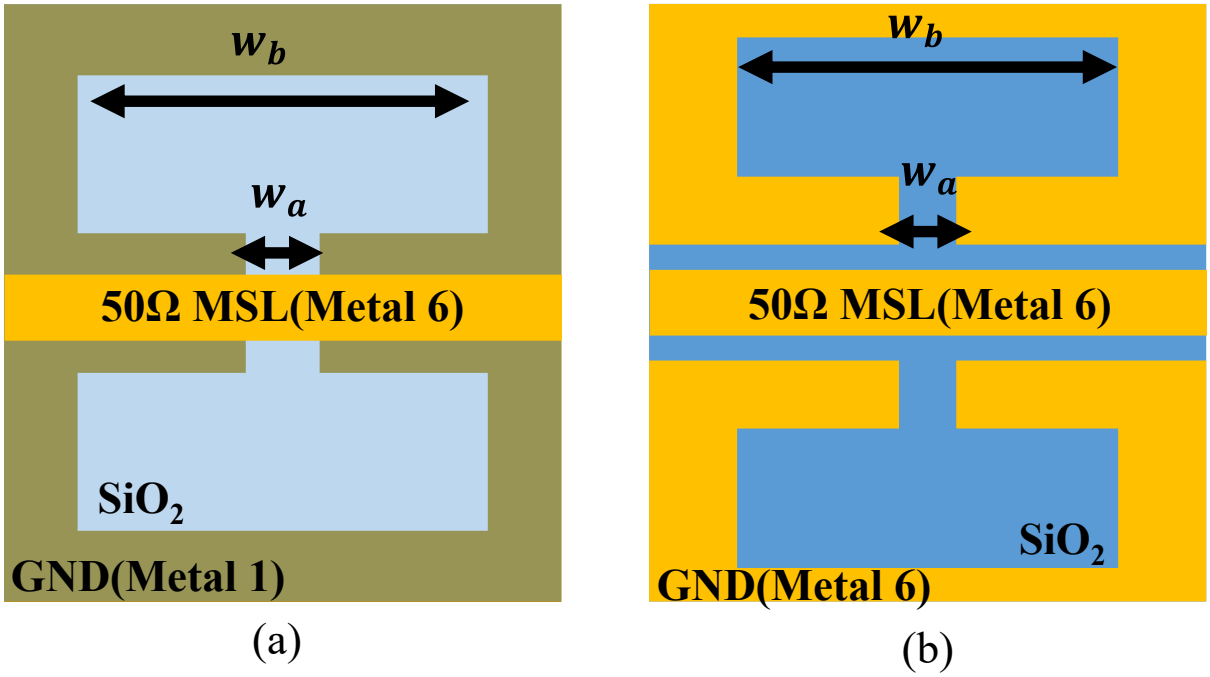


Fig. 3. 1 Conventional DGS resonators. (a) H-shape DGS resonator [32]. (b) H-shape CPW type DGS resonator [34].

DGS resonator [32], [34]. Fig. 3. 1(a) is the basic H-shape DGS resonator where the signal line is on the top metal layer and the ground plane is etched on the bottom plane, and Fig 3. 1(b) is the H-shape DGS resonator based on coplanar waveguide (CPW) where the signal line and ground plane are etched on the top metal layer [34]. These DGS resonators have been implemented in K band VCOs [32]-[34].

Fig. 3. 2 shows a typical equivalent circuit of a VCO using the DGS resonator. To start oscillation, transistors are connected to two ports of the DGS resonator and work as the negative resistance. In order to prevent interrupting DGS's EM fields, these transistors are normally placed next to the DGS resonator rather than below it. Because of the significant size difference between the DGS resonator and transistors, the interconnects can only be put along the edge of the DGS resonator. Additionally, the ports of the conventional DGS resonators are on opposite sides. This also increases interconnects' length. As a result, interconnects' total length is roughly two times longer than the DGS resonator. In [31], the present authors have experimentally verified the effect of long interconnects, which not only influence determining the VCO's output frequency but also deteriorate its phase noise performance.

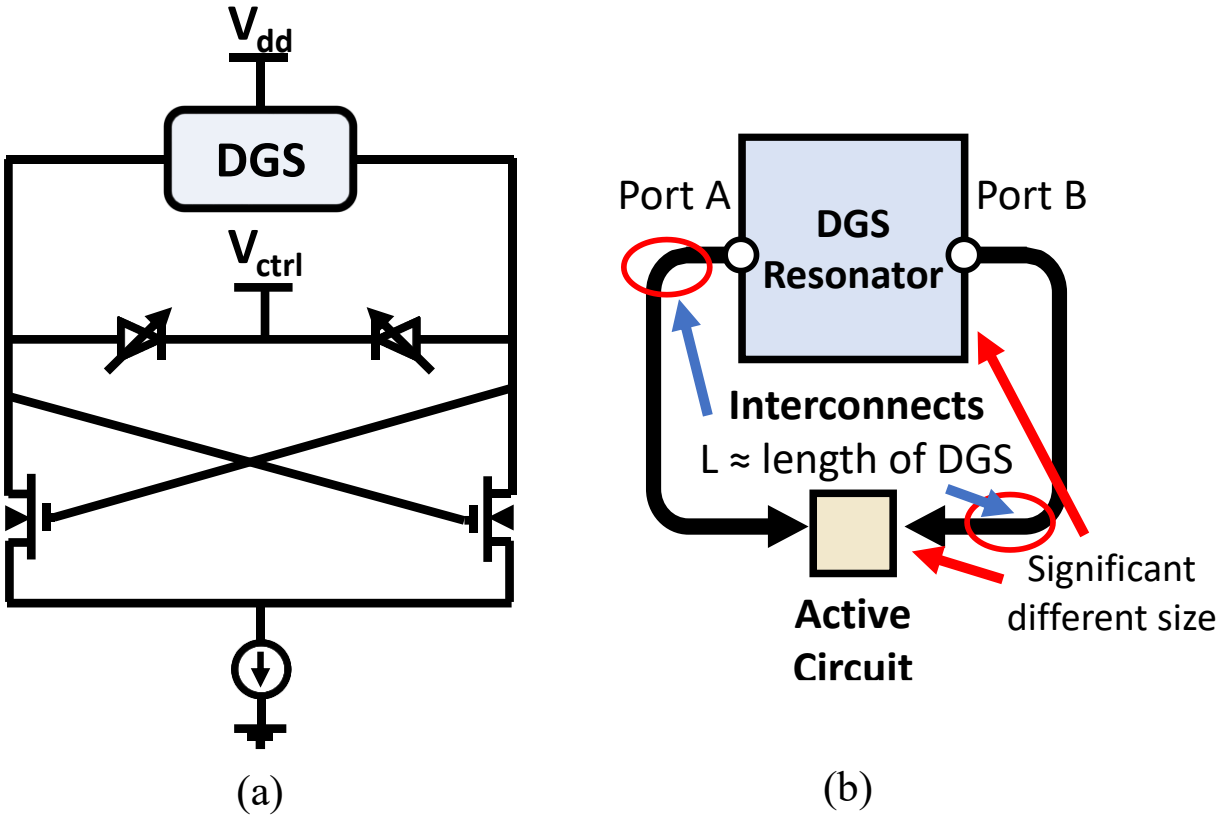


Fig. 3. 2 Equivalent circuit of VCO using DGS resonator. (a) Circuit topology. (b) To connect conventional DGS resonator to active circuit, interconnects which is roughly same as DGS's border length is necessary.

3.1.2 Proposed Novel Two-branches DGS Resonator with Compact Size and High Q-factor

As discussed above, the distance between ports of the DGS resonator influences the length of interconnects. To reduce the distance between these two ports, we divide the conventional DGS resonator into two small resonators at first without altering its resonance frequency. The concept is shown in Fig. 3. 3(a). The divided DGS resonators are lifted and set face to face on either side of the supply voltage, V_{dd}. As shown in Fig. 3. 3(b), the distance between Port 1 and Port 2 is reduced from the length of the DGS resonator to a minimum distance preventing two resonators from affecting each other.

Then, different from the conventional H-shape DGS resonator [34], only one side of the DGS resonator is used for increasing the Q-factor. This one-side DGS resonator realizes a higher Q-factor than the conventional H-shape DGS resonator by reducing the number of current loops in

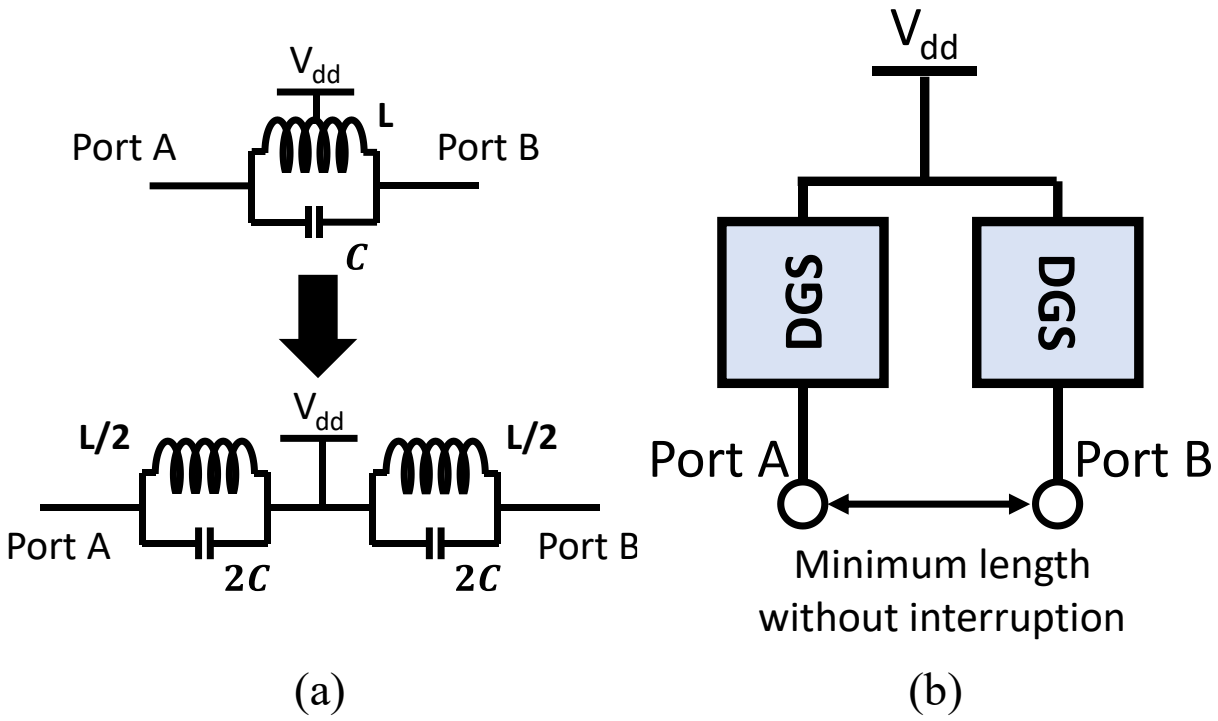


Fig. 3. 3 Design concept. (a) Dividing one DGS resonator to two resonators maintaining the same resonance frequency. (b) Distance between ports of DGS is reduced to the minimum length which two resonators don't interrupt each other.

the ground plane [26]. The DGS resonator can be seen as a parallel LC tank resonator where the capacitance part is generated by the gap w_a (Fig. 3. 1) and the inductance part is generated by the outside loop [26]. Lengthening both w_a and w_b will decrease the capacitance part of the DGS resonator and increase the inductance part. This will increase the Q-factor of the DGS resonator furthermore. In addition, enough space is created for integrating the varactor inside the DGS and saves the chip area.

Fig. 3. 4 shows the top view and the 3D model of the proposed two-branches DGS resonator. Both transmission line and ground plane are implemented on the top metal layer (Metal 6), which

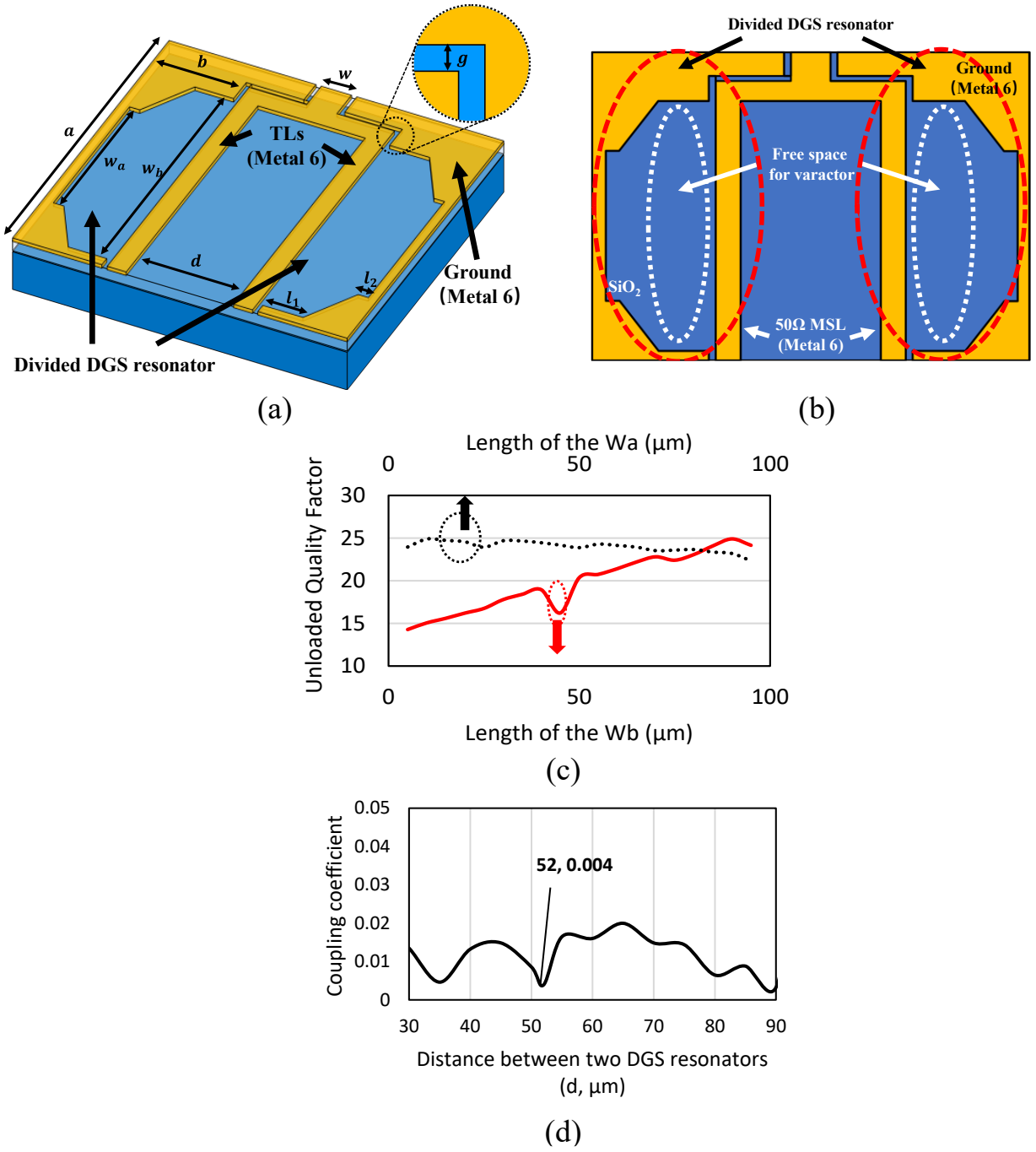


Fig. 3. 4 Proposed DGS resonators and its implementation in CMOS technology. (a) Overview of the proposed DGS resonator. (b) Top view. (c) Relationships amongw_a, w_b, and Q_u. (d) Simulated coupling between the two DGS resonators while changing the distance d.

TABLE 3. 1 Design parameters of the DGS resonator

Parameters	a	b	d	g	l_1	l_2	w	w_a	w_b
Dimension(μm)	120	37.5	52	1	20	5	6.5	45	95

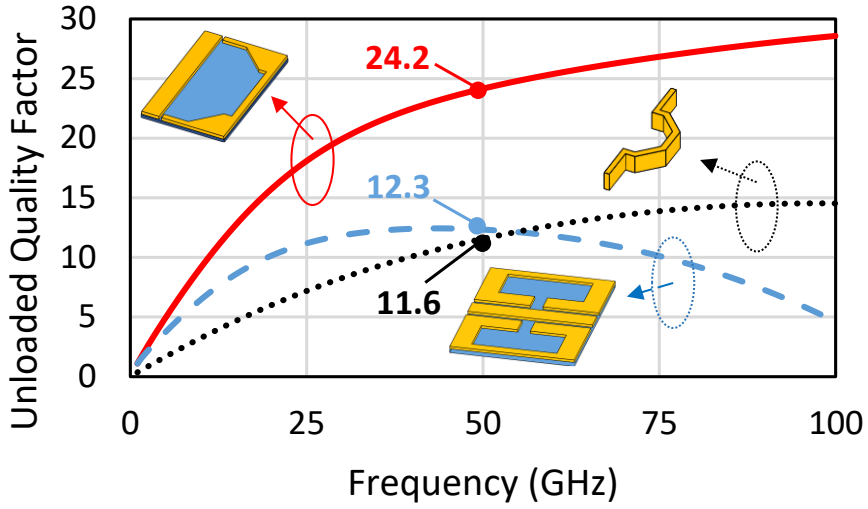


Fig. 3. 5 Simulated Q_u of the proposed DGS inductor.

TABLE 3. 2 Comparison of Q-factor with Reported Works

	Proposed DGS	[10]	[12]	[13]	[14]	[16]
Q_u	24.2	18	15	18	≈18	15

is the thickest metal layer in the used technology. The self-inductance (L_{eq}), the resistance (R_{EQ}), and the unloaded Q-factor (Q_u) of the DGS resonator can be calculated by (3.1). Fig. 1(b) shows the simulated Q_u while changing the length of w_a and w_b. Increasing w_b increases Q_u of the proposed two-branches DGS resonator, while changing w_a doesn't have significant effect. Due to that DGS resonators are close and possibly affect each other, we investigated the coupling between them. The simulated result is shown in Fig. 1(c), which shows that although there isn't an obviously relationship between distance d and the coupling of the two resonators, but the coupling is weakest when d equals to 52 μm.

$$L_{eq} = Im(Z_{11})/\omega \qquad R_{EQ} = Re(Z_{11}) \qquad Q_u = Im(Z_{11})/Re(Z_{11}) \tag{3.1}$$

A comparison of the simulated Q_u among the proposed DGS resonator, the conventional spiral inductor, and the CPW-type H-shape DGS resonator is given in Fig. 3. 5. These three types of resonators are compared under an approximately same inductance value. It can be found that both the proposed DGS resonator and the spiral inductor have an increasing Q_u during the simulation interval, while the Q_u of the conventional H-shape DGS drops after 50 GHz, which is caused by

its self-resonance. At 50 GHz, which is the design target frequency, the proposed DGS resonator has a Q_u of 24.2. This is two times those of the conventional spiral inductor and conventional H-shape DGS, which are 11.6 and 12.3, respectively. The high Q_u of the proposed DGS resonator is expected to achieve a good phase noise. The optimized dimension of the proposed DGS resonator is summarized in Table 3. 1.

As people normally customize a specific inductor in their V band VCO designs, a comparison of Q_u among the proposed DGS resonator and those reported inductors is given in Table 3. 2. The proposed DGS inductor has the highest Q_u when compared to other resonators used in the reported V band VCO designs.

3.2 SIW Resonators

In section 3.1, it has been verified that DGS resonators have high Q-factor during mm-wave designs. However, because the DGS resonator is realized based on an "open" structure, it has radiation problems and can be easily interfered with by other nearby lines. This results in the inconvenience that the DGS resonator has to be placed a certain distance apart from other wires during the design of the circuit layout. Although the VCO implementing DGS resonator is still more compact than that using conventional LC resonator, it hindered the further miniaturization. To overcome this inconvenience, we set our sights on the SIW structure.

SIW, which has outstanding performance on low loss, high quality (Q-) factor, and high power handling capability, has drawn a lot of attention and is well developed in the printed circuit board (PCB) process [50]-[57],[74] in these years. However, its relatively huge dimension compared to other on-chip components becomes an obstacle while implementing it in CMOS technology.

To miniaturize the size of the SIW cavity, in printed circuit board (PCB) technology, several techniques include quarter-mode SIW (QMSIW) [50][51], eighth-mode SIW [52], folded ridged QMSIW [53], and mixed-mode [54] have been reported. In CMOS technology, because of the stringent requirements for size, metal density, and design rules, miniaturization and fabrication of the SIW cavity become very challenging. Until now, SIW cavities still have not been exploited well in commercial CMOS technology [58]-[60]. Additionally, because of the limited metal thickness and distance between each metal layer of CMOS technology, conventional coupling methods of SIW cavities become invalid for on-chip design.

In this section, a novel miniaturization method of SIW cavity in CMOS process is proposed, which is called slot-loaded folded ridged quarter-mode SIW (QMSIW) technology. The characteristic of the minimized slot-loaded folded ridged quarter-mode SIW cavity resonator is investigated at first. Then, to make it suitable for utilizing in the future design of integrated feedback type oscillators for W band applications, the proposed resonator is transformed from one port resonator to two ports resonator by three different methods. Three types of W band two ports resonators are designed, fabricated, and measured. One of them is with two transmission zeros using shielded folded ridged QMSIW resonator but without slot-load. This resonator is proposed to verify if the SIW resonator works properly at a frequency beyond 100 GHz.

3.2.1 Slot-loaded Shielded Folded Ridged QMSIW cavity Resonator

Fig. 3.6 shows the comparison of 3D models of a conventional folded ridged QMSIW cavity and the proposed cavity. In Fig. 3.6(a), a conventional folded ridged cavity that has recently been proposed in PCB [53] under 2GHz applications is shown. In Fig. 3.6(b), the proposed cavity and its 3D view for implementation in a commercial 1P6M CMOS technology are illustrated. As illustrated in Fig. 3.6(c), the conventional folded ridged QMSIW cavity has leakage from the open

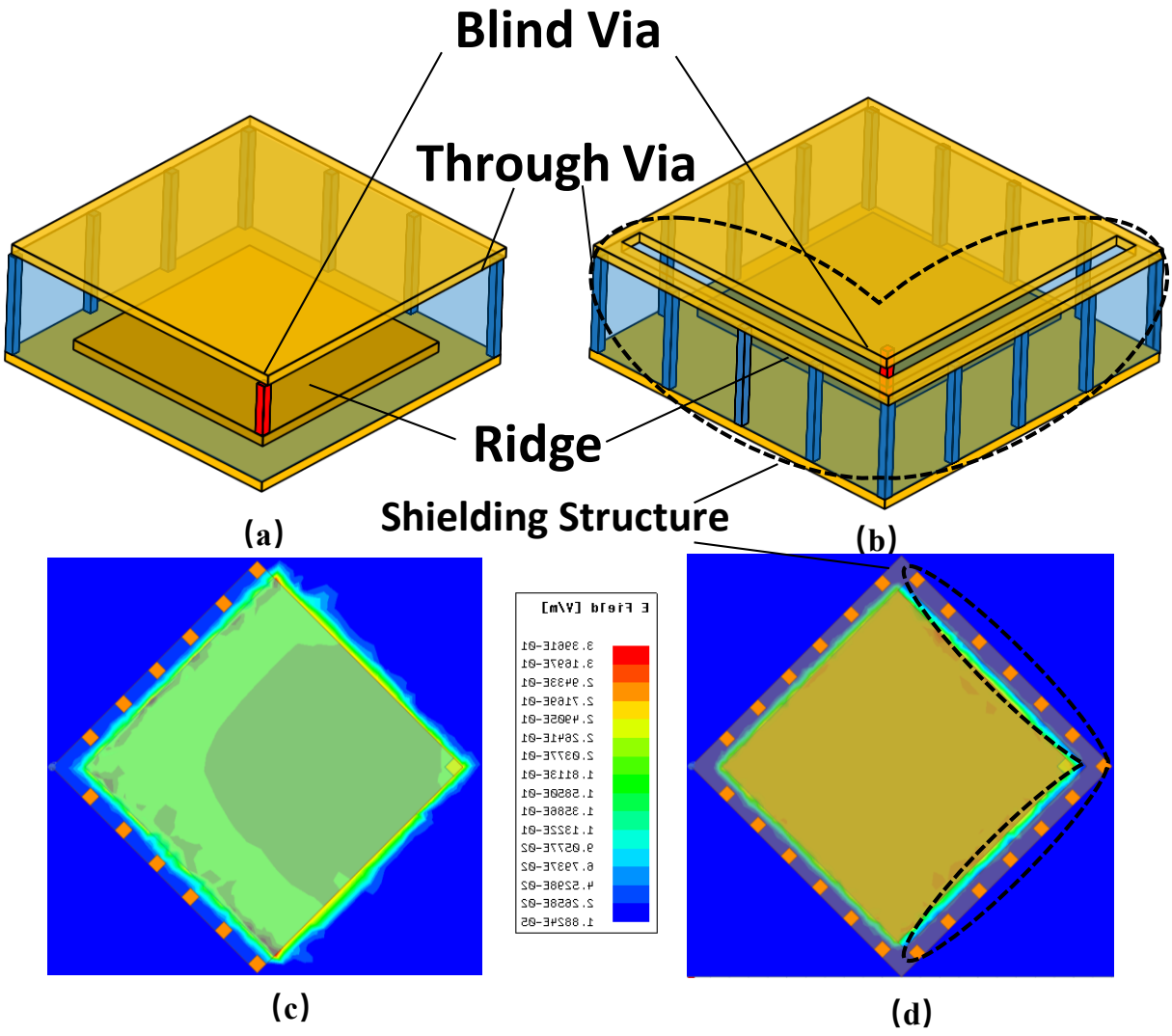
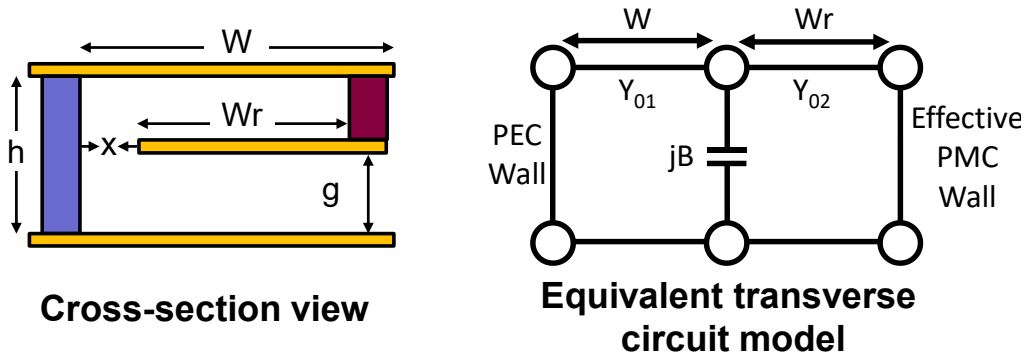


Fig. 3. 6 3D models implemented in CMOS technology and simulated electric field distribution of the folded ridged QMSIW and the shielded folded ridged QMSIW. (a) and (c) are of the folded ridged QMSIW. (b) and (d) are of the shielded folded ridged QMSIW.

sides. In the proposed cavity of Fig. 3.6(b), the open sides are replaced with a right-angled slot and vertical shorted 'walls' which are composed of through vias. This mitigates the leakage from the open aperture as shown in Fig. 3.6(d).



(a) (b)

Fig. 3. 7 (a) Cross-section view and (b) Equivalent transverse circuit model of the folded ridged QMSIW and the shielded folded ridged QMSIW.

The dimension of the folded ridged QMSIW cavity can be calculated by (3.2) using the method introduced in [53] with its equivalent transverse circuit model shown in Fig. 3.7(b),

$$-\cot\left(\frac{2\pi}{\lambda_c}W\right)+\frac{B}{Y_{01}}+\frac{Y_{02}}{Y_{01}}\tan\left(\frac{2\pi}{\lambda_c}W_r\right)=0 \tag{3.2}$$

where W and Wr are the widths of the waveguide and ridge as shown in Fig. 3.7(a), respectively, λ_c the wavelength of the target resonance frequency, Y_{01} and Y_{02} the transverse characteristic admittance of the waveguide channel and ridge sections, respectively, and B the transverse step capacitance due to the transition between the channel and ridge. The ratio of B/Y_{01} and Y_{02}/Y_{01} can be calculated using the equations in [53] and [57].

$$\frac{Y_{02}}{Y_{01}}=\frac{h}{g} \tag{3.3}$$

$$B=B_S+B_C \tag{3.4}$$

$$\frac{B_S}{Y_{01}}=\frac{2h}{\lambda_g}\left[\ln\left(\frac{1-\alpha^2}{4\alpha}\right)\left(\frac{1+\alpha}{1-\alpha}\right)^{0.5\left(\alpha+\frac{1}{\alpha}\right)}+2\frac{A+A'+2C}{AA'-C}+\left(\frac{h}{4\lambda_g}\right)^2\left(\frac{1-\alpha}{1+\alpha}\right)^{4\alpha}\left(\frac{5\alpha^2-1}{1-\alpha^2}+\frac{4\alpha^2C}{3A}\right)^2\right] \tag{3.5}$$

$$\frac{B_C}{Y_{01}} = (\frac{2\pi}{\lambda_c})(\frac{h-g}{\varepsilon_r \varepsilon_0})C_f \tag{3.6}$$

$$C_f = \frac{\varepsilon_r \varepsilon_0 t}{x}[1 + \frac{x}{\pi t}(1 + \ln(\frac{2\pi t}{x}))] \tag{3.7}$$

where

$$\alpha = \frac{g}{h} \tag{3.8}$$

$$\lambda_g = \frac{\lambda}{\sqrt{1 - (\frac{\lambda}{\lambda_c})^2}} \tag{3.9}$$

$$A = \left(\frac{1-\alpha}{1+\alpha}\right)^{2\alpha} \frac{1 + \sqrt{1 - (\frac{h}{\lambda_c})^2}}{1 - \sqrt{1 - (\frac{h}{\lambda_c})^2}} - \frac{1 + 3\alpha^2}{1 - \alpha^2} \tag{3.10}$$

$$A' = \left(\frac{1-\alpha}{1+\alpha}\right)^{2/\alpha} \frac{1 + \sqrt{1 - (\frac{g}{\lambda_c})^2}}{1 - \sqrt{1 - (\frac{g}{\lambda_c})^2}} + \frac{3 + \alpha^2}{1 - \alpha^2} \tag{3.11}$$

$$C = (\frac{4\alpha}{1 - \alpha^2})^2 \tag{3.12}$$

g is the distance between the ridge and the ground, h is the distance between the top metal layer and the ground, t is the thickness of the ridge, and x is the distance between the folded ridge and thru vias.

By adding the shielding structure, the proposed cavity's size increases around 20% while the unloaded quality factor (Q_U) is maintained. At 80 GHz, which is the frequency of interest, it has a side length of 156 μm (~$0.08\lambda_g$). Compared to the standard full-mode SIW cavity (side length ~λ_g), a 92% reduction in size with respect to length and a 99.3% reduction in size with respect to

TABLE 3. 3 Quality Factor of the Cavities at 80 GHz

Type	Normalized Size (Area)	Q_u
Folded Ridged QMSIW	1	11.1
Shielded Folded Ridged QMSIW	1.21	11.19
Slot-loaded Shielded Folded Ridged QMSIW	0.49	11

area is realized by the proposed cavity. Comparison of normalized size and $Q_U$is shown in Table 3. 3. The Q_U is extracted by the eigenmode simulator of ANSYS High-Frequency Structure Simulator (HFSS).

To further reduce the size of the resonator, two inductive slots are etched on the top metal layer of the shielded folded ridged QMSIW resonator as shown in Fig. 3.8. With these two slots, additional inductance is introduced to the resonator so that the resonance frequency drops to the lower band. The effect of proposed inductance loaded slots can be modeled as an extension of the width of the basic QMSIW cavity (W). The following equation (3.13) is the modified equation for calculating the resonance frequency of the proposed slot-loaded folded ridged QMSIW cavity.

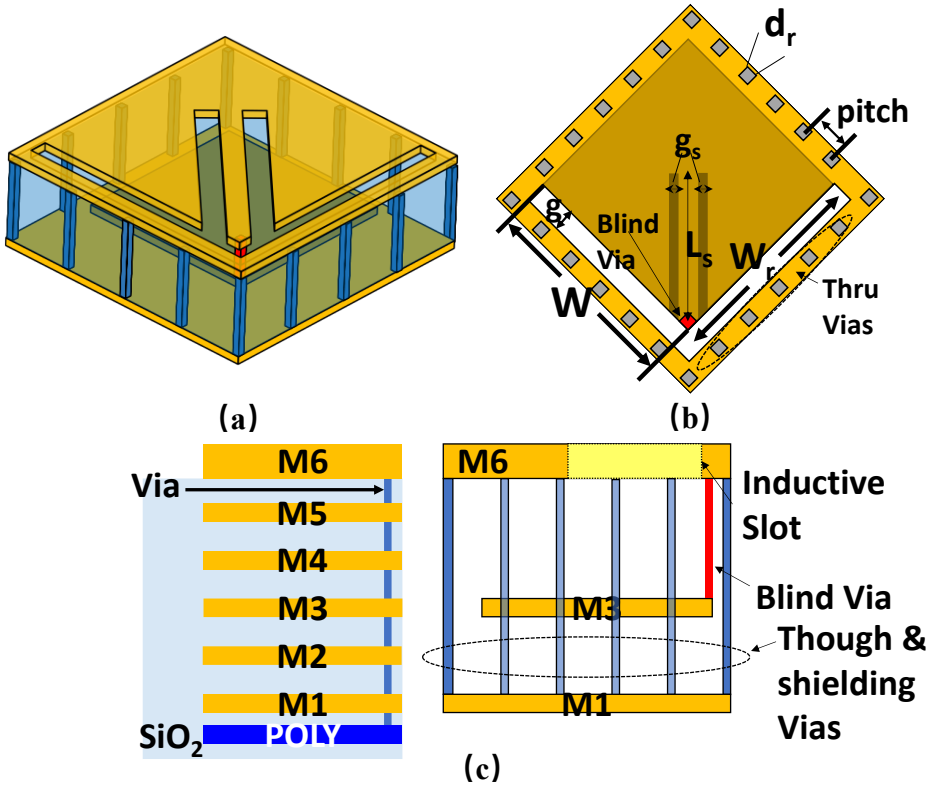


Fig. 3. 8 Slot-loaded shielded folded ridged QMSIW. (a) 3D layout. (b) Top view and dimensions. (c) Cross-section view of the proposed resonator and structure of levels of metal in 1P6M CMOS technology.

$$-\cot\left(\frac{2\pi}{\lambda_c}(W+2*Ls)\right)+\frac{B}{Y_{01}}+\frac{Y_{02}}{Y_{01}}\tan\left(\frac{2\pi}{\lambda_c}W_r\right)=0 \qquad (3.13)$$

where L_s is the length of the inductance slots.

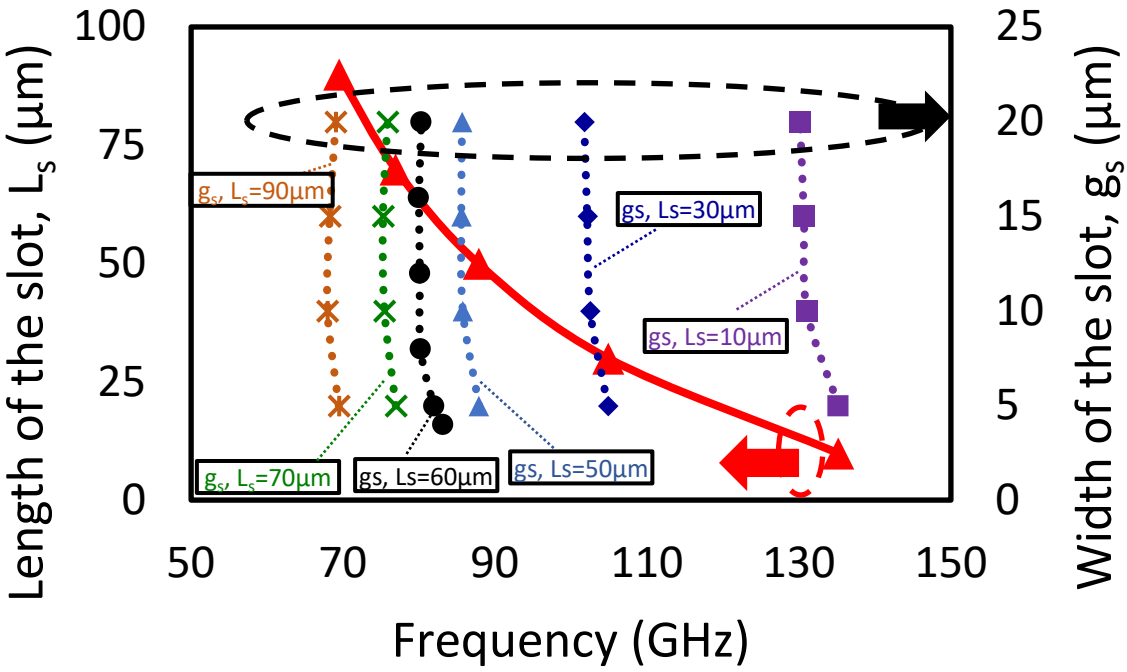


Fig. 3. 9 The resonance frequency variation by changing the length (L_s) and the width (g_s) of the slot with W = 88.4 μm, W_r = 80 μm, d_r = 3 μm, pitch = 23 μm, g = 5 μm.

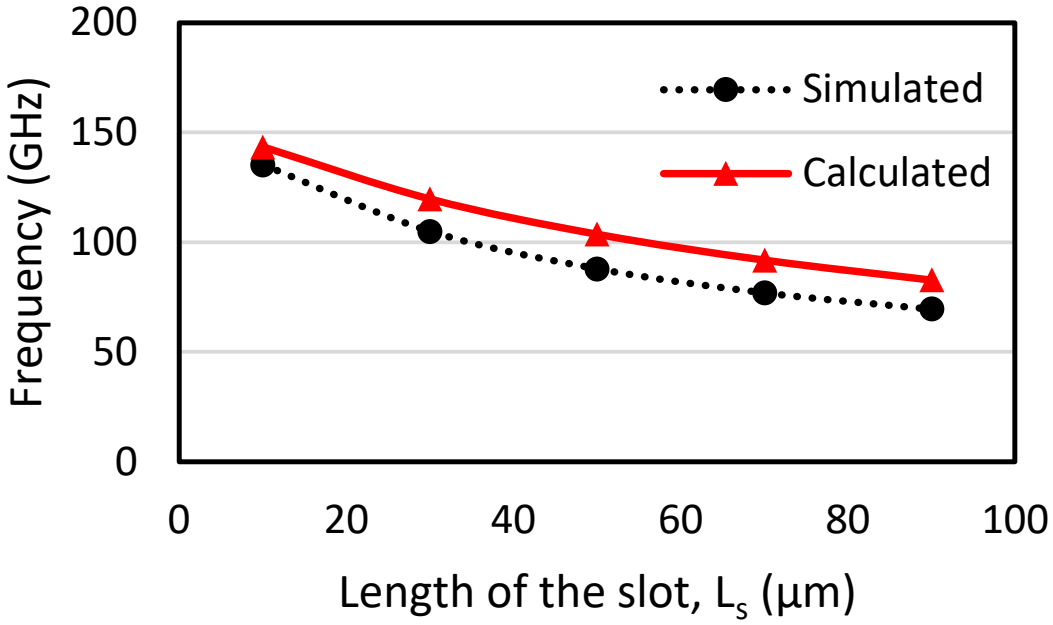


Fig. 3. 10 Comparison of simulation result and Theoretical calculation

Fig. 3.10 compares the simulated and calculated result of the resonance frequency. The error between simulation and calculation is around 10%. Fig. 3.9 shows the frequency variation of the slot-loaded shielded folded ridged QMSIW resonator while changing the length (L_s) and the width (g_s) of the slots. They are plotted by the solid line and dot lines respectively. Different from the significant change of the resonance frequency while changing L_s, changing g_s has almost no effect on the resonance frequency. By adding these two slots, miniaturization of 51% compared with folded ridged QMSIW cavity resonator and 60% comparing with shielded folded ridged QMSIW cavity resonator is realized while Q_U is maintained. These can be interpreted from Table 3.3.

3.2.2 W band 0.01 mm^2 Cavity Resonator Employing Slot-loaded Shielded Folded Ridged Quarter-Mode in CMOS Technology

In this section, the one-port slot-loaded shielded folded ridged QMSIW cavity resonator is converted to a two-port cavity resonator for the future design of a bandpass filter (BPF) and oscillators [29],[32] in W band applications. The proposed two-port cavity resonator is implemented in 1P6M CMOS technology, fabricated and measured.

3.2.2.1 Filter Design Using the Slot-loaded Shielded Folded Ridged QMSIW Resonator

The proposed slot-loaded shielded folded ridged QMSIW resonator is implemented to design a BPF in this section. The 3D layout and the top view of the proposed resonator are shown in Fig. 3.11 (a) and Fig. 3.11(b), respectively. Ports connected to source and load are coupled to slot-loaded shielded folded ridged QMSIW resonator directly. One of the ports is best positioned on the Metal 6 layer with the maximum electric field. Another port is put in the same layer (Metal 3) of the ridge. As the total size of the cavity is tiny and the field distributes evenly on the ridge, this port can be connected wherever to the ridge without changing the characteristic of the filter. For measurement convenience, we choose to put the second port in the opposite, connected to the

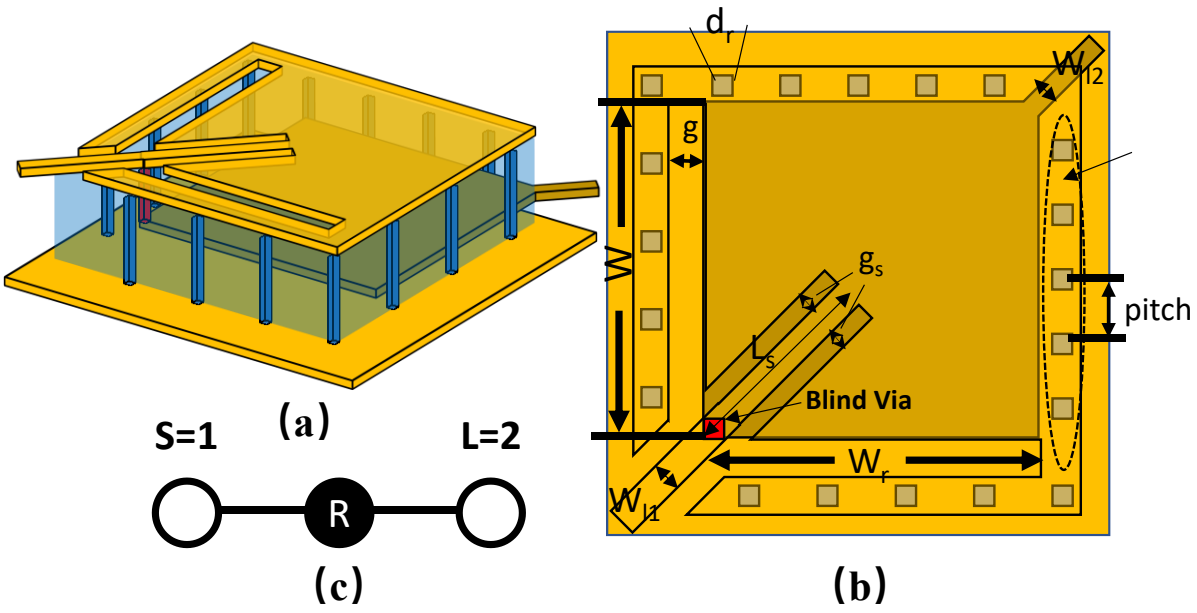


Fig. 3. 11 Proposed BPF using slot-loaded shielded folded ridged QMSIW resonator. (a) 3D layout. (b) Top view and dimensions. (c) Circuit topology.

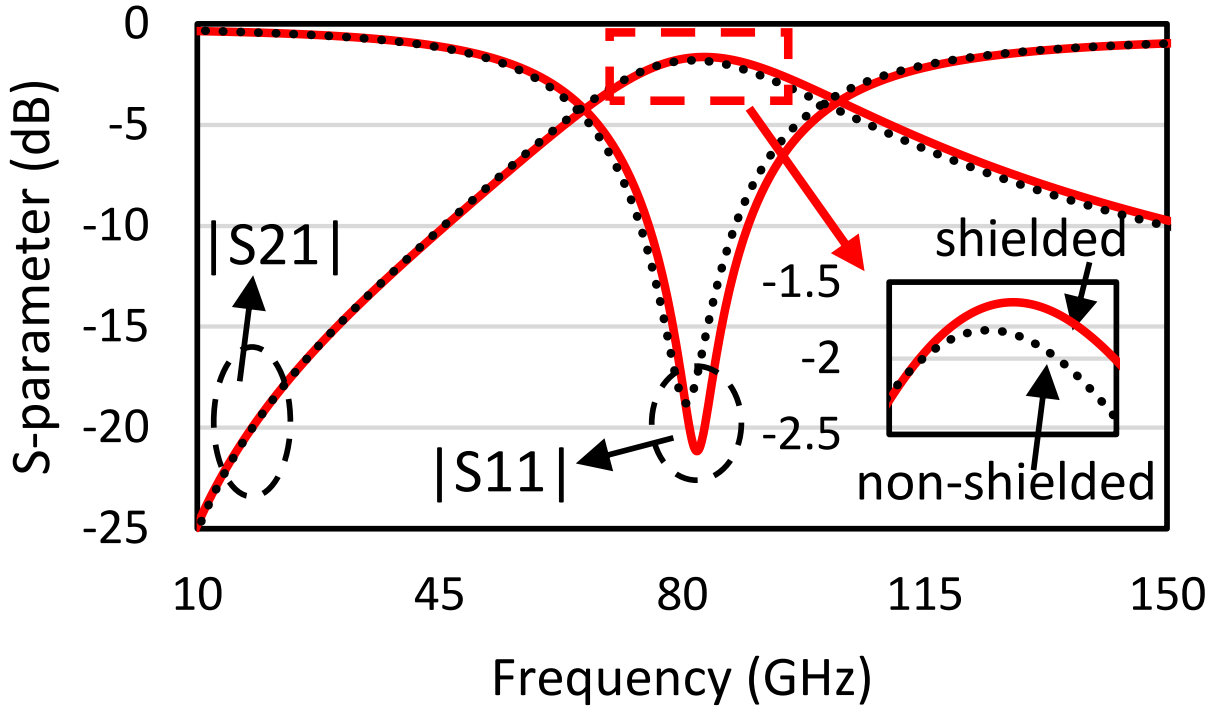


Fig. 3. 12 Comparison of simulated scattering parameters of the proposed BPF using slot-loaded folded ridged QMSIW resonator with and without shielding structure.

TABLE 3. 4 Design Parameters of the BPF Using Slot-loaded Shielded Folded Ridged QMSIW Resonator

Parameters	W	W_r	W_{l1}	W_{l2}	d_r	pitch	g	g_s	L_s
Dimension (μm)	88.4	77	5	6	3	23	5	5	60

furthest corner from the blind via. The circuit topology is shown in Fig. 3.11(c). By optimizing the width of each port (W_{l1}, W_{l2}), the width of vias, and the distance between vias, the input impedance is designed to equal 50 Ω. Table 3.4 depicts the optimized dimensions of the proposed filter.

The BPF using slot-loaded shielded folded ridged QMSIW resonator is built and simulated in HFSS. The simulation result is shown in Fig. 3.12 by red lines. With a 99 μm × 99 μm ($0.054\lambda_g \times 0.054\lambda_g$) compact size, a low insertion loss (IL, $|S_{21}|$) of 1.66 dB is realized at 83 GHz by the proposed BPF. The simulated fractional bandwidth (FBW) is 50.7%. This filter is designed to illustrate the future application of SIW cavity in CMOS technology, the transmission zeros which can control the FBW were not considered in this design. In addition, the performance of the proposed BPF when extra transmission lines are put close is also investigated. Benefit from the

shielding structure, no effect of the extra transmission lines is observed. However, if the shielding structure is removed, both IL and return loss will deteriorate. The simulation result (black dotted lines) of the BPF without shielding structure is compared in Fig. 3.12.

3.2.2.2 Fabrication and Measurement

The proposed mm-wave resonator was implemented in 1P6M CMOS technology, and its micrograph is shown in Fig. 3.13 (a). The core size of the fabricated resonator is only 0.0098 mm^2. Compared to the standard full-mode SIW resonator (1875 µm × 1875 µm, $\lambda_g \times \lambda_g$), a miniaturization of 99.68% is achieved. Even compared to the resonator by the folded ridged QMSIW technology (the reported most effective miniaturization method), which is 145.6 µm × 145.6 µm (0.021 mm^2) as shown in Fig. 3.6, a miniaturization of 51 % is realized.

The measurement environment consisting of a Keysight N5227B PNA microwave network analyzer and two Keysight N5293AX03 110 GHz frequency extenders is shown in Fig. 3.13(b). This measurement environment supports a measured frequency range from 900 Hz to 110 GHz. Fig. 3.14 shows the measurement result of the proposed resonator using a slot-loaded shielded folded ridged QMSIW resonator (red solid lines). The measured IL is 2.26 dB at 84.4 GHz. The degradation of the IL is considered caused by fabrication tolerance and measurement errors. Due to the upper-frequency limitations of the measurement environment, the measurement results beyond 110 GHz could not be shown. A performance comparison with the recently reported W band BPFs is given in Table 3.5, where the proposed resonator is more 50% compact than the BPF presented for 77 GHz [63]. The IL is also the lowest among the CMOS BPFs proposed so far for millimeter wave applications. However, the FBW is a bit higher which can be controlled by creating transmission zeros in the stopband.

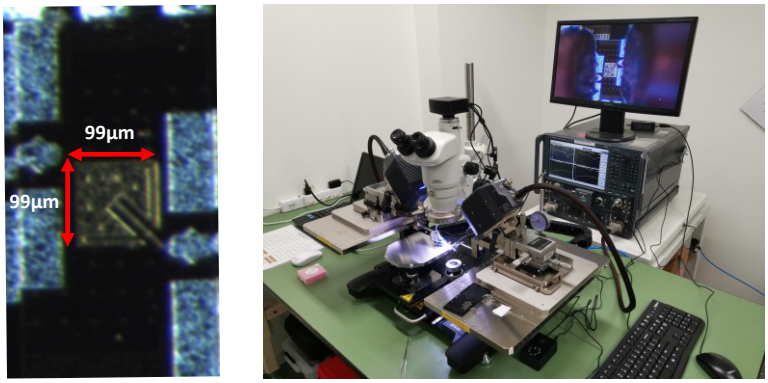


Fig. 3. 13 (a) Die photo of the proposed BPF using slot-loaded shielded folded ridged QMSIW resonator. (b) Measurement environment.

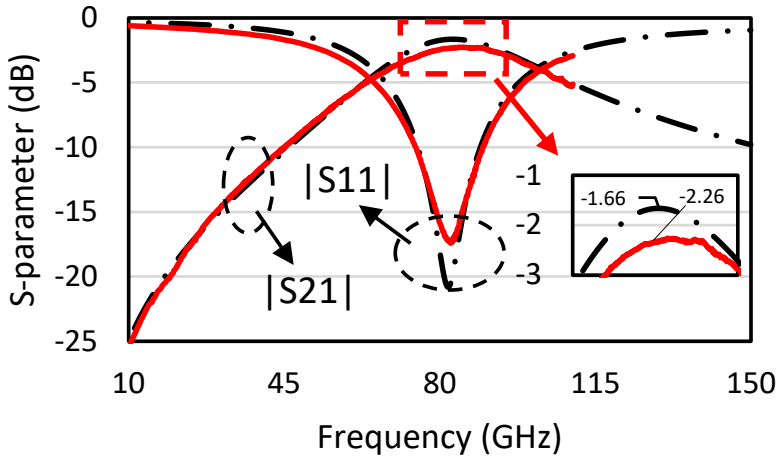


Fig. 3. 14 Comparison of scattering parameter between measurement result and simulation.

TABLE 3. 5 Performance Comparison of the BPFs in CMOS Technology

Ref.	Process	Shielded Structure	Freq. (GHz)	FBW %	IL (dB)	Area (mm^2)
This work	CMOS	Yes	83	50.7	2.26	0.0098
[61] 2008		No	70	25.7	3.6	0.4355
[62] 2008		No	60	18.8	4.9	0.504
[63] 2014		No	77	27	2.9	0.02
[20] 2016		No	60	21	2.5	0.15
[21] 2016		No	59	26.3	2.85	0.096
[22] 2017		No	59.5	21.7	3.3	0.054
[23] 2018		No	59	23.7	3.2	0.0165
[64]2018	IPD GaAs	No	60	56.1	1.2	0.232
[65]2019	GaAs	Yes	93	3.4	4.3	9.24
[66]2020	micro fabrication	Yes	88.7	6.1	2/3.7	>10.21/ >20.93

3.2.3 A W band Compact Substrate Integrated Waveguide Bandpass Filter With Defected Ground Structure in CMOS Technology

In CMOS technology, because of the stringent requirements for size, metal density, and design rules, miniaturization and fabrication of the SIW cavity become very challenging. Until now, SIW cavities still have not been exploited well in commercial CMOS technology [58]-[60]. Additionally, because of the limited metal thickness and distance between each metal layer of CMOS technology, conventional coupling methods of SIW cavities become invalid for on-chip BPF design.

In this section, a novel coupling method of SIW cavities using a defected ground structure (DGS) is proposed to build an on-chip BPF (BPF can be seen as a resonator with two ports). The designed BPF is implemented in 1P6M CMOS technology with a compact size. In addition, the effect of the design rules of CMOS technology is also investigated. The proposed BPF is finally fabricated and measured. Electromagnetic (EM) and circuit simulations in this work are done using High-Frequency Structure Simulator (HFSS) and Keysight Advanced Design System (ADS), respectively.

3.2.3.1 Conventional Coupling Coefficient of CMOS SIW resonators

Normally, a SIW-based BPF can be realized by coupling two SIW cavities using an iris window or coupling gap [56],[67], which corresponds to magnetic coupling or electric coupling. However, both of these two methods become unavailable when designing the BPF in CMOS technology.

Fig. 3.15(a) shows the 3D layout and the top view of a folded ridged QMSIW cavity. This type of cavity is first proposed in [56], and its folded ridge has an outstanding performance on SIW based components' miniaturization. However, the resulting coupling between two SIW cavities may be lower when using the ridge. In the PCB process, the height of the substrate is in the order of micrometers. So, the in-between SIW cavities coupling is not affected significantly. On the contrary, in CMOS, the metal layers are placed within a SiO_2 substrate with a height of a few micrometers, typically less than 10 μm.

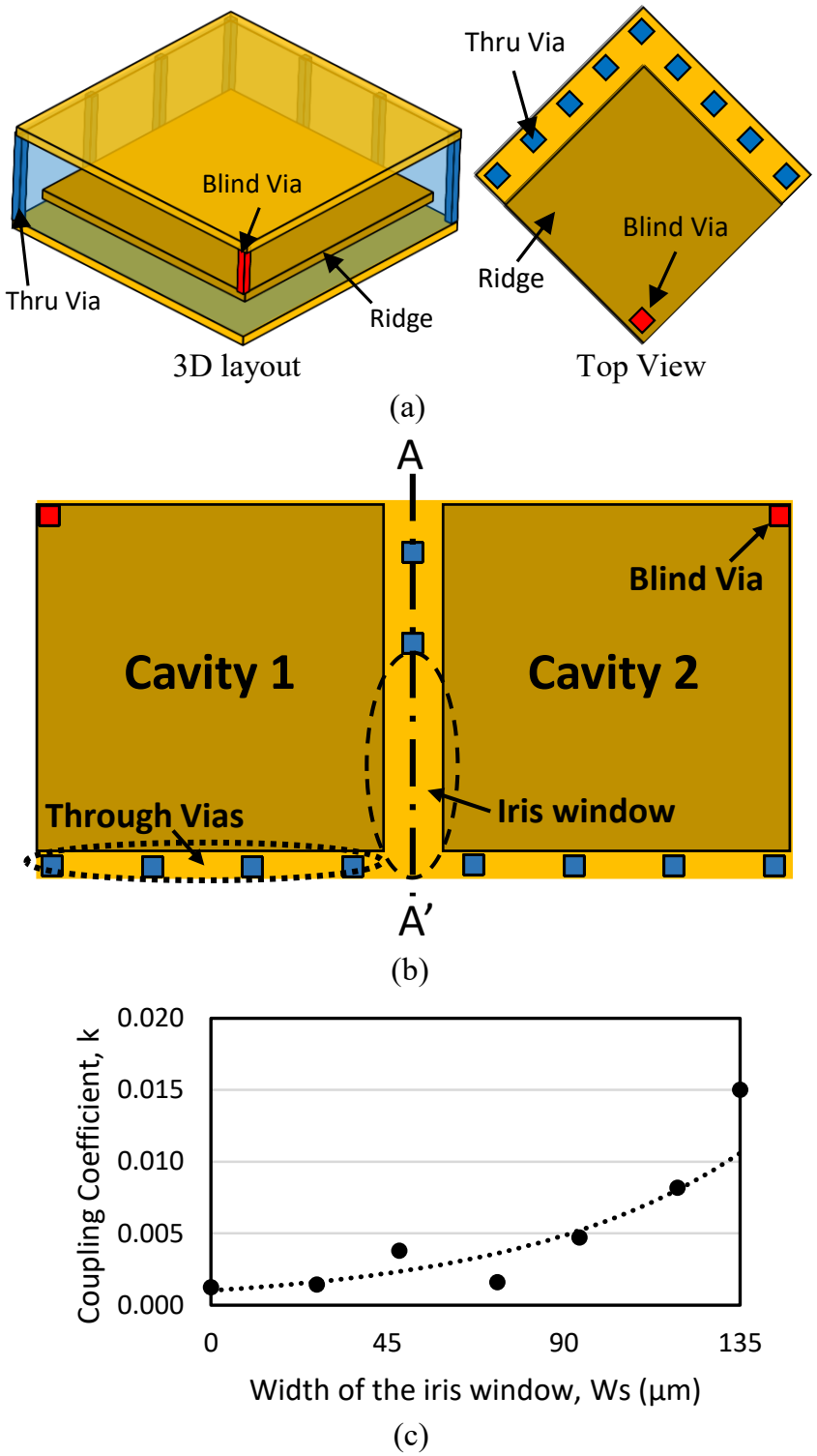


Fig. 3. 15 Folded ridged QMSIW cavity. (a) 3D layout and top view of the folded ridged QMSIW cavity. (b) Conventional coupling method with an iris window. (c) Extracted coupling coefficient versus width of the iris window.

Fig. 3.15(b) shows the circuit layout of a BPF in CMOS process, which is realized by coupling two folded ridged QMSIW cavities through an iris window. Because of the above-explained dimensions, the energy is almost bounded under the ridge of each cavity. This leads to a big decline of the coupling coefficient, which is shown in Fig. 3.15(c), and it results in a low level of insertion loss (IL, |S21|). The coupling coefficient is calculated by (3.14) [68],

$$k = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} \tag{3.14}$$

where f_e and f_m the even- and odd-mode resonant frequencies, respectively, extracted by eigenmode solver of HFSS.

3.2.3.2 Proposed W band Filter Using the Slot Loaded Shielded Folded Ridged QMSIW Resonator with DGS

In order to solve the above problem, we coupled two SIW cavities directly by a series inductive wire to enable control over the coupling coefficient and the miniaturization of the SIW cavity using a folded ridge at the same time.

Fig. 3. 16(a) shows the top view of the proposed two-pole BPF designed using the slot-loaded

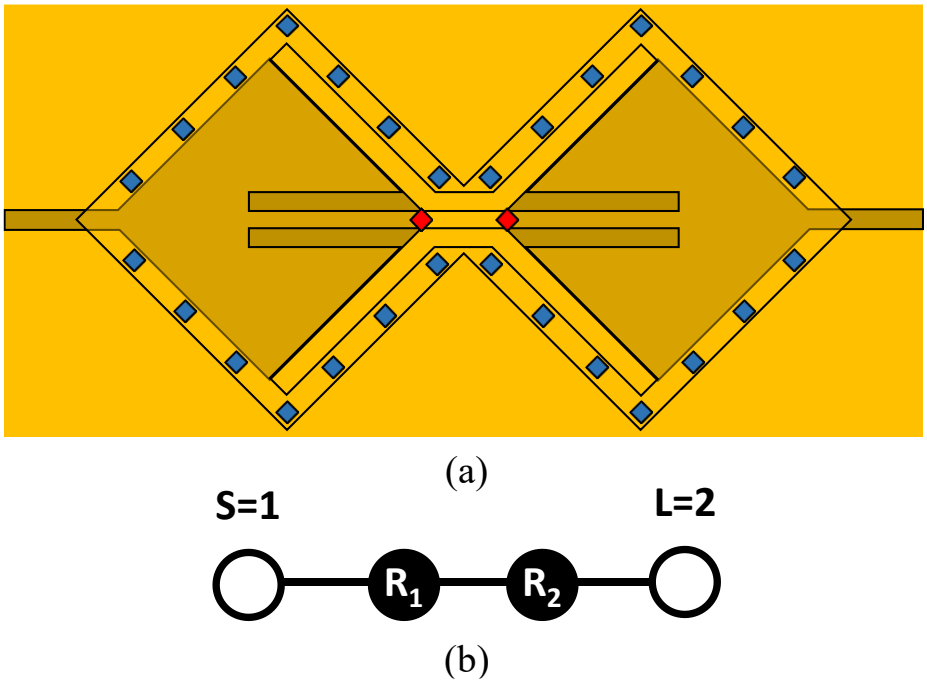


Fig. 3. 16 Basic BPF using two slot-loaded shielded folded ridged QMSIW resonators. (a) Top view. (b) Equivalent topology

folded ridged QMSIW cavity resonator in 1P6M CMOS technology, and Fig. 3.16(b) shows its equivalent topology. The slot-loaded folded ridged QMSIW cavity resonator is realized by etching two slots on the top metal layer of the conventional folded ridged QMSIW cavity to form a series inductive wire. This extra inductive load decreases the resonance frequency and realizes the miniaturization of the cavity, eventually. The simulated scattering (S-) parameters of the basic BPF are shown in Fig. 3.17. Because of the strong coupling by the inductive wire, ripple appears in the passband, and BPF also suffers from big return loss within the passband. To fix this problem, we propose a defected ground structure to control the coupling and suppress the unwanted ripple as shown in Fig. 3.18.

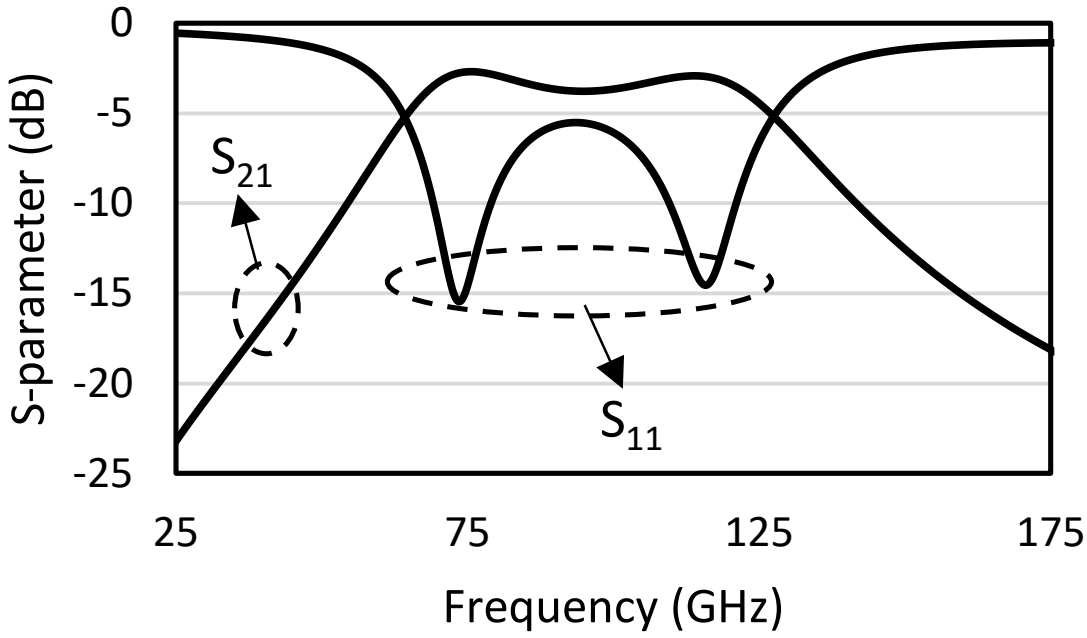


Fig. 3. 17 Simulated scattering parameter of basic BPF using two slot-loaded shielded folded ridged QMSIW resonators.

Fig. 3.19(a) shows an equivalent circuit of the BPF with DGS, which is extracted using the same method with [69]. A DGS is usually used in mm-wave filter design, and an LC tank can be used as its equivalent circuit. In this design, due to the big ratio of W_d to L_d, the capacitance part of DGS can be ignored, which means the proposed DGS works as a series inductor here. Two slot-loaded folded ridged QMSIW resonators are coupled by the L_m and L_b, where L_m is the total inductance of the wire and DGS, and L_b is the tank inductance of the proposed cavity resonator. C_1

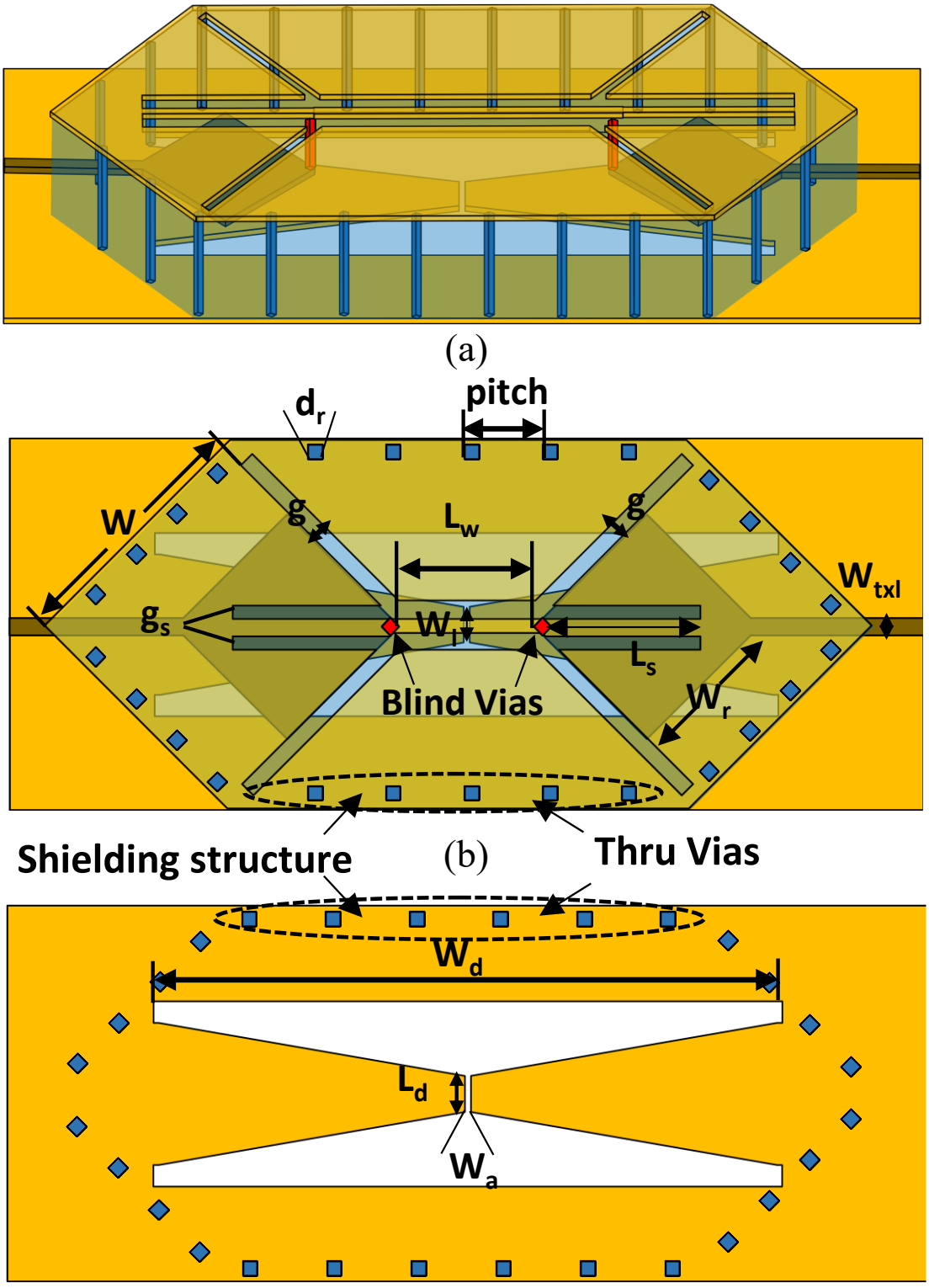


Fig. 3. 18 Proposed W-band Compact BPF with DGS. (a) 3D model. (b) Top view and dimensions. (c) Decoupling DGS and its dimensions.

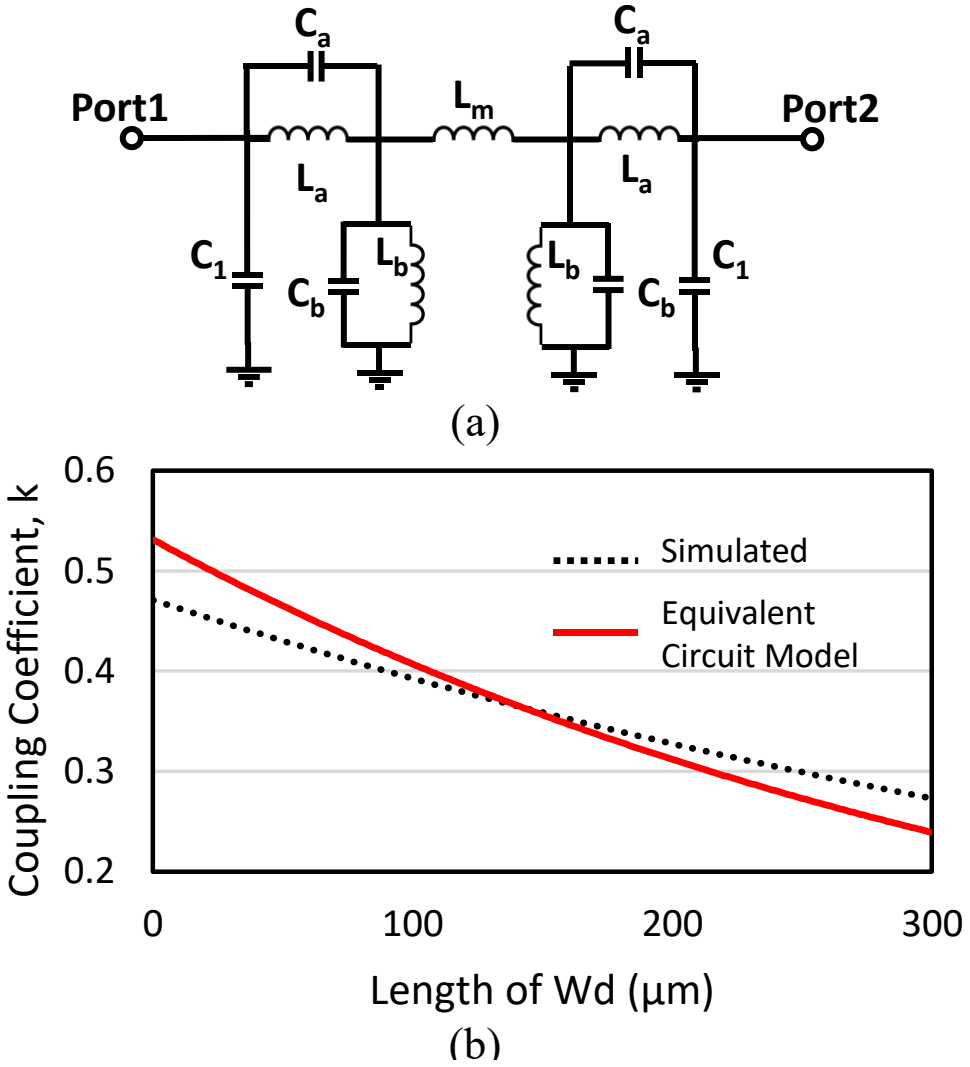


Fig. 3. 19 (a) Equivalent circuit of the proposed BPF (C_1 = 96.8 fF, C_a = 39.4 fF, C_b = 98.1 fF, L_a = 3.7 pH, L_b = 22.2 pH). (b) Coupling coefficient versus length of the DGS (W_d).

is the capacitance between the ridge and the ground, Ca is the capacitance between the ridge and top metal layer, C_b is the capacitance of the QMSIW cavity, and L_a is the inductance of the ridge.

Fig. 3.20(a) is the enclosed part of the equivalent circuit of Fig. 3.19(a). With a T-π transformation, we can get its equivalent circuit as shown in Fig. 3.20(c), where

$$L_1 = \frac{L_m L_b}{2L_b + L_m} \tag{3.15}$$

$$L_2 = \frac{(L_b)^2}{2L_b + L_m} \tag{3.16}$$

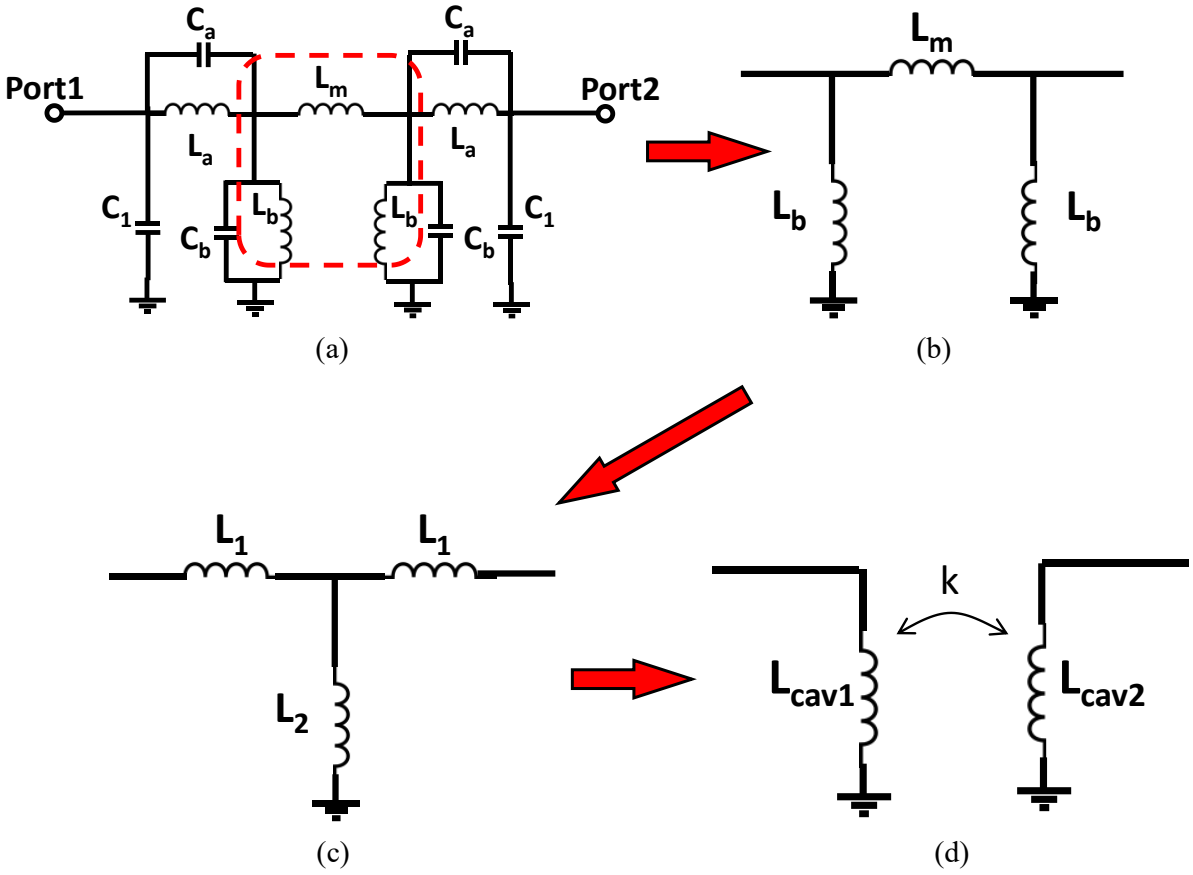


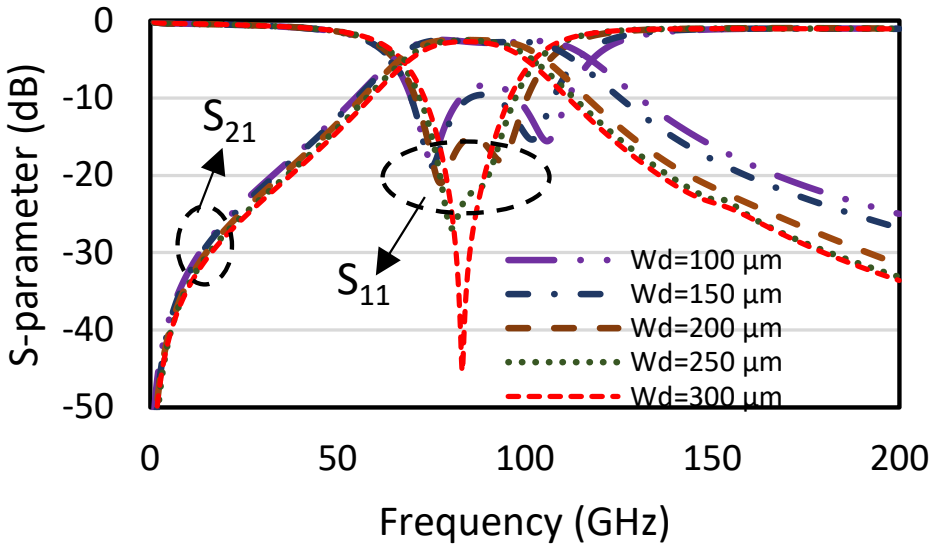
Fig. 3. 20 (a) Equivalent circuit in Fig. 4. 13. (b) Coupling is realized by L_m and L_b. (c) After the T-π transformation. (d) The T-network is transformed two coupled inductors with a coupling coefficient k.

Then, this T-circuit can be seen as an equivalent circuit of two coupled inductors with a coupling coefficient k as shown in Fig. 3.20(d). L_{cav1} and L_{cav2} are the inductors in the effective coupled cavities. The value of coupled inductors and their coupling coefficient can be extracted using the following equations.

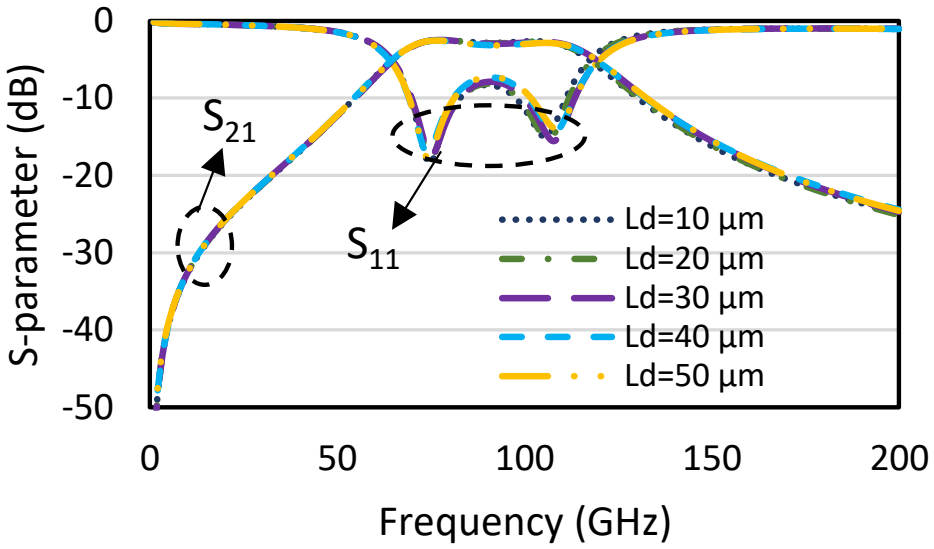
$$L_{cav1} = L_{cav2} = L_1 + L_2 \tag{3.17}$$

$$k = \frac{L_2}{\sqrt{L_{cav1}L_{cav2}}} = \frac{L_2}{L_1 + L_2} \tag{3.18}$$

Finally, by substituting the value of L_1 and L_2, the relationship between coupling coefficient k, L_b and L_m can be calculated as shown in (3.19). Using this equation, the coupling coefficient can be extracted from the equivalent circuit.



(a)



(b)

Fig. 3. 21 Simulated scattering parameter while optimizing the dimensions of DGS in Metal 1. (a) Changing W_d. (b) Change L_d.

$$k = \frac{(L_b)^2}{L_m L_b + (L_b)^2} \tag{3.19}$$

According to this equivalent circuit, it's easy to find that the coupling coefficient can be reduced by increasing L_m. The calculated result of the coupling coefficient using an equivalent

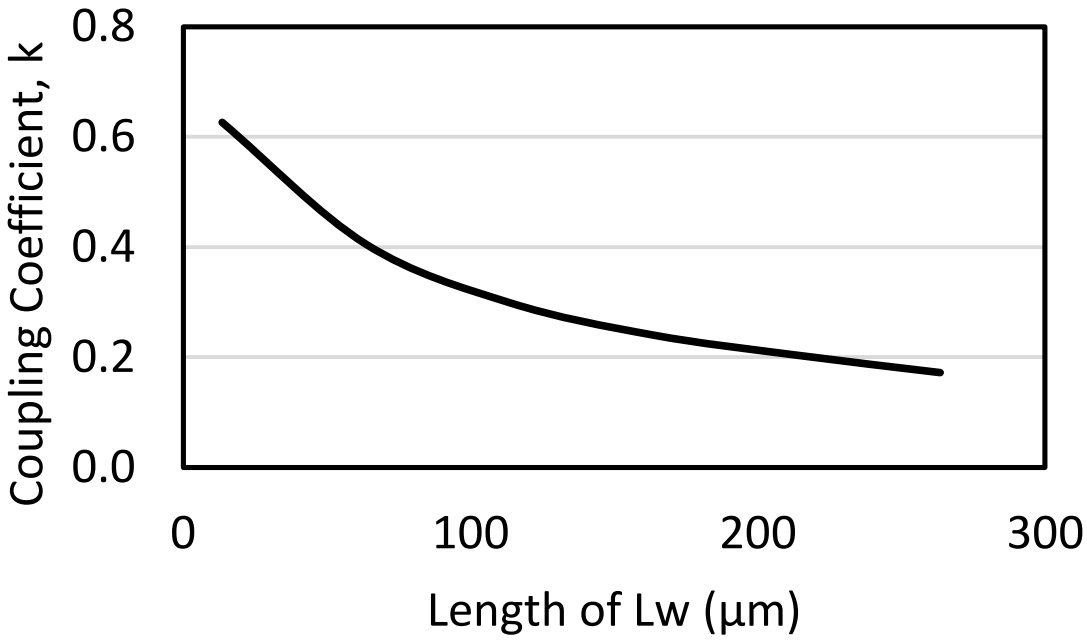


Fig. 3. 22 Coupling coefficient versus length of the inductive wire (L_m).

circuit is plotted in Fig. 3.19(b). Based on [35], it's known that the inductance of DGS is related to the length of W_d. Therefore, it is possible to conclude that the over coupling can be fixed by optimizing W_d to improve the performance of the BPF.

Fig. 3.19(b) shows the HFSS simulated relationship between the coupling coefficient and W_d. As W_d increases, the coupling coefficient reduces. This result also shows a good agreement with that calculated by an equivalent circuit. The performance of the proposed BPF while changing W_d is shown in Fig. 3.21(a). The simulated S-parameters while changing the length of the slot of DGS, L_d, are shown in Fig. 3.21(b). Because this slot affects the capacitance of the DGS rather than its inductance, it has a negligible effect on the performance of the proposed BPF, which proves the above discussion.

It should be noted that increasing the length (L_w in Fig. 3.18) of this inductive wire increases its inductance and weakens the coupling between two cavities (see Fig. 3.22). However, without the DGS, only using a wire to reduce the coupling coefficient to the target is very costive in the size. This contradicts our goal of miniaturization. The dimensions after optimization of the proposed BPF are shown in Table 3.6 and the corresponding simulation result is shown in Fig. 3.

TABLE 3. 6 Optimized Design Parameters of the BPF Using Slot-loaded Shielded Folded Ridged QMSIW Resonator

Parameters	W	W_r	W_l	W_{txl}	Wd	Wa	d_r
Dimension (μm)	88	63	93.5	6	235	3	3
Parameters	pitch	g	g_s	L_s	Lw	Ld	
Dimension (μm)	23	5	10	60	105.8	15	

23(b) (solid red lines). The proposed BPF is realized with a 405 μm × 185 μm ($0.22\boldsymbol{\lambda_g} \times 0.1\ \boldsymbol{\lambda_g}$) compact size and a low insertion loss (IL, $|S_{21}|$) of 2.7 dB at 84.2 GHz. Also, a wide simulated fractional bandwidth (FBW) of 40.7% is achieved. Besides the above characteristics, a shielding structure realized by though-vias is implemented enclosing the proposed BPF to prevent leakage and disruption from other adjacent components [70].

3.2.3.3 Layout Considerations of the Proposed BPF in 1P6M CMOS Technology

Different from fabrication in PCB technology, CMOS technology has a lot of special design rules, such as dummy metal, slots in wide metal, and specific size of vias. The effect of these design rules is investigated and discussed in this section.

- **Wide metal rule**: it's prescribed that every wide metal should have slots on it. As shown in Fig. 3.23(a), in the layout of the proposed BPF, 5 μm × 5 μm slots are chopped on the ground layer, folded ridge, and top metal layer every 35 μm.
- **Via size**: the used CMOS process has a pre-defined via size, which is not appropriate for our design. To realize a big via with the optimized size of 3 μm × 3 μm, 6×6 vias arrays are used in the layout. Fig. 3.23(b) shows the comparison result between before and after clearing these design rules. Both insertion loss and center frequency dropped, but return loss is still bigger than 25 dB while center frequency's variation is smaller than 4.5% (84.2 GHz to 88 GHz).
- **Dummy metal filling rule**: Each metal layer should cover a predefined ratio of the chip. Dummy metals are filled to satisfy this rule without affecting the original performance. Fig.

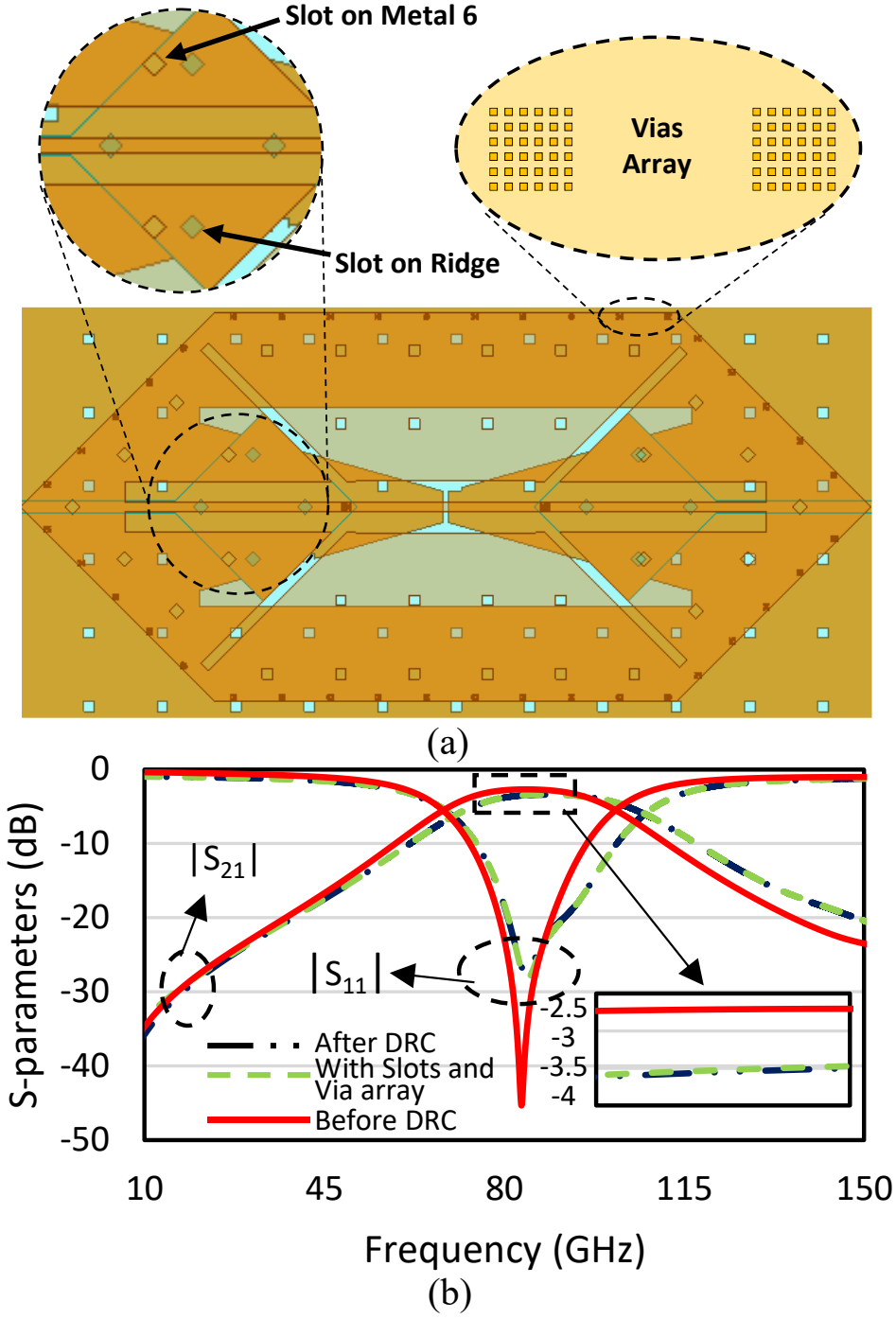


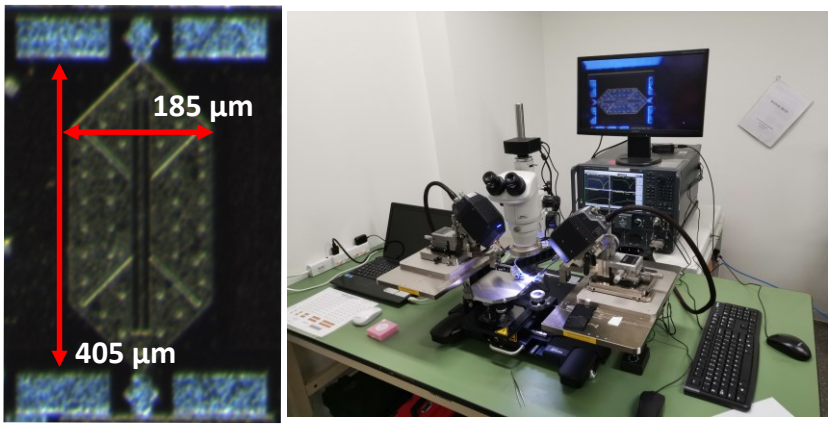
Fig. 3. 23 (a) Slots and via array implemented to clear the design rules of CMOS technology. (b) Effect of applying these arrangements.

3.23(b) compares the simulation result with and without the dummy metals. Benefit from the shielding structure of the proposed BPF, there is no variation of scattering parameter and the center frequency is observed even when the dummy metals are adjacent to the BPF.

3.2.3.4 Fabrication and Measurement

The proposed W band BPF was implemented in 1P6M CMOS technology, and its micrograph is shown in Fig. 3.24(a). The core size of the fabricated BPF is only 0.075 mm^2. The measurement environment consisting of a Keysight N5227B PNA microwave network analyzer and two Keysight N5293AX03 110 GHz frequency extenders are shown in Fig. 3.24(b). This measurement environment supports a measured frequency range from 900Hz to 110GHz.

Fig. 3.25 shows the measurement result of the proposed BPF using a slot-loaded shielded folded ridged QMSIW resonator. The measured insertion loss is 3.15 dB at 85.5 GHz. Due to the upper-frequency limitations of the measurement environment, the measurement results beyond 110 GHz could not be shown. The measurement results show good agreement with the simulation. A performance comparison with the recently reported wide-band BPFs is given in Table 3.7. Compared to on-chip filters in [20],[21],[64],[69], and [71]-[73], only the proposed wide-band filter is based on an integrated cavity and implements a shielding structure. While comparing with [20],[64], this filter has a more compact relative size per unit wavelength. Furthermore, compared to the filter of [71],[72] lower in-band insertion loss is realized by this work.



(a) (b)

Fig. 3. 24 (a) Die photo of the proposed BPF using slot-loaded shielded folded ridged QMSIW resonator. (b) Measurement environment.

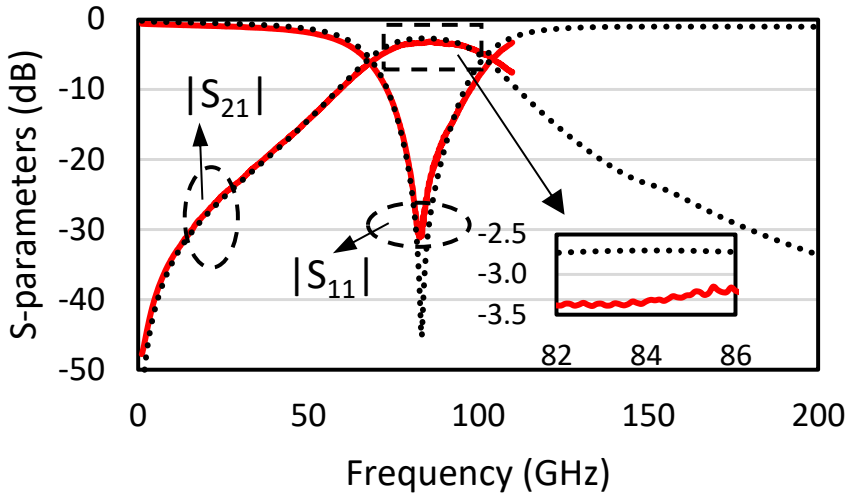


Fig. 3. 25 Comparison of measured and simulated S-parameters of the proposed BPF.

TABLE 3. 7 Performance Comparison of the BPFs in CMOS Technology

Ref.	Process	Shielding Structure	Order	Freq. (GHz)	FBW %	IL (dB)	Area (λ_g^2)
This work	CMOS	Yes	2	85	43.8	3.15	0.022
[20] 2016		No	1	60	21	2.5	0.024
[21] 2016		No	1	59	26.3	2.85	0.015
[64] 2018	IPD GaAs	No	1	60	56.1	1.2	0.078
[71] 2018	SiGe	No	1	26.5	50.9	3.8	0.005
[72] 2018		No	3	31	51	3.9	0.004
[73] 2020		No	1	18	66.7	2.9	0.002
[69] 2021	CMOS	No	1	34.5	61.2	1.6	0.002

3.2.4 A 100GHz Bandpass Filter Employing Shielded Folded Ridged Quarter-Mode SIW Resonator in CMOS Technology

In this section, a shielded folded and ridged quarter-mode SIW cavity is analysed and applied to significantly reduce the footprint of the SIW resonator. A bandpass resonator with two transmission zeros at mm-wave frequency is designed using the proposed shielded FRQMSIW resonator in the standard CMOS technology. Then, the proposed shielded FRQMSIW BPF is fabricated and verified by experiment in 1P6M CMOS technology.

3.2.4.1 Proposed shielded FRQMSIW cavity

The top view and the simulated electric field of the shielded FRQMSIW cavity are shown in Fig. 3.26. The shielded technology first encloses FRQMSIW with through-vias like standard SIW, and with etching two gaps on the top metal layer, two nearly ideal magnetic walls can be realized. If we check the simulated field in Fig. 3.26(b), it's clear that the electric field is limited inside the shielded FRQMSIW without any leakage.

To investigate the characteristics of the shielded FRQMSIW cavity, a feeding line is best positioned on the Metal 3 layer connecting to the ridge at the furthest corner from the blind via (Fig. 3.27). Placing the feeding line in Metal 3 retains the integrity of the top metal layer to prevent the

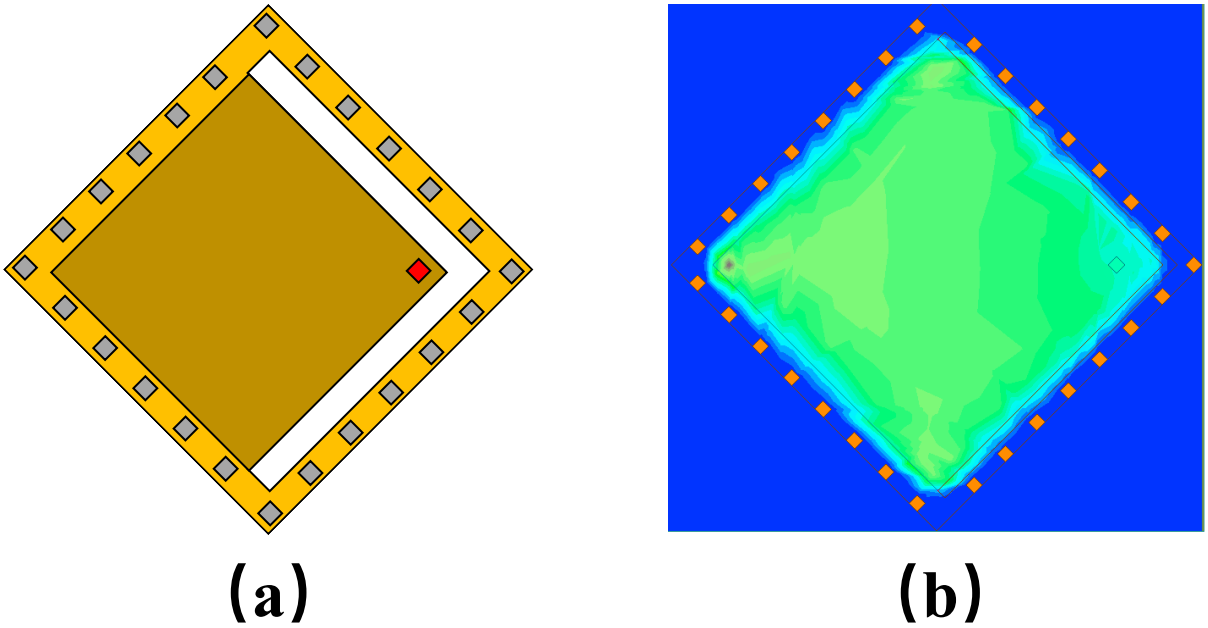


Fig. 3. 26 The shielded FRQMSIW resonator. (a) Top view. (b) Electric field distribution.

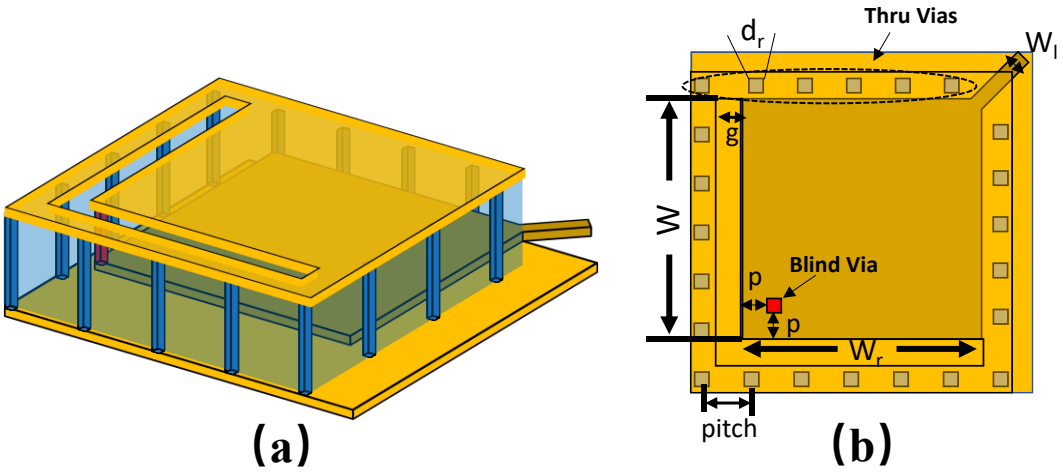


Fig. 3. 27 The shielded FRQMSIW resonator with feeding line. (a) 3D layout. (b) Top view.

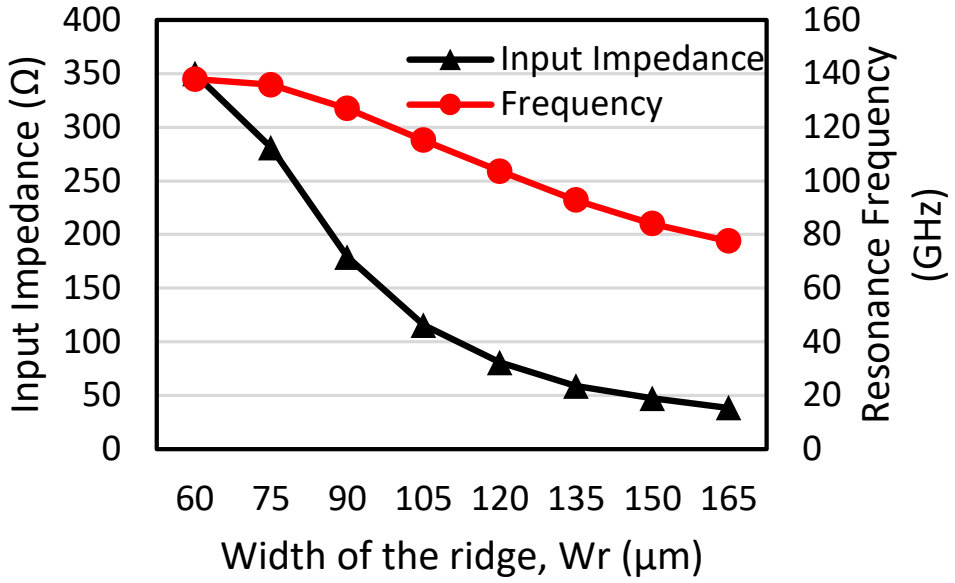


Fig. 3. 28 The resonance frequency and input impedance variation by changing the width of the ridge. Other dimensions except the width of the ridge (W_r) used for simulation are W = 165 μm, W_l = 6 μm, pitch = 23 μm, d_r = 6 μm , p = 14 μm, g = 5 μm.

disruption of the shield structure. The shielded FRQMSIW cavity is built in ANSYS High Frequency Structure Simulator (HFSS), and Fig. 3.28 shows the simulation result of the relationship between input impedance and width of the ridge. As the width of the ridge (W_r) decreases, the resonance frequency and input impedance will increase.

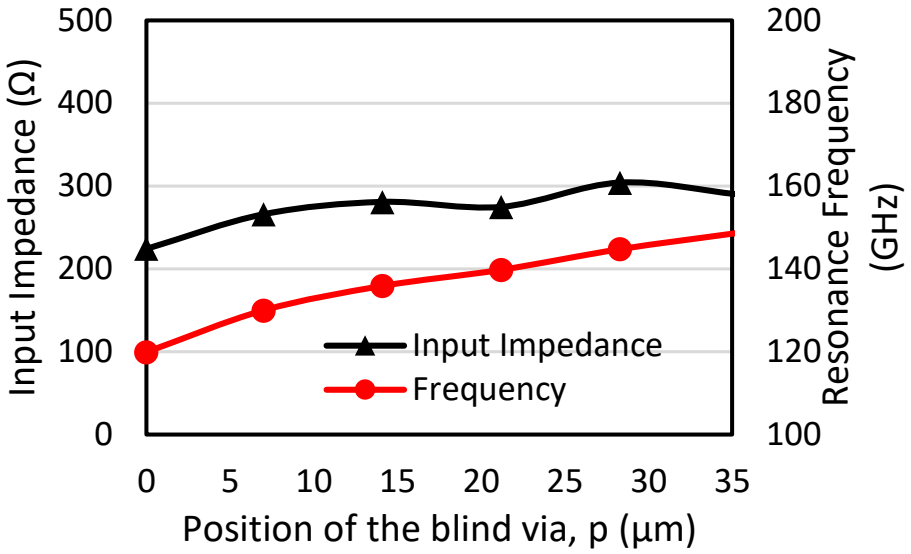


Fig. 3. 29 The resonance frequency and input impedance variation by changing the position of blind via.

Fig. 3.29 plots the resonance frequency of the shielded FRQMSIW resonator versus blind via's position p. As the blind via goes deeper along the diagonal of the ridge, the resonance frequency will become higher, while the input impedance increases slightly.

3.2.4.2 Filter Design Using the Shielded FRQMSIW

Due to the low conductivity of vias in CMOS technology, letting power go through the SIW resonator and designing a filter will decrease the power transmission ($|S_{21}|$) a lot. Therefore, we choose to couple the shielded FRQMSIW resonator (R=3 in Fig. 3.30) to the 50-Ω microstrip line in parallel, connecting both source (S=1) and load (L=2) to form the BPF. Fig. 3.30 (a) shows the design layout of the BPF and the coupling-matrix diagram respectively.

To make the power transmission as high as possible at our target resonance frequency, the impedance of the resonator in Fig. 3.27 should be large enough. To get the large enough input impedance at the target frequency, the width of the FRQMSIW (W), the position of the blind via, and the width of the ridge (W_r) are well optimized. The final dimensions of the proposed filter are depicted in Table 3.8.

The proposed filter is built and simulated by HFSS. The simulation result is shown in Fig. 3.31. At 100GHz, the shielded FRQMSIW resonator and its input impedance increases rapidly so that a

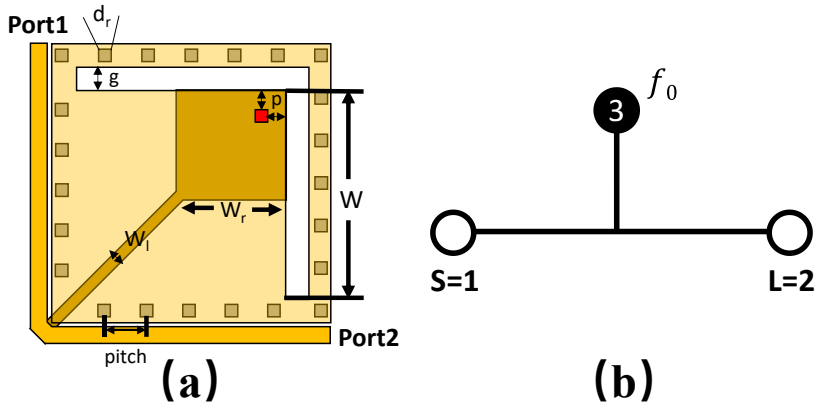


Fig. 3. 30 Proposed BPF using shielded FRQMSIW resonator and its (a) top view and (b) coupling-matrix diagram.

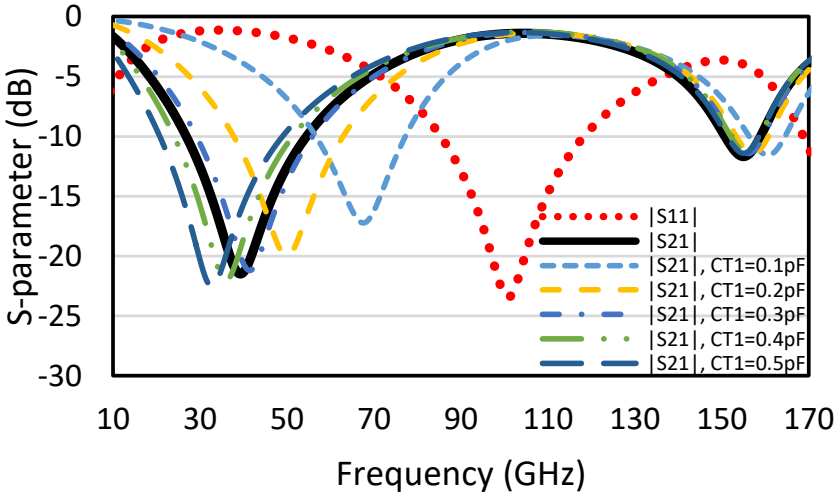


Fig. 3. 31 Simulated scattering parameters of the BPF using shielded FRQMSIW resonator.

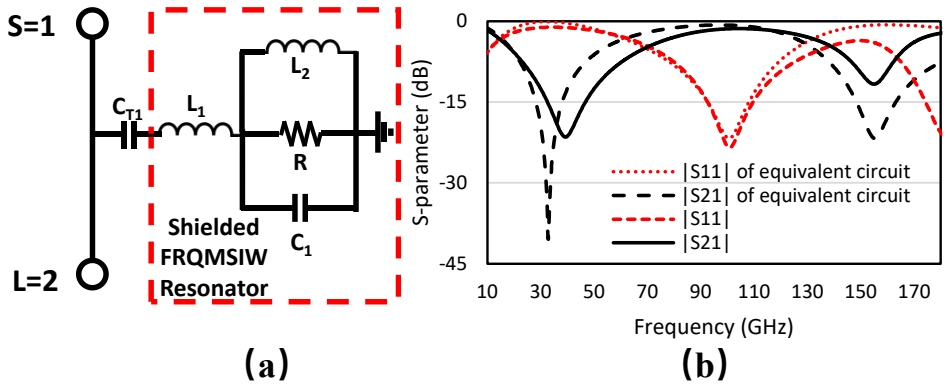


Fig. 3. 32 Equivalent circuit of the BPF using shielded FRQMSIW resonator. (b) Comparison of scattering parameters between the equivalent circuit and the original filter.

TABLE 3. 8 Design parameters of the BPF using shielded FRQMSIW resonator.

Parameters	W	W_r	W_l	d_r	pitch	p	g
Dimension (μm)	175	75	6	6	23	7	5

passing band appears. What's more, to add the transmission zeros to improve the performance of the filter, a series capacitor is introduced between the 50 Ω microstrip line and resonator. By controlling the value of this capacitor, the transmission zero at low frequency can be realized and optimized as illustrated in Fig. 3.31. The second transmission zero at the higher band is realized by the inductance of the feeding line and ridge. Changing the length of the feeding line may also change the transmission zero at the higher band, which is not implemented this time.

An equivalent circuit of the proposed BPF is given in Fig. 3.32(a) with $C_{T1} = 0.345pF$, $C_1 = 70.93fF$, $L_1 = 28.69pH$, $L_2 = 35.15pF$, $R = 279.73\Omega$, where C_{T1} is the capacitor for controlling first transmission zero, L_1 represents the inductance from the feeding line and ridge, C_1, L_2, and R together consist of the resonator. Fig. 3.32(b) plots a comparison of scattering parameters between the equivalent circuit and the original circuit, which shows good agreement.

3.2.4.3 Fabrication and Measurements

The proposed mm-wave bandpass resonator was implemented in 1P6M CMOS technology, and its micrograph is shown in Fig. 3.33. The measurement environment consists of a Keysight N5227B PNA microwave network analyzer and two Keysight N5293AX03 110 GHz frequency extenders. This measurement environment supports a measured frequency range from 900Hz to 110GHz.

The measurement result of the proposed bandpass resonator using the shielded FRQMSIW cavity is plotted in Fig. 3.34. Because a metal-insulator-metal capacitor (MIMCAP) is utilized in this design, which is not available for this high frequency, the passing band shifted to the lower band, although the shape of the filter didn't change. A modified simulation result considering the effects of parasitic parameters of MIMCAP, slots, dummy metals, and AC pads is given and compared with the original simulation result and measurement result in Fig. 3.34.

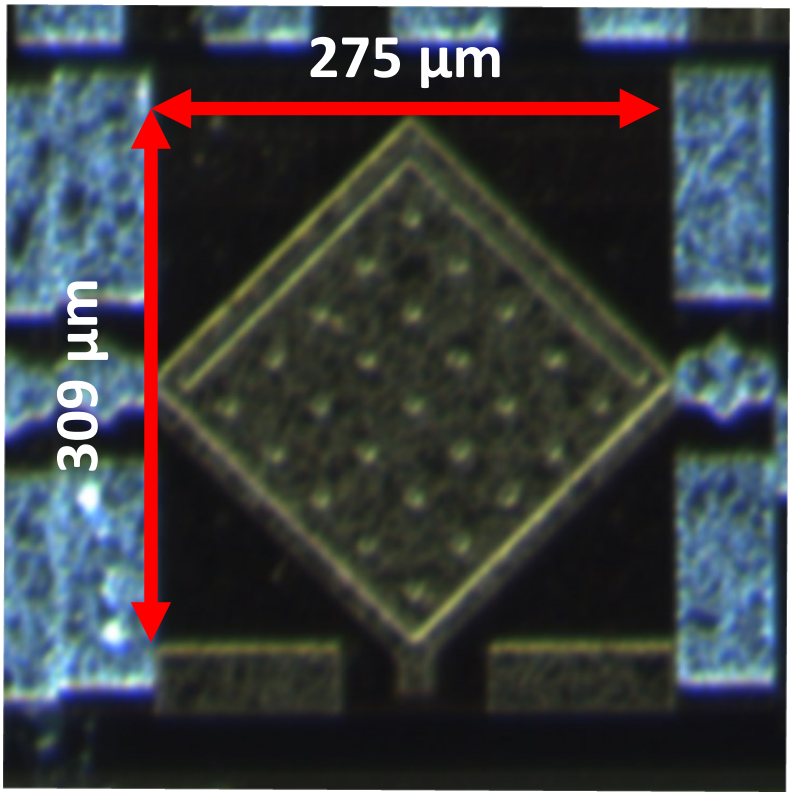


Fig. 3. 33 Die photo of the fabricated BPFs using the shielded FRQMSIW resonator.

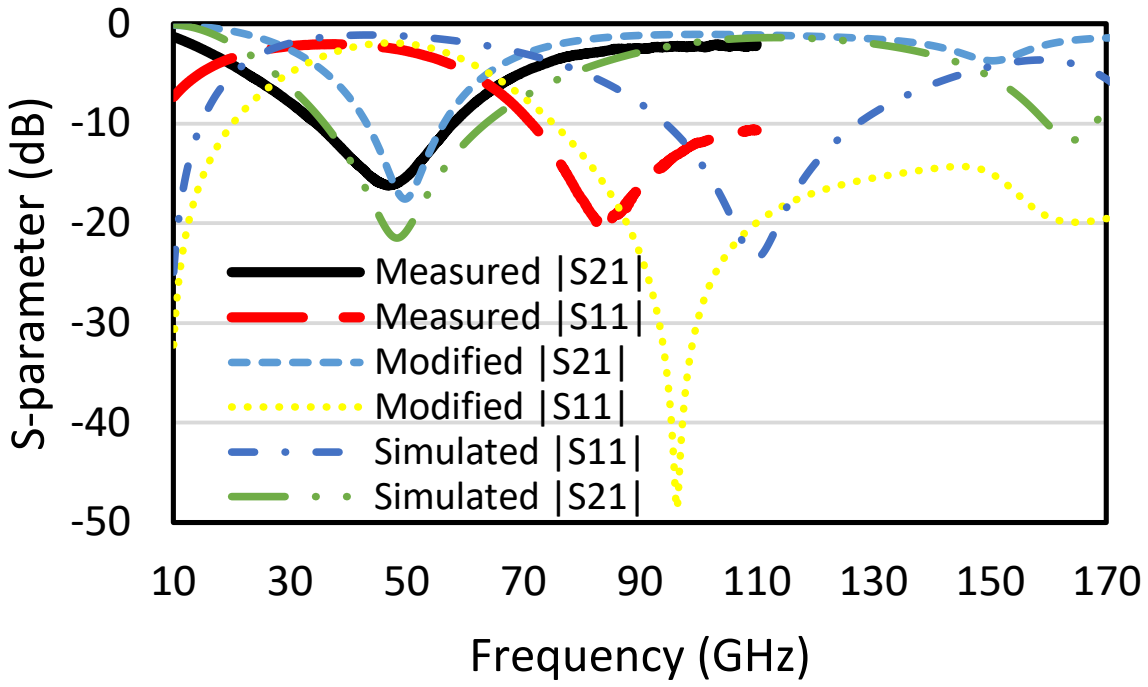


Fig. 3. 34 Measured scatting parameters of the BPF using shielded FRQMSIW resonator.

3.3 Conclusion

At the beginning of this chapter, a novel two-branches DGS resonator has been proposed and investigated for the first time to design low phase noise VCOs in 0.18-µm CMOS technology for mm-wave applications. Compared with its predecessors, the proposed DGS resonator has not only a higher Q-factor but is also effective to reduce the length of interconnects.

Then, a miniaturized slot-loaded shielded folded ridged QMSIW cavity resonator in CMOS technology is presented and investigated. The proposed slot-loaded shielded folded ridged QMSIW cavity resonator has a significant compact size. This firstly makes it practical to utilize a SIW resonator in a commercial integrated process that has stringent requirements for size and metal density like CMOS technology. Later, the one-port cavity is converted to a two-port cavity resonator. A W band two ports resonator with an extremely compact size (99 µm × 99 µm, $0.054\lambda_g \times 0.054\ \lambda_g$) is designed, implemented, and measured. The designed two ports resonator realizes a measured insertion loss (|S21|) of 2.26 dB. Then, the problem of weak coupling between two SIW-based resonators in CMOS technology is pointed out and investigated. A novel coupling method through DGS is proposed and used for designing a wideband two ports resonator. The two ports bandpass resonator realized by coupled slot-loaded shielded folded ridged QMSIW resonators is designed, implemented, and measured. The measurement result shows good agreement with the design. The active size of the proposed cavity resonator is only 405 µm × 185 µm ($0.22\lambda_g \times 0.1\ \lambda_g$), and the measured insertion loss (|S21|) is 3.15 dB with a central frequency of 85.5 GHz. Finally, to validate the feasibility of a SIW-base resonator working at a frequency beyond 100 GHz, a two ports bandpass resonator with two transmission zeros using shielded folded ridged QMSIW resonator without slot-load is implemented in 1P6M CMOS technology and measured. The active size of the proposed bandpass resonator without pads is 309µm × 275µm ($\sim 0.1\lambda_g \times \sim 0.09\ \lambda_g$), and the measured insertion loss (|S21|) is 2.06dB. The measured results show a good tendency of the simulation results, although there is a frequency shift at the resonance frequency. All of these proposed resonators and BPFs are for the future design of integrated oscillators for W band applications.

CHAPTER 4: Defected Ground Structure Resonator based VCO

In this chapter, to verify their performance, the integrated high-Q resonators proposed in the last chapter are implemented in VCO applications. This chapter discusses the design methodology of VCOs which use DGS resonators instead of the conventional LC tank. In the beginning, the two-branches resonator introduced in section 3.1 is used in the design of the 50 GHz low phase noise VCO. Then, the two-branches DGS resonator is optimized and utilized in the design of K band VCOs. In the end, an investigation of the relationship between interconnects and phase noise is implemented for improving the layout design of the VCO has been done. All of the proposed VCO designs are fabricated in 180 nm CMOS technology and measured in our laboratory.

4.1 50 GHz Low Phase Noise VCO Employing Two-Branches Defected Ground Structure Resonator in 0.18-µm CMOS Technology

Wireless communication systems based on millimeter-wave (mm-wave) bands have drawn increasing interest because of the explosive growth in demand for high-speed data transfer. As the essential component of a mm-wave wireless communication system, the voltage-controlled oscillator (VCO) dictates the performance of the whole system. To realize the modulation/demodulation functions in the V band wireless communication system, the phase-noise of a CMOS VCO should be better than -90 dBc/Hz [39]. This gives the challenge to design an on-chip VCO at V band and beyond.

Recently, many K band VCOs using defected ground structure (DGS) resonators as an alternative to the LC-tank resonator have been reported [24]-[30], [32]-[34]. Due to its higher quality (Q-) factor than the on-chip spiral inductor, the VCO using a DGS resonator exhibits better phase noise than the VCO employing a conventional LC resonator. However, the effectiveness of a DGS resonator has not been verified yet in the mm-wave and above frequency band.

In this section, the two-branches DGS resonator, which has a higher Q-factor than its predecessors [32]-[34], is employed to design a low phase noise 50 GHz VCO. The proposed DGS resonator is also effective to reduce the length of the interconnect that connects the resonators and MOS transistors. Finally, the designed VCO is fabricated in 0.18-µm CMOS technology and measured.

4.1.1 VCO Design

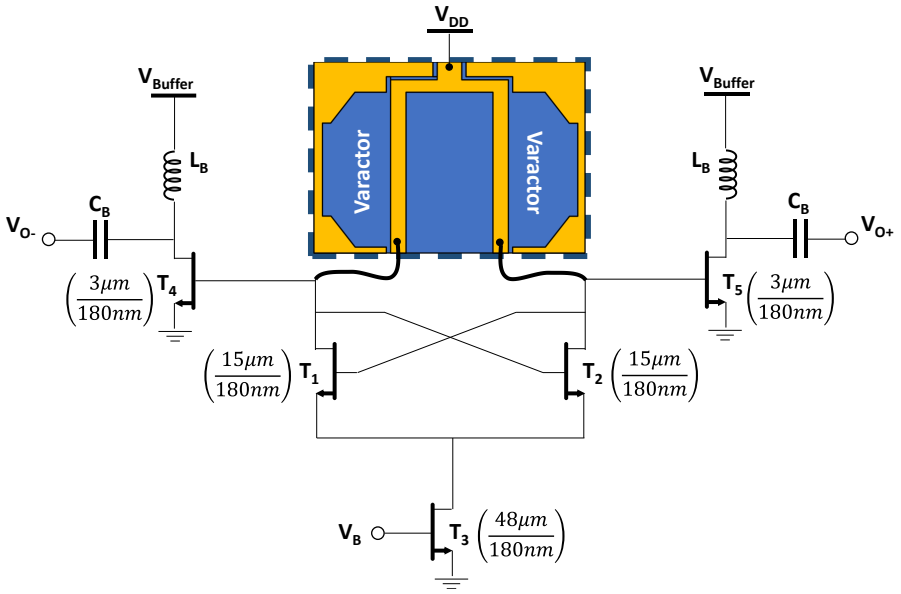
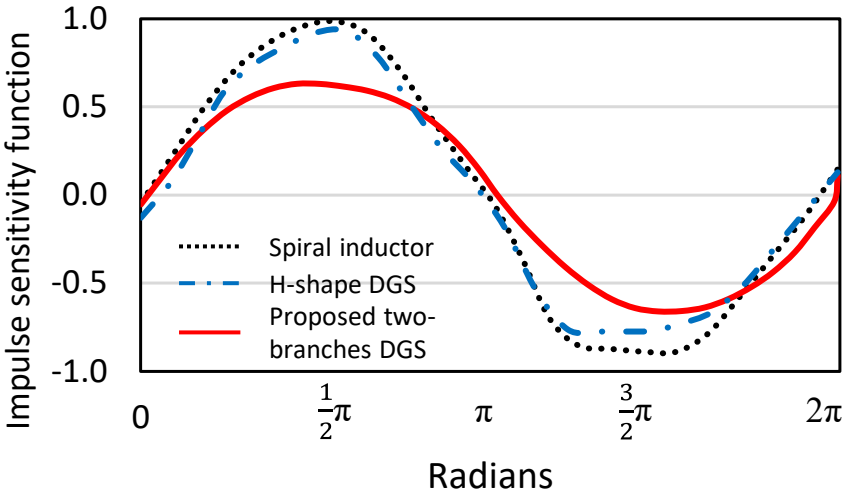


Fig. 4. 1 Schematic of the proposed VCO design.

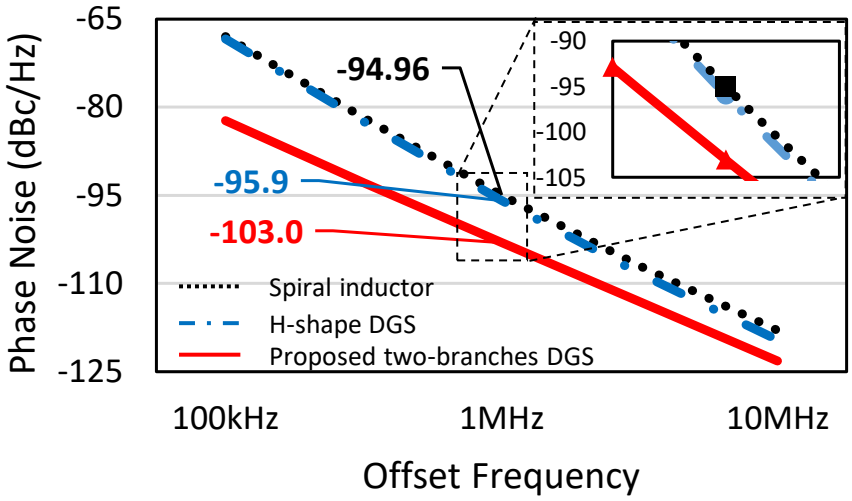
To verify our design concept introduced in the previous chapter, the proposed two-branches DGS resonator is implemented in a Class B topology to design a 50 GHz VCO. The schematic of the VCO using the proposed DGS resonator is shown in Fig. 4.1. The VCO core is composed of the DGS resonator, a cross-coupled pair of NMOS transistors (T_1 and T_2), and a tail current source (T_3). NMOS transistors switch on and off alternately and generate a negative resistance to cancel the losses of the DGS resonator. The tail current source drives the whole VCO and controls the power consumption to get the best figure of merit (FoM). For saving the chip area, instead of connecting MOS varactors in parallel of the resonator, they are positioned in the free space inside the DGS resonator as shown in Fig. 4.1.

The proposed DGS resonator is designed and simulated by the commercial High-Frequency Structure Simulation (HFSS) ver. 13 from the Ansoft Corporation. Its scattering parameters (S-parameter) are extracted as an s2p file and used in the circuit simulation and post-layout simulations by Keysight Advanced Design System (ADS) and Cadence Virtuoso, respectively.

Besides the proposed VCO, VCOs using the conventional spiral inductor and conventional H-shape DGS resonator are built and simulated at the same time. The comparison in terms of the calculated impulse sensitivity function (ISF) and simulated phase noise for these three VCOs has



(a)



(b)

Fig. 4. 2 The calculated ISF (a) and simulated phase noise (b) comparisons using DGS resonator, conventional spiral inductor, and conventional H-shape DGS resonator.

been illustrated in Fig. 4.2. According to the results shown in Fig. 4.2(a), the proposed VCO implementing two-branches DGS resonator shows the least sensitivity to the impulse noise current, then the VCO using conventional H-shape resonator, and the highest sensitivity is the VCO utilizing conventional spiral inductor. The simulated phase noise performance in Fig. 4.2(b) shows good agreement with the ISF comparison. The VCO using the proposed two-branches DGS resonator has a much lower phase noise than others. At its operating frequency, the proposed VCO

achieves a phase noise of -103 dBc/Hz at the 1 MHz offset in the simulation.

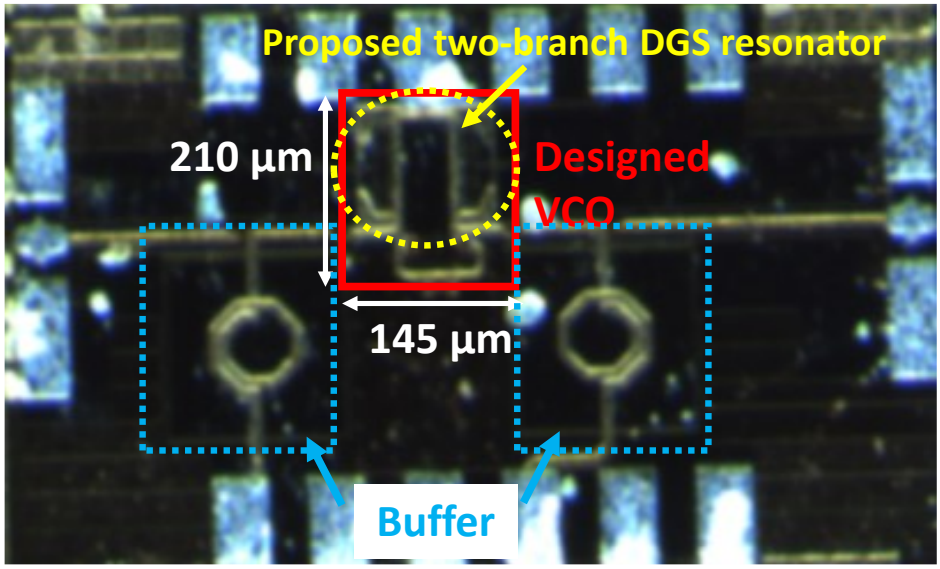
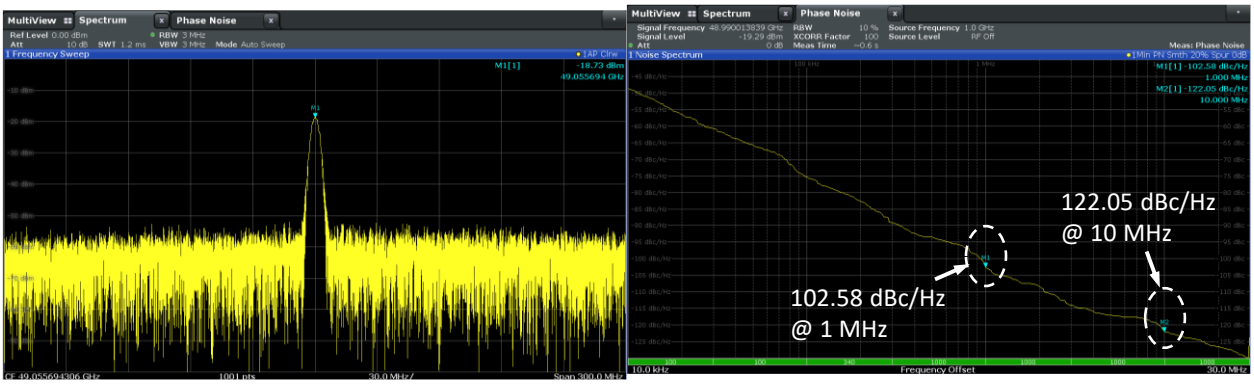


Fig. 4. 3 Chip photograph.



(a) (b)

Fig. 4. 4 Measured performance of the VCO based on the proposed two-branches DGS (a) Output spectrum. (b) Phase noise at frequency offsets.

4.1.2 Measurement

The designed low phase noise VCO with the integrated DGS resonator was implemented in 0.18-µm CMOS technology and its micrograph is shown in Fig. 4.3. The proposed two-branch DGS resonators are enclosed by the yellow line. The core of the designed VCO, which is enclosed by the red line, occupies 210 µm ×145 µm area. Two buffers are designed to drive the 50 Ω load output on both sides of the VCO, which are enclosed by the blue line in Fig. 4.3. As the DGS

resonator is first implemented at such a high frequency, we didn't choose to instead the conventional spiral inductor in the buffer design by the DGS. In our future work, we plan to use DGS instead of the inductor in the buffer for further saving the chip area. The core area including buffers is 0.19 mm^2. The measurement setup included a probe station using on-wafer probing with Infinity RF probes from Cascade Microtech, a ROHDE & SCHWARZ FSWP 50 signal source analyzer (SSA), Eye-Pass Probes for dc biasing. The pads on the left and right sides are the RF Infinity probe for the output signals (G-S-G) from the buffer. The pads on the top and bottom are the dc probe (P-G-P-P-G-P), which is used for supply and gate bias voltages.

The measured output spectrum and phase noise are shown in Fig. 4.4(a) and Fig. 4.4(b), respectively. In the measurement, when the supply voltage of the proposed VCO is set to 1.1 V, it performs the best phase noise of -102.58 dBc/Hz at a 1 MHz offset with a carrier frequency of 49 GHz. The dc power dissipation is 5.5 mW. This leads to an FoM of –189 dBc/Hz. The measured tuning range up to 50 GHz range is 1.24% (48.79 GHz ~ 50 GHz). However, this does not represent the actual possible tunning range due to the limitation of the used SSA as it has a maximum measurement range of up to 50 GHz only. So, the accurate tuning range could not be fully measured.

The overall performance of the proposed VCO design, except the tunning range, is compared with V band VCOs reported recently in TABLE 4.1. Comparing V band VCO designs published recently [40]-[42], [44]-[47] the proposed VCO has a much better performance on phase noise while low power consumption is achieved as well.

TABLE 4. 1 Performance Comparison with Published V-band VCOs

	Technology	Freq. (GHz)	Phase Noise (dBc/Hz)	P_{DC} (mW)	FoM* (dBc/Hz)	Core Area (mm^2)
[40]2009	65nm CMOS	56	-99.4	15	-182.2	0.05
[41]2015**	65nm CMOS	49.7	-94	14.1	-177	0.39
[42]2018	65nm CMOS	49.23	-93.7	7.2	-179.3	0.02
[43]2019	65nm CMOS	62.8	-105.5	61.2	-183.6	0.15
[44]2019	65nm CMOS	55	-89.9	6.2	-178.9***	0.06
[45]2020**	40nm CMOS	46.75	-91.8	81.8	-166.8	1.17
[46]2021	22nm FDSOI	60	-92.1	31.7	-170.4	0.09 (include pads)
[47]2021	90nm CMOS	56.52	-87.83	7.08	-174.3	0.42 (include pads)
This work	**180nm CMOS**	**49**	**-102.6**	**5.5**	**-189**	**0.19**

*$FoM = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log(P_{DC})$

** Phase-locked loop

*** Average value

4.2 Wide Tuning Range DGS-based VCO for K band Applications in 0.18-µm CMOS Technology

Due to the proliferating demand for high data rate communication, more and more applications in K band and above have been reported [24]-[30], [36]-[38]. Voltage-Controlled Oscillator (VCO), as the key circuit component of a wireless communication system, also attracts a lot of interest from researchers because the system performance is directly affected by the phase noise of a VCO. Recently, many K band VCOs employing DGS as the resonator have been reported [24]-[30], which showed good performance in phase noise and miniaturization, because the DGS resonator implemented in the same CMOS technology has a higher Q-factor than its counterpart on-chip spiral inductor. However, because of the narrow resonance band of the DGS resonator and position-based capacitance, the varactor cannot be connected straight to a DGS resonator, which results in its narrow-tuning range compared with an LC-based VCO in the same frequency.

In this section, a new method for designing a wide tuning range DGS-based VCO with good phase noise performance is proposed and analyzed. The proposed two-branches DGS resonator is optimized for this concept. By employing the proposed DGS resonator, the varactor can be integrated with this DGS resonator making the chip more compact. Finally, a wide tuning range Ka-band VCO, employing the proposed DGS resonator, is designed, and fabricated in 0.18-µm 1P6M CMOS technology.

4.2.1 Theory and Concept

Fig. 4.5 shows the schematic and simplified equivalent circuit of a typical push-pull VCO. This topology shows good performance in controlling power consumption. The resonator, which determines the oscillation frequency, includes an inductor, a parallel capacitor, and the varactor. Its oscillation frequency (f_{osc}) can be calculated by (4.1).

$$f_{osc} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L(C_p + C_{var})}} \tag{4.1}$$

where C_p is the capacitance of the parallel capacitor, C_{var} is the capacitance of the varactor without any bias and ΔC is the capacitance variation because of the bias. From this equation, we can get the tuning range (the variation of the frequency) in (4.2).

$$\Delta f = \frac{1}{2\pi} \cdot \left[\frac{1}{\sqrt{L \cdot (C_p + C_{var} + \Delta C)}} - \frac{1}{\sqrt{L \cdot (C_p + C_{var})}} \right] \tag{4.2}$$

Then, with a little transformation, we can get (4.3). Here C_{total} is used to indicate the sum of the C_p and the C_{var}.

$$\Delta f = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L \cdot C_{total}}} \left(\frac{1}{\sqrt{1 + \frac{\Delta C}{C_{total}}}} - 1 \right) \tag{4.3}$$

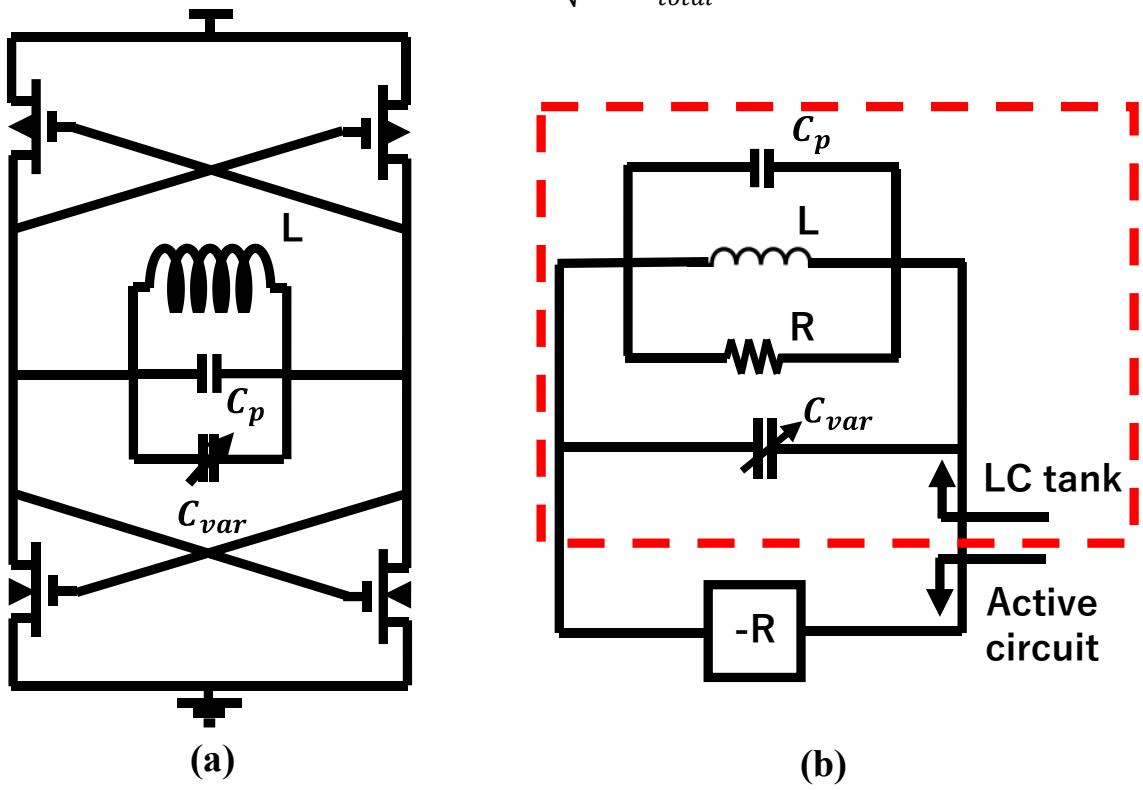


Fig. 4. 5 Conventional push-pull VCO. (a) Its typical schematic. (b) Its equivalent circuit.

From (4.3), it's easy to find that in the normal LC tank VCO's design, there are two ways to improve its frequency tuning range. One is increasing the capacitance variation of the varactor (ΔC) and another is using a parallel capacitor (C_p) as small as possible. Consequently, the inductor should become larger to maintain the oscillation frequency. However, while the tank capacitance decreases, the loaded quality factor of the tank will decrease as well, which may worsen the VCO's phase noise characteristic.

Fig. 4.6(a) illustrates the variation of phase noise and tuning range with the capacitor's size. We obtained these simulation results using the ideal LC tank, so only the influence of the topology is considered. It's clear that when the capacitance decreases, the tuning range will be improved while the phase noise will deteriorate on the contrary, which means there is a contradiction between achieving a low phase noise and a wide tuning range at the same time. Additionally, if we check the FoM_T in Fig. 4.6(b), we find that although the phase noise is improved, the FoM_T still becomes worse because of its poor tuning range. This gives a big challenge to design a wide tuning VCO using DGS resonator while keeping it with a good overall performance.

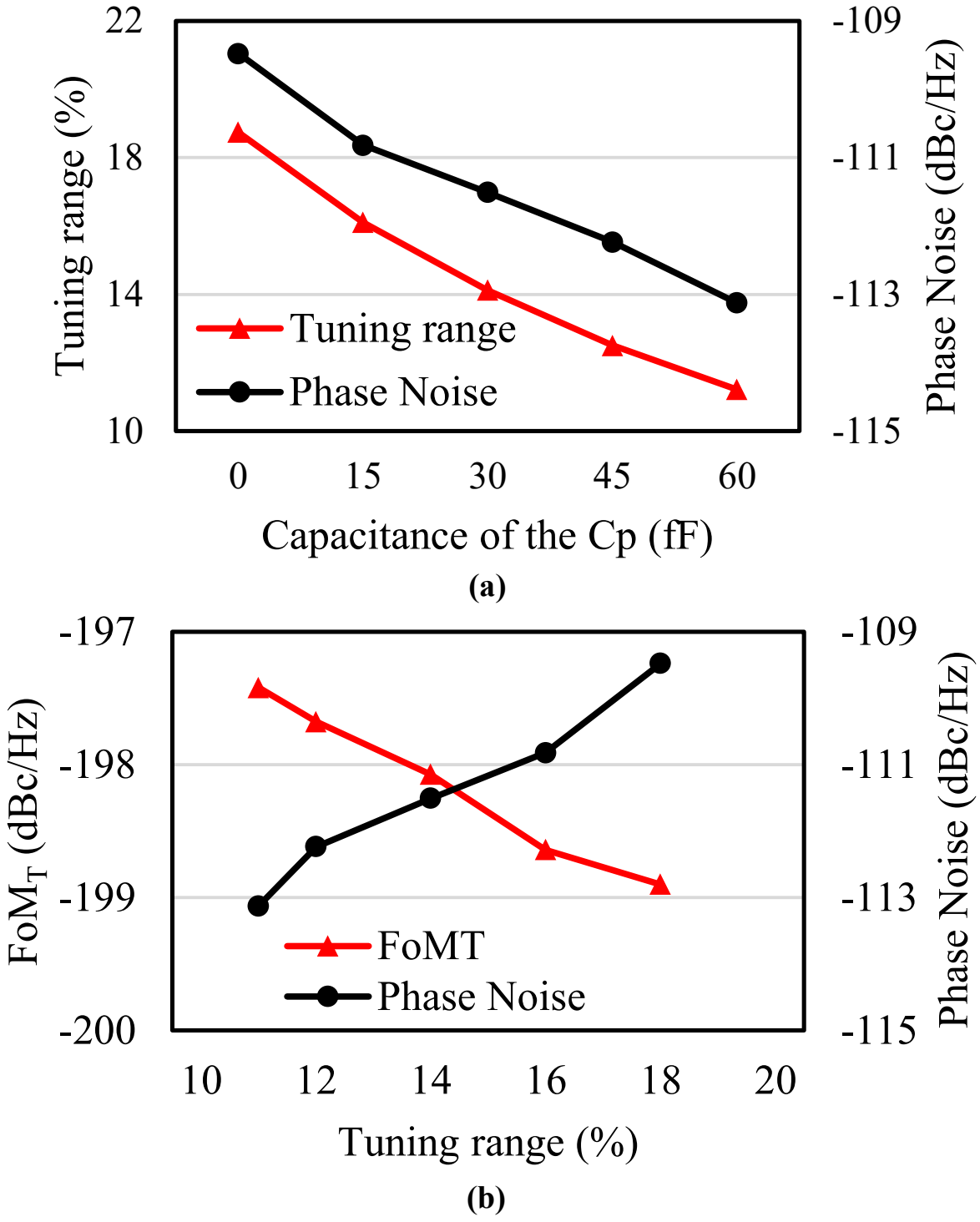


Fig. 4. 6 Performance of the VCO versus the loading capacitor, C_p, while fixing oscillation frequency, f_{osc}. (a) Phase noise and tuning range. (b) FoM$_T$ and phase noise versus tunning range.

4.2.2 Implementation of Compact and High-Quality Factor Resonator in DGS Topology

To overcome the problems mentioned above, a new type inductor realized by DGS resonator with compact size and high-quality factor is proposed in this section.

By etching a specific pattern on the ground, the electromagnetic (EM) fields of the transmission line will be interrupted, so that DGS can work as a parallel resonator generating a virtual inductor paralleled with a virtual capacitor [26]. Normally, DGS is used as the compact resonator structure with high Q-factors directly. However, if we can decrease its capacitance, an inductor with a high Q-factor will remain and suit our purpose. In Fig. 4.7(a), a conventional square-shaped DGS is shown.

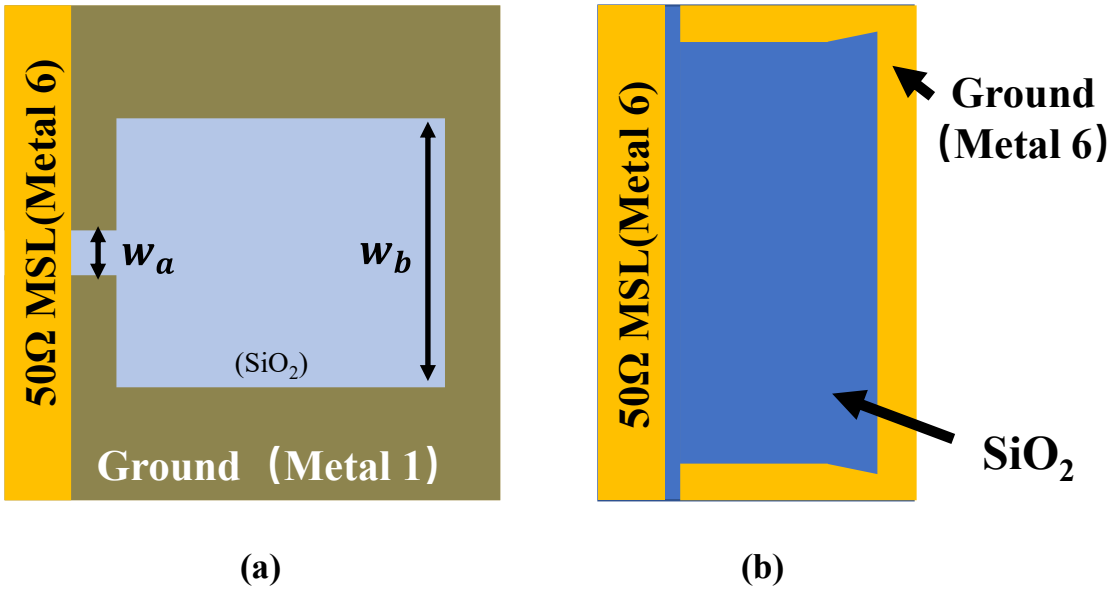


Fig. 4. 7 Model of DGS in CMOS technology. (a) H-shaped DGS resonator [6]. (b) Proposed DGS resonator.

According to [26], it's known that the virtual capacitor generated by the DGS resonator is controlled by the width of the gap w_a and the virtual inductor is almost controlled by the length w_b respectively. By lengthening both w_a and w_b, the capacitance part will decrease, and relatively, the inductance will increase. Meanwhile, this also brings enough space for integrating the varactor inside DGS. In Fig. 4.7(b), the proposed inductance-specific DGS is shown. Besides the above arrangement, the conventional resonator is divided into two small resonators which have the same resonance frequency as shown in Fig. 4.8(a).

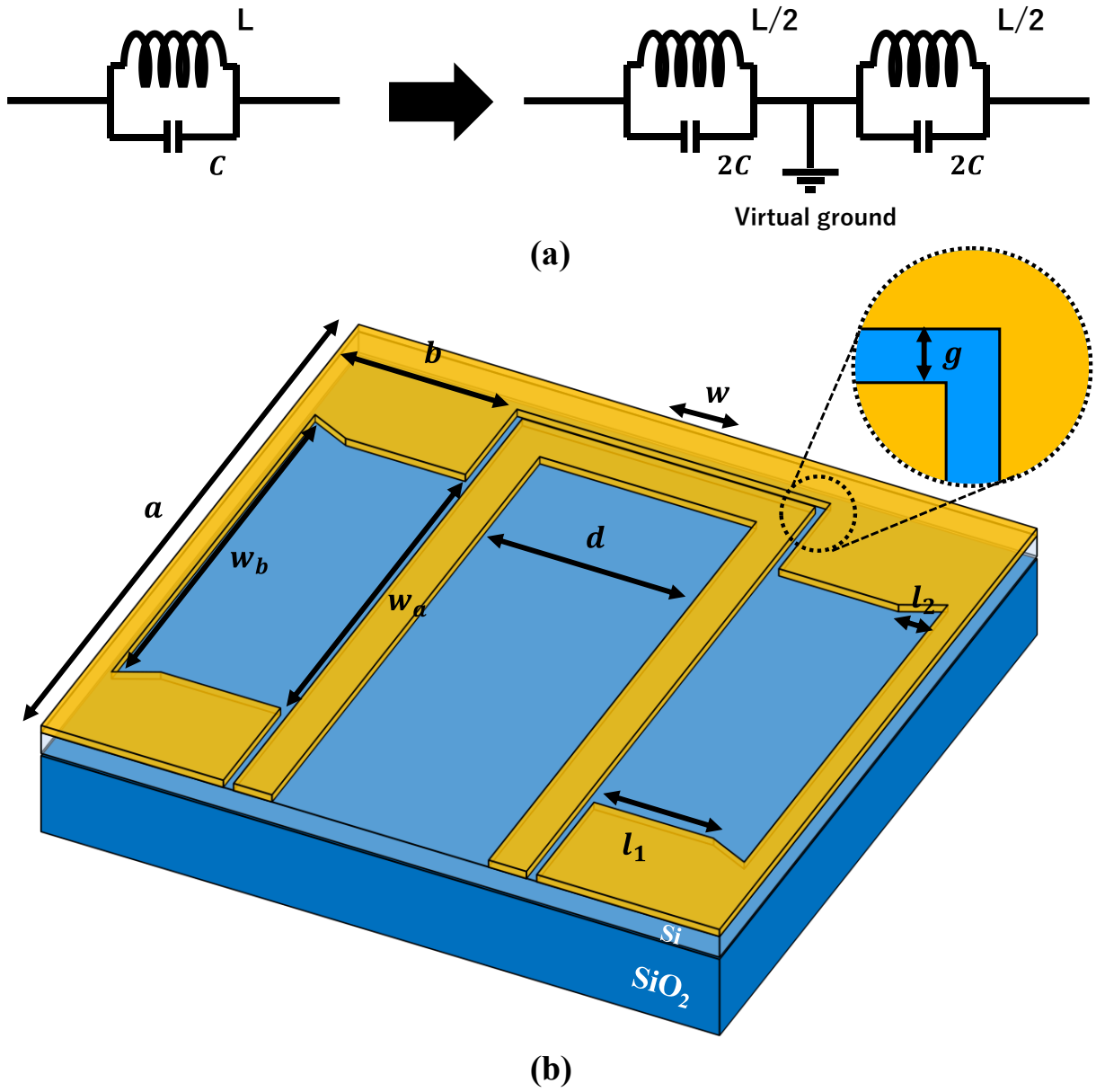


Fig. 4. 8 Concept of cascading of two proposed DGS resonators and its implementation in CMOS technology. (a)Design concept based on equivalent circuit. (b) Overview of the proposed DGS resonator.

TABLE 4. 2 Design Psarameters of the DGS resonator

Parameters	a	b	d	g	l_1	l_2	w	w_a	w_b
Dimension(μm)	200	80	52	1	65	15	10	175	180

Normally, inductors occupy most of the chip area. Increasing the number of inductors equals to bigger chip size. People will avoid this method. However, in this design, using two DGS resonators and setting them as shown in Fig. 4.8(b) can decrease the distance between two ports that connects the active circuits. This will help reduce the length of the interconnects to reduce the total layout size and curb the drop of the quality factor [31]. The optimized dimension of the proposed DGS resonator is summarized in Table 4.2.

The proposed DGS resonator is implemented in 0.18-μm 1P6M CMOS technology and simulated by ANSYS High Frequency Structure Simulator (HFSS). Fig. 4.9 shows the comparison of the quality factor between the DGS resonator and the conventional spiral inductor. A lumped port is inserted into the excitation gap of DGS to calculate its unloaded Q-factor. The self-inductance (L_{eq}), resistance (R_{EQ}), and Q_u of the DGS can be calculated by (4.4).

$$L_{eq} = Im(Z_{11})/\omega \qquad R_{EQ} = Re(Z_{11})$$
$$Q_u = Im(Z_{11})/Re(Z_{11}) \tag{4.4}$$

From Fig. 4.9, we can find that the conventional spiral inductor's quality factor will deteriorate rapidly after 15 GHz. This is caused by its self-resonance. However, the DGS resonator has over 20 of the quality factors in the Ka-band, which is much higher than the conventional ones at the

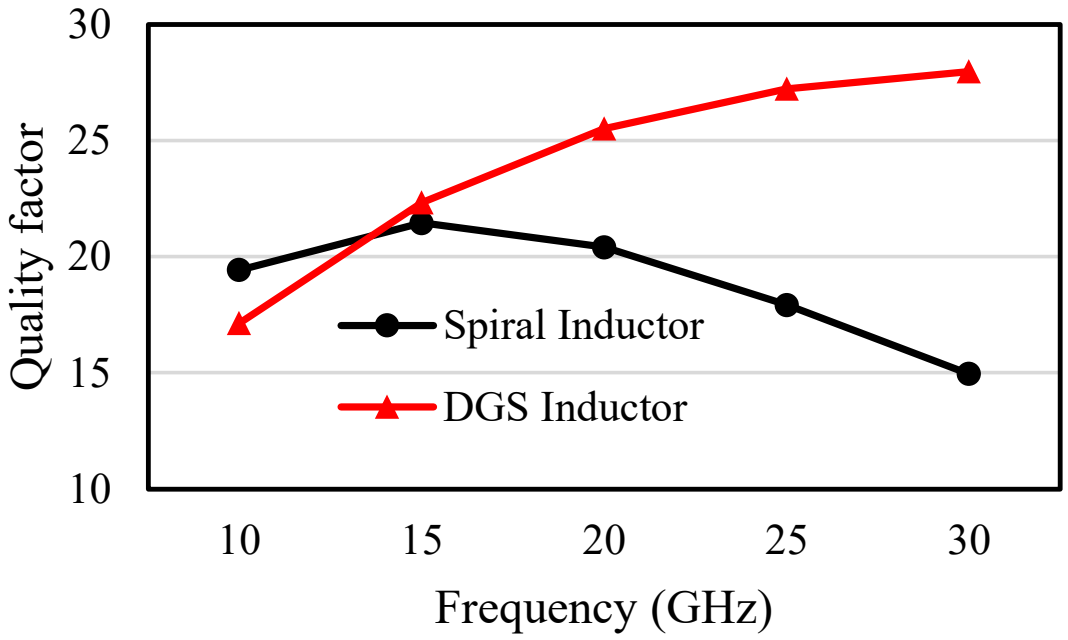


Fig. 4. 9 Comparison of the quality factor between spiral inductor and proposed DGS inductor.

target frequency band. And Q-factor keeps increasing during the whole band, which means no self-resonance will happen in this band. Therefore, this high-quality factor is expected to remain a good phase noise.

4.2.3 Proposed VCO Design

To prove the design concept, the proposed DGS resonator is implemented in a simple Class-B VCO topology as shown in Fig. 4.10. NMOS (T1, T2) will switch on in each half period and generate a negative resistance to cancel the losses of the DGS resonator. A tail current source is added to drive the whole circuit and control the power consumption to get the best FoM. To evaluate the designed VCO's performance, we implement it in Agilent ADS. The scattering parameters (S-parameter) and the impedance parameters (Z-parameter) of the proposed DGS resonator are obtained after EM simulation by the commercial High Frequency Structure Simulation (HFSS) ver. 13 from the Ansoft Corporation.

At first, our VCO realized by the DGS resonator is compared with a VCO employing a conventional spiral inductor. The comparison of simulation results is shown in Fig. 4.11. From Fig. 4.11, it can be found that because of its better quality factor, VCO employing the proposed DGS resonator provides better phase noise performance than the conventional one. It brings a 4dBc/Hz phase noise improvement at 1MHz offset. It should be noted that because the varactor cannot be integrated inside the conventional DGS resonator, during this comparison, the varactor is connected in area 1 of Fig. 4.10 for fair.

Secondly, the impact of a different connecting way of the varactor is investigated. Fig. 4.12 shows the comparison of insertion loss between connecting varactors in areas 1 and 2 of Fig. 4.10. According to the simulation result in Fig. 4.12, connecting the varactors inside the DGS resonator will make the insertion loss ($|S_{21}|$) wider and deeper than the conventional connecting way. This improves the loaded quality factor of the resonator and therefore, the phase noise performance also gets an improvement. In Fig. 4.13, it can be confirmed that the best phase noise during the tuning will be improved by about 2dBc/Hz.

Fig. 4.14 shows the simulated phase noise and the output frequency of the proposed VCO while changing the tuning voltage. A 19.3 GHz to 22.54 GHz wide tuning range is realized and phase noise is lower than -102dBc/Hz during the tuning, while the best phase noise performance is

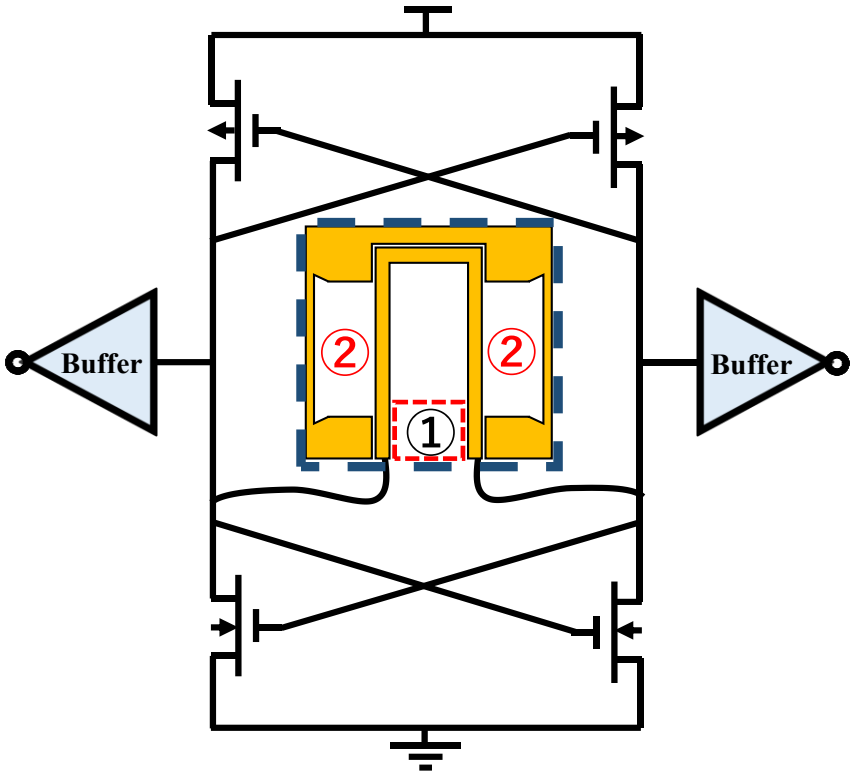


Fig. 4. 10 Proposed VCO with DGS resonator.

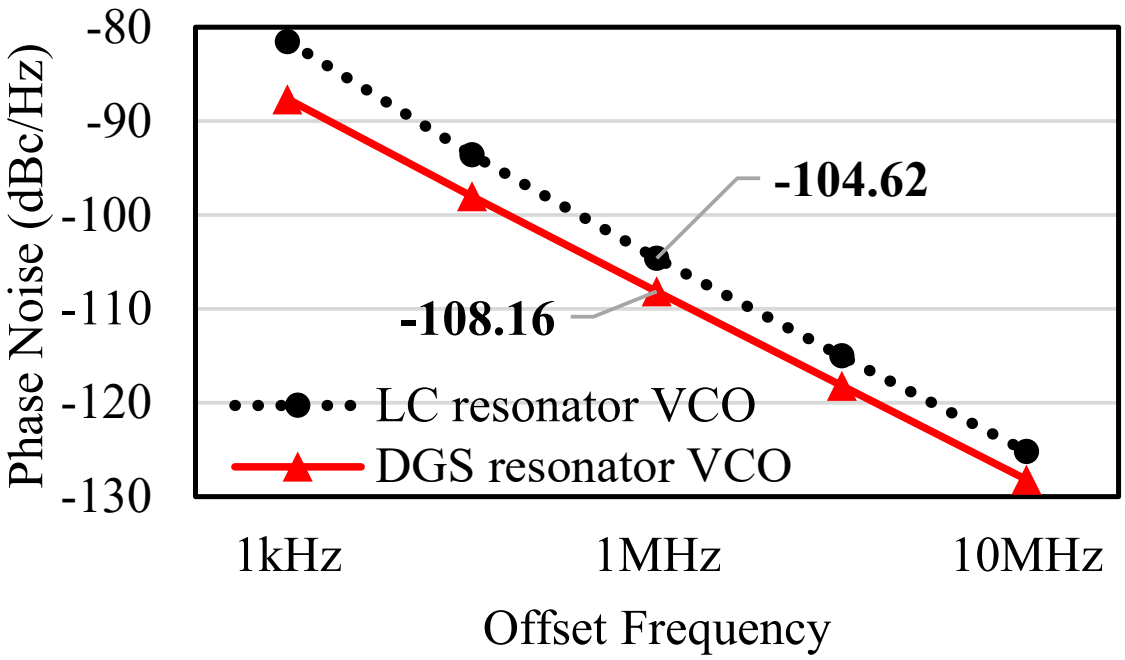


Fig. 4. 11 Comparison of simulated phase noise of the VCO employing an LC resonator and a DGS resonator.

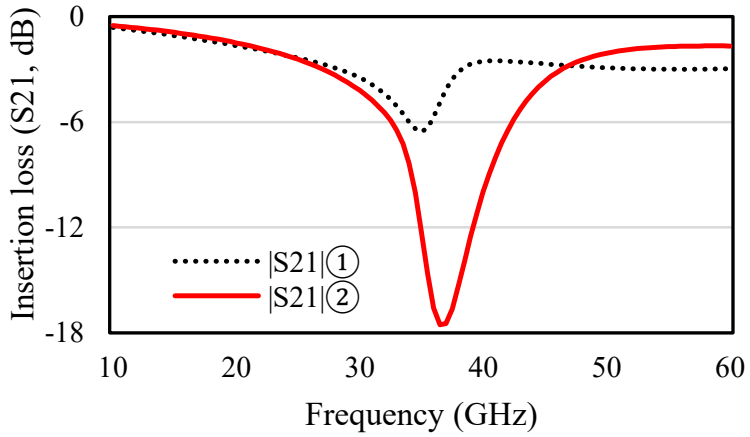


Fig. 4. 12 Simulated insertion loss comparison between two connection ways of varactor.

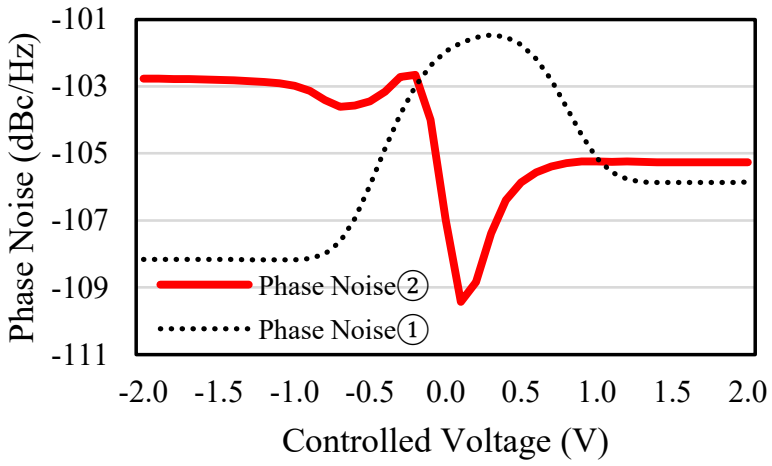


Fig. 4. 13 Simulated phase noise comparison between two connection ways of varactor with tuning.

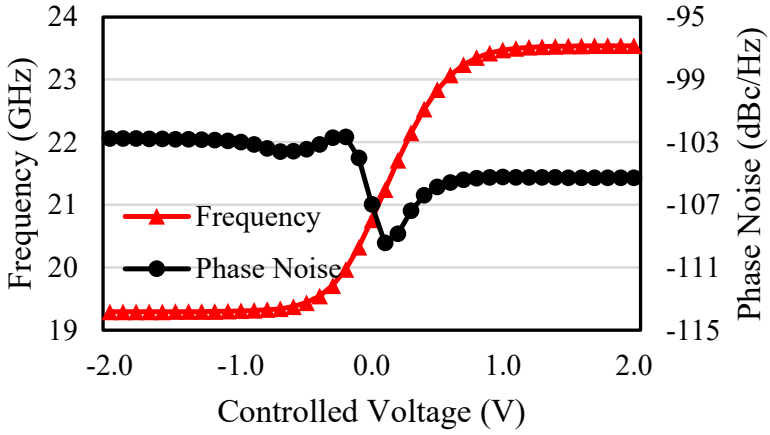


Fig. 4. 14 Simulated phase noise and frequency during tuning.

-109.43dBc/Hz. The designed VCO consumes only 1.38 mA current from a 1.8 V voltage supply, which leads to a -192.5dBc/Hz of the best FoM and -198.44dBc/Hz of the best FoM_T respectively. The overall performance of the proposed VCO design is compared with VCOs employing other types of DGS resonators in Table 4.3. Although the phase noise deteriorates, the FoM_T is extremely improved because of the excellent wide tuning range of the proposed VCO.

4.2.4 Measurement

The designed wide tuning VCO with the integrated DGS resonator was implemented in 0.18-µm 1P6M CMOS technology and its micrograph is shown in Fig. 4.15. The VCO core is only 0.105 mm^2. Two DGS resonators are enclosed by red lines. A signal source analyzer (ROHDE & SCHWARZ FSUP.SSA) was used in the measurement. The measured output spectrum and phase noise are shown in Fig. 4.16(a) and Fig. 4.16(b), respectively. The measurement shows that the VCO has a -108.41dBc/Hz of phase noise at a 1 MHz offset chip with a carrier frequency of 18.5GHz. The proposed VCO also showed a good voltage sensitivity.

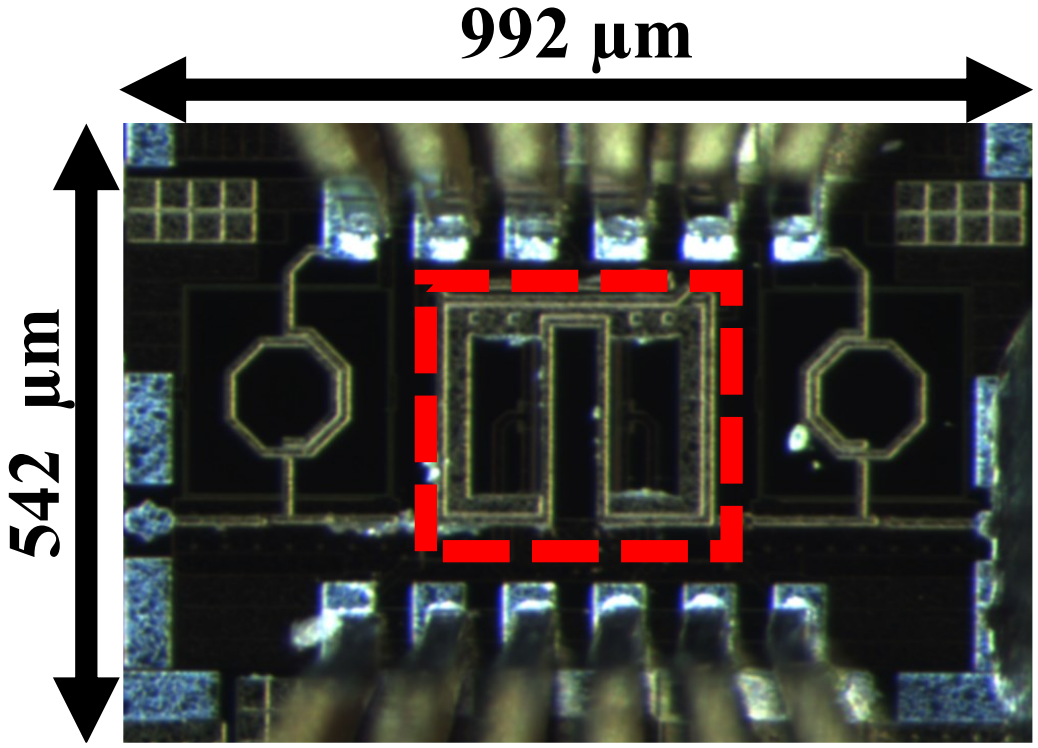
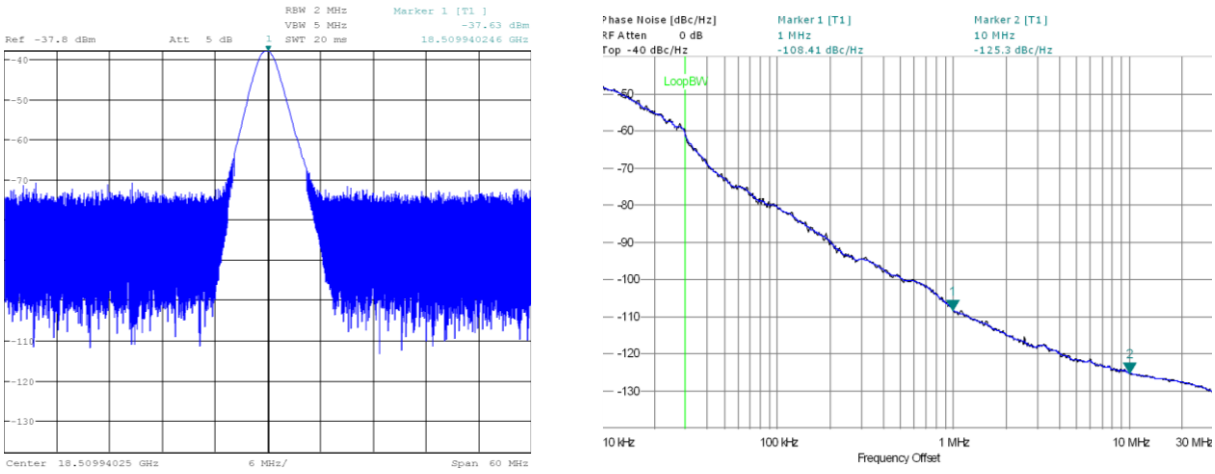


Fig. 4. 15 The fabricated VCO chip.



(a) (b)

Fig. 4. 16 Measurements of the proposed VCO. (a)Output spectrum at 18.51 GHz. (b)Measured phase noise.

TABLE 4. 3 Performance Comparison* with Recently Proposed DGS-BASED VCOs

Reference	**[24]**	**[30]**	**This work**
f_{osc}**(GHz)**	21.04	22.07	20.69
FTR(%)	3.4	2	19.8
P_{dc}**(mW)**	7.5	4	2.48
Phase Noise @1MHz (dBc/Hz)	-111.9	-112.31	-109.4
Resonator Type	Dual Series and parallel resonance based DGS	Parallel+ Dual Series Resonances based DGS	Dual branch DGS
FoM (dBc/Hz)	-188.7	-193.2	-192.5
FoM$_T$ (dBc/Hz)	-184.0	-179.7	-198.4

*All of these are simulation results.

$$FoM = -Phase\ Noise - 20log\frac{f_{osc}}{\Delta f} + 10logP_{dc} \qquad FTR = \frac{\Delta f}{f_0} \qquad FoM_T = FoM + 10log\frac{FTR}{10}$$

4.3 Study of the Effect of Interconnects on Phase Noise of K band VCO

To ensure the communication quality, VCO is asked for having low phase noise. According to the Lesson's equation [12], the resonator's phase noise is almost generated by the resistance in the inductor. Therefore, there are many people who focus on improving the quality factor of the inductor in an LC tank to compress the phase noise [24],[26],[42],[48],[49]. However, besides the quality factor, the parasitic inductance of the interconnecting transmission lines, which connect the resonator with transistors, will also have a significant impact on the phase noise and of course the oscillation frequency.

In the lower frequency domain, the inductance component in the resonator is considerable, so the influence of parasitic inductance can be ignored. However, when it goes to Quasi-millimeter-wave or millimeter-wave band, parasitic inductance becomes comparable to that in the resonator. For this reason, it's necessary to quantitatively figure out the effect of parasitic inductance. In this paper, two K band VCO are compared for discussing the effect of interconnects inductance on VCO's operation frequency and phase noise. Finally, a K band VCO is fabricated in 0.18-μm 1P6M CMOS technology to verify our view.

4.3.1 Analysis of Parasitic Inductance Effect

First, a model of the transmission line is built and simulated by the commercial High Frequency Structure Simulation (HFSS) 13.0 from the Ansoft Corporation. The relationship among transmission line length, its resistance and the parasitic inductance generated by itself are shown in Fig. 4.17.

Then, DGS is designed and simulated by HFSS (full form) and co-simulation of both circuits was carried out by Keysight Advanced Design System (ADS). By keeping the DGS unchanging, which means the quality factor of the inductor in the resonator doesn't change, several VCOs that work at 25 GHz but with different lengths of interconnecting transmission lines are designed. Simulation results of phase noise, figure of merit (FoM), and figure of merit considering tuning range (FoM_T) are shown in Fig. 4.18.

In the first half of Fig. 4.18, as the length of the interconnecting transmission line increases, the phase noise of the VCO is improved. Because of this, FoM and FoM_T also get an improvement.

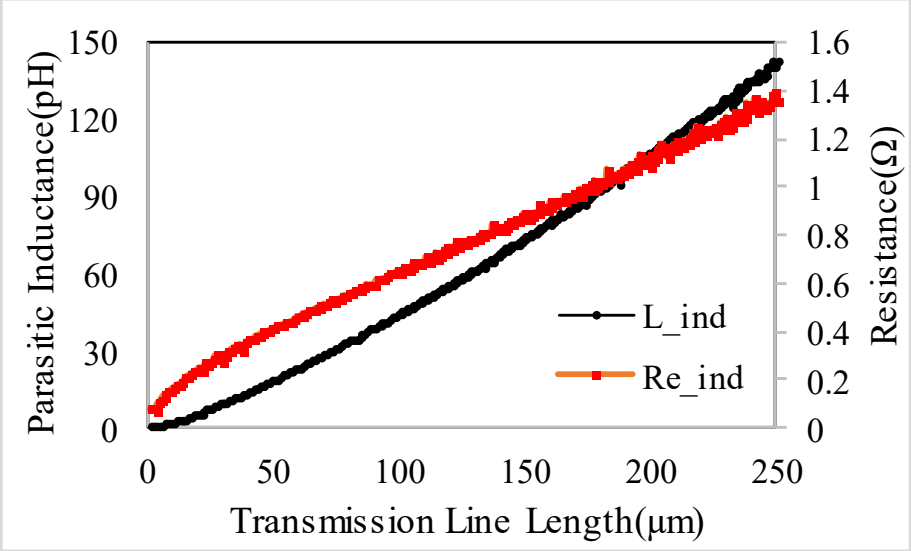


Fig. 4. 17 The relationship among transmission line length, resistance and the parasitic inductance generated by itself.

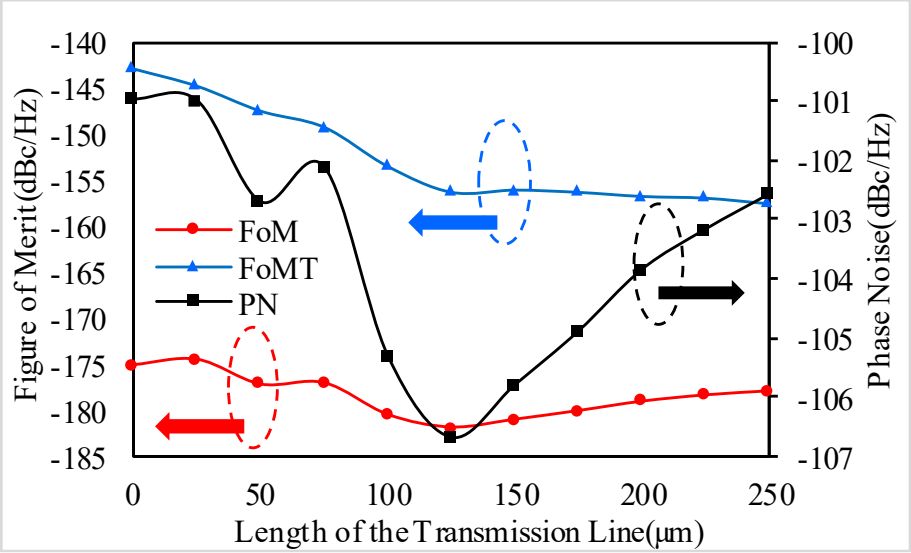


Fig. 4. 18 Simulated phase noise, FoM and FoM_T during changing the length of interconnecting transmission line

However, when the interconnecting transmission lines become longer than 125 μm, phase noise starts deteriorating rapidly although FoM and FoM_T change smoothly.

To find the proper explanation for this phenomenon, both loaded and unloaded quality factors, which are given by equations (4.5) and (4.6), are simulated and shown in Fig. 4.19. In these simulation results, besides the DGS inductor, the effect of transmission lines also has been considered, so we refer to them as the total loaded (Q_{ltotal}) and unloaded (Q_{utotal}) quality factor.

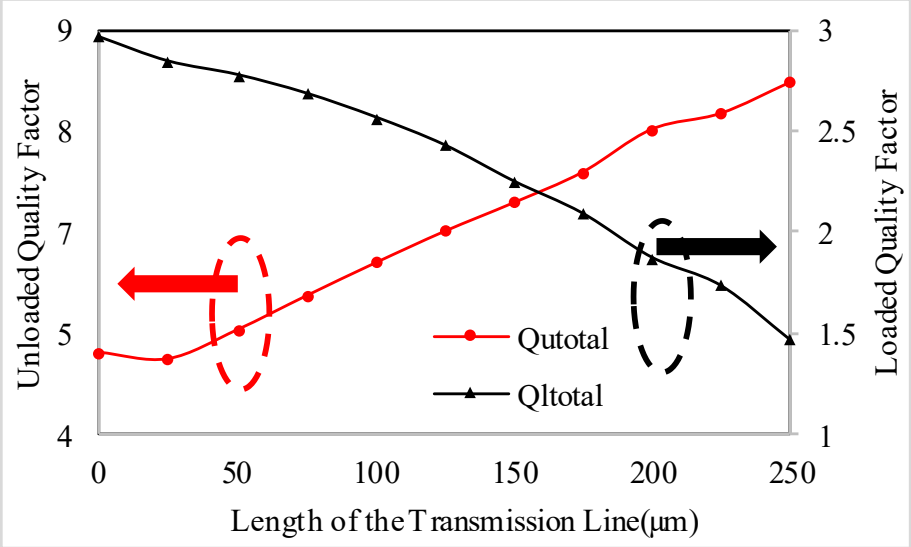


Fig. 4. 19 Simulated total loaded/unloaded quality factor considering transmission line with DGS together.

$$Q_{ltotal} = \frac{f_{OSC}}{BW} \tag{4.5}$$

$$Q_{utotal} = \frac{\omega(L_{DGS} + L_{TL})}{R_{total}} \tag{4.6}$$

As the transmission line lengthens, although its resistance will increase, generated parasitic inductance increases faster resulting in the continued growth of the Q_{utotal}. However, with the increment of the parasitic inductance, to keep the oscillation frequency unchanging, smaller parallel capacitors should be employed, which will decrease the Q_{ltotal}. What's more, increasing resistance also will cause a reduction in Q_{ltotal}. Back to the simulation result in Fig. 18, we can get a conclusion: before the length of the interconnecting transmission line exceeding 125 μm, the Q_{utotal} plays a major role in determining the phase noise. In this interval, the transmission line helps compensate for the inductance part of the resonator. However, when the length of the interconnecting transmission line exceeds 125 μm, Q_{ltotal}'s influence will become significant. As the length increases, phase noise deteriorates with the Q_{ltotal} together.

4.3.2 Measurement Result

As our purpose is to verify the effect of inductance on the phase noise, we chose to fabricate the VCO with poor performance instead of the best performance. Based on circuit topology and up until the conclusion, the K band VCO has been implemented in 0.18 μm 1P6M CMOS technology and its micrograph is shown in Fig. 4.20. Two interconnecting transmission lines around 250 μm

long are enclosed by red lines. A signal source analyzer (ROHDE & SCHWARZ FSUP.SSA) was used in the measurement. The measured output spectrum and phase noise are shown in Fig. 4.21 and Fig. 4.22 respectively. The measurement shows that the VCO chip operates at 25.4 GHz and its phase noise is -99 dBc/Hz by 1 MHz offset. The deviation between simulation and measurement is considered caused by the measurement equipment or other parasitic parameters.

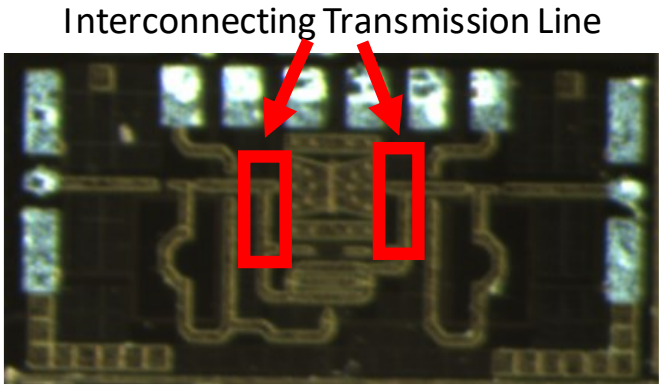


Fig. 4. 20 Fabricated chip's photo.

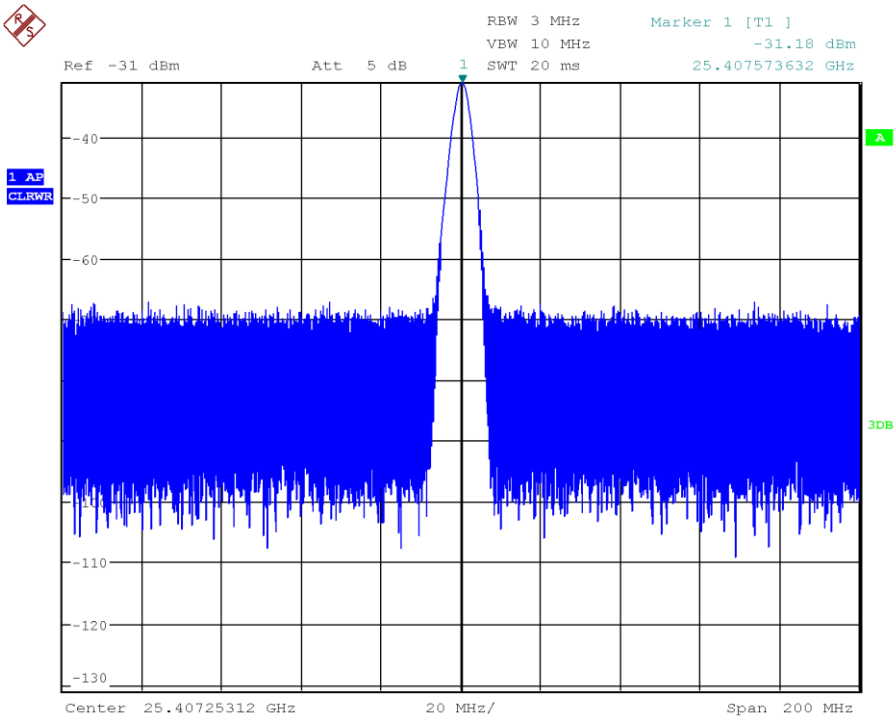


Fig. 4. 21 Output spectrum around 25.4GHz

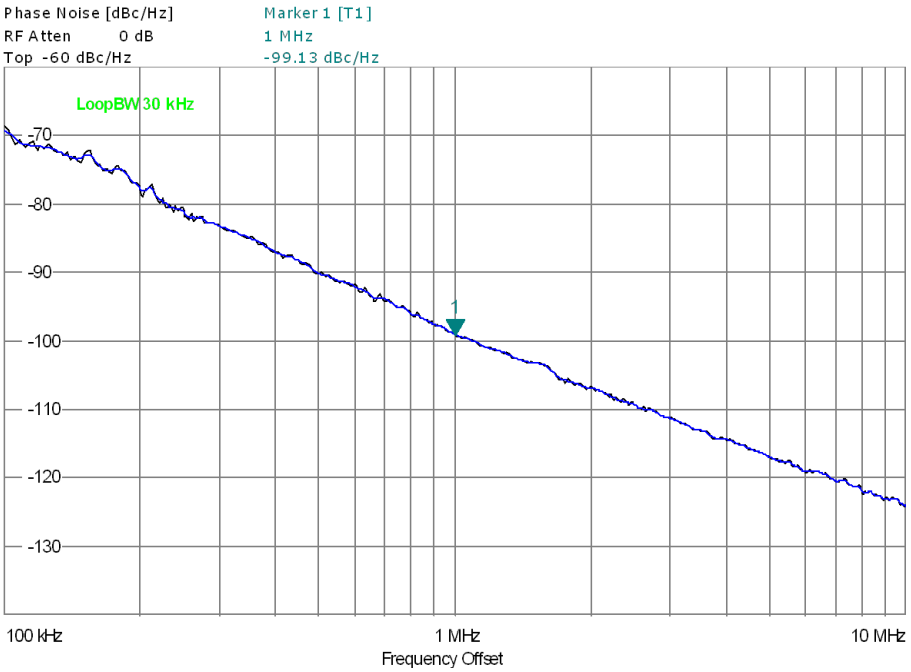


Fig. 4. 22 Measurement result of phase noise

4.4 Conclusion

A 50 GHz VCO implementing the proposed two-branches DGS resonator is designed, fabricated, and measured. The measurement shows that the phase noises of the fabricated VCO are -122.05 dBc/Hz and -102.58 dBc/Hz at 10-MHz and 1 MHz offsets, respectively, from a 49 GHz carrier frequency. The dc power consumption was only 5.5 mW. This leads to the best FoM of -189 dBc/Hz among the recently published V band VCOs in CMOS technology. This demonstrates the feasibility of the design approach introduced in chapter 3. The proposed design using the two-branches DGS resonator may give an alternative for the design approach of VCO and frequency synthesizers at V band and beyond.

Then, a design concept of VCO with wide frequency tuning range (FTR) is introduced. The two-branches DGS resonator is customized for this design approach in K band. According to the simulation results, the proposed DGS resonator is known as suitable for the realization of the wide tuning VCO design. A K band VCO employing the novel DGS resonator is demonstrated in 0.18-µm CMOS technology and the measurement result shows good agreement with simulation in phase

noise and carrier frequency. The measurement shows that the VCO has a -108.41dBc/Hz of phase noise at a 1 MHz offset chip with a carrier frequency of 18.5GHz.

Finally, research about the effect of interconnects on the phase noise of K band VCO has been done. It has shown that not only the quality factor of the inductor in the LC tank, but the parasitic inductance also has an effect on phase noise especially at high-frequency VCO designs such as K band and above. The effect of parasitic on the phase noise has been studied and verified with measurement results obtained on a chip fabricated using 0.18-µm CMOS technology. According to the simulation result and measurement, we suggest that it's better to avoid using a transmission line longer than 125 µm during the design of a K band VCO.

Chapter 5: Conclusion and Prospect

5.1 Contribution and conclusion

The recent exponential growth of wireless communication systems, such as cellphones, wireless local area networks (LANs) and RFIDs, has promoted a great demand for more compact size, lower production cost, and decreased power consumption. With the ongoing scaling down, Si-based integrated circuits, especially the CMOS technology, have become the most attractive solution and the best component operating at the frequency of millimeter-wave and beyond bands for these design demands. As a vital component of the wireless communication system, mm-wave frequency generation in CMOS technology faces many design challenges. One of them is the stringent requirements on the phase noise. Based on the reported research on phase noise, the phase noise is inversely proportional to the Q-factor of the resonator in an oscillator. However, because of the thin metallization and the lossy substrate, conventional resonators implemented in CMOS technology are normally realized with poor quality. In turn, this tradeoff constrains the development of Si-based wireless applications.

For this reason, this dissertation focuses on the analysis, design and implementation of high-Q integrated resonators technology which can be implemented by Si-based IC technologies for mm-wave oscillator applications. The proposed high-Q resonators can be divided into two main categories. The first category is the DGS resonator. This type of resonator is proposed to be implemented in the LC oscillator instead of the conventional spiral inductors. DGS resonators generally have two times the Q-factor than the conventional spiral inductor. In the reported VCO designs which use DGS as the resonator, it's thought difficult to achieve low phase noise and wide tuning range functions at the same time. A novel DGS resonator is optimized for the design of a K band VCO which achieves wide tuning and low phase noise performance at the same time. This type of DGS resonator realizes higher virtual inductance to get the wider tuning characteristic. Compared with reported its predecessors, the proposed DGS resonator is more compact and suitable to realize a wider tuning range. Then, an optimized two-branches DGS for the V band VCO application is designed and analyzed. This two-branch DGS doesn't only achieve a higher Q-factor than the conventional spiral inductor but also achieves a higher Q-factor than its predecessors of DGS resonators. It is the first time that the DGS resonator is implemented in the VCO working

for a such high frequency band. This proves that the DGS resonator may be a proper candidate for the design of high-performance mm-wave VCO applications. Finally, experimental research of the relationship between interconnects and phase noise of the K band VCO is given. During the layout design of the VCO, people mainly focus on the design of the active circuits or the resonator. The effect of the interconnects is usually ignored. Our research shows that, even when their length is not comparable to the wavelength, the interconnect affects VCO's phase noise performance significantly. This result is available for the improvement of the future VCO layout design.

In this dissertation, another type of resonator based on SIW structure is proposed as the post design of the DGS resonator. The DGS resonators are implemented in microstrip line (MSL)/ coplanar stripline (CPS)/ coplanar waveguide (CPW), which is an "open" structure. Therefore, during the layout design of the VCO implemented DGS as its resonator, redundant space is normally needed. The SIW-based resonator is the "closed" structure and is proposed to solve this problem. We proposed a novel miniaturization method of SIW resonator to remove the stumbling blocks of the implementation of SIW-based resonator in CMOS technology, which is its huge footprint. The proposed miniaturization method is very effective and available to reduce the area of the SIW resonator to 0.3%. The proposed miniaturized SIW resonator is transformed into two ports resonators (or called BPFs) for the future mm-wave VCO applications by different methods. A novel coupling method that couples two SIW resonators through a DGS is proposed to solve the weak coupling coefficient problem in CMOS technology. This is the first time that a SIW resonator/ BPF is implemented in a commercial Si-based technology successfully, which gives more choice in the future on-chip circuits design.

Table 5. 1 and Table 5. 2 summarize the performance of the oscillators and the W band bandpass resonators respectively. The phase noise of the proposed oscillators is extremely low. For example, at 1 MHz offset from the carrier, the phase noise of the 2nd VCO design is -102 dBc/Hz for 50 GHz. This result is much better than other reported VCOs which are even implemented with advanced technology. All the proposed W band bandpass resonators are realized with a low insertion loss, which remains less than 3.15 dB. In addition, benefitting from the compact size of the miniaturized SIW resonator, these bandpass resonators have an area that is comparable to the

conventional on-chip components. This makes on-chip SIW applications possible to be used in practice.

TABLE 5. 1 A Summary of the Performance of the Proposed VCOs Using DGS resonators

VCO Design	**1st Design**	**2nd Design**
f_{osc}**(GHz)**	20.69	49
FTR*****(%)**	19.8	14.5
P_{dc}**(mW)**	2.48	5.5
Phase Noise @1MHz (dBc/Hz)	-109.4	-102.6
FoM***(dBc/Hz)**	-192.5	-189
FoM$_T$****(dBc/Hz)**	-198.4***	-192.2***
Area(mm^2)	0.29	0.19

* $FoM = PN - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log(P_{DC})$

** $FoM_T = FoM - 20\log\left(\frac{FTR}{0.1}\right)$

*** $FTR = \frac{\Delta f}{f_0}$, Simulation Result

TABLE 5. 2 Performance Comparison of the Bandpass Resonators in CMOS Technology

Ref.	Process	Shielding Structure	Transmission zero	Order	Freq. (GHz)	FBW %	IL (dB)	Area (λ_g^2)
1st Design	CMOS	Yes	0	2	83	50.7	2.26	0.0098
2nd Design		Yes	0	2	85	43.8	3.15	0.022
3rd Design*		Yes	2	1	111	49.4	1.55	0.009

* Simulation Result

5.2 Prospect

Based on the research work, this section will provide future work.

1. DGS resonators also provide a wide range of freedom in their design and optimization. Therefore, further investigation needs to be done in order to see other prospects that could enhance the Q-factor further.
2. Although the DGS resonator has been designed structurally available to realize the low phase noise VCO with a wide tuning range, the used MIM capacitor and, MOS varactor

have limited Q-factor which results in a poor measured narrow tuning range on the contrary. Studying or developing techniques such as enhancing varactor's Q-factor are urgently needed.

3. As the research of the implementation of SIW resonator in a Si-based process is still in its initial stage, and there is a lack of transistors in the advanced process, the development of W band VCOs is failed to be implemented. I'm looking forward to realizing the low phase noise W band VCO with SIW BPFs in the future.
4. In the 180 nm CMOS process, the maximum achievable spacing between two metal layers is less than 7 μm, which deteriorates the Q-factor of the SIW resonator from hundreds to tens. Enhancement methods of the integrated SIW resonator are urgently needed.
5. The proposed low phase noise VCOs are expected to be developed to PLL for future reducing the output phase noise.

Reference

[1] Mobile data traffic outlook, Telefonaktiebolaget LM Ericsson [Online]. Available: https://www.ericsson.com/en/reports-and-papers/mobility-report/dataforecasts/mobile-traffic-forecast, Accessed on Dec. 2, 2021.

[2] Cisco Annual Internet Report (2018–2023) White Paper, Cisco Systems, Inc., [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html, Accessed on Dec. 2, 2021.

[3] "IEEE 802.15 Task Group 3c." [Online]. Available: http://www.ieee802.org/15/pub/TG3c.html, Accessed on Dec. 2, 2021.

[4] J. N. Bughartz and B. Rejaei, "On the design of RF spiral inductors on silicon", IEEE Transactions on Electron Devices, vol. 50, no. 3, March 2003.

[5] Seok-Ju Yun, So-Bong Shin, Hyung-Chul Choi and Sang-Gug Lee, "A 1mW current-reuse CMOS differential LC-VCO with low phase noise," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., 2005, pp. 540-616 Vol. 1.

[6] M. Wei, S. Chang and S. Huang, "An Amplitude-Balanced Current-Reused CMOS VCO Using Spontaneous Transconductance Match Technique," in IEEE Microwave and Wireless Components Letters, vol. 19, no. 6, pp. 395-397, June 2009.

[7] D. Zito, D. Pepe and A. Fonte, "13 GHz CMOS Active Inductor LC VCO," in IEEE Microwave and Wireless Components Letters, vol. 22, no. 3, pp. 138-140, March 2012.

[8] A. Mazzanti and P. Andreani, "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," in IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2716-2729, Dec. 2008.

[9] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3120-3133, Dec. 2013.

[10] W. Deng, K. Okada and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," 2011 Proceedings of the ESSCIRC (ESSCIRC), 2011, pp. 499-502.

[11] W. A. Edson, "Noise in oscillators," *Proc.of IRE*, Aug. 1960, pp. 1454–1466.

[12] B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, vol. 54, no. 2, pp. 329–330, Feb. 1966.

[13] B. Razavi, "A study of phase noise in CMOS oscillators," IEEE J. Solid-State Circuits, Vol. 31, pp.331-343, March 1996.

[14] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 326 –336, Mar. 2000.

[15] J. Maget, M. Tiebout, and R. Kraus, "MOS varactors with n- and p- type gates and their influence on LC-VCO in digital CMOS", IEEE J. Solid-State Circuits, vol. 38 (7), pp. 1139–1147, July 2003.

[16] D. Manstretta and R. Castello, "An intuitive analysis of phase noise fundamental limits in LC oscillators", in proc. of IEEE International Conference on Noise and Fluctuations, pp. 1-6, June 2015 (invited paper).

[17] E. Hegazi, H. Sjoland, and A. A. Abidi, “A filtering technique to lower LC oscillator phase noise,” IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
[18] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Sibased RF ICs," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 743-752, May 1998.
[19] J.Park, C. Kim, J. Kim, J. Park, Y. Qian, Dal Ahn; T. Itoh, "Modeling of a photonic bandgap and its application for the low-pass filter design," in Proc. Asia Pacific Microwave Conference (APMC), 1999, pp. 331-334 vol.2.
[20] N. Mahmoud, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, “Compact Size On-Chip 60 GHz H-Shaped Resonator BPF,” IEEE Microw. Wireless Compon. Lett., vol. 26, no. 9, pp. 681-683, Sept. 2016.
[21] Barakat, R. Pokharel, and T. Kaho, “60 GHz on-chip mixed coupled BPF with H-shaped defected ground structures,” Electron. Lett., vol. 52, no. 7, pp. 533–535, Apr. 2016.
[22] S. A. El-Hameed, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, “Ultracompact 60-GHz CMOS BPF Employing Broadside-Coupled Open-Loop Resonators,” IEEE Microw. Wireless Compon. Lett., vol. 27, no. 9, pp. 818-820, Sept. 2017.
[23] Elsaidy, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, “Ultracompact CMOS 60-GHz Tapped-Line Combline BPF With Two Transmission Zeros Using Defected Ground Structures,” IEEE Trans. Compon., Packag., Manuf. Technol., vol. 8, no. 9, pp. 1642-1649, Sept. 2018.
[24] N. Jahan, C. Baichuan, R. K. Pokharel, and A. Barakat, “A K band VCO Employing High Active Q-factor Defected Ground Structure Resonator in 0.18-µm CMOS Technology,” in Proc. IEEE Int. Symp. on Circuits and Syst., Florence, Italy, 2018, pp. 1-5.
[25] N. Jahan, C. Baichuan, A. Barakat, and R. K. Pokharel, “Analysis and Application of Dual Series Resonances for Low Phase Noise K band VCO Design in 0.18-µm CMOS Technology,” in Proc. IEEE Int. Symp. on Circuits and Syst., Sapporo, Japan 2019, pp. 1-5.
[26] N. Jahan, S. A. E. Ab Rahim, A. Barakat, T. Kaho, and R. K. Pokharel, “Design and Application of Virtual Inductance of Square-Shaped Defected Ground Structure in 0.18-µm CMOS Technology,” IEEE J. Electron Devices Soc., vol. 5, no. 5, pp. 299–305, Sep. 2017.
[27] N. Jahan, A. Barakat, and R. K. Pokharel, “Ku-band oscillator using integrated defected ground structure resonator in 0.18-µm CMOS technology,” in Proc. 47th Eur. Microw. Conf., Nuremberg, Germany, 2017, pp. 763-766.
[28] N. Jahan, A. Barakat, and R. K. Pokharel, “Study of phase noise improvement of K band VCO using additional series resonance realized by DGS resonator on CMOS technology,” in Proc. IEEE Asia Pacific Microw. Conf., Kuala Lumpur, Malaysia, 2017, pp. 1014-1017.
[29] N. Jahan, A. Barakat, and R. K. Pokharel, “A −192.7dBc/Hz FoM Ku-Band VCO Using a DGS Resonator With a High-Band Transmission Pole in 0.18-µm CMOS Technology,” IEEE Microw. Wireless Compon. Lett., vol. 29, no. 12, pp. 814-817, Dec. 2019.
[30] N. Jahan, C. Baichuan, A. Barakat, and R. K. Pokharel, “Utilization of Multi-Resonant Defected Ground Structure Resonators in the Oscillator Feedback for Phase Noise Reduction of K band VCOs in 0.18-µm CMOS Technology,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 4, pp. 1115-1125, April 2020.
[31] Baichuan, N. Jahan, A. Barakat, and R. K. Pokharel, “Experimental Study of the Effect of Interconnects on Phase Noise of K band VCO in 0.18µm CMOS Technology,” in Proc. IEEE Asia Pacific Microw. Conf., Singapore, 2019, pp. 1670-1672.

[32] N. Jahan, S. A. E. A. Rahim, H. Mosalam, A. Barakat, T. Kaho, and R. K. Pokharel, "22-GHz-Band Oscillator Using Integrated H-Shape Defected Ground Structure Resonator in 0.18-μm CMOS Technology," IEEE Microw. Wireless Compon. Lett., vol. 28, no. 3, pp. 233-235, Mar. 2018.
[33] N. Jahan, A. Barakat, and R. K. Pokharel, "A −192.7-dBc/Hz FoM Ku -Band VCO Using a DGS Resonator With a High-Band Transmission Pole in 0.18-μm CMOS Technology," IEEE Microw. Wireless Compon. Lett., vol. 29, no. 12, pp. 814-817, Dec. 2019.
[34] N. Jahan, A. Barakat and R. K. Pokharel, "Design of Low Phase Noise VCO Considering C/L Ratio of LC Resonator in 0.18-μm CMOS Technology," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 12, pp. 3513-3517, Dec. 2021.
[35] S. Hekal, A. B. Abdel-Rahman, H. Jia, A. Allam, A. Barakat, and R. K. Pokharel, "A novel technique for compact size wireless power transfer applications using defected ground structures," IEEE Trans. Microw. Theory Techn., vol. 65, no. 2, pp. 591–599, Feb. 2017.
[36] Z. Peng, D. Hou, J. Chen, Y. Xiang, and W. Hong, "A 28 GHz Low Phase-Noise Colpitts VCO with Wide Tuning-Range in SiGe Technology," in *Proc. IEEE Int. Symp. on Radio-Freq. Integration Technol.*, Melbourne, VIC, Australia, 2018, pp. 1-3.
[37] Masnadi, M. Mahani, H. M. Lavasani, S. Mirabbasi, S. Shekhar, R. Zavari, H. Djahanshahi, "A Compact Dual-Core 26.1-to-29.9GHz Coupled-CMOS LC-VCO with Implicit Common-Mode Resonance and FoM of-191dBc/Hz at 10MHz," in Proc. IEEE Custom Integr. Circuits Conf., Boston, MA, USA, 2020, pp. 1-4.
[38] Y. Shang, H. Yu, D. Cai, J. Ren, and K. S. Yeo, "Design of High-Q Millimeter-Wave Oscillator by Differential Transmission Line Loaded With Metamaterial Resonator in 65-nm CMOS," IEEE Trans. Microw.. Theory. Techn., vol. 61, no. 5, pp. 1892-1902, May 2013.
[39] N. Nouri and J. F. Buckwalter, "A 45-GHz Rotary-Wave Voltage-Controlled Oscillator," IEEE Trans. Microw. Theory Techn., vol. 59, no. 2, pp. 383-392, Feb. 2011.
[40] J. L. G. Jimenez, F. Badets, B. Martineau and D. Belot, "A 56GHz LC-tank VCO with 17% tuning range in 65nm bulk CMOS for wireless HDMI applications," in Proc. IEEE Radio Frequency Integrated Circuits Sym., Boston, MA, USA, 2009, pp. 481-484.
[41] Y. Chao, H. C. Luong, and Z. Hong, "Analysis and Design of a 14.1-mW 50/100-GHz Transformer-Based PLL With Embedded Phase Shifter in 65-nm CMOS," IEEE Trans. Microw. Theory Techn., vol. 63, no. 4, pp. 1193-1201, Apr. 2015.
[42] J. Y. Jin, L. Wu and Q. Xue, "A V band CMOS VCO With Digitally-Controlled Inductor for Frequency Tuning," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 65, no. 8, pp. 979-983, Aug. 2018.
[43] J. Zhang, C. Zhao, Y. Wu, H. Liu, Y. Zhu and K. Kang, "An Ultralow Phase Noise Eight-Core Fundamental 62-to-67-GHz VCO in 65-nm CMOS," IEEE Microw. Wireless Compon. Lett., vol. 29, no. 2, pp. 125-127, Feb. 2019.
[44] M. H. Kashani, A. Tarkeshdouz, R. Molavi, A. Sheikholeslami, E. Afshari and S. Mirabbasi, "On the Design of a High-Performance mm-Wave VCO With Switchable Triple-Coupled Transformer," IEEE Trans. Microw. Theory Techn., vol. 67, no. 11, pp. 4450-4464, Nov. 2019.
[45] Z. Chen, W. Deng, H. Jia, Y. Liu, J. Wu, P. Guan, J. zhu, L. Mao, Z. Wang, and B. Chi, "A U-Band PLL Using Implicit Distributed Resonators for Sub-THz Wireless Transceivers in 40 nm CMOS," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 67, no. 9, pp. 1574-1578, Sep. 2020.

[46] M. Cui, C. Carta and F. Ellinger, “Two 60-GHz 15-dBm Output Power VCOs in 22-nm FDSOI,” IEEE Microw. Wireless Compon. Lett., vol. 31, no. 2, pp. 184-187, Feb. 2021.
[47] Y. -H. Chang, “Low-Voltage Dual-Band CMOS Voltage-Controlled Oscillator for Ka-Band and V band Applications,” IEEE Microw. Wireless Compon. Lett., early access, doi: 10.1109/LMWC.2021.3097212.
[48] Y.-C. Chiang and Y.-H. Chang, “A 60 GHz CMOS VCO using a fourth-order resonator,” IEEE Microw. Compon. Lett., vol. 25, no. 9, pp. 609–611, Sep. 2015.
[49] Ning Li, K. Okada, T. Inoue, T. Hirano, Q. Bu, A. T. Narayanan, T. Siriburanon, H. Sakane, and A. Matsuzawa, “High-Q inductors on locally semi-insulated Si substrate by helium-3 bombardment for RF CMOS integrated circuits,” Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, 2014, pp. 1-2.
[50] S. Moscato, C. Tomassoni, M. Bozzi, and L. Perregrini, “Quarter-Mode Cavity Filters in Substrate Integrated Waveguide Technology,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 8, pp. 2538-2547, Aug. 2016.
[51] A. Iqbal, J. J. Tiang, S. K. Wong, S. W. Wong, and N. K. Mallat, “QMSIW-Based Single and Triple Band Bandpass Filters,” IEEE Trans. Circuits Systems II: Express Briefs, DOI: 10.1109/TCSII.2021.3055904.
[52] X. Wang, X. Zhu, Z. H. Jiang, Z. Hao, Y. Wu, and W. Hong, “Analysis of Eighth-Mode Substrate-Integrated Waveguide Cavity and Flexible Filter Design,” IEEE Trans. Microw. Theory Techn., vol. 67, no. 7, pp. 2701-2712, July 2019.
[53] T. R. Jones and M. Daneshmand, “Miniaturized Folded Ridged Quarter-Mode Substrate Integrated Waveguide RF MEMS Tunable Bandpass Filter,” IEEE Access, vol. 8, pp. 115837-115847, 2020.
[54] P. Kim and Y. Jeong, “Compact and Wide Stopband Substrate Integrated Waveguide Bandpass Filter Using Mixed Quarter- and One-Eighth Modes Cavities,” IEEE Microw. Wireless Compon. Lett., vol. 30, no. 1, pp. 16-19, Jan. 2020.
[55] Iqbal, A. W. Ahmad, A. Smida, and N. K. Mallat, “Tunable SIW bandpass Filters With Improved Upper Stopband Performance,” IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 67, no. 7, pp. 1194-1198, July 2020.
[56] H. W. Xie, K. Zhou, C. X. Zhou, and W. Wu, “Compact SIW Diplexers and Dual-Band Bandpass Filter With Wide-Stopband Performances,” IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 67, no. 12, pp. 2933-2937, Dec. 2020.
[57] T. R. Jones and M. Daneshmand, “The characterization of a ridged half-mode substrate-integrated waveguide and its application in coupler design,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 11, pp. 3580–3591, Nov. 2016.
[58] T. R. Jones and M. Daneshmand, “Microfabrication of a Miniaturized Monolithic Folded Half-Mode Integrated Waveguide Cavity for W band Applications,” in Proc. IEEE MTT-S Int. Microw. Symp., 2020, pp. 127-130.
[59] M. Bertrand, E. Pistono, G. Acri, D. Kaddour, F. Podevin, V. Puyal, S. T. Wipf, C. Wipf, M. Wietstruck, M. Kaynak, P. Ferrari, “Substrate Integrated Waveguides for mm-wave Functionalized Silicon Interposer,” in Proc. IEEE MTT-S Int. Microw. Symp., 2018, pp. 875-878.
[60] M. S. Mahani and G. W. Roberts, “A mmWave Folded Substrate Integrated Waveguide in a 130-nm CMOS Process,” IEEE Trans. Microw. Theory Techn., vol. 65, no. 8, pp. 2775-2788, Aug. 2017.

[61] C. Hsu, C. Chen, and H. Chuang, “70 GHz Folded Loop Dual-Mode Bandpass Filter Fabricated Using 0.18 μm Standard CMOS Technology,” IEEE Microw. Wireless. Compon. Lett., vol. 18, no. 9, pp. 587-589, Sept. 2008.
[62] C. Hsu, C. Chen, and H. Chuang, “A 60-GHz Millimeter-Wave Bandpass Filter Using 0.18-μm CMOS Technology,” IEEE Electron Device Lett., vol. 29, no. 3, pp. 246-248, March 2008.
[63] L. Yeh, Y. Chen, and H. Chuang, “A novel ultra-compact and low-insertion-loss 77GHz CMOS on-chip bandpass filter with adjustable transmission zeros,” in Proc. 44th Eur. Microw. Conf., Rome, Italy, 2014, pp. 1056-1059.
[64] L. Li, W. Shen, J. Ding and X. Sun, “Compact 60-GHz On-Chip Bandpass Filter With Low Insertion Loss,” IEEE Electron Device Lett., vol. 39, no. 1, pp. 12-14, Jan. 2018.
[65] Y. Xiao, P. Shan, Y. Zhao, H. Sun and F. Yang, “Design of a W band GaAs-Based SIW Chip Filter Using Higher Order Mode Resonances,” IEEE Microw. Wireless Compon. Lett., vol. 29, no. 2, pp. 104-106, Feb. 2019.
[66] N. Jguirim, C. Dalmay, D. Passerieux and P. Blondy, “W band Micro-Fabricated Waveguide Band-Pass Filters,” in Proc. IEEE MTT-S Int. Microw. Symp., 2020, pp. 135-138.
[67] S. K. Thapa, B. Chen, A. Barakat, K. Yoshitomi, and R. K. Pokharel, “X-Band Feedback Type Miniaturized Oscillator Design with Low Phase Noise Based on Eighth Mode SIW bandpass Filter,” IEEE Microw. Wireless Compon. Lett., vol. 31, no. 5, pp. 485-488, May 2021.
[68] J. S. G. Hong and M. J. Lancaster, Microstrip Filters for RF / Microwave Applications. John Wiley & Sons, 2004.
[69] Z. Ge, L. Chen, R. Gómez-García, and X. Zhu, “Millimeter-Wave Wide-Band Bandpass Filter in CMOS Technology Using a Two-Layered Highpass-Type Approach With Embedded Upper Stopband,” IEEE Trans. Circuits and Systems II: Express Briefs, vol. 68, no. 5, pp. 1586-1590, May 2021.
[70] K. Zhou, C. Zhou and W. Wu, “Dual-Mode Characteristics of Half-Mode SIW Rectangular Cavity and Applications to Dual-Band Filters With Widely Separated Passbands,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 11, pp. 4820-4829, Nov. 2018.
[71] M. Li, Y. Yang, K. D. Xu, X. Zhu, and S. W. Wong, “Microwave On-Chip Bandpass Filter Based on Hybrid Coupling Technique,” IEEE Trans. Electron Devices, vol. 65, no. 12, pp. 5453-5459, Dec. 2018.
[72] H. Zhu, X. Zhu, Y. Yang, and Q. Xue, “Design of wideband third-order bandpass filters using broadside-coupled resonators in 0.13-μm (Bi)- CMOS technology,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 12, pp. 5593–5604, Dec. 2018.
[73] K. D. Xu, X. Zhu, Y. Yang, and Q. Chen, “A Broadband On-Chip Bandpass Filter Using Shunt Dual-Layer Meander-Line Resonators,” in IEEE Electron Device Lett., vol. 41, no. 11, pp. 1617-1620, Nov. 2020.
[74] S. K. Thapa, B. Chen, A. Barakat, K. Yoshitomi and R. K. Pokharel, "Miniaturized Slot-Loaded SIW Resonator and Its Application to C-band Low Phase Noise Oscillator," in Proc. 50th European Microwave Conference (EuMC), 2021, pp. 161-164.

LIST OF PUBLICATIONS

❖ Journals/Transactions/Letters

1. **B. Chen**, S. K. Thapa, A. Barakat and R. K. Pokharel, "A W band 0.01 mm² Cavity Resonator Employing Slot-Loaded Shielded Folded Ridged Quarter-Mode in CMOS Technology," *IEEE Microwave and Wireless Components Letters*, doi: 10.1109/LMWC.2021.3122149.
2. **B. Chen**, S. K. Thapa, A. Barakat and R. K. Pokharel, "A W band Compact Substrate Integrated Waveguide Bandpass Filter With Defected Ground Structure in CMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, doi: 10.1109/TCSII.2021.3123655.
3. **B. Chen**, R. K. Pokharel, S. K. Thapa, N. Jahan*, and* A. Barakat, "Design of 50 GHz Low Phase Noise VCO Employing Two-Branches DGS Resonator in 0.18-µm CMOS Technology," *IEEE Microwave and Wireless Components Letters*. (Under review).
4. S. K. Thapa, **B. Chen**, A. Barakat, K. Yoshitomi and R. K. Pokharel, "X-Band Feedback Type Miniaturized Oscillator Design With Low Phase Noise Based on Eighth Mode SIW bandpass Filter," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 5, pp. 485-488, May 2021.
5. N. Jahan, **C. Baichuan**, A. Barakat and R. K. Pokharel, "Utilization of Multi-Resonant Defected Ground Structure Resonators in the Oscillator Feedback for Phase Noise Reduction of K band VCOs in 0.18- µm CMOS Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 4, pp. 1115-1125, April 2020.

❖ Conference/Proceedings

1. S. K. Thapa, **B. Chen**, A. Barakat and R. K. Pokharel, "Millimeter-Wave High Q-factor Sixteenth Mode SIW Cavity Resonator Implemented in 0.18-µm CMOS Technology," IEEE/MTT-S International Microwave Symposium (IMS), 2022. (in press)
2. **B. Chen**, S. K. Thapa, A. Barakat and R. K. Pokharel, "Design Methodology of Wide Tuning Range DGS-based VCO for K band Applications in 0.18-µm CMOS Technology," *16th European Microwave Integrated Circuits Conference (EuMIC)*, 2022. (in press)
3. **B. Chen**, S. K. Thapa, A. Barakat and R. K. Pokharel, "A 100GHz Bandpass Filter Employing Shielded Folded Ridged Quarter-Mode SIW Resonator in CMOS Technology," *51st European Microwave Conference (EuMC)*, 2022. (in press)
4. T. Fukuda, **B. Chen**, S. K. Thapa, A. Barakat and R. K. Pokharel, "Design of Compact and High Q-factor W band Cavity in 0.18µm CMOS Technology," *51st European Microwave Conference (EuMC)*, 2022. (in press)
5. S. K. Thapa, **B. Chen**, A. Barakat, K. Yoshitomi and R. K. Pokharel, "Miniaturized Slot-Loaded SIW Resonator and Its Application to C-band Low Phase Noise Oscillator," *50th European Microwave Conference (EuMC)*, 2021, pp. 161-164.
6. **B. Chen**, N. Jahan, A. Barakat and R. K. Pokharel, "Experimental Study of the Effect of

Interconnects on Phase Noise of K band VCO in 0.18-µm CMOS Technology," *IEEE Asia-Pacific Microwave Conference (APMC)*, 2019, pp. 1670-1672.

7. N. Jahan, **C. Baichuan**, A. Barakat and R. K. Pokharel, "Analysis and Application of Dual Series Resonances for Low Phase Noise K band VCO Design in 0.18-µm CMOS Technology," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1-5.
8. N. Jahan, **C. Baichuan**, R. K. Pokharel and A. Barakat, "A K band VCO Employing High Active Q-factor Defected Ground Structure Resonator in 0.18µm CMOS Technology," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1-5.