Investigation of Si paste for coated solar cell application

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Investigation of Si Paste for Coated Solar Cell Application

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ABSTRACT

Energy crisis has increasingly become a bottleneck restricting the economic development of the international community. Among all kinds of renewable and clean energy sources, solar power is considered to be one of the most promising energy sources. A solar cell is the core device of photovoltaic power generation system. Among all kinds of solar cells, the crystalline Si wafer based solar cell is the most matured and commercialized photovoltaics device. However, the cost of Si wafer which mainly comes from the costly Czochralski Si ingot growth and the kerf loss remains the major barrier that prevent further large-scale installation. In the previous researches, utilizing Si pastes fabricated by planetary ball milling the n- or p-doped Si fragments was one of the simple kerf-less approaches that could skip the ingots growth and sawing process. The Si paste consists of Si nanocrystals owned some extraordinary properties due to the size effect. However, Si paste was found to be oxidized easily even in high purity Ar gas atmosphere due to the high surface to volume ratio of the Si nanocrystals. Hence, this PhD research intended to investigate the oxidation reduction technologies employed on Si paste, while continuing to further improve the Si paste electronic device performance, especially the photovoltaic performance.

There were three topics investigated in this dissertation:

(1) In Chapter 2, the first attempt was to lower the annealing temperature. p- and n-type Si paste films coated on Al and Al-sputtered Fe substrates were annealed at low temperatures to fabricate pn homo-junction devices for development of low-cost solar cell devices. This process based on aluminum-induced-crystallization (AIC) which enabled one to recrystallize Si paste films with reduction of residual tensile stress while suppressing oxidation even at low temperatures (400 to 550°C). The current-voltage characteristic of the pn homo-junction device using the Si paste films showed

rectification with the on/off current ratio of about 3200 and the reverse current density of the order of 10^{-9} A/cm^2 at room temperature. The photocurrent of 0.058 μA/cm^2 in the pn homo-junction diode under AM1.5 illuminations was observed.

(2) In Chapter 3, the second attempt was rapid thermal annealing (RTA). RTA was conducted in order to recrystallize the Si paste. It was possible to minimize the oxidation during the melting process of Si nanoparticles with RTA even at 1200°C in 1 s. Lowering of the melting temperature appeared to be due to the size effect and release of surface energy from the Si nanoparticles. RTA was conducted in an infrared furnace with temperatures varying from 1150 to 1300°C. Si pn homo-junction structure was also fabricated by coating p-type followed by n-type Si pastes on a carbon substrate. Typical rectifying characteristics and slight photo-induced current of 10 μA/cm^2 was observed.

(3) In Chapter 4, the third attempt was to introduce a layer of material that was more susceptible to oxidation. In order to reduce the oxidation of Si paste during the RTA, Ti was deposited on the p-type Si paste since the Gibbs' free energy of Ti oxidation was smaller than Si oxidation. It was found that the RTA condition of 1200°C/2 s enabled the Si paste to obtain the least oxidation and the best crystallization conditions as well as the transformation of the Ti layer into rutile TiO_2 phase. It was observed that some molten Si grain lumps appeared on the surface of the sample annealed at 1200°C for 2 s. This phenomenon was due to the melting process of the surface Si particles promoted by the Ti layer. Typical rectifying characteristic with a photocurrent density of 36 μA/cm^2 was observed with the TiO_2/p-Si paste heterojunction device annealed at 1200°C for 2 s.

In conclusion, this dissertation presented significant progress in oxidation reduction technologies as well as the advancement of photovoltaic performance for Si paste. Together with detailed explanations of the underlying fundamentals, the results

presented in the dissertation are expected to shorten the gap between c-Si wafer and Si paste. It is expected that after adopting the oxidation reduction methods introduced in this investigation, the Si paste will be regarded as an alternative raw material for manufacturing the low-cost coated solar cells which will be beneficial to the large installation of photovoltaic system in the future human society.

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CHAPTER 1:

Introduction

With the continuous rapid development of global industrialization, the economy as well as our human society, the demand for energy is dramatically increasing. At present, more than 80% of the world's energy supply comes from fossil fuel energy [1–3]. However, these fossil fuel energy sources, including coal, oil, and natural gas, are not only non-renewable sources, but the continuous use of these fossil fuel energy sources will also cause the ecological damage [4–8] which have become an important factor hindering the realization of sustainable development of human society.

In all kinds of renewable energy, such as solar energy [9], wind energy [10], water energy [11], geothermal energy [12] and so on, solar energy has a greater potential due to no geographical restrictions and an abundant energy reserve. It is estimated [13] that the annual solar radiation received by the Earth's surface of 120,000 TW (1.2×10^{17} W), exceeds 8,000 times mankind's total primary energy supply (TPES).

Generally, there are two basic approaches to take advantage of solar energy, namely, photovoltaic (PV) electricity, and solar thermal electricity [14]. Among them, PV is considered to be the most feasible and effective way for the photoelectric direct conversion.

1.1. Photovoltaic (PV) industry

Solar cells have come a long way since a French physicist A.E. Becquerel's discovery in 1839 [15]. It was found that the electrical currents were generated from a silver coated platinum electrode immersed in an electrolyte under the light. This

discovery laid the theoretical foundation of the photovoltaic technology today. The so-called photovoltaic effect is a phenomenon in which an electrical potential difference is generated at combination regions between semiconductor materials that are exposed to light. Then the researchers (D.M. Chapin, C.S. Fuller, and G.S. Pearson [16]) at Bell Laboratory in the U.S. successfully developed a practical crystalline silicon (c-Si) solar cell based on pn junction technology (with an efficiency of about 6%) in 1945. Since then, with the technological breakthroughs in solar cells, the photoelectric conversion efficiency has continued to rise while the costs have been continuously falling. Nowadays, a variety of PV technologies, using different materials, device structures and manufacturing processes, are commercially available on the PV market, and more are being developed in laboratories all around world.

According to the type of raw materials and the development history of solar cells, there are three main categories of solar cells. The first type of solar cells is c-Si solar cells [17], which include monocrystalline Si and polycrystalline Si solar cells. The c-Si solar cells are usually made of highly-purified solar-grade Si wafer (purity is above 99.9999% or referred as "6N") as a raw material with a photoelectric conversion efficiency of typically more than 25%, as shown in the Fig. 1.1 [18]. Due to the relatively matured manufacturing process and stable performance, the c-Si solar cells still occupy more than 90% of the whole PV market share [19], However, the complicated manufacturing processes and the high price of the raw material (c-Si wafer), still limit the large-scale installation of the c-Si solar cells.

The second type of the solar cells is known as the thin-film solar cells, which mainly include amorphous Si (a-Si) [20], copper indium gallium selenide (CIGS) [21] and cadmium telluride (CdTe) [22] solar cells. The a-Si solar cells have lower cost and high conversion efficiency, but the performance of the cells is not stable. If the stability problem is solved and the conversion efficiency is further improved, they will be a

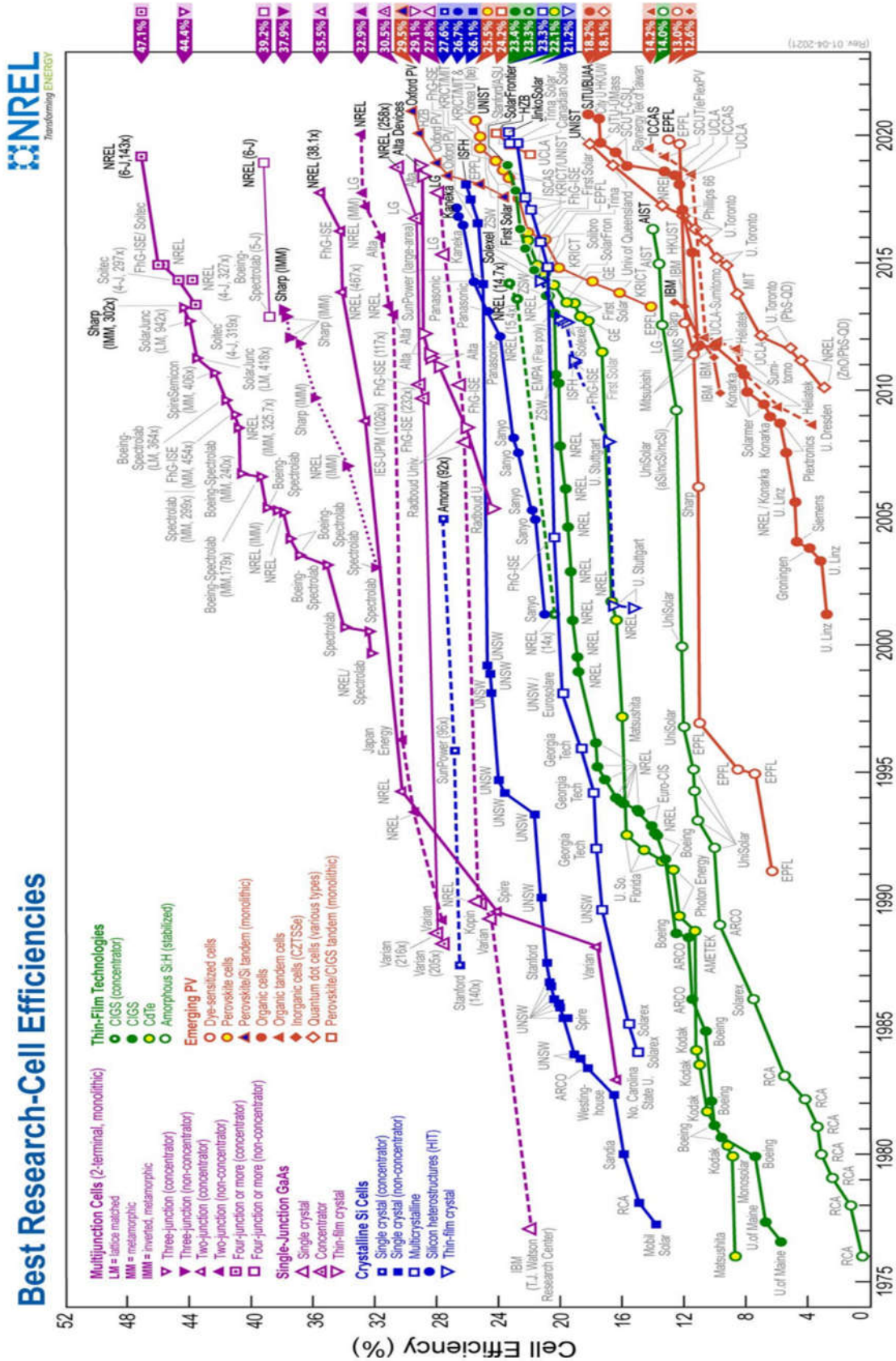

Fig. 1.1 Efficiency of various certified solar cells by National Renewable Energy Laboratory (NERL, 1976~2020) [18].

strong competitor to the high-cost c-Si solar cells. As for the CIGS solar cells, the photoelectric conversion efficiency is close to that of polycrystalline Si solar cells, and the highest certified photoelectric conversion efficiency has reached 23.4%, as shown in Fig. 1.1. However, the main problem of the CIGS cells is the expensive elements, such as indium and selenium. The highest photoelectric conversion efficiency of the CdTe solar cells is verified as 22.1%, as shown in Fig. 1.1. Nevertheless, the main disadvantages are the toxic element cadmium, and the poor performance stability. Furthermore, another remarkable feature of the thin film solar cells is flexibility. At present, the flexible thin film solar cells have been applied to many fields, such as rechargeable backpacks and mobile chargers.

The second law of thermodynamics [23] states that not all of the energy absorbed by any object can be converted into work, so there is a theoretical conversion efficiency limit for solar cells. For single-junction solar cells, the theoretical maximum conversion efficiency is about 30%, which is also known as the Shockley-Queisser limit [24]. Thus, the birth of the emerging solar cells, such as dye sensitized solar cells (DSCs) [25–27], quantum dot sensitized solar cells (QDSCs) [28–30], organic solar cells (OPVs) [31–32] and perovskite solar cells (PSCs) [33–35], further improves the theoretical efficiency, but they are still in the laboratory development stage.

1.2 Crystalline Si wafer based solar cells

1.2.1. Development of crystalline Si wafer based solar cells

The c-Si wafer based solar cells have the most matured manufacturing process and long term performance stability. Therefore, the c-Si wafer based solar cells still remain the mainstream production in the whole cell market for decades, as shown in the blue bars of Fig. 1.2 [19].

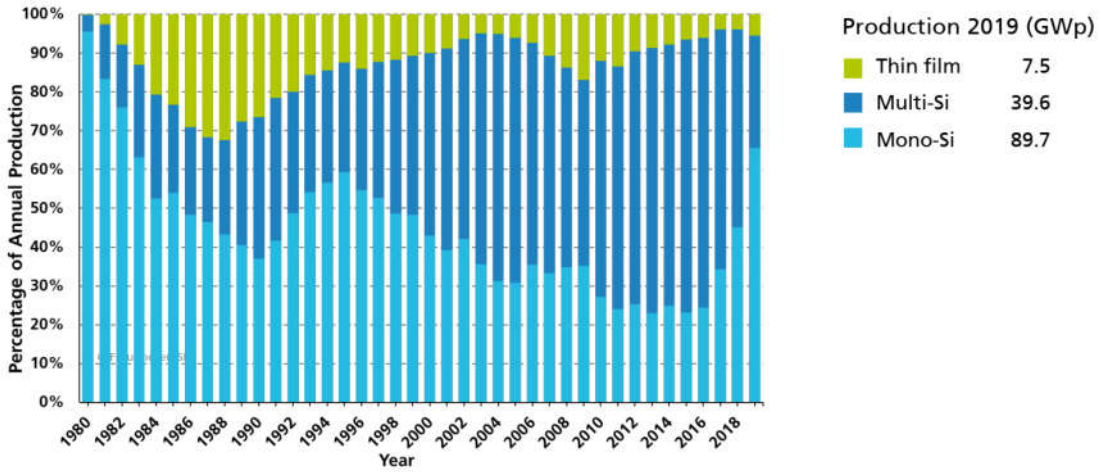

Fig. 1.2 Percentage of global annual solar cell production [19].

The first development period of the c-Si wafer based solar cells began with the first monocrystalline Si solar cell invention. Subsequently, the c-Si solar cells was applied when the USA launched the first satellite using a PV power supply in 1958 [36]. Over the next decade, the application of the c-Si wafer based solar cells in the space field continued to expand, the manufacturing technology continued to improve, and the design of the cell gradually finalized. However, during this period, the use of the c-Si wafer based solar cells did not extend to the ground applications.

The second period began in the early 1970s, driven by the oil crisis and lower energy source costs, the c-Si wafer based solar cells were first introduced for ground applications, not just in the space field. By the end of 1970s, the production of c-Si solar cells in the ground application field exceeded the production of space cells, and the cost continued to decrease. During this period, c-Si wafer based solar cells began a vigorous development. Not only many new types of solar cells appeared, but also many new technologies were introduced. For example, (1) the back surface field (BSF) technology [37–38]: the same doping type but heavily doped region called back surface field was introduced into the back contact area of the solar cells, which increased the cells' short circuit current due to improved collection performance near the contact area,

furthermore, the back field could reduce the saturation current, thus improving the open circuit voltage and increasing the efficiency. (2) The surface texturing technology [39–40]: due to the anisotropic corrosion rate of the lattice plane, the surface of the c-Si was corroded into pyramid morphology by the alkali solution. The adapted textured surface was the key factor to reduce the reflectivity, so as to enhance the absorption of incident light and improve the output power of the solar cells. (3) Surface passivation technology [41–43]: in the fabrication process of a c-Si wafer based solar cells, a large number of defect states, surface state and impurities in Si bandgap formed the excess energy level and became recombination centers, these centers trapped light generated carriers, thus reducing the efficiency. To overcome these drawbacks, the dielectric layers such as silicon oxide, silicon nitride, aluminum oxide, were fabricated on the Si surface, acting as the carrier-selective passivation layers to prevent the surface recombination of the carriers. There were also other technologies, such as the grid metallization [44], shallow junction [45], and so on, which also improved the efficiency of the c-Si wafer based solar cell in this period.

In the early 1980s, the c-Si wafer based solar cells entered their third period of rapid development. The main features of this period were applying the combined technologies appeared in the second period to fabricate the high-efficiency c-Si solar cells. For example, the local back surface field (LBSF) solar cells [46] fabricated by the Fraunhofer Solar Energy Institute in German has adopted the technologies of the passivation oxide layer, the surface texturing as well as the boron-diffused local BSF under the rear point contacts. The structure of the LSBF c-Si solar cell was shown in Fig. 1.3. The efficiency of the 2cm×2cm LSBF c-Si solar cell reached 23.3%. In this period, the efficiency of the c-Si wafer based solar cells has been significantly improved, the cost of commercial production has been further reduced, and the application has been expanded.

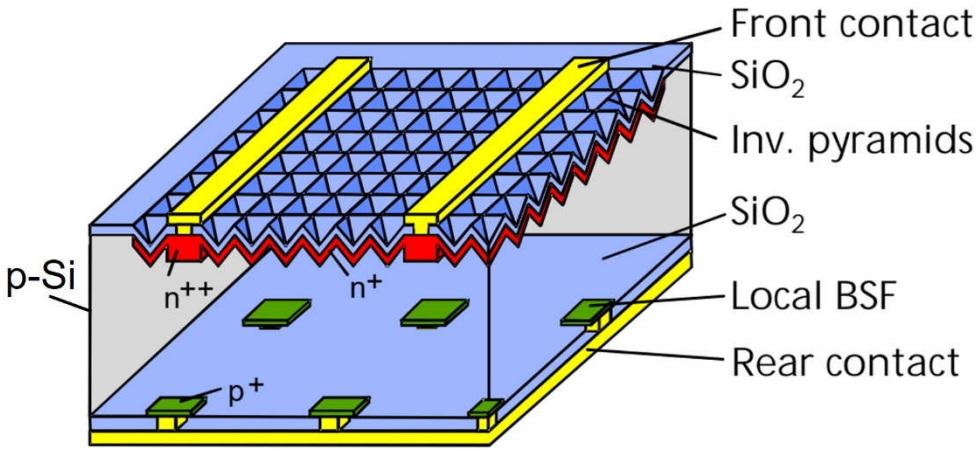

Fig. 1.3 Structure of local back surface field (LBSF) c-Si solar cells [46].

1.2.2. Crystalline Si wafer based solar cells

The basic principle of the c-Si wafer based solar cells is based on the photovoltaic effect of semiconductor pn junction. The pn junction consists of p-type Si and n-type Si. The p-type Si is the Si doped with acceptor impurities, such as boron (B), aluminum (Al) and gallium (Ga). The n-type Si is made by doping donor impurities, such as nitrogen (N), phosphorus (P) and arsenic (As) into the Si.

The pn junction formation process is illustrated by Fig. 1.4. When the p-type Si is in contact with n-type Si, the difference in the concentration of carriers (electrons and holes) on both sides of the pn junction will drive the carriers on each side to diffuse from the side with high concentration to the lower concentration side. Thus, the electrons with high concentration in the n-type Si diffuse to the p-type Si, while the holes with high concentration in the p-type Si diffuse to the n-type Si. After the diffusion process of the majority carriers, those dopant element ions that cannot move will be left to form a positive ionization donor in the n-type region, namely the positive charge region. A negative ionization acceptor, the negatively charged region, is formed in the p-type region. Thus, the regions of the ionization donors and ionization acceptors at the interface form the space charge region called the depletion region. Because the polarity

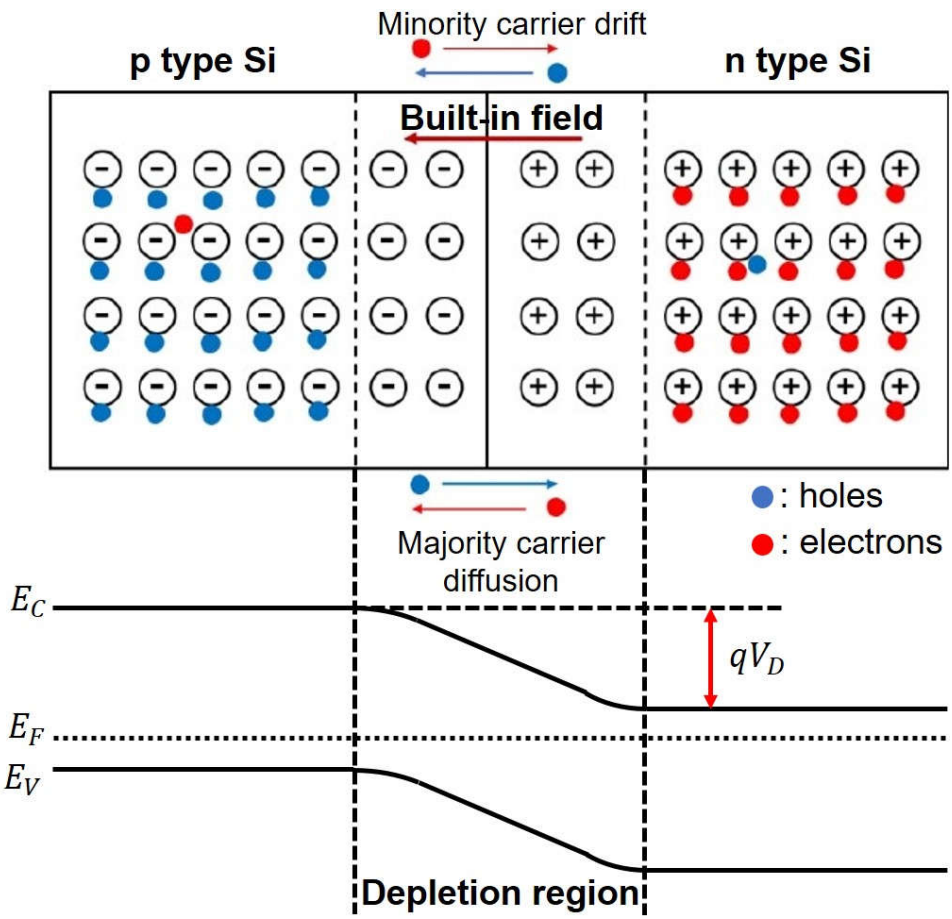

Fig. 1.4 Schematic diagram of the pn junction formation.

of the two sides of the pn junction is different, a built-in electric field (qV_D) is generated from the n-type Si region to the p-type Si region. Since the direction of the built-in electric field is opposite to the diffusion direction of the majority carriers, the diffusion motion is impeded, while the built-in field will also drive the minority carriers to drift, namely, the electrons in p-type Si region will drift to n-type Si region, and the holes in n-type Si will move oppositely. Eventually, the diffusion motion of the majority carriers and the drift motion of the minority carriers will reach dynamic equilibrium, forming the stable pn junction.

If a forward bias V is applied on the pn junction, that is opposite to the built-in field, then the potential barrier or the built-in field will be decreased to $q(V_D - V)$. With the increasing forward-bias voltage, the current increases slowly and the curve

obtained is non-linear as the voltage applied to the diode is overcoming the potential barrier. Once the depletion region eventually become narrow enough that the built-in field cannot block the diffusion motion of the majority carriers, which as a consequence that diode behaves as a normal resistor and the current rises sharply as the external voltage increases and the I-V curve obtained is linear.

The strength of the built-in electric field will be increased to $q(V_D + V)$, if a reverse bias is applied on the pn junction. The increase of the voltage barrier causes a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the pn junction. The increase in resistance of the pn junction results in the junction, behaving as an insulator.

Therefore, the pn junction in the c-Si solar cell behaves like a normal diode without illumination, the current flowing through the pn junction diode, which is called the dark current I_D can be described by the Shockley equation eq. (1-1) [47]:

$$I_D = I_s \left\{ exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1 \right\} \tag{1-1}$$

where I_s represents the reverse saturation current, k is the Boltzmann constant, T refers to the absolute temperature, q is the electron charge, n is the diode ideality factor, and R_s is a series resistance due to the resistivity of the electrode contact and the material itself.

When the continuous light irradiates the pn junction, as shown in Fig. 1.5, according to the theory of photoelectric effect proposed by Einstein, the semiconductor material absorbs the photon with an energy of $h\nu$ greater than its bandgap E_g, thus excite electrons in the valence band to the conduction band, leaving a hole in the valence band. The built-in electric field in the pn homojunction will separate the photogenerated

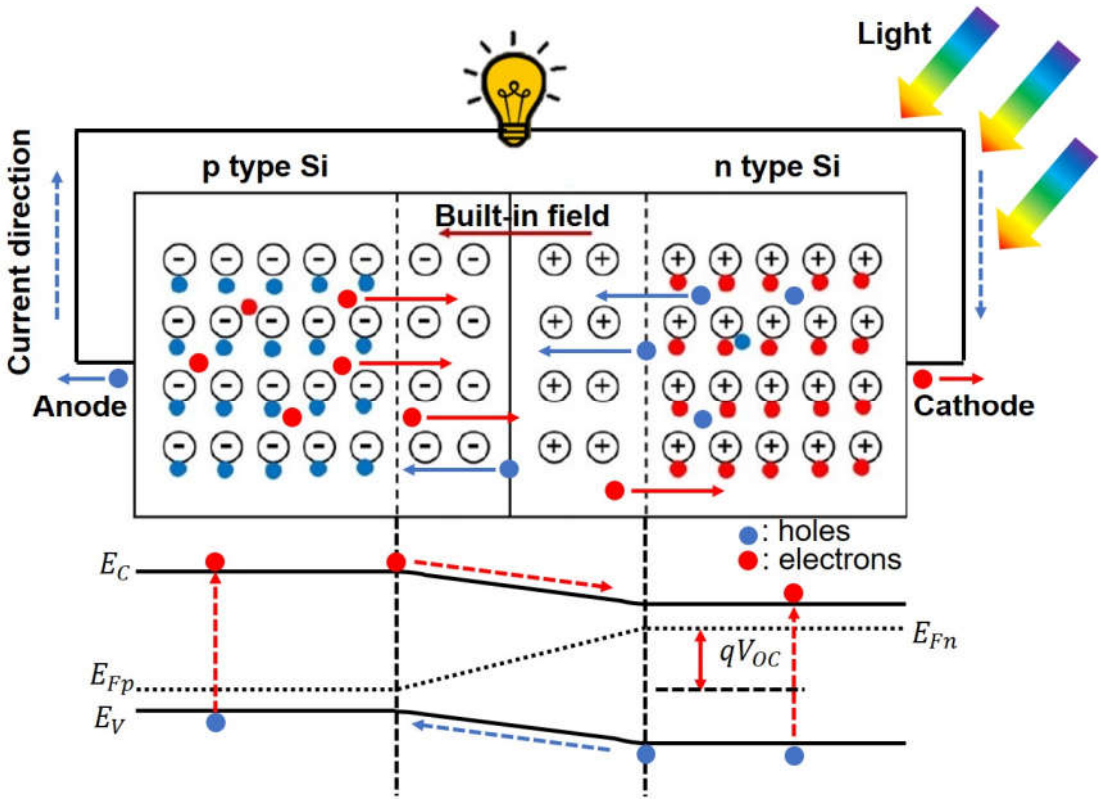

Fig. 1.5 Schematic diagram of the pn junction under illumination.

carriers and drive them to opposite directions. During continuous illumination, a large number of photogenerated carriers move towards p and n sides, forming the two so-called quasi-Fermi energies E_{Fn} and E_{Fp}. The accumulated holes on the valence band of p-Si and the accumulated electrons on the conduction band of n-Si form the difference of electrical potential, namely, the open-circuit voltage V_{OC}. When Ohmic contacts and an external circuit are connected to pn junction, the generated electrons are swept in the n-type side by the built-in field, then eventually recombine with holes at the p-type side. When the external circuit of a pn junction is shortened, the current generated in the external circuit is called short-circuit current I_{SC}.

In the ideal case, the solar cell model can be equivalent represented by a constant current source connecting with an ideal diode in parallel [48], as shown in Fig. 1.6. The current of constant current source I_L, is the photogenerated current, R_L is the load, and the current flowing through the load is I. Nevertheless, in practice, there will be a

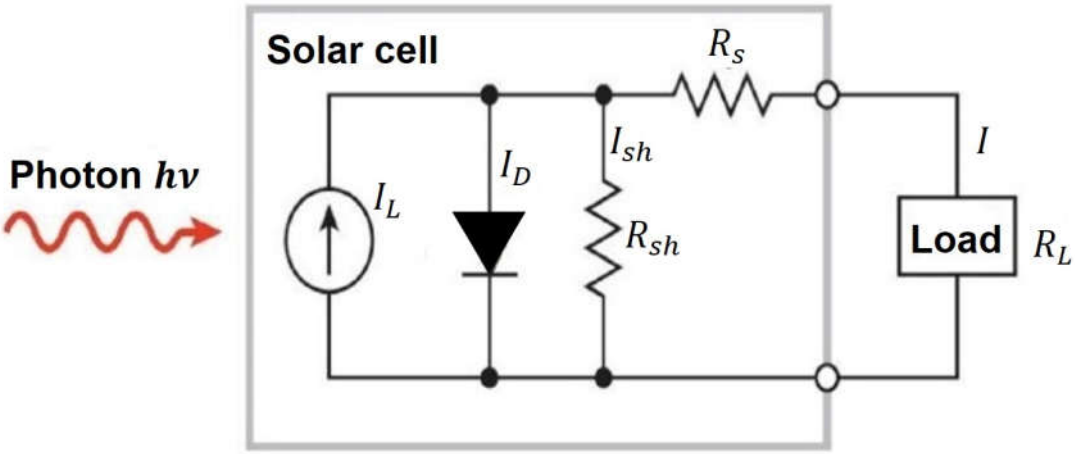

Fig. 1.6 Equivalent circuit of the ideal solar cell.

parasitic shunt resistor R_{sh} due to the leakage at the edge of the solar cell and the leakage of the metal electrode. According to the equivalent circuit diagram, the I-V characteristic equation of the pn junction of the solar cell under illumination can be obtained:

$$I = I_L - I_D - I_{sh} = I_L - I_s\left\{exp\left[\frac{q(V-IR_s)}{nkT}\right] - 1\right\} - \frac{V+IR_s}{R_{sh}} \tag{1-2}$$

The I_{sh} part is usually ignored because the parasitic shunt resistor R_{sh} are extremely large, and I_{sh} approaches 0.

Consequently, the I-V curve of a pn junction diode (marked with Dark) shifts downward by an interception of I_L, and then we get the I-V curve of a solar cell under illumination, as shown in Fig. 1.7. The open-circuit voltage V_{OC} and the short-circuit current I_{SC} directly derived from the I-V curve are the key parameters to characterize the performance of solar cells. The V_{OC} depends on the saturation current which is mainly related to the recombination of the cells. Therefore, the V_{OC} indirectly reflects the recombination condition of the solar cells. In the actual manufacturing process, the

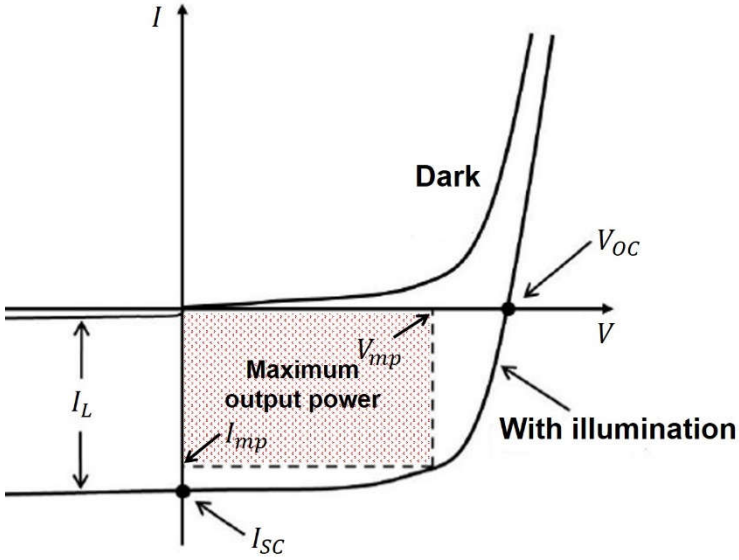

Fig. 1.7 I-V curve of a solar cell without (marked with Dark) or under illumination.

surface passivation technology is used to effectively reduce the surface recombination, so as to further increase the V_{OC}. The I_{SC} reflects the number of photogenerated carriers produced and collected by the solar cell under illumination. The maximum output power:

$$P_{max} = I_{mp} \times V_{mp} \tag{1-3}$$

can be found somewhere in between the V_{OC} and the I_{SC} points of the I-V curve. Fill factor (FF) is another important performance parameters for the solar cells which can be expressed in the following formula:

$$FF = \frac{V_{mp} \times I_{mp}}{V_{OC} \times I_{SC}} \tag{1-4}$$

The FF represents the maximum power output performance of the solar cells under the optimal load condition. In practice, the most intuitive parameter to measure the

quality of a solar cell is the conversion efficiency of the device, that is, the maximum energy conversion of the solar cell after normal load connection. The most important parameter of a solar cell is called the photoelectric conversion efficiency (η), which is described as:

$$\eta = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}} \times 100\% \tag{1-5}$$

where the P_{in} represents the input light power. The photoelectric conversion efficiency (η) directly evaluates the performance of a solar cell.

1.2.3. Manufacture process of crystalline Si wafer

The c-Si wafer is known as the most basic and important raw material for manufacturing the c-Si solar cell. The most conventional fabrication process of the pn junction for solar cells is forming the n-type layer by the diffusion of a phosphorus (P) source into the surface portion of the p-type Si wafer [49]. The quality of the c-Si wafer directly affects the performance of the solar cells.

In nature, the silica-rich sands typically contains large amounts of impurities. So the initial stages of the manufacturing process are concerned with reduction and purification of the silica sand to produce metallurgical grade (MG) polysilicon through the carbothermic reduction [50],

$$SiO_2 + 2C \longrightarrow Si + 2CO \tag{1-6}$$

The purity of the producing MG Si is typically 98% or 99%. The second step is to purify MG Si to electronic grade (EG) polycrystalline Si chunks. The standard method

in this step is called the Siemens process [51], the MG Si is converted into volatile compounds by the chemical reaction, next purified by the fractionation, then reduced to obtain EG Si:

$$\mathrm{Si\ \ (MG) + 3HCl \longrightarrow SiHCl_3 + H_2} \tag{1-7}$$

$$\mathrm{SiHCl_3 + H_2 \longrightarrow Si\ \ (EG) + 3HCl} \tag{1-8}$$

The EG polycrystalline Si chunks has impurities in the low parts per billion (ppb) range or less, a necessary requirement for production of semiconductor devices. The next step is the growth of mono c-Si from the EG polycrystalline Si chunks. Nowadays, there are two different matured techniques for the mono c-Si growth in the industrial production, namely, the Czochralski (CZ) and the floating zone (FZ) growth method [52]. They are both well established for the growth of dislocation free Si single crystals. However, due to the high cost and the size limitation of the product, FZ method occupies much smaller share in the c-Si market, while the CZ method accounts for more than 95% of the total mono c-Si production [52].

The flow chart of the CZ method is shown in the Fig. 1.8. During the CZ method, the EG polycrystalline Si chunks are placed into a crucible (typically made of quartz [52]) and heated to about 1500°C, it will make the Si melt (melting point: 1414°C). If the dopant elements, such as B and P are accurate quantitative mixed with molten Si, it will become a p-type Si or n-type Si, respectively. When the Si chunks is completely melted, a rod of mono c-Si, or so-called "seed crystal Si stick" is slowly immersed into the molten Si. The rod rotates counterclockwise and the crucible rotates clockwise. Then, the rod is gradually lifted up, so that a nearly cylindrical Si ingot can form below. By continuously lifting rod, this c-Si ingot length can reach 1~2 meters, depending on the amount of molten Si in the crucible. If the temperature gradient, the rate of lifting,

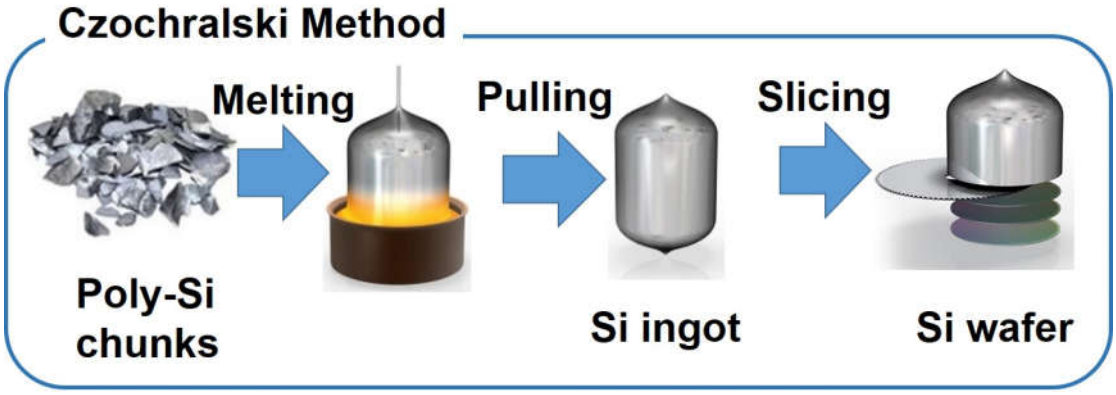

Fig. 1.8 Schematic diagram of Czochralski (CZ) method for manufacturing the c-Si wafer.

and the rate of rotation of the rod are precisely controlled, a large, cylindrical mono c-Si ingot can be obtained at the end of the rod.

Although the above processes are usually carried out in an inert gas (e.g. argon) atmosphere, due to the thermal decomposition of the quartz crucible, an inevitable result is that the molten Si will be mixed with oxygen with a concentration of typically in the order of 10^{18} cm^{-3} [53]. Nevertheless, a moderate amount of oxygen impurities will provide some benefits. The oxygen can trap unnecessary transition metals in the c-Si and improve the mechanical strength of Si wafers by pinning dislocations introduced in the manufacturing process [54].

The final c-Si wafer manufacturing process is the slicing of the c-Si ingot. Two slicing methods have been used in the c-Si wafer industry: the internal diameter (ID) saw [55] and the wire saw [56]. The ID saw method uses the inner circular blade inlaid with diamond particles as the sawing tool, as shown in Fig. 1.9 (a) [57]. This method is simple, convenient, flexible, and low risk, but the efficiency is low, the raw material loss is large. While the wire saw method as shown in Fig. 1.9 (b) [58] uses a steel wire attached with a silicon carbide (SiC) slurry for sawing, showing the higher sawing efficiency and the potential for lower kerf losses by using thinner wire.

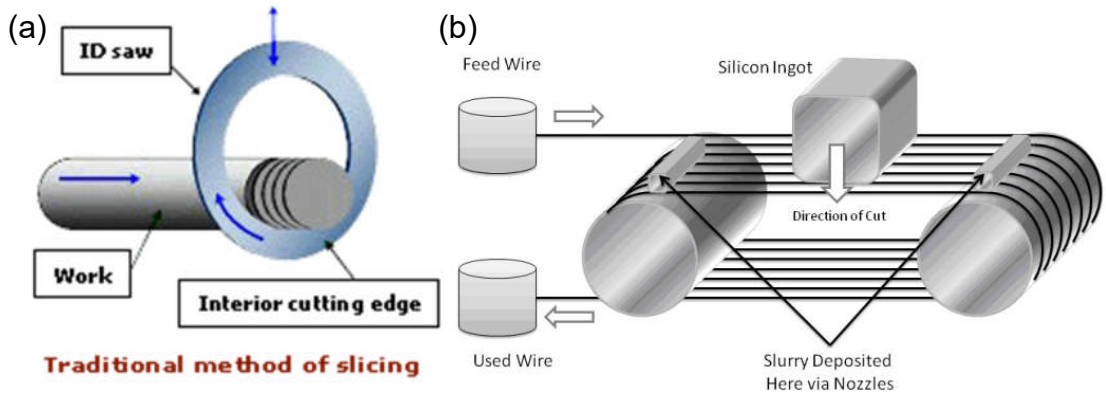

Fig. 1.9 Schematic diagram of (a) ID saw [57] and (b) wire saw [58].

1.2.4. Existing problems of crystalline Si wafer based solar cells

Although the manufacturing technology and the process of the c-Si wafer based solar cells are relatively mature, the manufacturing process of the c-Si wafer, namely, the Czochralski (CZ) is cumbersome, the pulling up and growth process of a c-Si ingot takes as long as 10~12 days, furthermore, during the slicing process, a large amount of saw dust called kerf loss is generated, it is estimated that the kerf loss is a fundamental result of any sawing process. There is currently 40–50% kerf loss for 180-200 μm thick wafers, lower wafer thickness slicing can even increase the kerf loss to ~70% [59]. It is also estimated that the c-Si wafer accounts for nearly half of the final solar cell module costs [60]. To achieve grid parity, the industrial solar cells modules must be mass produced at a price level of less than \$1/W_p (W_p, the peak power under standard test conditions) with a total system price of \$2/W_p, so as to be competitive with non-renewable energy source, such as coal or nuclear [61]. However, the lowest cost for a c-Si wafer based solar cell module today is still above \$1/W_p [62].

In order to reduce the raw material loss during the slicing process, many kerf-less approaches have been developed in the past few decades.

(1) The most industrialized kerf-less wafering methods is the solidification of the liquid phase Si. The main advantage is the faster effective deposition rates making 20

μm to 300 μm wafer thicknesses readily achievable in mass-production. In this way, the ribbon growth on substrate (RGS) method [63] which is the direct solidification of molten Si onto high-temperature substrates such as ceramic. The edge-defined film-fed growth (EFG) and string ribbon (SR) methods [64] which are the direct crystallization processes from the Si melt, have been developed. The process of the EFG method is shown in the Fig. 1.10. The capillary action drives the molten Si to a slit at the center of the die to form a liquid Si film. When a seed crystal Si is touched to the liquid Si film and lifted up, a mono c-Si forms at the interface between the seed crystal Si and the liquid Si film. By continuing to pull the seed crystal Si upwards, the mono c-Si grows and finally matches the shape of the die.

However, the high defect density caused by the rapid crystallization in these methods as well as the increased contamination in the products prevent these liquid phase Si crystallization methods from being applied on a large scale installation.

(2) Another attempt called the direct film transfer (DFT) technology has been developed by SiGen company [65]. It is a solid phase Si wafering process. This process uses 2-step implant-cleave method as shown in the Fig. 1.11. The high-energy ion light

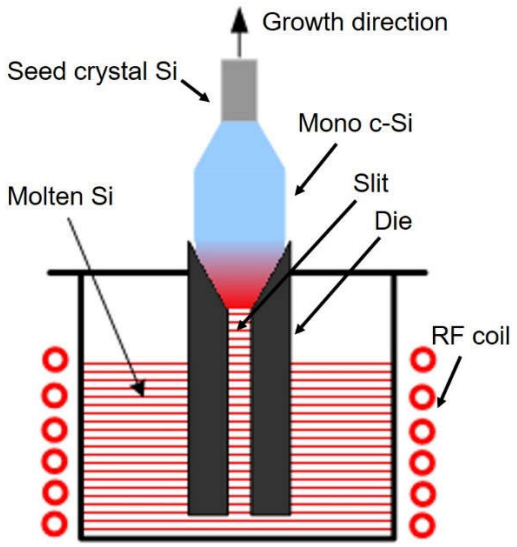

Fig. 1.10 Schematic depiction of the edge-defined film-fed growth (EFG) method [64].

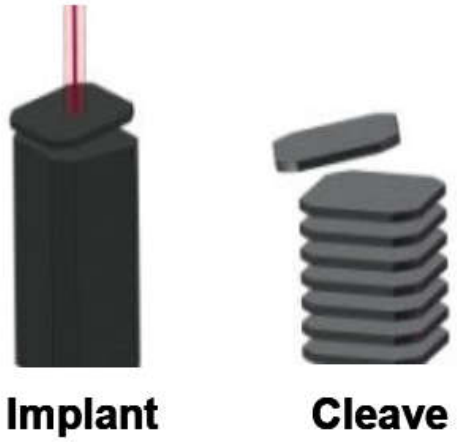

Fig. 1.11 Schematic diagram of the direct film transfer (DFT) method [65].

irradiation first forms a cleave plane followed by advanced controlled cleaving to initiate and propagate a fracture plane in a controlled manner along the cleave plane to release a large-area wafer from a shaped ingot. However, this method is still under laboratory development, and the introduction of the high energy light irradiation would increase the internal stress.

1.3. Dissertation objectives

Nowadays, the human society are mainly powered by fossil fuel energy, however, the fossil fuel shortage and the environmental problems follow closely. Solar energy is considered to be the most promising way to solve the current problems. The c-Si wafer based solar cells are the most matured and widely used commercial products to convert solar energy into electrical energy in the present market, but the cost of making a Si wafer is the biggest barrier to prevent further large scale installation. Nearly half of the cost comes from the slicing and the long-time mono c-Si growth process in the CZ method. Reduction of production cost of the c-Si solar cell is required so as to make the solar energy more cost-competitive with the conventional non-renewable or other renewable sources of energy.

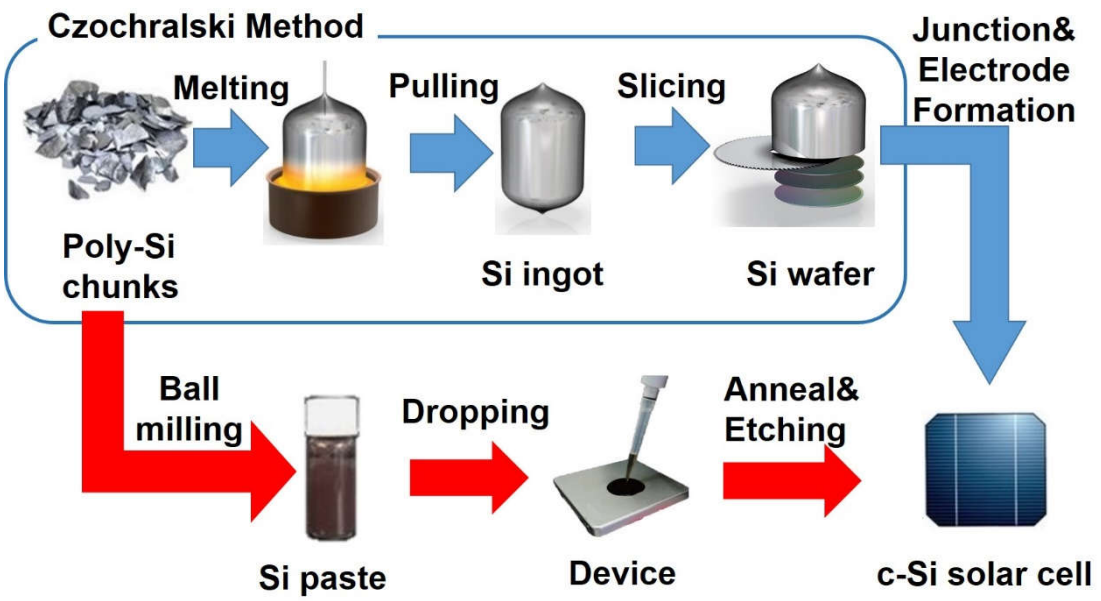

Fig. 1.12 Schematic diagram of solar cell fabrication, showing the possibility that ingot growth and wafering steps could be skipped with the novel Si-paste method.

In the previous researches [66–67], utilizing Si pastes fabricated by solar-grade polycrystalline Si chunks instead of the c-Si wafer, was one of the simple approach to eliminate the kerf-loss by skipping the ingots growth and slicing process. The preparation process of the c-Si solar cell by the Si paste compared with the conventional process is shown in Fig. 1.12. The Si chunks were only required to be crushed to the nanoscale by ball milling, and the resulting Si powder is mixed with organic solution to produce the Si paste.

There are also some similar works concerning the Si paste [68–71]. They have developed a method of making Si ink by plasma and applied this technique for making low-cost photovoltaics device. However, these reports were still based on c-Si wafer. Instead of fabricating a solar cell by Si paste only, the Si ink was just printed on the surface of a normal c-Si wafer based solar cell to enhance the efficiency by back-surface field (BSF) effect. On the contrary, in this research, not only the preparation method of Si paste was low-cost but also the whole device was fabricated by Si paste only.

It has been already estimated that the cost of our Si paste (24 mL), was roughly $2

[67], our experiment suggested that ~0.02 mL of Si paste could cover an area of 1×1 cm^2. The typical commercial c-Si solar cell unit has a cell size of around 240 cm^2. Hence, one bottle of Si paste could fabricate 2.5 solar cell units, and cover 600 cm^2. Therefore, the cost in our case is approximately \$0.0033/cm^2. Commercial solar cells with general photoelectric conversion efficiency $\eta = 20\%$ often cost money by generating power, nowadays, it is estimated as \$1.31/W_p [72]. If we assume the maximum power output of Si paste device reaches only 0.005 W/cm^2 (photoelectric conversion efficiency $\eta = 5\%$) in the future, the cost for our device will be about \$0.66/W which is much less than that of commercial one.

Up to now, we have made such a solar cell by the aforementioned steps and succeeded to observe typical rectification I-V characteristics but limited output power for photovoltaic performance. After all characterizations being analyzed, it could be concluded that the serious oxidation and high defect density contributed to the high resistance and conversion efficiency degradation. Hence, in order to realize the fabrication of the low-cost c-Si solar cells with high performance by Si paste, the current objectives in this thesis are reducing the oxidation during the thermal treatment process and further optimizing the device structure.

1.4. Outline of this dissertation

The general preparation procedures of the Si pastes are introduced in the experimental part of Chapter 2, while all the characterization methods employed in this research are separately introduced in the experimental part of Chapter 2–4. Besides, most of the results of this PhD thesis have been published in peer-reviewed journals or in the leading international conferences.

The annealing process of the Si pastes plays a key role in the fabrication of devices

such as pn junction. However, it has been concluded that the oxidation of the Si paste mainly came from the annealing treatment, although the whole annealing process was conducted in the ambient inert atmosphere (Ar). Hence the optimization of the annealing process parameters, including the annealing temperature, annealing duration, and so on, is the most effective way to reduce the oxidation.

Therefore, Chapter 2 concentrates on low temperature annealing combined with aluminum induced crystallization (AIC) technology. In this way, the targets of both the reduced oxidation and the reasonable crystallization quality can be achieved. In this chapter, the effect of annealing temperature on the Si paste device performance is also studied.

Chapter 3 discusses the rapid thermal annealing (RTA) technology. RTA is an alternatively method for reducing oxidation due to the extremely short annealing duration. Besides, the annealing temperature in RTA process can reach higher than the conventional annealing process, thus, it may have unexpected beneficial effect on the crystallization condition and the microstructure of the Si paste. In this chapter, the effect of RTA on the structure and performance of the Si paste device is studied.

Another approach is considered to change the normal pn homojunction structure of the Si paste diode device. It is known that there are some other elements, such as Al, Ti, Ca, and so on, react with oxygen more preferentially than Si. Hence, in Chapter 4, a Ti film is deposited on the p-type Si paste surface as an oxidation sacrifice layer. During the annealing process, the Ti layer reacts preferentially with the surrounding oxygen atoms, furthermore, Ti can also react with native SiO_2 through reduction reaction to form TiO_2. In this chapter, the performance of TiO_2/p-Si paste heterojunction device is studied.

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CHAPTER 2:

Low Temperature Annealing of Nanocrystalline Si Paste for pn Junction Formation

2.1. Introduction

Si, as one of leading electronic materials, is widely employed in almost every aspect of electronic industries due to the high material quality and widespread technological know-how [1, 2]. Unlike the computer industry, the large-area electronic devices such as liquid crystal displays and solar cells can endure larger feature sizes even by using lower quality Si instead of high-quality c-Si wafers [3]. In order to lower the manufacturing cost, several high-throughput manufacturing techniques such as deposition of a-Si films and dropping Si paste made of Si nanocrystals dispersed in solvents that can be adopted [4]. However, the use of a-Si films tends to degrade performance of electronic devices because of a relatively low carrier mobility of ~0.5 $cm^2/V{\cdot}s$ [5], thus limiting its application. Besides, chemical vapor deposition as the typical manufacturing technique of a-Si films costs high because of requirement of vacuum equipment [6].

Utilizing Si paste fabricated by Si nanocrystals is another feasible approach for fabricating the large area electronic devices, such as the low-cost coated solar cells instead of c-Si wafer. The Si paste composed of Si nanocrystals also owns some excellent electrical properties similar to single crystal c-Si [7]. The nanocrystalline Si is considered to be a low conductive phase surrounded by an amorphous phase, its conductivity is much higher than amorphous phase due to an enhanced upward shift of

the Fermi level permitted by the reduction in the tail-state width.

In our previous study, an attempt was made to fabricate a whole device using both p- and n-type Si pastes without using a c-Si wafer [8]. The resulting pn homojunction diode showed rectification characteristics only when the doped Si pastes were annealed at a temperature of 1100°C for enhancing crystallization. However, the Si paste composed of Si nanocrystals was found to be oxidized easily even in high purity 6N Ar gas atmosphere due to the high surface to volume ratio. Therefore, it is still desired to develop an annealing technique at lower temperatures for suppressing oxidation fundamentally. It is known [9] that the oxidation level of a c-Si as well as the thickness of SiO_2 layer decreases with the decrease of annealing temperatures, as shown in the Fig. 2.1. So lowering the annealing temperature can be an effective approach to reduce the oxidation of Si paste during the annealing process.

Metal-induced crystallization is a promising process to crystallize an amorphous Si (a-Si) film at temperatures below 600°C by using metal species such as Au, Al, and

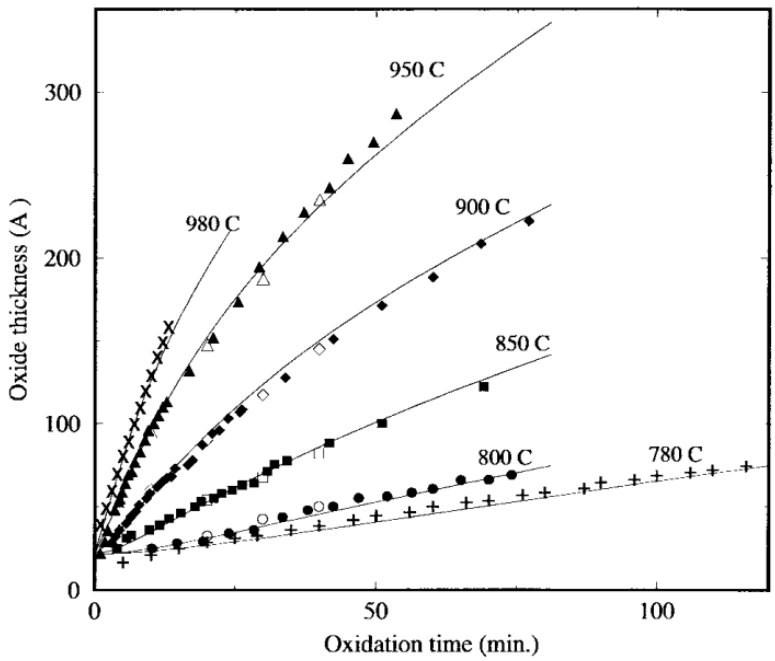


Fig. 2.1 Oxidation level of Si under various temperatures [9].

Ni [10]. Al is considered to be most favorable because it plays a multiple role such as back contact electrode and BSF in solar cells [11]. Nast et al. showed that, after low temperature annealing of an a-Si film on an Al layer at 600°C or less, a c-Si film appeared under the Al layer [12]. Additionally, Si grains started nucleation primarily at the Al/a-Si interface, where the Al grain boundaries met the reduction of the free energy [13]. This aluminum-induced-crystallization (AIC) process is illustrated in Fig. 2.2.

In the step 1 of Fig. 2.2, it involves the diffusion of Si atoms into the Al layer. According to the Al/Si binary phase diagram [14], as shown in the Fig. 2.3, adjacent Al and Si layers are not in thermal equilibrium at elevated temperatures, and up to 1.5 at.% of Si can be dissolved in Al layer at temperatures below the eutectic temperature 577°C [14]. Thus, the partial dissolution of Al or the native Si oxide interlayer of a-Si occurs at the beginning. During this initial interaction, the native oxide interlayer is transformed by the Al into a mixture of Al oxide and Al silicide phase. Both Al oxide and Al silicide phase can be considered to provide an interface diffusion channel for both Al and Si atoms [12]. The step 2 depicts the diffusion of Si atoms within the Al layer after passing through the interface diffusion channels between Al layer and native Si oxide layer. There are 3 typical diffusion channels for Si atoms in this stage, diffusion inside the Al grains, diffusion along the Al grain boundaries, and diffusion along the

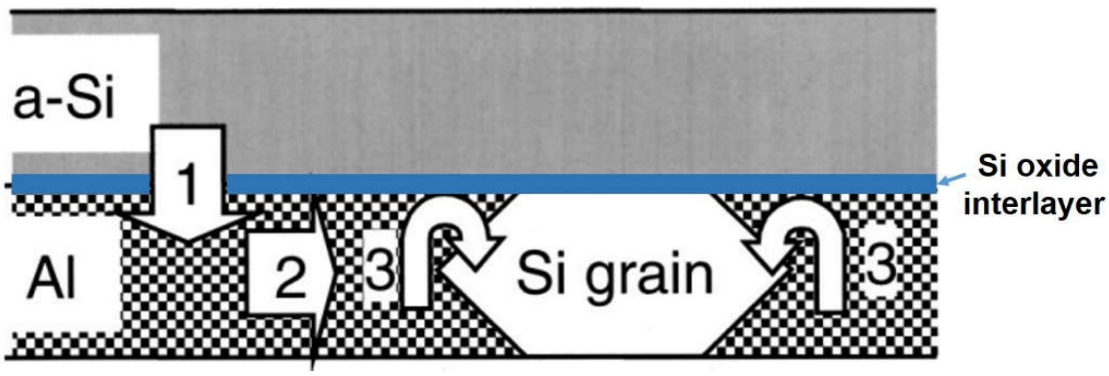


Fig. 2.2 Schematic diagram of the diffusion and interface processes involved in the grain growth during AIC [12].

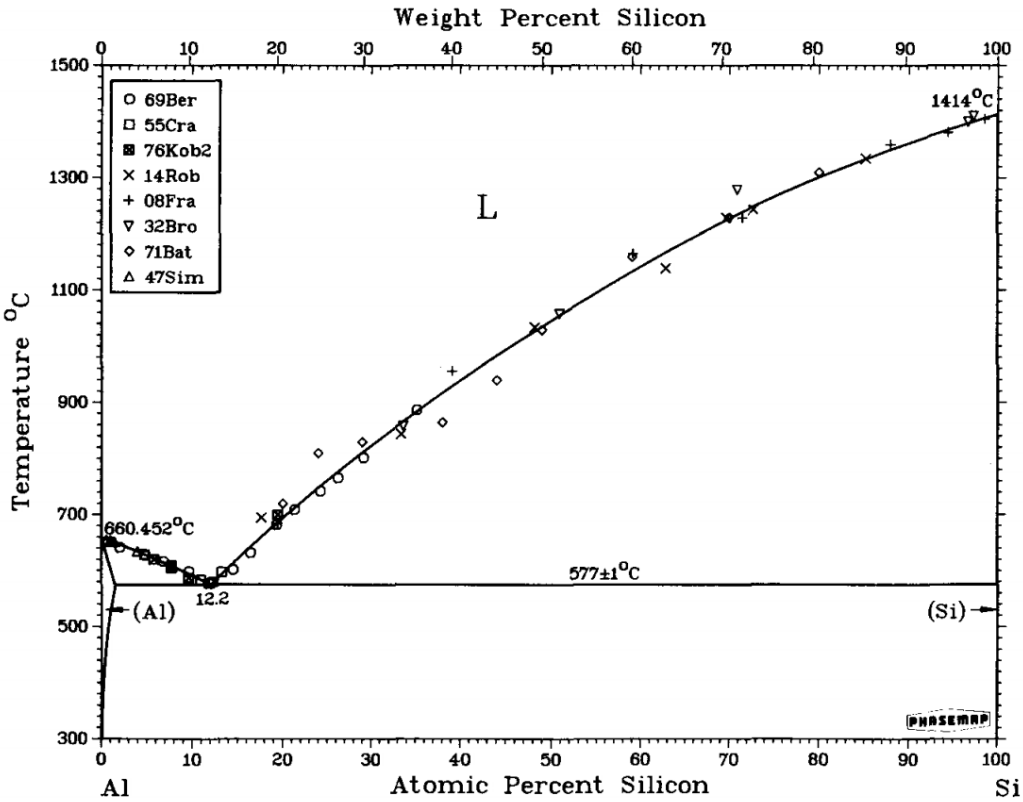


Fig. 2.3 Phase diagram of Al-Si binary system [14].

interface. As the step 2 continues, Si atoms diffuse within the Al layer and gather together to form a Si cluster. Once the size of this Si cluster reaches the critical nucleation size, the Si nuclei forms. Then, the actual incorporation of the dissolved Si atoms into the newly formed Si nuclei will occur, as illustrated in the step 3. Step 3 is faster than step 1 and 2 because of the incoherent interface between the Al matrix and the Si crystal [15]. Then, the Si crystal growth in the AIC technology can be considered as a diffusion-controlled process.

If the Si crystal growth within the Al layer proceeds into the amorphous Si layer, it will involve direct phase transformation of the Si atoms from the amorphous into the crystalline phase in the manner of seeded solid-phase crystallization [12]. However, it is found that during the low temperatures annealing (typically below 600°C), this direct phase transformation process is much slower compared to the diffusion controlled Si

crystal growth process of AIC. The Si atoms dissolved in the Al layer, have a higher mobility and, hence, diffuse faster within the Al layer and along the interfaces towards the growing Si grains, while the mobility of Si atoms within the a-Si layer is much slower at temperature lower than 600°C [16]. Therefore, it can be concluded that at low temperature, the Si crystallization mainly attributes to the diffusion-controlled AIC process.

In this chapter, the process based on AIC was utilized for enhancing recrystallization of Si paste films at low temperatures to suppress oxidation and improve rectification characteristics of the pn junction diodes using the Si paste.

2.2. Experimental methods

2.2.1 Milling procedures of Si pastes

For the preparation of p and n-type Si pastes, the c-Si fragments from commercially available c-Si (100) wafers with resistivity of 6.5–7.3 mΩ·cm and 13–16 mΩ·cm for p-type (boron doped, 10^{19} cm^{-3}) and n-type (antimony doped, 6×10^{18} cm^{-3}), respectively, were used as Si paste sources. It should be noted that both the p- and n-type Si source materials were heavily doped in order to achieve the Ohmic contact with Al layer and Ag electrodes in the following steps. The first step is hand grinding in a mortar. The c-Si fragments were ground to powder in this step. It has been found that the grinding atmosphere had influence on oxidation, the grinding process was performed in a glove box filled with protective 6N nitrogen gas. For one 24 ml Si paste preparation, 1 g Si powder with 24 ml of acetonitrile (AN) solution were transferred into a ZrO_2 milling pot with 50 g ZrO_2 milling beads (2mm ϕ). Other solvent, such as ethanol, has also been tested, however, the resistance of the Si paste using ethanol was much higher than the Si paste using acetonitrile (AN) solution. In addition, 1.5 ml of

acetyl acetone (acac) was also added to the Si paste. It has been reported that the acac could be used to stabilize ZrO_2 and to form non-aggregated particles [17]. Therefore, the purpose of the acac addition was to prevent aggregation of nanocrystal Si (nc-Si) particles in the Si pastes, considering their large surface to volume ratio and thus the high tendency to stick together.

The second step was pulverizing Si fragments by planetary ball milling (PBM) process using a ball miller (Fritsch Pulverisette7) with a rotation speed of 500 rpm for one hour. This ball milling condition has already been optimized to achieve finer Si particles in the Si pastes. In advance of PBM process, the air inside the milling pot was replaced with 6N Ar gas to inhibit the oxidation during the high energy ball milling process. The shape of the ball miller and the milling mechanism are shown in the Fig. 2.4 [18]. The milling pots were placed on a sun-wheel which rotates clockwise, while the milling pot self-spun in the opposite direction. The Si particles and the milling beads were pushed towards the wall of the milling pot by the centrifugal force. By means of

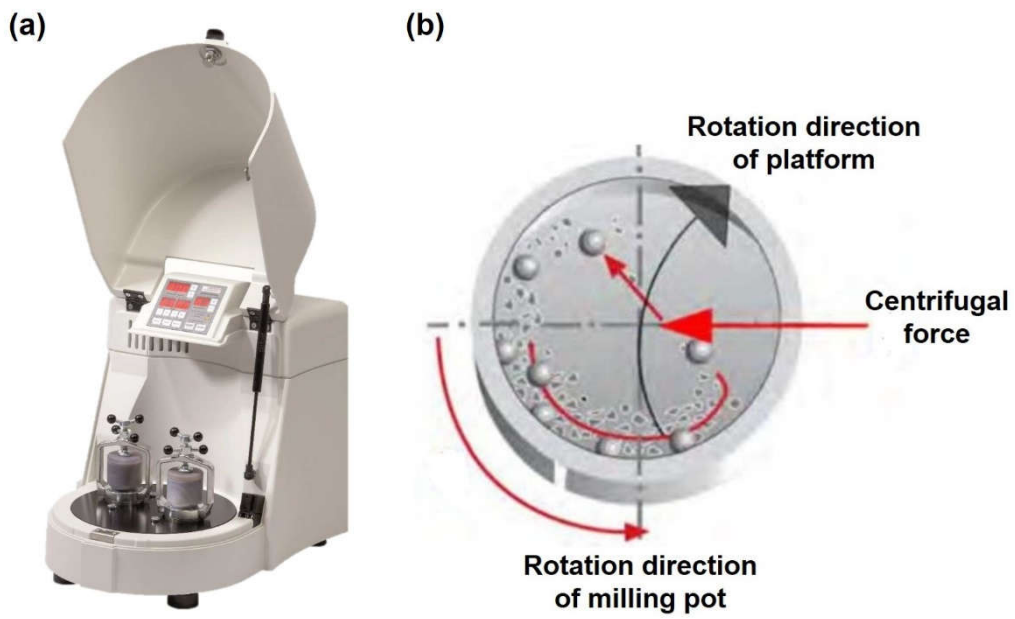


Fig. 2.4 (a) Photo of the planetary ball miller (Fritsch Pulverisette7) used in this research; (b) schematic diagram of mechanism of planetary ball milling (PBM) process [18].

the physical collision and friction, the Si particles would be crushed into nano-sized powders. Since the PBM process took advantage of centrifugal acceleration instead of the conventional gravitational acceleration and was regarded as high energy ball milling method, thus achieving even finer powders than that of the conventional ball milling process [19]. Finally, a sieve was used to remove the ball milling beads, then the Si paste was transferred into a reagent bottle in the nitrogen gas filled glovebox. The as-received mixture was the Si paste for subsequent experiments.

The ball milling process shows many advantages, including cost-effectiveness, reliability, ease of operation, reproducible results due to energy and speed control, applicability in wet and dry conditions. Therefore this method has already been widely employed in industrial mass production of various materials (e.g. cellulose, chemicals, fibres, polymers, hydroxyapatite, metal oxides, pigments, catalysts) [20]. So it is expected that the ball milling method can be also adopted in the future mass production of Si paste. Since the semiconductor devices such as solar cell is very sensitive to the contamination within the Si, there is a concern in crushed ZrO_2 (from milling beads and pot) mixing into the Si paste. However, according to the EDS results of all the Si paste samples, the presence of Zr element has not been observed. Besides, the mass of the ball milling bead did not reduce after 3 time ball milling experiments (the new beads have usually been recycled twice). However, the recycling frequency of the beads should be further studied to avoid the mixing of impurities for the future mass production.

2.2.2 Si paste device preparation by low temperature annealing

Two kinds of substrates, that is, Al and Al-sputtered Fe with a size of 10×10 mm^2, were used. Fe was used here as a substrate because of lower cost and higher hardness,

which are beneficial to pressing process to form a denser Si layer. Prior to sputtering of Al, the Fe substrate was ultrasonically cleaned in ethanol. The substrate was placed on a sample holder in a vacuum chamber, which was evacuated to a base pressure of 4×10^{-4} Pa. The flow rate of Ar gas (99.9999%) was set at 30 sccm. Then, a layer of Al with a thickness of around 100 nm was deposited on the Fe substrate by using magnetron sputtering at 3.0 Pa. After the sputtering, two types of junction device were fabricated using the Si paste. First, 20 μl of p- and n-type Si pastes were sequentially coated on the Al substrate. Second, 20 μl of n-type Si paste was only coated on the Al substrate. All Si paste films were naturally dried in a N_2 filled glove box. In order to reduce the internal porosity of the Si paste films, pressing was applied using an oil hydraulic presser at a load of approximately 13 kN. For subsequent annealing treatment, the Si paste films were placed in a quartz tube of 52 cm in length and 1.4 cm in inner diameter with flowing 6N Ar gas at a rate of 0.7 L/min at atmospheric pressure. The films were then annealed in a conventional tubular furnace at 400, 500 and 550°C for 3 h. After the annealing, the films were etched with 3 wt. % HF solution for 1 min to remove the native oxide. Finally, electrodes were formed on the films using silver paste.

During the annealing process, it is necessary to pay attention to the Fe-Al and Al-Si binary systems. As for the Fe-Al system, as shown in the Fig. 2.5 [21], when the temperature is elevated to 400~550°C, Al does not melt, but a small amount of Al atoms may diffuse into Fe lattice, so only the lower left region of the Fe-Al phase diagram needs to be considered.

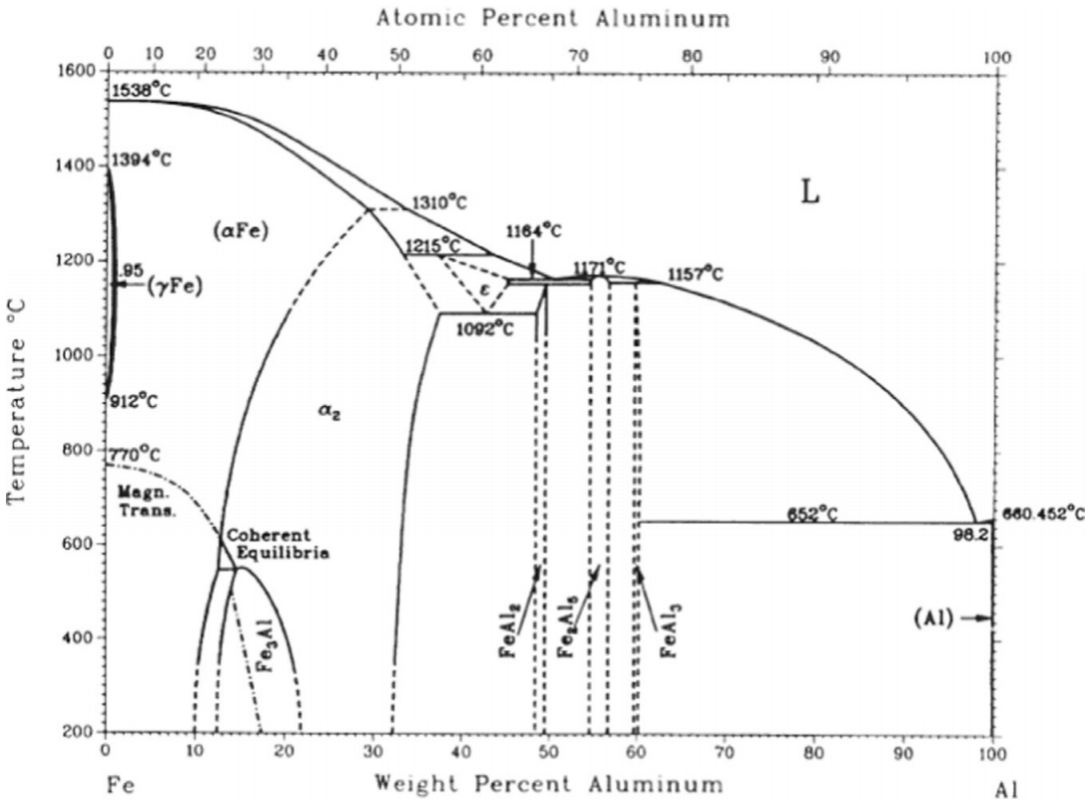


Fig. 2.5 Phase diagram of Fe-Al binary system [21].

2.2.3 Characterization of Si paste and its device

(a) Fourier-transform infrared spectroscopy (FT-IR)

FTIR is utilized for evaluating the oxidation level of Si pastes after annealing process. It is manifested as the change of the light intensity with the wavelength or the wavenumber, mainly including the positions of spectral peaks and intensity distribution, etc. The spectra must be generated under the following conditions: the initial state of energy level has a corresponding distribution, and the transition from the initial state to the final state is allowed. The infrared light accounts for only a small part of the whole electromagnetic wave range, with the wavelength range of 0.75–1000 μm (refer to the wavenumber range 13333–10 cm^{-1}). The infrared spectrum is equivalent to the molecular vibration spectrum [22]. The spectrum is generated by the change of the internal motion mode of the molecule. When the molecular energy state transitions, it

absorbs or emits a certain amount of energy (i.e., photons with frequency ν), and the Bohr frequency condition [23] states that these energies and the photon frequency should satisfy:

$$\Delta E = h\nu = E'' - E' \tag{2-1}$$

where the E'' and E' represents the final energy state and initial energy state, respectively. The precondition of generating infrared spectrum is that molecules must have permanent electric dipole moment, so the monatomic molecules, such as He, Ne, and homonuclear diatomic molecules, including O_2, N_2, H_2 do not have infrared spectrum. Infrared light can be divided into three parts: near infrared, middle infrared and far infrared, in which near infrared light (0.75–2.5 μm) corresponds to the transition between atomic energy levels and the vibrational spectral range in the molecular vibration diffuse region, the mid-infrared (2.5–25 μm) corresponds to the transition between molecular rotational and vibrational energy levels, and the far-infrared (25–1000 μm) corresponds to the transition between molecular rotational energy levels.

The FT-IR spectrometer has the characteristics of convenient operation and fast analysis speed, which can be applied to real-time measurement. It is mainly used to measure the interferogram of the sample and use the Fourier integral transform to transform the interferogram. Figure 2.6 [24] shows the photo and the internal structure of the FTIR spectrometer (PerkinElmer Spectrum Two) used in this research, in which the Dynascan interferometer is its core component. The incoming infrared light interferes after passing through the interferometer, so that a set of interferogram signals can be detected by the detector, and then the restored infrared spectrum can be obtained by using the Fourier integral transform of this interferogram signals.

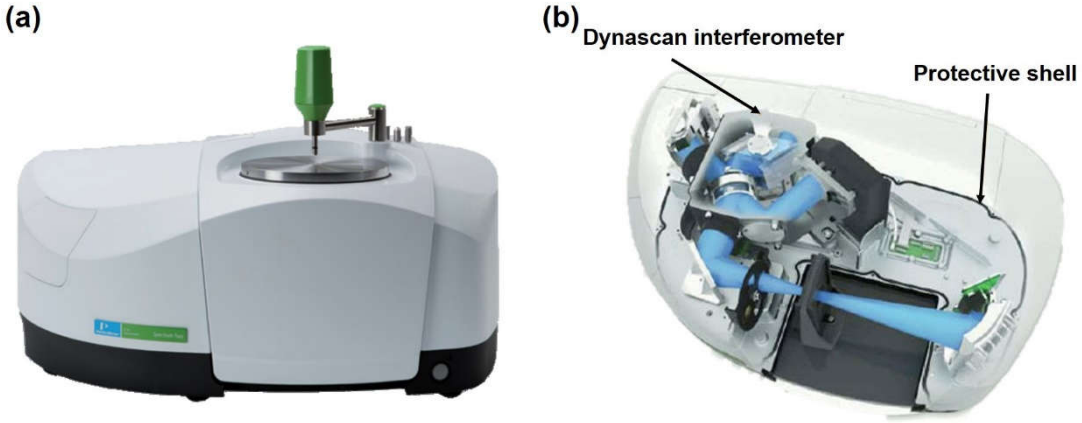


Fig. 2.6 (a) Photo of FT-IR spectrometer (PerkinElmer Spectrum Two) used in this research; (b) internal structure of FT-IR machine [24].

In this study, the Si-Si bond is not infrared-active, so it does not appear in the IR spectra. On the other hand, the Si-O bond, as shown in the Fig. 2.7, can absorb infrared radiation. There are typically three absorption peaks corresponding to various Si-O transverse-optic (TO) vibrational modes. They are the asymmetrical stretching mode (AS) located at 1000-1200 cm^{-1}, symmetrical stretching mode (SS) centered at 800.0 cm^{-1}, and rocking mode (R) [25–27]. The lowest frequency TO band is located around 450.0 cm^{-1}, attributed to the out-of-plane rocking of O atoms [28].

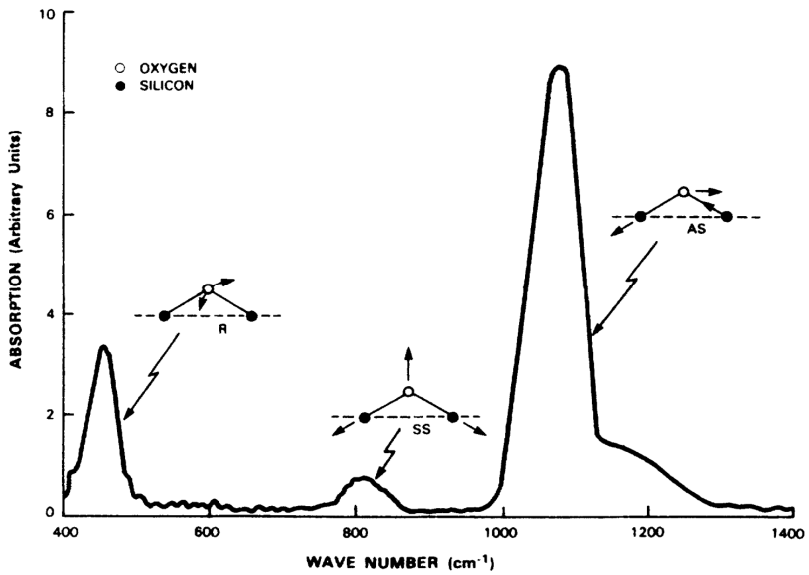


Fig. 2.7 Infrared spectrum of thermally grown amorphous SiO_2 [28].

(b) Raman spectroscopy (Raman)

Raman spectrum is a scattering spectrum. When a beam of incident photon with a frequency of ν_0 has the inelastic collision with the sample molecules, in the scattering spectrum, the scattered light with a frequency same as the incident light is called the Rayleigh scattering. The spectral lines whose frequencies are symmetrically distributed on both sides of ν_0 are called Raman spectra, in which the lower frequency $\nu_0 - \nu_1$ part is also called the Stokes scattering, while the part with higher frequency $\nu_0 + \nu_1$ is called anti-Stokes scattering. The intensity of the Raman spectrum is only about 10^{-9}–10^{-7} of the intensity of the incident light.

Under normal circumstances, since most molecules are in the ground state, the intensity of the Stokes scattering is much stronger than that of the anti-Stokes scattering, so in general Raman spectral analysis, only the Stokes scattering is used to identify the Raman shift. The Raman shift only depends on the energy level structure of the molecule, and its range is 25–4000 cm^{-1}.

The intensity of Raman spectrum is directly proportional to the intensity of incident light and the concentration of sample molecules, so the Raman spectrum can be used for quantitative analysis. In the direction perpendicular to the laser incident direction, the luminous flux (ϕ_R) of Raman scattered light that can be expressed by [29]:

$$\phi_R = 4\pi\phi_L \cdot A \cdot N \cdot L \cdot K \cdot \sin^2(\theta/2) \tag{2-2}$$

where, ϕ_L is the luminous flux of the incident light irradiating on the sample; A is the Raman scattering coefficient, approximately 10^{-29}–10^{-28} mol/sr; N is the number of molecules per unit volume; L is the effective volume of the sample; K is the coefficient taking into account the influence of refractive index and sample field effect; θ is the angle of the Raman beam in the direction of the focusing lens. Consequently,

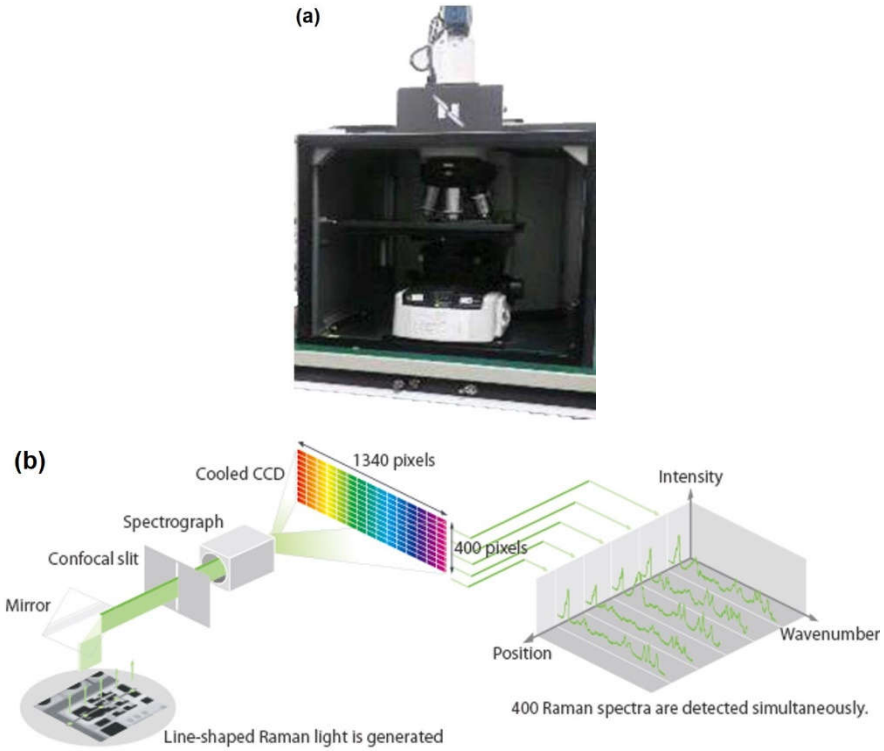


Fig. 2.8 (a) Photo of Raman spectroscopy (Nano-photon RAMAN touch) used in this research; (b) structural diagram of Raman spectroscopy [30].

The Raman analysis can be used to analyze the structure and concentration of samples.

The Raman spectroscopy used in this research is model RAMAN touch manufactured by Nano-photon using a 532 nm-wavelength excitation laser. The photo and the structural diagram of the Raman spectroscopy are shown in Fig. 2.8 [30]. The whole Raman spectroscopy system consists of mirror, confocal slit, spectrograph, and cooled charge coupled device (CCD). Raman is used to examine the crystallinity of the Si paste films in this research.

(c) X-ray diffraction (XRD)

The X-ray diffractometer used in this research is the model Rigaku Ultima IV, using a Cu Kα radiation (λ=1.54 Å). The photo of the X-ray diffractometer and the mechanism diagram of XRD are shown in Fig. 2.9 [31].

When a high-energy electron beam bombards a Cu target to produce X-rays, this

X-ray has a specific wavelength corresponding to the target element, which is called the characteristic X-ray. Considering the X-ray wavelengths is close to the interplanar spacing of a crystal. When a beam of monochromatic X-ray incident to a crystal, since crystals are composed of unit cells with regular arrangement of atoms, and the distance between these regularly arranged atoms is of the same order of magnitude as the wavelength of the incident X-ray, therefore, the X-rays scattered by the different atoms interfere with each other and produce strong X-ray diffraction in some specific directions. The distribution and the intensity of the diffraction lights are related to the crystal structure which is the basic principle of the XRD [32].

In 1913, British physicists W.H. Bragg and W.L. Bragg put forward the famous formula as the basis of crystal diffraction, the Bragg's equation:

$$2d \sin\theta = n\lambda \tag{2-3}$$

where, θ is the incident angle, d is the interlanar spacing, n is the diffraction order, λ is the wavelength of the incident X-ray. All the phases of the atomic diffraction wave

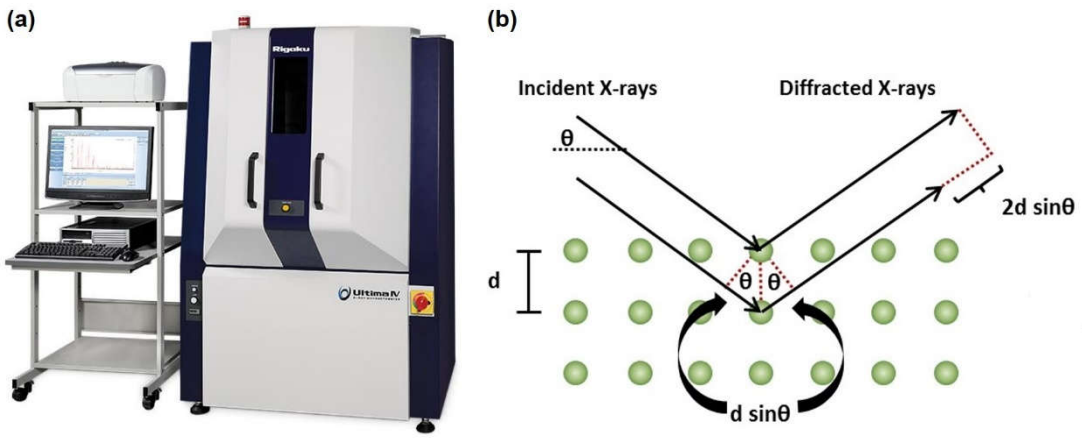


Fig. 2.9 (a) Photo of the X-ray diffractometer (Rigaku Ultima IV) used in this research [31] and (b) the mechanism diagram of XRD.

on crystal lattice planes satisfying the Bragg's equation are exactly the same and their amplitudes reinforce each other. Thus, diffraction peaks appear in the 2θ direction, while elsewhere they cancel each other out.

At the same time, the width of the peaks in the XRD pattern is related to the grain size. The smaller the grain is, the diffraction peak will become diffuse and wider. The Scherer's equation describes the relationship between the grain size and the full width of half maximum (FWHM) of the diffraction peak:

$$D = \frac{K\lambda}{\beta \cos\theta} \tag{2-4}$$

where, K is the Sherrer constant, when β is the FWHM of the diffraction peak, $K = 0.89$, and when β is the integral width of the diffraction peak which is defined as the integral area of a peak divided by the peak height, $K = 1$ [33]. θ is the diffraction angle, λ is the X-ray wavelength, and D is the grain size.

(d) Field emission scanning electron microscope (FE-SEM)

The surface morphology and element distribution of the Si paste films are observed by the model Hitachi SU6600 and SU8000, equipped with an energy dispersive X-ray spectrometer (EDX, Apollo XLT SDD), while the SU8000 has higher scanning resolution. The photos of the SEM and the structural diagram of SEM are shown in Fig. 2.10 [34].

The SEM system is mainly composed of three parts, namely vacuum system, electron beam system and imaging system. The basic working principle [35] of SEM is to focus a high-energy electron beam, and the focused electron beam is used to scan the sample. The inelastic collision will happen when the high-energy incident electrons

bombard the surface of the valence electrons on the sample surface. The incident electrons will lose a part of energy (30–50 eV) during the collision, this part of the lost energy will continue to excite the nucleus of the atomic electrons, when the electron obtains enough energy to overcome the material's work function, it will be separated from the atom and become free electrons in vacuum, which is called secondary electron, the most important SEM signal. The main surface topography information in SEM is carried out with the help of the secondary electron signal, because the secondary electrons escaping into the vacuum are very sensitive to the surface condition of the sample under certain vacuum conditions can be in a certain vacuum conditions, and can

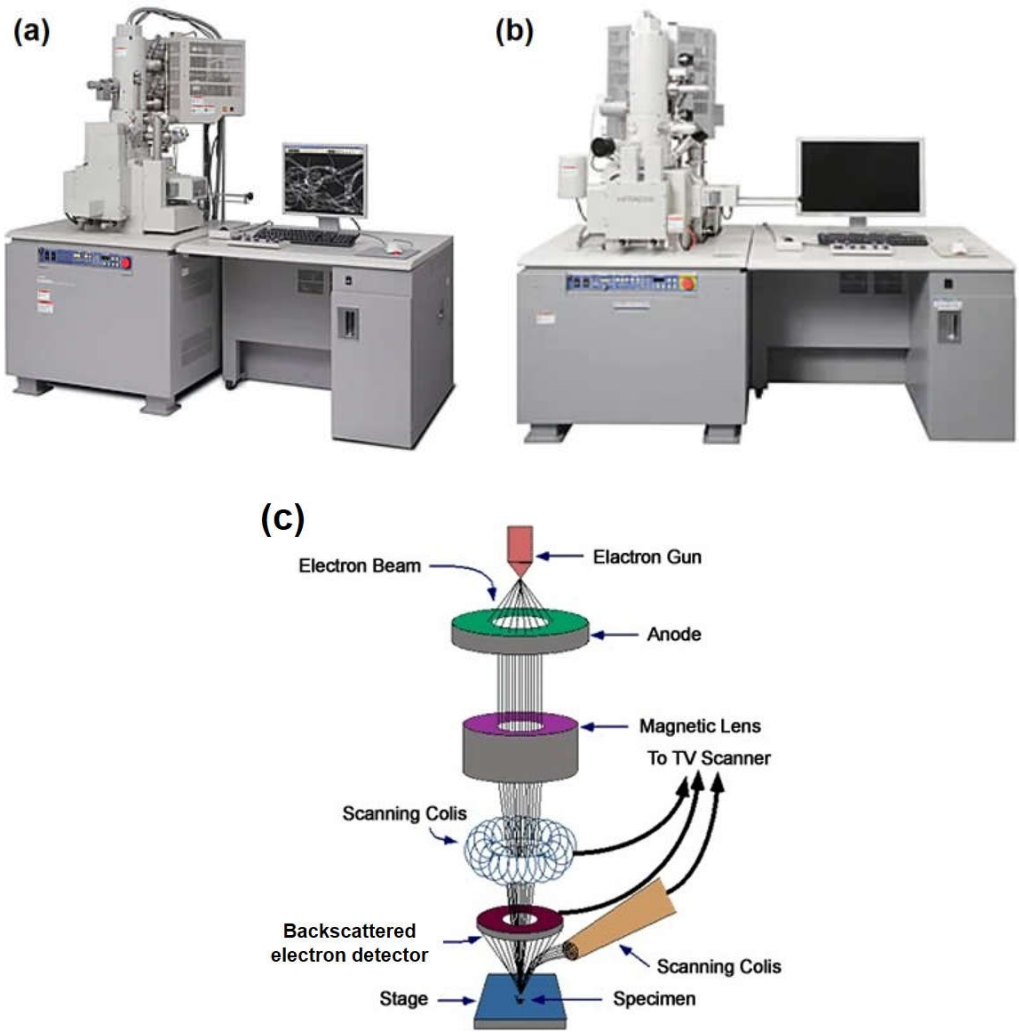


Fig. 2.10 Photos of Hitachi (a) SU6600; (b) SU8000 [34]; and (c) structural diagram of SEM [35].

display the surface appearance information of the sample under certain vacuum conditions effectively with a resolution of 5–10 nm.

The EDX is used to quantitatively analyze the composition of the sample by analyzing the wavelength and intensity of the elemental characteristic X-ray emitted by the sample. When an electron on the inner orbit is excited and a hole left in place, the whole atomic system is in an unstable excited state, then the outer electron will spontaneously jumps from a high energy state into this hole with a low energy state. This process is called the relaxation process. The energy released in this process is emitted in the form of X-ray radiation. The elements contained in the sample can be determined according to the different characteristic X-ray wavelengths. By comparing the intensity of different elemental spectra, the elemental concentration can be determined.

(e) Current-voltage (I-V) plotter

Among all the performance characterization methods of solar cells, I-V characteristic test is the most commonly used one. By measuring the I-V characteristic curve, and further data analysis, we can directly understand the physical properties of solar cells, including photoelectric conversion efficiency (η), filling factor (FF), short-circuit current (I_{SC}), open-circuit voltage (V_{OC}), etc. These data can provide reliable basis for the research, and application of the solar cells.

In this research, the current-voltage (I-V) characteristics measurements are performed by a power device analyzer/curve tracer (Agilent Technologies B1505A), as shown in Fig. 2.11 [36]. The performance of device as a solar cell is also tested by using a solar simulator (Asahi Spectra, LAXC100) as shown Fig. 2.12 [3]. Dark/light current is measured without/with illumination of this solar simulator (AM1.5 condition at 75 mW/cm^2, xenon lamp).

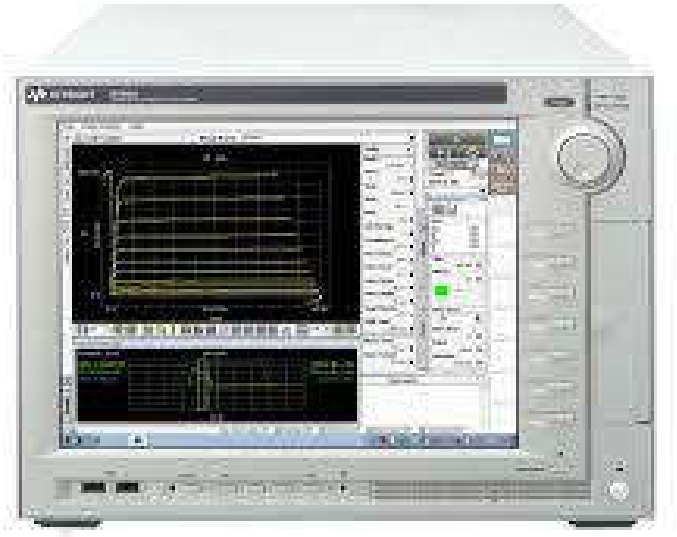


Fig. 2.11 Photo of (a) power device analyzer/curve tracer (Agilent Technologies B1505A) [36].

Fig. 2.12 Solar simulator (Asahi Spectra, LAXC100) [37].

During the experiment, the two conductive probes of the I-V tracer are connected to the electrodes of the sample. By uniformly changing the magnitude and direction of the applied voltage at both probe ends and recording the corresponding changes in the current flowing through the samples, the I-V characteristic curve can be obtained.

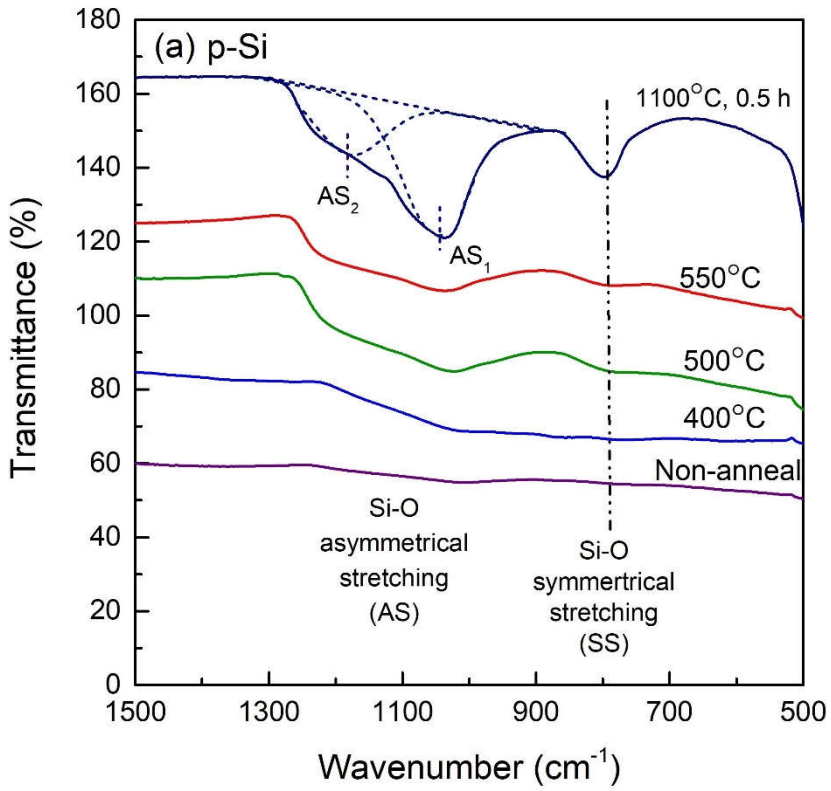
2.3. Results and Discussion

2.3.1 Effect of low temperature annealing on oxidation

Figures 2.13 (a) and (b) show the FT-IR spectra of the p- and n-type Si paste films on Al substrates before and after annealing at temperatures of 400, 500, and 550°C. The spectrum for the p-type film on a Mo substrate annealed at 1100°C for 0.5 h is also shown as a reference [8]. As the annealing temperature rises, an absorption peak near 800 cm^{-1} attributed to the SS vibration mode appears. The rocking vibration mode located at around 500 cm^{-1} is slightly observed in Fig. 2.13 (a). To compare the degree of oxidation of the Si paste film before and after annealing, the peak areas of the AS and SS modes were calculated. For p-type Si paste films, the peak areas for the films on Al are much smaller than that for the film on Mo. This means that the degree of oxidation is reduced greatly by lowering annealing temperature from 1100°C down to 400°C despite an increase in annealing time from 0.5 to 3 h. In contrast, the peak areas for the n-type Si paste films on Al are large, almost comparable with the film on Mo.

It is considered that the oxidation rate of Sb doped Si is higher than B doped Si below 1000°C even with a lower dopant concentration, through comparison of oxidizability of Sb, P, and B doped Si [38, 39]. A higher oxidizability of Sb doped Si is attributed to a lower degree of crystal perfection as follows: (1) acceptor impurities (Al, B, Ga, and In) are depleted near the Si surface, while donor impurities (As, P, and Sb) are piled up near the Si surface [38], thus introducing larger lattice distortion into the surface, and (2) due to the large atomic radius of Sb (0.136 nm) relative to Si (0.117 nm), Sb doping causes heavier lattice strain in the Si bulk, thus introducing excess vacancies into the bulk [39].

It is interesting to note that the peak areas for the film annealed at 550°C are rather smaller than that at 500°C, indicating the less oxidation. This could be due to the grain



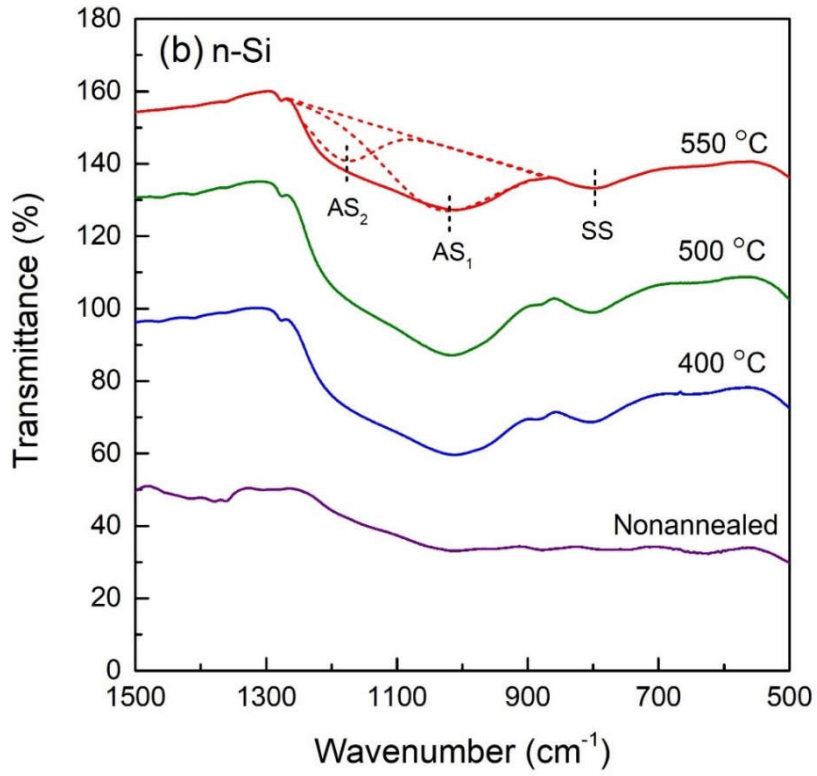


Fig. 2.13 FT-IR spectra of the (a) p- and (b) n-type Si paste films on Al substrates before and after annealing at 400, 500, and 550°C. The spectrum for the p-type film on a Mo substrate annealed at 1100°C for 0.5 h is given in (a) as a reference.

boundary diffusion of Al from the substrate to the film as also shown later by EDX. A diffusion coefficient generally increases exponentially with temperature, following an Arrhenius type relation [40–42]. It is reasonable to consider that Al atoms in the film annealed at 550°C diffuse faster and fill more into the pores. These Al atoms filling into the pores prevent Si atoms from contacting with remaining air in the pores. On the other hand, as the Ellingham diagram [43] indicates that O atoms are more likely to react with Al than Si, Al atoms could be the sacrificial substance of oxidation instead of Si.

2.3.2 Crystallization condition of Si paste using AIC process

The Raman spectra of the p- and n-type Si paste films on Al substrates before and after annealing at temperatures of 400, 500, and 550°C are shown in Figs. 2.14 (a) and (b), respectively. The spectrum for a c-Si wafer is also shown as a reference. The Raman shifts and the FWHM of Si peaks derived from Figs. 2.14 (a) and (b) are also shown in Figs. 2.15 (a) and (b), respectively. While the peak position of the Si paste film before annealing is centered at around 521 cm^{-1}, that after annealing shifts to higher wavenumbers towards 525.4 cm^{-1} for c-Si. This could be due to the relaxation of tensile stress in the Si paste film, which resulted from distortion of Si lattice by ball milling process [44].

The peak shape of the films after annealing becomes sharper as its FWHM actually becomes closer to that of c-Si, confirming an increase in crystallinity by annealing. The typical fitting of the 521 cm^{-1} peak for the film before annealing using two Gaussian distribution functions is shown in in Fig. 2.14 (c). The broad peak centered at a lower wavenumber of 515 cm^{-1} is attributed to small crystallites with diameters below 10 nm [45], rather than wurtzite phase [46], thus suggesting inclusion of a number of Si nano-crystals, as also shown later by SEM. The weak and broad feature centered at around

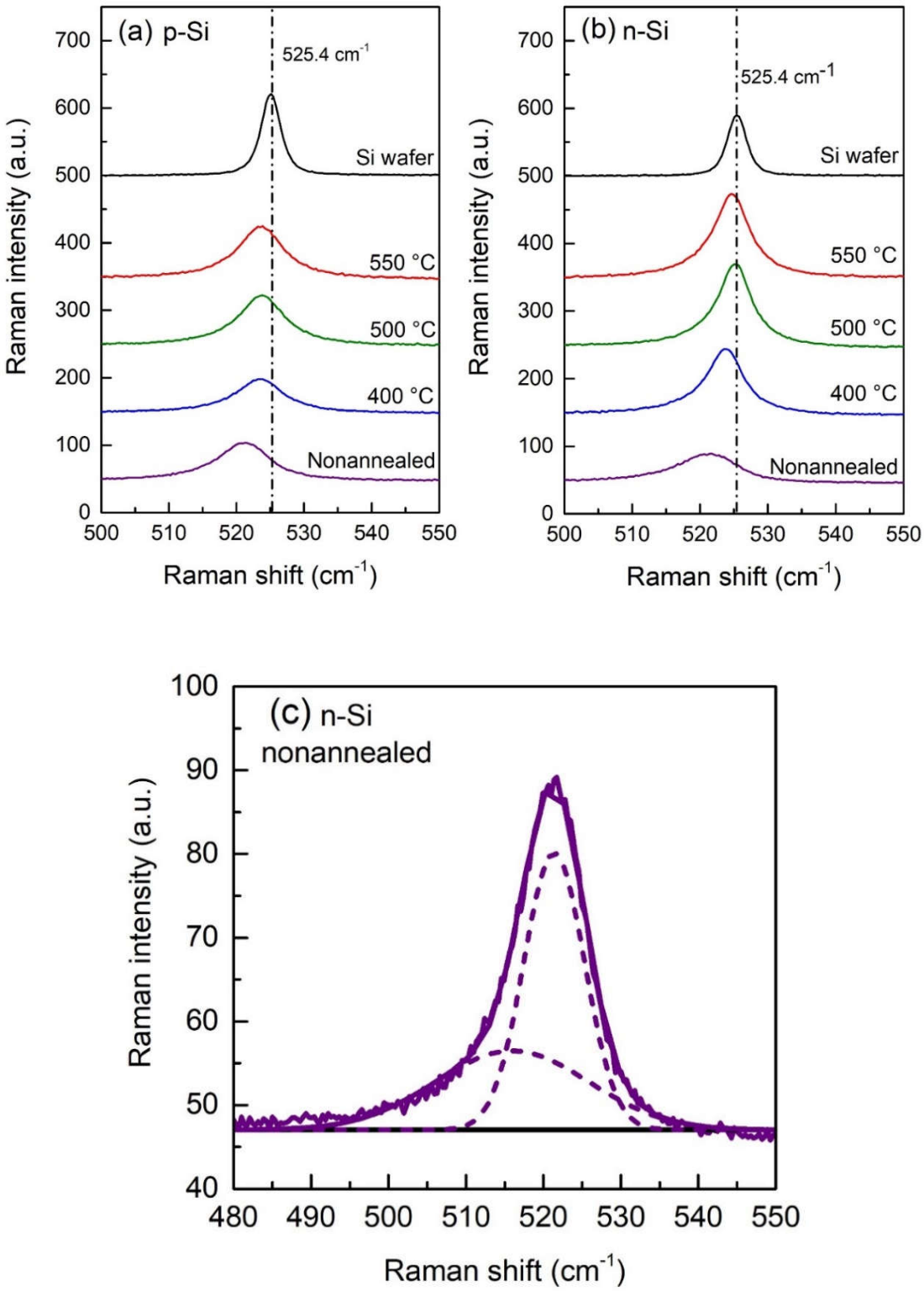


Fig. 2.14 Raman spectra of the (a) p- and (b) n-type Si paste films on Al substrates before and after annealing at 400, 500, and 550°C. The spectrum for a c-Si wafer is given in (a) and (b) as a reference. (c) Typical fitting of the 521 cm^{-1} peak for the film before annealing using two Gaussian distribution functions.

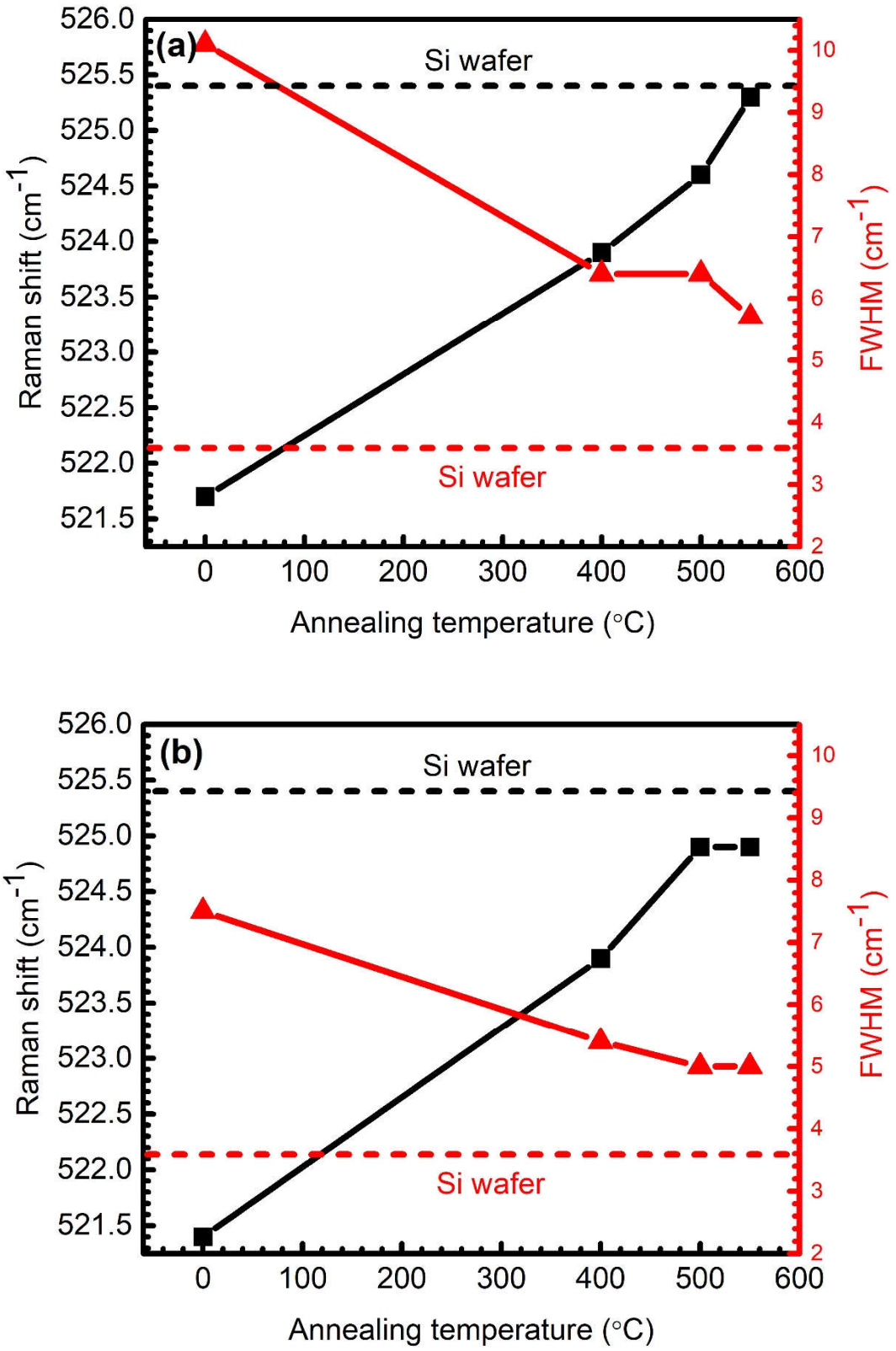


Fig. 2.15 Variation of Raman data of Si wafer, (a) p-type Si paste films, and (b) p-type Si paste films at different annealing temperatures.

490 cm^{-1} is referred to a-Si phase. The a-Si phase could be formed in the instantaneous collision/friction among Si nanocrystals, miller wall, and milling beads. This a-Si phase surrounding Si nanocrystals like shells was so thin that the corresponding Raman peak was very weak. After the annealing, this weak feature disappeared due to increasing crystallization of a-Si towards c-Si. Besides, there was another way of increasing crystallization. During the annealing, fine Si nanocrystals could be coalesced each other to grow and, eventually, form larger Si crystals.

The XRD patterns of the p-type Si paste films on Al substrates before and after annealing at 500°C are shown in Fig. 2.16. The XRD patterns show some diffraction peaks of the underlying Al substrate. While only weak diffraction peaks of Si are observed before annealing, three distinct large peaks of Si (111), Si (220) and Si (311) appear after the annealing. It is observed that the XRD intensity ratio of Si (111) / Al

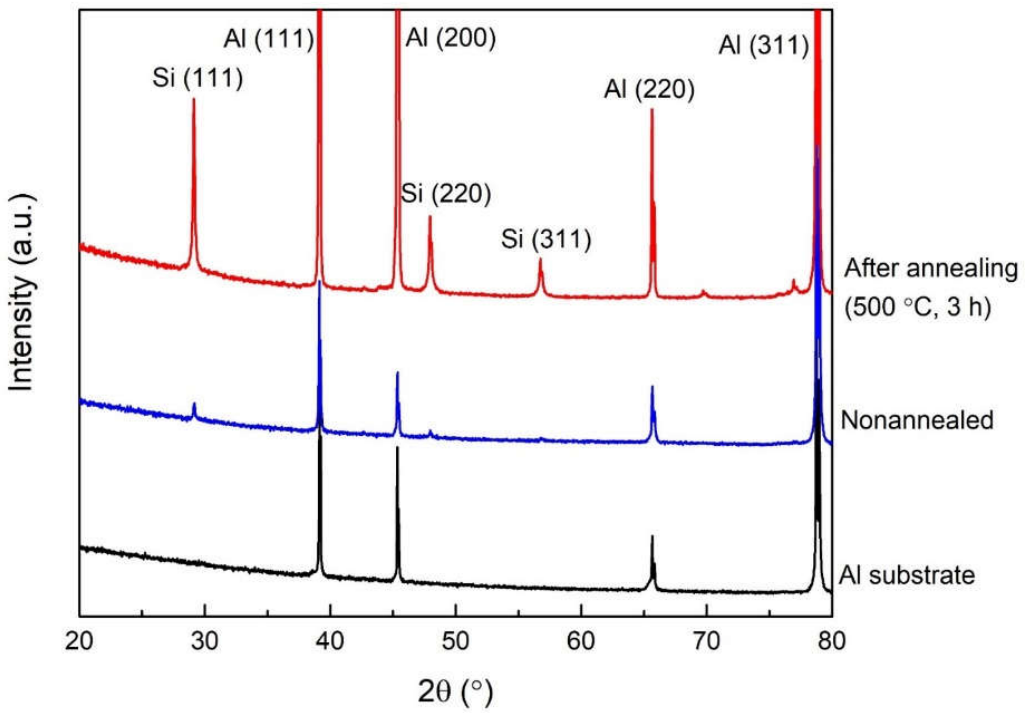


Fig. 2.16 XRD patterns of the p-type Si paste films on Al substrates before and after annealing at 500°C. The XRD pattern of an Al substrate is given as a reference.

(111) of nonannealed Si paste increases from 0.11 to 0.25 after the annealing at 500°C for 3 h. The increase of Si peak intensity is due mainly to an increase in fraction of crystalline Si phase in the film after annealing via recrystallization. The FWHM of the Si (111) peak before and after annealing at 500°C are measured to be 0.20° and 0.16°, respectively, thus confirming an increase in crystallinity by annealing. The diffraction patterns after annealing at other temperatures were almost similar.

2.3.3 SEM observation of Si paste device

Figure 2.17 (a) shows the SEM image of the surface morphology of the p-type Si paste film on Al substrates annealed at 500°C. Figures 2.17 (b) and (c) are the higher magnification images and the EDX spectrum of the square part of Fig. 2.17 (a), respectively. Fig. 2.17 (b) reveals that the film has porous structure and consists of grains with nominal sizes smaller than a few hundreds of nm. In particular, a large number of small grains with sizes below tens of nm exist.

Fig. 2.17 (c) reveals that film surface consists dominantly of Si with small amounts of O, Fe, and C as impurities during the fabrication process. During the SEM samples preparation, some organic and metal contaminants may adhere to the surface of the Si paste film, causing these impurity peaks in the EDX spectra. Hollow- or hole-like regions with sizes up to several micrometers are occasionally observed as shown typically in Fig. 2.17 (d). The EDX spectra for two positions marked with cross symbols 1 and 2 in Fig. 2.17 (d) are shown in Figures 2.17 (e) and 2.17 (f), respectively. Fe and O peaks appear to come from ambient dusts because some particles containing only Fe and O were occasionally observed on the surface by SEM. As Fig. 2.17 (e) shows the presence of a considerable amount of Al, indicating that Al was plied up to the surface by grain boundary diffusion. As the non-annealed Si film consists of nano-sized particle

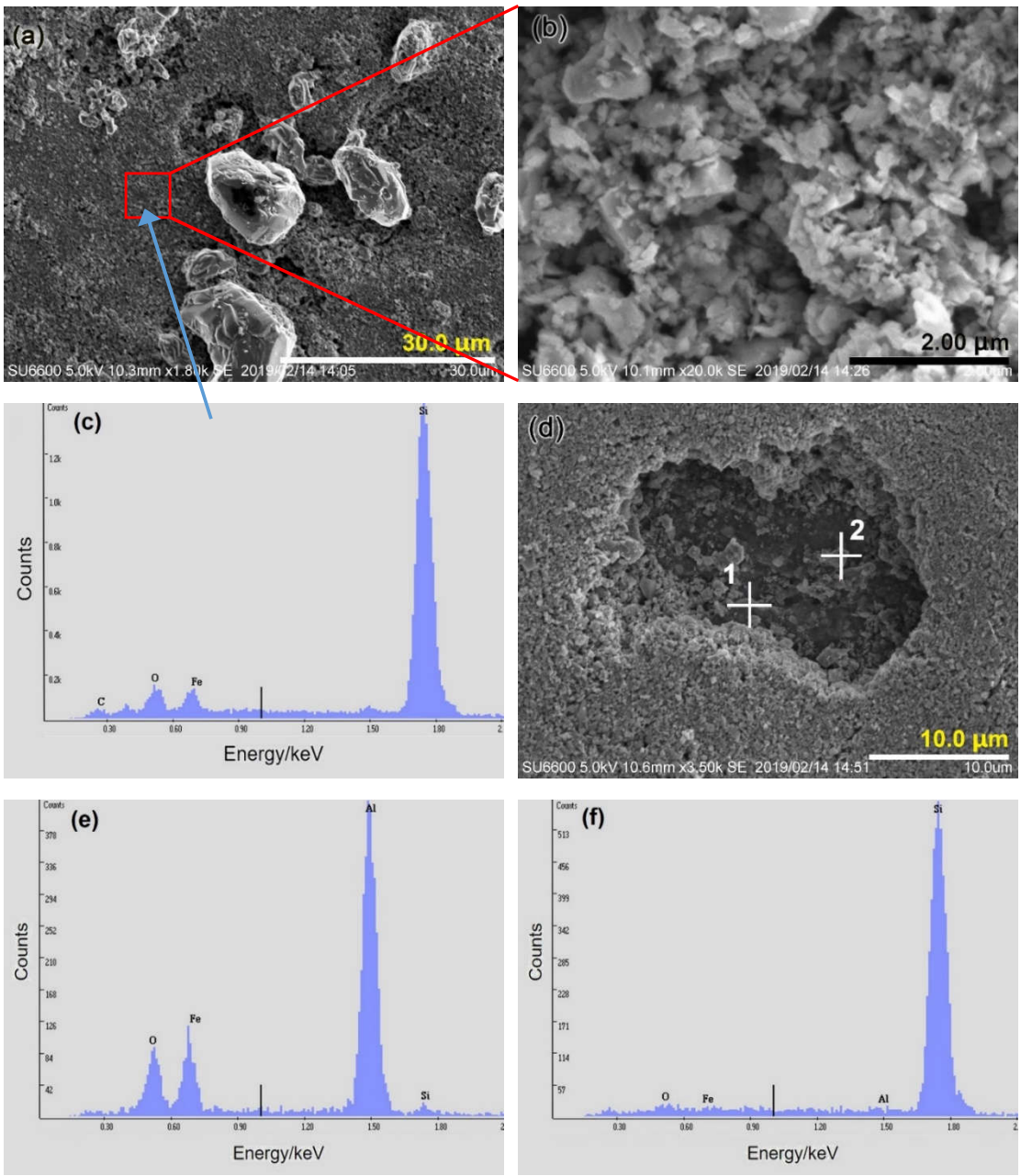


Fig. 2.17 (a) SEM image of the surface morphology of the p-type Si paste film on Al substrates annealed at 500°C. (b) Higher magnification SEM image and (c) EDX spectrum of the square part of (a). SEM image of a hollow-like region [(d)] and EDX spectra for two positions marked with cross symbols 1 [(e)] and 2 [(f)] in (d).

grains, the annealing process had a similar effect to sintering process of powder materials. There are two significant mass transport mechanisms during sintering, that is, grain boundary diffusion and lattice diffusion [41]. Due to the high concentration of

defects in the grain contact area resulting from their crystallographic misalignment, Al atoms can diffuse along the grain boundaries much faster than inside the Si grains, since the defect concentration inside the Si grains is much smaller (bulk diffusion) than that of grain boundaries [47]. Grain-boundary diffusion is one of the main mechanisms of low-temperature sintering used in powder materials, such as sliver powder [40] and alumina powder [42], which are similar to Si paste case. Therefore, Al atoms are transported through grain boundaries into pores by the chemical potential gradient in the boundary plane, thus infilling the pores and densifying the film. Furthermore, other impurities such as Zr was not detected by the EDX spectra. It is also found 50 ball milling beads with a weight of 1310 mg did not reduce after PBM process, but slightly increased to 1312 mg. The extra weight may be due to a layer of Si paste covering the milling bead. Therefore, it is confirmed that Zr has not been significantly mixed into the Si paste as impurity during the preparation of Si paste.

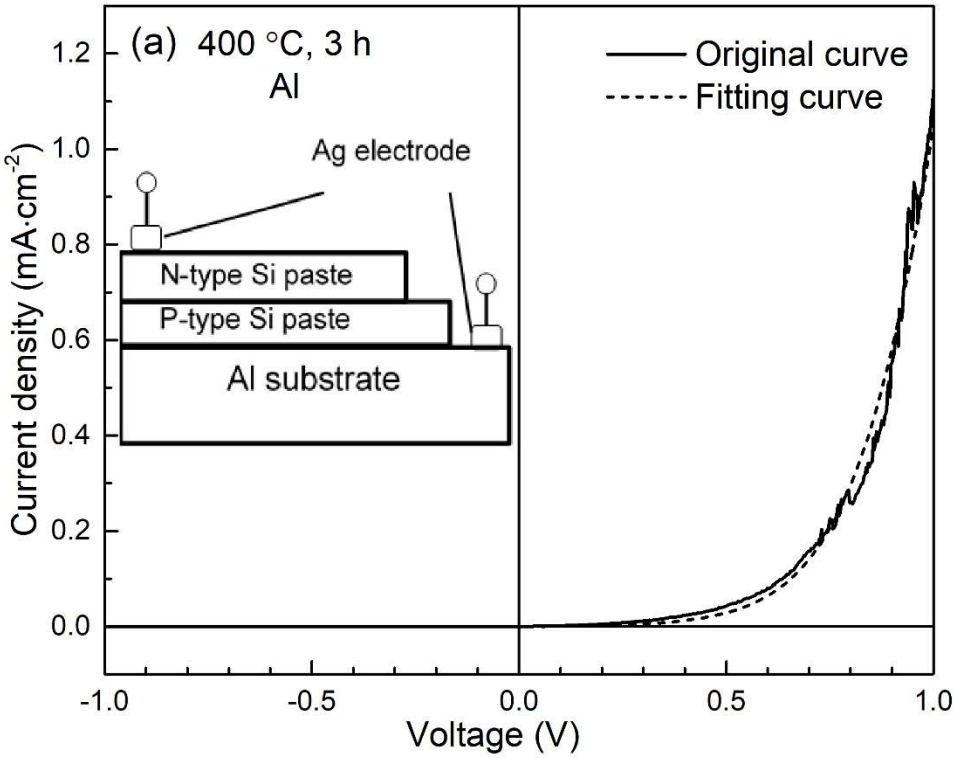
2.3.4 I-V characteristic of Si paste device

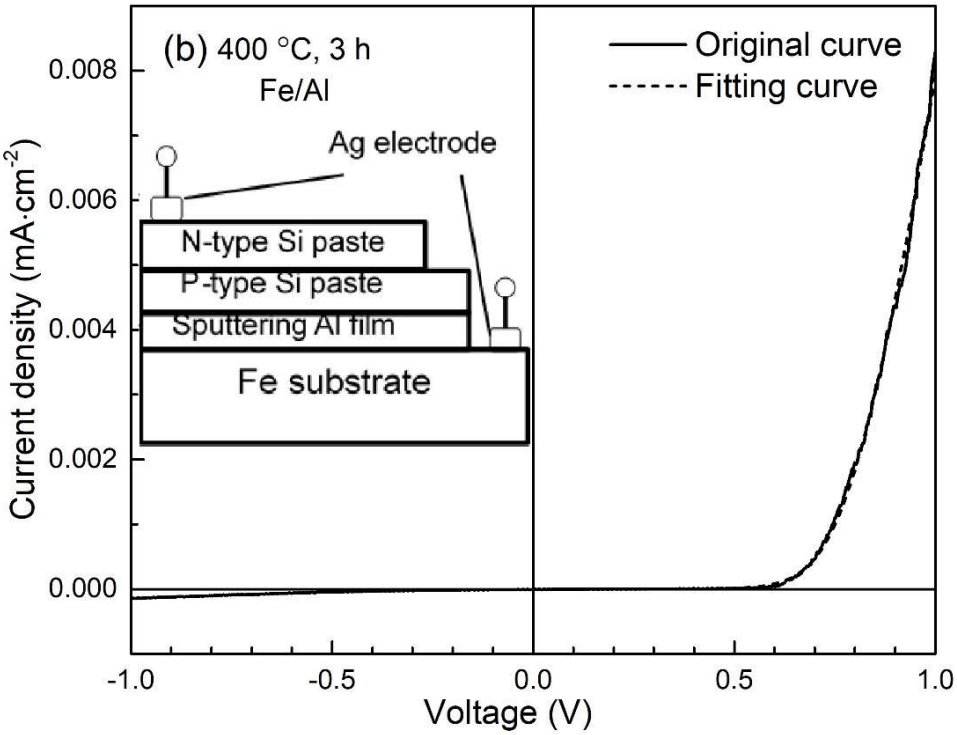
The I-V characteristic of the pn junction diode using p- and n-type Si paste films annealed at 400°C fabricated on an Al substrate is shown in Fig. 2.18 (a), in which the device structure is depicted in the inset. The I-V characteristic shows rectification with an on/off current ratio corresponding to the rectification ratio of about 3200 @ ±1 V. The I-V characteristic is fitted using the standard equivalent circuit for the first-order diode modeling [48]. The total current at a given temperature (T) can be described by eq. (2-5) [49]:

$$I = I_s \left\{ exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1 \right\} \tag{2-5}$$

where I_s represents the reverse saturation current, q is the elementary charge, n is the ideality factor, k is the Boltzmann constant, and R_s is the series resistance. Curve fitting results using eq. (2-5) are reasonably in agreement with the experimental data as shown in Figs. 2.18 (a) and (b). From the fitting result, the ideality factor is estimated to be about 4.3 with R_s =1.8 kΩ. Such a high series resistance is attributed to a high defect density in Si paste films and an oxide layer surrounding each particle. The ideality factor was increased to about 4.8 with R_s=4.0 kΩ when the annealing temperature was increased to about 500°C. This could be due to easier oxidation of higher temperature annealing, in agreement with the FT-IR results in Figs. 2.13 (a) and (b). Besides, the I-V characteristic for the annealing temperature of 550°C exhibited an almost linear relation similar to Ohm's law, due probably to enhance Al diffusion into the Si paste film as shown by EDX. Since the diffusion coefficient of Al at 550°C should be larger than that at 500°C, Al diffusion from the substrate to the surface could form conductive channels for short circuit.

The I-V characteristic of the pn junction diode using p- and n-type Si paste films annealed at 400°C fabricated on an Al-sputtered Fe substrate is shown in Fig. 2.18 (b). The I-V characteristic shows rectification with the rectification ratio of about 57 @ ±1 V. The ideality factor is estimated to be around 3.0 with R_s=1.7 MΩ. The much higher resistance is attributed to diffusion of Fe atoms into the Si paste film because Fe could act as a deep-level transient impurity and introduce trap levels into the Si band gap even at low temperature (100~175°C), and these traps have also high thermal stability [50]. In addition, the pn junction diode using p- and n-type Si paste films on an Al sputtered-Fe substrate annealed at 500°C showed the best photovoltaic characteristic under AM1.5 illumination of a solar simulator among all other samples. A short circuit current density of 5.8×10^{-5} mA/cm^2 and an open circuit voltage of 0.14 V were obtained. The


(a) 400 °C, 3 h
Al
Original curve
Fitting curve
Ag electrode
N-type Si paste
P-type Si paste
Al substrate
Current density (mA·cm-2)
Voltage (V)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-1.0
-0.5
0.0
0.5
1.0


(b) 400 °C, 3 h
Fe/Al
Original curve
Fitting curve
Ag electrode
N-type Si paste
P-type Si paste
Sputtering Al film
Fe substrate
Current density (mA·cm-2)
Voltage (V)
0.008
0.006
0.004
0.002
0.000
-1.0
-0.5
0.0
0.5
1.0

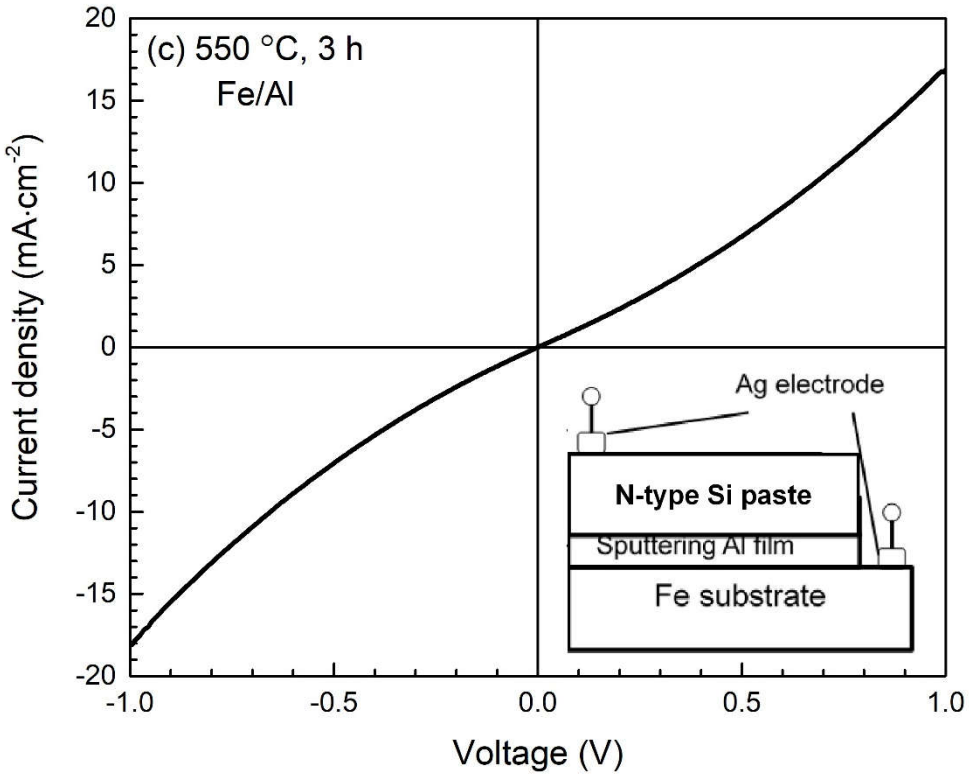


Fig. 2.18 I-V characteristics of the pn junction diodes using the Si paste films annealed at 400°C fabricated on (a) Al and (b) Al-sputtered Fe substrates together with curve-fitting results (dash line) using eq. (2-5). (c) I-V characteristics of the Al-sputtered Fe substrate coated with single n-Si paste annealed at 550°C.

Table 2-1 Performance parameters of Si paste device using low temperature annealing derived from fitting results of Fig. 2.18.

	Rectification Ratio	**Ideality factor (n)**	**Series resistance (R_s, kΩ)**	**Reverse saturation current (I_s, μA/cm^2)**
Al sub.	3200	4.3	1.8	1.8×10^{-3}
Fe/Al sub.	57	3.0	1700	7.6×10^{-7}

relatively limited output power is attributed to the defects and oxides in the Si paste film. Further work will continuously focus on the reduction of these defects and oxides, in particular, at grain boundaries.

Besides, the I-V characteristic of the Al sputtered Fe substrate coated with single layer of n-Si paste annealed at 550°C is also shown in Fig. 2.18 (c). The linear Ohmic I-V curve indicates that n-Si paste has formed Ohmic contacts with both Al layer and Ag electrode.

It is also noticed that the diode ideality factors *n* of all the Si paste devices are higher than 2. This non-ideal phenomenon is mainly due to the extended defects like the cell's edge or other defects in the cell area like scratches crossing the pn junction [51]. The extended defects cause a high local density of defect states, so that the carriers recombine via more than one defect (so-called multi-level recombination), leading to ideality factors higher than 2.

2.3.5 Models for AIC process in Si paste device

Models are introduced in the following to explain the possible mechanism of improving crystallinity of Si paste films by the AIC process. During the high energy ball milling process, the local temperature of the crushed nano-crystalline Si (nc-Si) particle surface rises up and cools down suddenly, thus forming a very thin amorphous Si (a-Si) shell and also oxidized to some degree, forming the core-shell structure [52], as illustrated in Figure 2.19 (a). In the meantime, as the size of the nc-Si decreases, the specific surface area will increase drastically. Therefore, the nc-Si can readily react with oxygen, making the particles vulnerable for oxidation. The oxide SiO_x is not favorable because it is an insulator and strongly impairs the conductivity of the Si paste film.

Inspired by the AIC process for nucleation and diffusion-controlled crystal growth at the Al/a-Si interface [12], schematic diagrams of the possible mechanism in our Si paste films are depicted in Figures 2.19 (b)–(d). Since the Si paste film is coated and pressed on an Al substrate, the Si particle in the film has a core shell structure in the order of

Al/SiO_x/a-Si/nc-Si from the outer to the inner of the particle as shown in Fig. 2.19 (b). When the Si paste film is annealed at a low temperature of around 400–500°C, a part of the Si oxide shell reacts with Al. The products of this reaction should be Al_xSi and Al_xO_y [53], and Al_xSi plays a role of a channel through which Al and Si atoms could diffuse each other. The Si atoms in a-Si phase diffuse outward into the Al layer and further form Al_xSi. Concurrently, Si clusters start growing inside and outside of the oxide shell during the annealing. The Al atoms also diffuse inwards into the a-Si/nc-Si shell at the same time as shown in Fig. 2.19 (b).

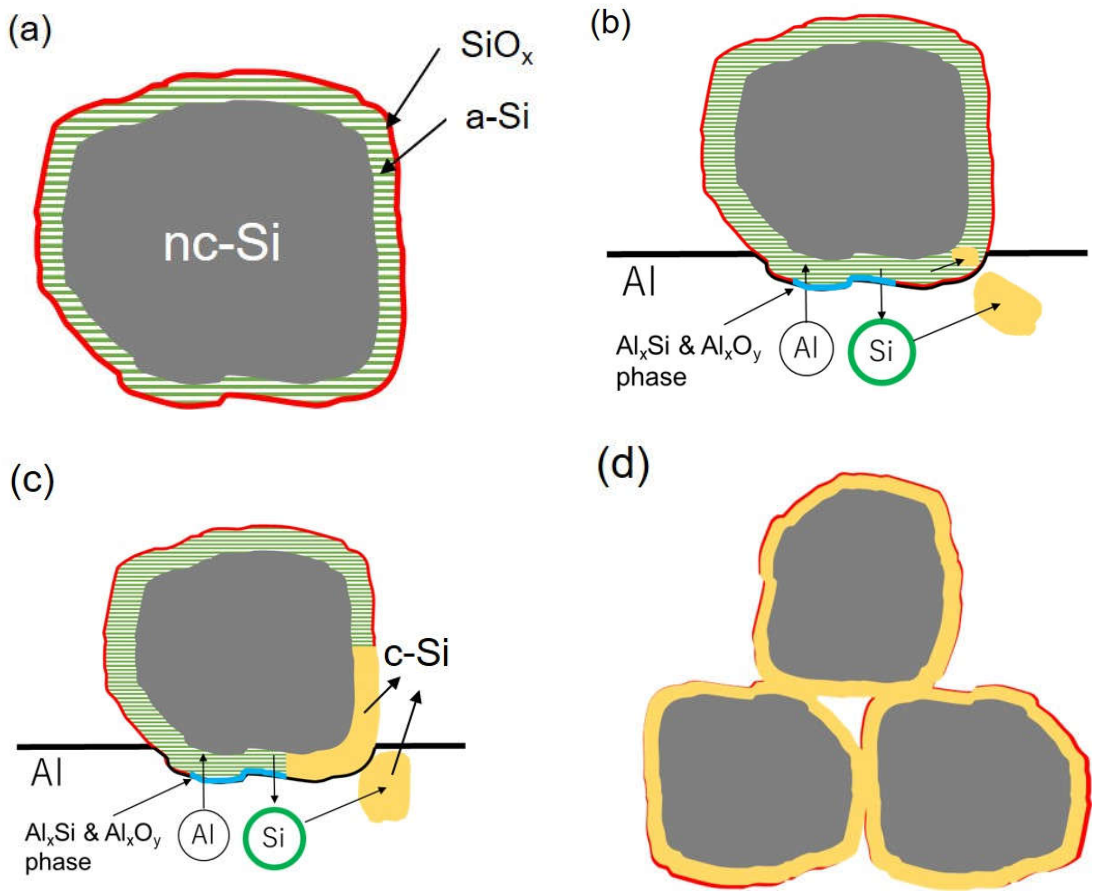


Fig. 2.19 Schematic diagrams of (a) a Si nano-crystallite structure in Si paste; (b) a first step of the AIC process: the reaction between Al and an oxide shell as well as the interdiffusion of Al and Si atoms; (c) a second step of the AIC process: nucleation and growth of Si; (d) Si particles contacting the neighboring particles without the oxide shell.

However, unlike the conventional AIC process with a-Si/Al system, the Si paste almost consists of Si nanocrystals. While the a-Si only accounts for a small portion, since there is a very small peak located at low wavenumber (480–490 cm^{-1}) region for nonannealed Si paste as shown in the Fig. 2.14 (c). Therefore, it suggests that the nucleation process during the Si atoms diffusion motion will become rare. Since there are so many Si nanocrystals already exists in the nonannealed Si paste, the Si atoms in the amorphous phase are more inclined to bond with the existing Si nanocrystals, allowing the Si nanocrystals to grow continuously. Consequently, in the case of Si paste, the enhanced crystallization maybe mainly attributed to the growth of existing Si nanocrystals during AIC process.

Since Al is known as a p-type dopant rather than a deep-level impurity in Si, a p^+ type Al layer is expected to be formed in the p-type Si layer. The Si atoms diffused from a-Si phase are gradually transformed into crystalline phase as shown in the thick hatched c-Si region in Fig. 2.19 (c). Then, the oxide shell gets thinner in this step. It should be noted that the reaction between the oxide shell and Al does not happen only at the bottom side of the particle that touches the Al layer because the Al diffuses closer to the surface region as indicated by EDX in Fig. 2.17 (e). The whole oxide shell tends to react with Al. In the last step of AIC as shown in Fig. 2.19 (d), most of the a-Si transforms into c-Si and the oxide shell disappears. As the c-Si region continues to grow, the Si particle starts contacting the neighboring particles directly owing to the absence of the oxide shell. The contacting areas between Si particles could become conductive routes for the carriers.

Since the native oxide shell of Si nanoparticle is thinner than 1 nm [52], it is also considered that the carriers may pass through the oxide shell by tunneling effect. However, in the case of Si paste, there are many Si nanoparticles with an oxide shell that carriers have to transport through, it is considered that carriers cannot pass through

many the oxide shells by tunneling. Therefore, the major carrier conductive mechanism should be due to the AIC process, namely, the oxide shells are decomposed by Al and form Al_xSi and Al_xO_y. Then the conductive channels are established between Si nanoparticles without oxide shells at the interface.

2.4. Conclusions

A metal-induced crystallization technique using Al as the metal species was utilized for enhancing recrystallization of nanocrystalline Si paste films on Al and Al-sputtered Fe substrates by annealing at low temperatures (400 to 550°C). The AIC process in the case of Si paste involved (a) the decomposition of Si oxide shell of Si particles by the interaction with Al, (b) the diffusion process of Si atoms in amorphous phase and Al atoms, and (c) the grain growth of Si nanocrystals originally present in the nonannealed Si paste. This low-temperature annealing process suppressed greatly oxidation of the Si paste films as confirmed by FTIR, contrastive to the conventional high-temperature annealing process above 1000°C. The I-V characteristic of the pn junction diode fabricated on an Al substrate by annealing at 400°C showed rectification with the on/off current ratio of about 3200@ ±1 V, and the low reverse current density of 1.8×10^{-9} A/cm^2 @ -1 V were also achieved. A preliminary test of the pn junction diode fabricated on an Al-sputtered Fe substrate by annealing at 500°C showed a photo generated current density of 5.8×10^{-5} mA/cm^2 under AM1.5 illumination.

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CHAPTER 3:

Rapid Thermal Annealing of Si Paste Film and pn Junction Formation

3.1. Introduction

In the last chapter, a low temperature annealing together with AIC technique was discussed to reduce the degree of oxidation of Si paste and improve rectification characteristics of the pn homo-junction diode [1]. Nevertheless, in this chapter, it was still desired to introduce another annealing technique using shorter annealing duration for suppressing oxidation fundamentally, namely, rapid thermal processing.

Rapid thermal processing (RTP) is commonly considered to be a versatile way for several different functions that include rapid thermal annealing (RTA) [2–4], rapid thermal chemical vapor deposition (RTCVD) [5], rapid thermal oxidation (RTO) [6], and rapid thermal nitridation (RTN) [7]. RTP systems are usually capable of increasing wafer temperatures at high rates over 200°C/s [8]. The high heating rate makes RTP an attractive alternative because of reduction of thermal budgets. In particular, RTA has been proved to be quite effective for reduction of oxidation [9] and also for reduction of residual stress in films when applied in short duration within a few seconds [10]. In this study, RTA was utilized to enhance the crystallization and reduce the oxidation as well as the residual stress of Si pastes to fabricate Si pn homo-junction diodes. The performance of the pn diodes as a solar cell was tested.

3.2. Experimental methods

3.2.1 Si paste device preparation by RTA

At first, the p- and n-type Si pastes were prepared according to the steps described in section 2.2.1. In this chapter, the C (carbon) substrates (Toyo Tanso, IG-43) with a size of 10×10×0.1 mm and resistivity of 9.2 μΩ·m were used in consideration of a similar coefficient of linear thermal expansion (CTE) between Si [11] and C [12] at a temperature higher than 1000°C. An Al layer with a thickness of about 100 nm was deposited on the C substrate by sputtering as the back electrode and back surface field (BSF) [13]. Prior to Al sputtering process, the C substrate was first ultrasonically cleaned with ethanol and then N_2 blow dried. Next, the substrate was placed on a sample holder and vacuumed to a base pressure of 4×10^{-4} Pa in a sputtering chamber. An Al film was deposited by magnetron sputtering at pressure of 3.0 Pa at an Ar flow rate of 30 sccm. The 20 μl of p- or n-type Si paste was coated on the Al sputtered C substrate and dried naturally in a glove box.

The RTA process was carried out in an infrared heating tube furnace (Yonekura: IR-QP1-4-S), and samples were placed in a quartz tube in which Ar gas (6N) has flowed (0.7 L/min). Then the samples were annealed in this furnace at 1150 ~ 1300°C for 1 s ~ 10 min. It should be noticed that the heating-up rate was about 150°C/s. During the cooling process, the temperature of furnace abruptly dropped from peak temperature to 200 °C within 10 s due to the sudden shutdown of the infrared lamp and the continuous flow of Ar gas in the heating furnace, the cooling rate from 1200°C to 200°C was considered to be larger than 100°C/s at the beginning. The heating processes of p- and n-type Si layers were done separately, that is, the p-type Si paste was first coated on the substrate and undergone RTA process, then the thermal oxide of p-type Si paste was etched off by 3 wt. % HF solution. After that, the sample was immediately transferred

to the glove box and coated with n-type Si paste. Then the n-type Si paste was annealed under the same RTA condition. A thermocouple was placed inside the quartz tube next to the sample with a distance of about 1mm. Prior to the electrodes formation with Ag paste, the samples were etched with 3 wt. % HF solution for about 1 min to remove the thermal oxide.

During the annealing process, the Si-C binary system should be considered. The Si-C binary phase diagrams are shown in Fig. 3.1 [14]. As for our RTA condition, when the temperature is elevated to 1150~1300°C (below the peritectic temperature 2545°C), the C substrate does not melt, though the Al layer may prevent some diffusion, a small amount of Si atoms may diffuse into the C substrate, so only the lower right region of the Si-C phase diagram should be studied. It is found that under RTA process conducted in this chapter, the products at the interface between Si paste and C substrate, should be a small amount of SiC whether in the heating or cooling stage. Since the SiC phase is

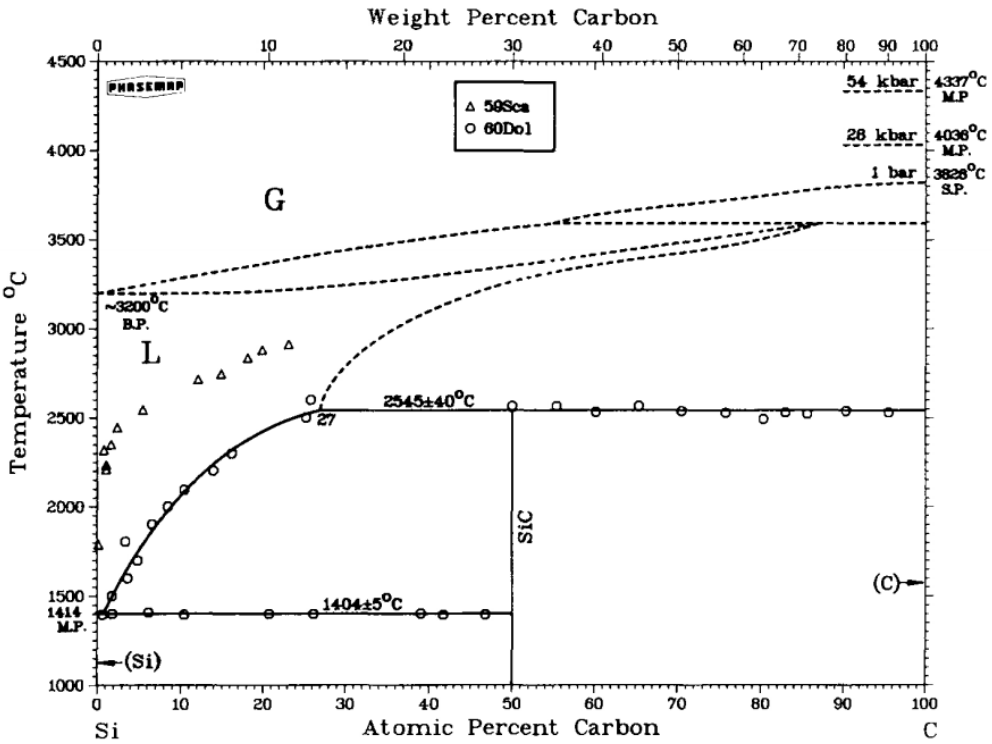


Fig. 3.1 Phase diagram of Si-C binary system [14].

transparent to the visible and IR light, as long as there are not many defects formed at the Si/SiC interface, the effect on the device is not significant.

3.2.2 Characterization methods for Si paste device

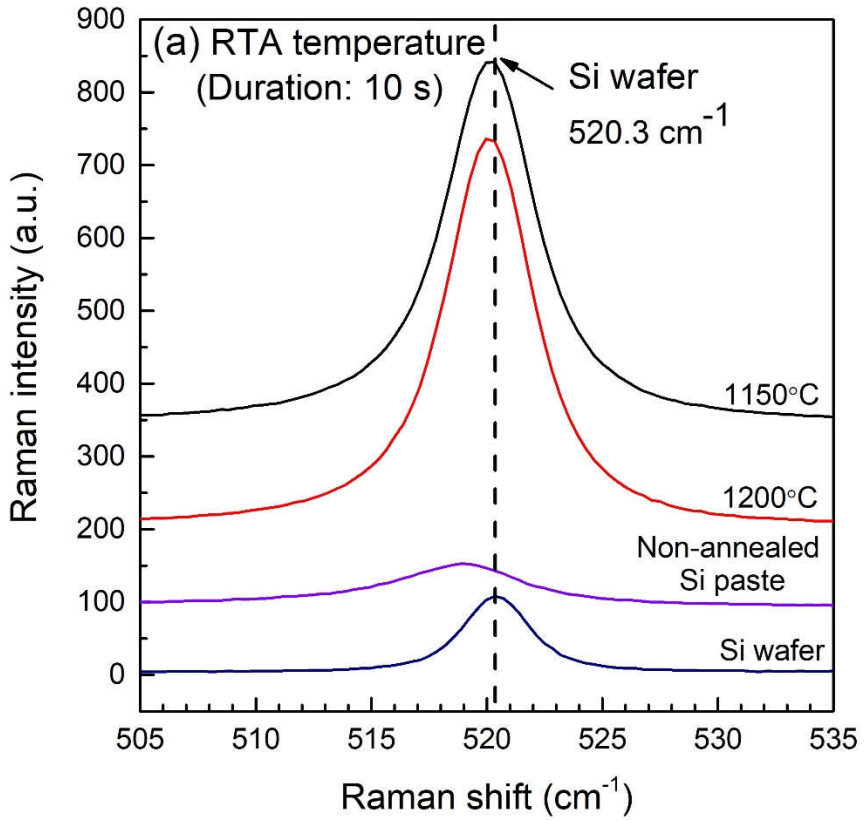
The oxidation conditions of samples were measured by a Fourier-transform infrared spectroscopy (FT-IR) (PerkinElmer: Spectrum Two), and it is considered as that the larger peak of Si-O bonding the more the sample is oxidized. Raman spectra were collected by using a Laser-Raman microscope (Nano-photon RAMAN touch) with a 532 nm-wavelength excitation laser. X-ray diffractometer (XRD) patterns were obtained with a multi-purpose XRD (Rigaku Ultima IV) by using Cu Kα radiation (λ=1.54 Å). Some parameters, such as FWHM, Raman shift, and peak position derived from Raman and XRD spectra are considered together to evaluate the crystallization of post-annealed Si paste more comprehensively. Current-voltage (I-V) characteristics measurements were performed by a power device analyzer/curve tracer (Agilent Technologies B1505A). During measuring the I-V characteristics of Si paste device without illumination, a black cap was covered on the window of instrument to prevent external light from entering the window and being absorbed by the Si paste. The photovoltaic performance of the pn device as a solar cell was also tested by using a solar simulator (Asahi Spectra, LAX-C100, AM1.5). During the test, the incident light from solar simulator was incident perpendicular to the sample surface. At the same time, the incident light spot was controlled to be a 20×20 mm square. The microstructure of samples was observed by field emission scanning electron microscopy (SEM) (Hitachi SU6600 and SU8000). Besides, details of all of the measurement principles as well as the above equipment structures have been introduced in Chapter 2, section 2.2.3.

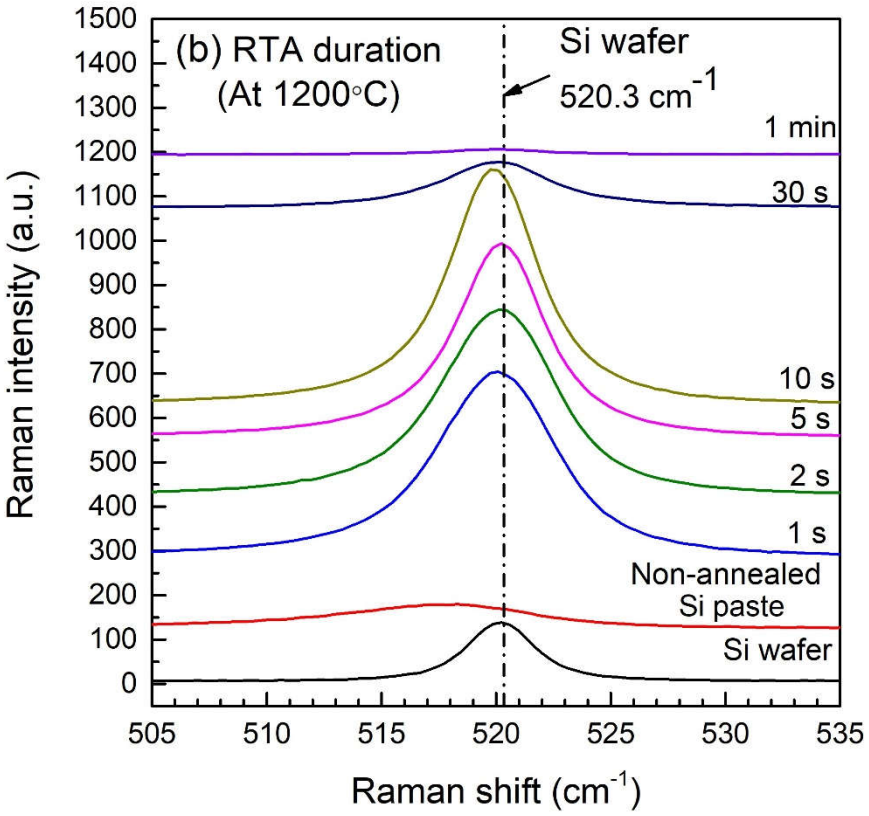
3.3. Results and Discussion

3.3.1 Crystallization condition of Si paste under RTA process

Raman spectra of a Si wafer and p-type Si pastes prepared at different RTA temperatures are shown in Fig. 3.2 (a). The Raman peak shift and width can qualitatively indicate the crystallinity of Si particles in the samples. The peak at 520.3 cm^{-1} corresponding to the transverse optical phonon mode of Si was taken as a reference. The peak of the non-annealed Si pastes is located at around 518.5 cm^{-1}. After annealing at around 1150~1200°C, the peak shows a slight shift to higher wavenumbers towards 520.3 cm^{-1} for a Si wafer, and full width at half maximum (FWHM) of the peaks became smaller for annealed samples. The downward shift of the peaks of non-annealed Si pastes could be due to the residual tensile stress in the Si [15]. This tensile stress resulted the most probably from the rending of the Si induced by the ball milling procedure. During the annealing process, the cubic structure was reordered and the tensile stress was relieved to some extent. Although the sample annealed at 1200°C shows the sharpest peak of Si in Fig. 3.2 (a), the Raman spectra for the samples annealed above 1200°C were not obtained well due to peeling off of a Si paste film. As a result, the sample annealed at 1200°C had the best crystallinity with the FWHM of 4.7 cm^{-1} and the peak location of 519.9 cm^{-1} comparable with 3.6 cm^{-1} and 520.3 cm^{-1}, respectively, for a Si wafer.

In order to further optimize the RTA conditions, the effect of RTA duration was studied at 1200°C as follows. Raman spectra of samples annealed at 1200°C for duration of 1 s to 1 min are shown in Fig. 3.2 (b). It is observed that when the RTA duration is extended from 1 s to 10 s, the Si bonding peak sharpened slightly from 6.0 to 4.7 cm^{-1} in FWHM. It could be also noticed that the peak intensity shows a marked decrease, towards a nearly flat line, by increasing the duration up to 30 s or 1 min, due


(a) RTA temperature
(Duration: 10 s)
Si wafer
520.3 cm-1
1150°C
1200°C
Non-annealed
Si paste
Si wafer
Raman intensity (a.u.)
Raman shift (cm-1)
900
800
700
600
500
400
300
200
100
0
505
510
515
520
525
530
535


(b) RTA duration
(At 1200°C)
Si wafer
520.3 cm-1
1 min
30 s
10 s
5 s
2 s
1 s
Non-annealed
Si paste
Si wafer
Raman intensity (a.u.)
Raman shift (cm-1)
1500
1400
1300
1200
1100
1000
900
800
700
600
500
400
300
200
100
0
505
510
515
520
525
530
535

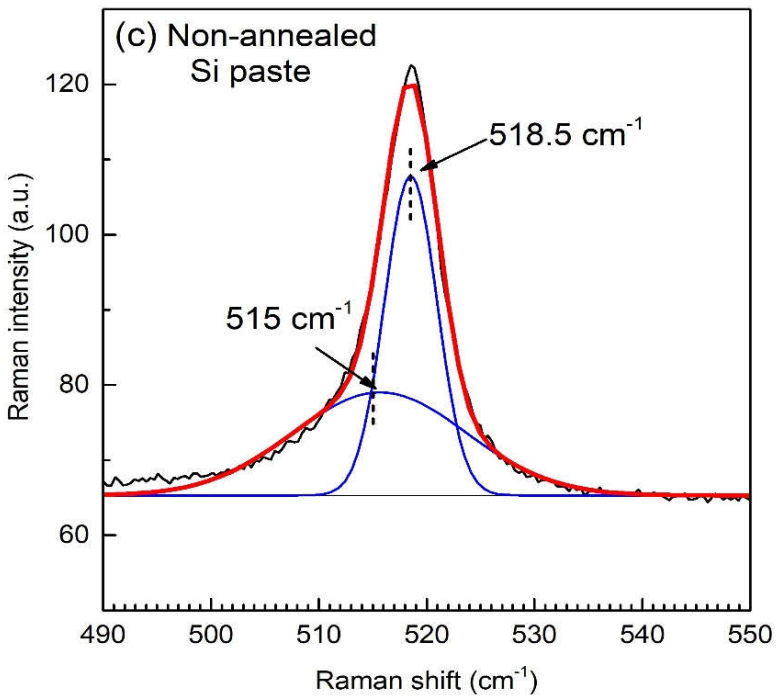


Fig. 3.2 Si Raman spectrum of Si wafer and p-type Si paste under (a) various RTA temperatures for 10 s, (b) various RTA durations at 1200°C, and (c) peak deconvolution of non-annealed Si paste Raman spectrum. Existence of Si nanoparticles with a size less than 10 nm was confirmed.

probably to enhanced oxidation by prolonged annealing. Actually, the samples for duration of 5 min and 10 min (not shown) had characteristics of silicon oxides in IR spectra as explained later. As a result, the sample annealed at 1200°C for 1 s has the highest crystallinity of Si with the FWHM of 4.6 cm^{-1} and the peak location of 520.2 cm^{-1} which are comparable with those of 3.6 cm^{-1} and 520.3 cm^{-1}, respectively, for a Si wafer. The Raman peak of the non-annealed Si paste shows an asymmetric line shape with tailing towards lower wavenumbers. Deconvolution of the peak using two Lorentzian line shapes confirms that a peak at 515.0 cm^{-1} is attributed to either to crystallites of diameters lower than 10 nm [16] or to a silicon Wurtzite phase [17] which is not likely the case. This indicates that some portion of 10 nm class Si particles were included in the non-annealed Si paste. Furthermore, according to the intensity ratio of deconvoluted peaks located at 515.0 and 518.5 cm^{-1}, the proportion of Si particle sizes less than 10 nm can be estimated as approximately 50%.

For XRD analysis, typical polycrystalline Si peaks were observed in wide XRD spectra. Effect of annealing temperature is shown in Fig. 3.3 (a) with XRD patterns of Si paste before and after RTA at 1150, 1200, and 1250°C for 10 s. Effect of annealing duration is shown in Fig. 3.3 (b) with XRD patterns of Si pastes before and after RTA at 1200°C for 1 s to 1 min. After annealing, the Si (111) peak shifts towards large 2θ angle. The interplanar spacing d can be calculated by the Bragg's Law, as shown in eq. (2-3). Compared with standard Si wafer (d = 3.137 Å) non-annealed Si paste shows larger spacing d = 3.152 Å, indicating tensile stressed. On the other hand, sample annealed at 1200°C for 1 s and 1 min show d = 3.148 Å and d = 3.141 Å, which are closer to that of Si wafer. This indicates that the tensile stress in Si pastes was somewhat relieved through melting and recrystallization during the RTA process at 1200°C. This phenomenon is also in good agreement with Raman results. The sample after RTA at1200°C for 1 s shows the highest peak intensity indicating either the larger crystallites or less crystalline distortion indicated by Raman data as showed in Fig. 3.2. Using Scherrer equation, as shown in eq. (2-4), the apparent grain size of non-annealed paste is calculated to be about 63 nm, while that of the RTA at 1200°C for 1 s sample is about 360 nm from FWHM of the Si (111) peaks. It is clear that Si grains have grown after RTA at 1200°C even within 1 s. Previous study [18] has proved that grain boundary states play a dominant role in determining the electrical and photovoltaic properties of polycrystalline Si by acting as traps and recombination centers. The bigger grain size, thus the less grain boundaries will result in higher photovoltaic conversion efficiency.

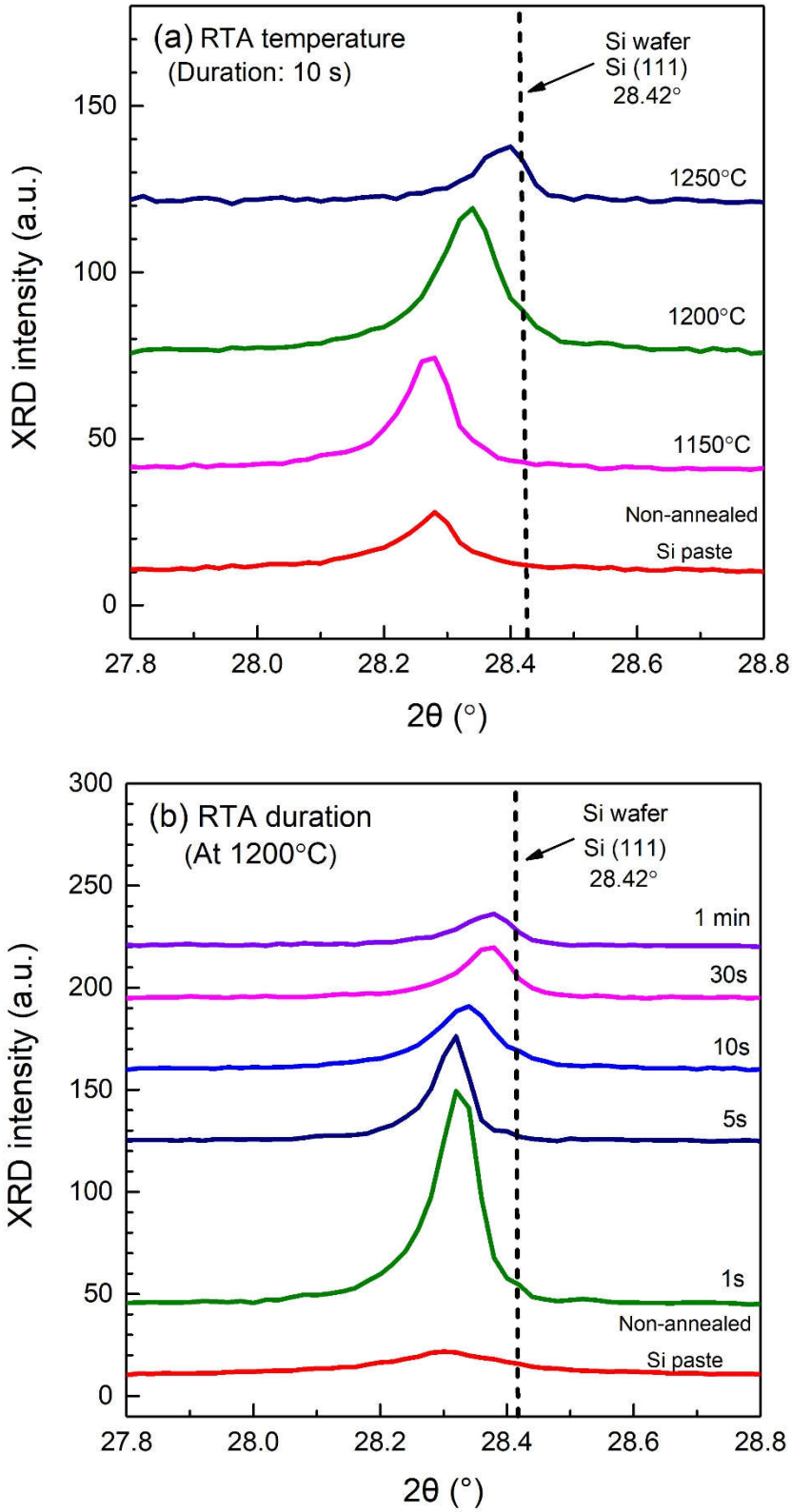


Fig. 3.3 XRD patterns of p-type Si paste under (a) various RTA temperatures for 10 s, (b) various RTA durations at 1200°C.

Table 3-1 Si grain parameters derived from Fig. 3.3 (b).

	Non-annealed	1200°C/1s	1200°C/10s	1200°C/1min	Si wafer
2θ (°)	28.28	28.32	28.34	28.38	28.42
Interplanar spacings *d* (Å)	3.152	3.148	3.145	3.141	3.137
FWHM (°)	0.20	0.08	0.08	0.06	0.02
Grain size (nm)	63	360	360	1800	∞

3.3.2 Effect of RTA on oxidation of Si paste

Oxidation conditions of Si paste with different annealing time were investigated by using FT-IR as shown in Fig. 3.4. The Si-Si bond is not infrared-active, so it does not appear in the IR spectra. On the other hand, the Si-O bond can absorb infrared radiation. There are typically three absorption peaks corresponding to various Si-O transverse-optic (TO) vibrational modes. They are the asymmetrical stretching mode (AS) located at 1000–1200 cm^{-1}, symmetrical stretching mode (SS) centered at 800.0 cm^{-1}, and rocking mode (R) [19-21]. The lowest frequency TO band is located around 450.0 cm^{-1}, attributed to the out-of-plane rocking of O atoms that is too weak to be detected in this study. The degree of oxidation Si pastes before and after annealing is compared with the intensity of the most prominent SS peak. It is found that as the duration increases, the intensity of the SS stretching of Si-O bond peak becomes stronger due to formation of SiO_2. It is also noticed that both Raman and XRD results show that the intensity of crystalline Si peaks decreases with the increase of the annealing duration, which implies that the fraction of Si atoms in crystalline phase has decreased. Combined with FT-IR spectra, it suggests that this portion of crystalline Si

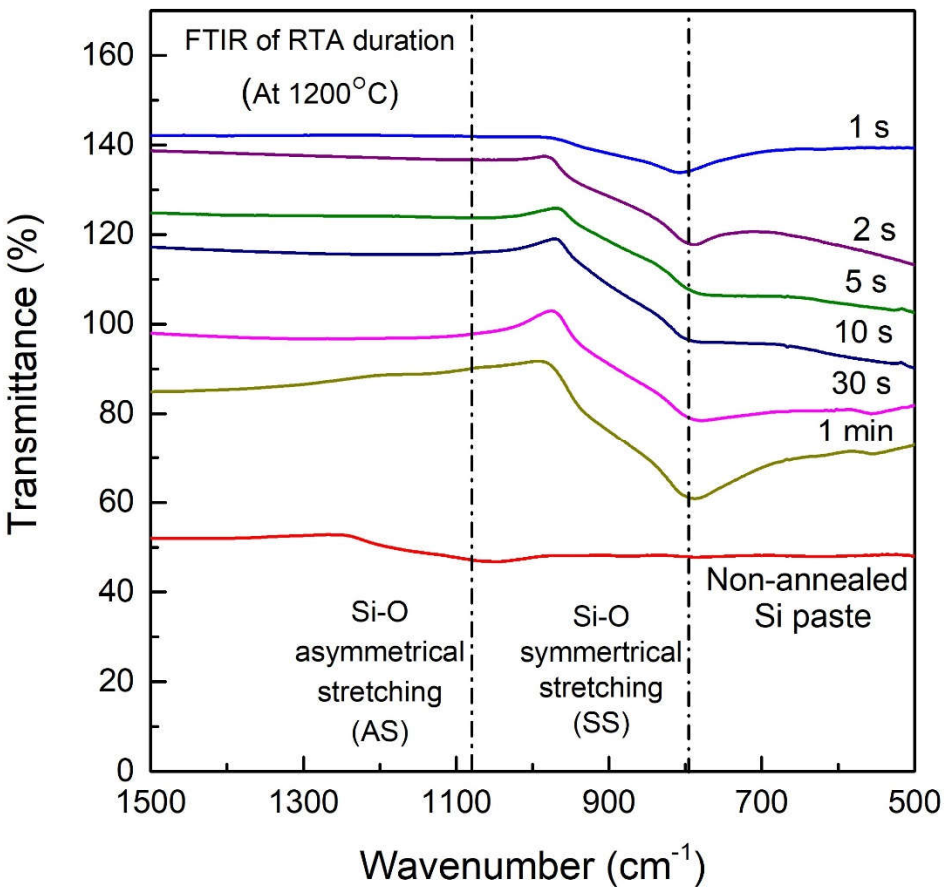


Fig. 3.4 FT-IR spectra of Si pastes with Si-O peaks at various RTA durations.

phase has transformed into amorphous SiO_2, hence, the oxidation peaks in FT-IR spectra become bigger while the crystalline Si peaks' intensity in the Raman and XRD results become weaker with increasing RTA duration.

3.3.3 SEM observation of Si paste device

For distinct observation of Si particles before and after the RTA process, SEM observation was conducted on the microstructure of Si paste. Fig. 3.5 (a) and (b) show cross-section of the Si paste for non-annealed sample and annealed samples at 1200°C for 1 s, respectively. As shown in Fig. 3.5 (a), it is clear that before the thermal treatment Si particles are more likely independent, and some small Si particles with a size of less than 10 nm are observed sticking to big Si chunks. In Fig. 3.5 (b), it seems a number of

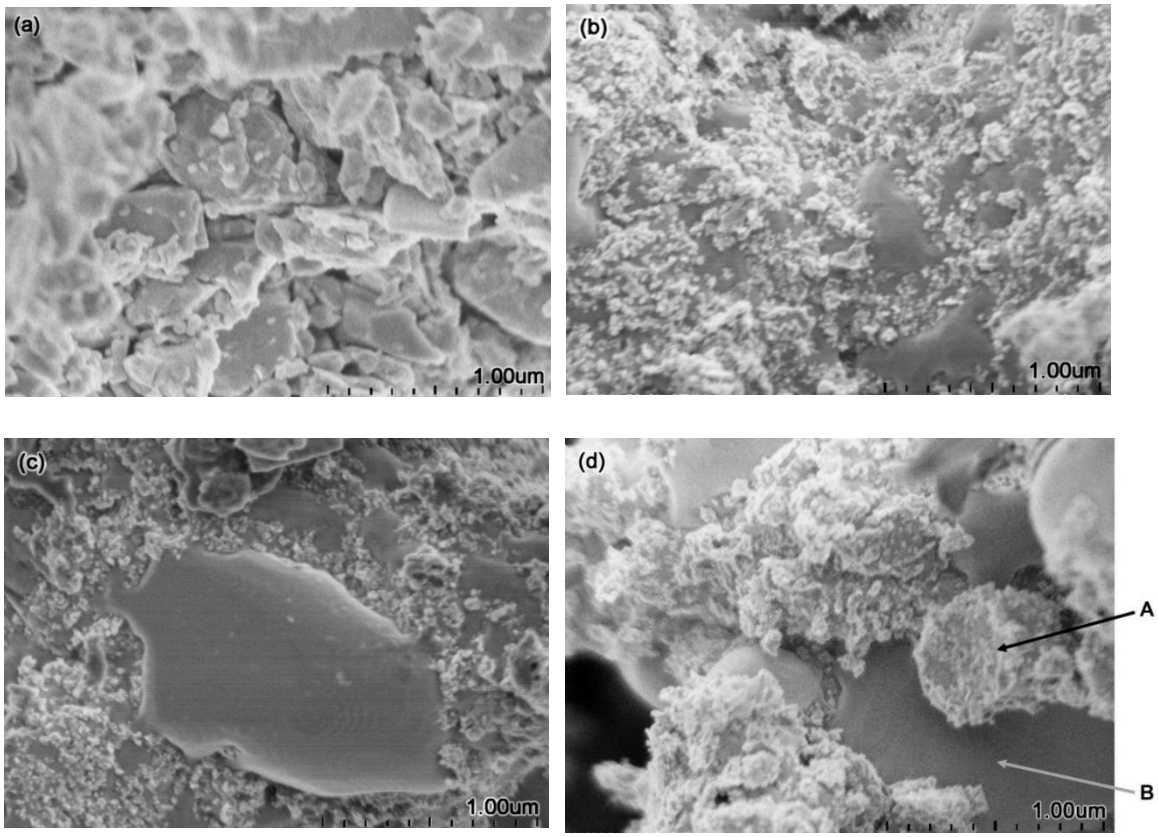


Fig. 3.5 SEM images of cross-sectional morphology of Si paste of (a) non-annealed sample, (b) RTA at 1200°C for 1 s sample, (c) RTA at 1200°C for 2 s sample, and (d) RTA at 1200°C for 2 s sample containing 500 nm-sized cluster marked as A which is considered to be the intermediate of the melting process, and a melted big grain is marked as B.

nano-meter sized Si particles are dispersed over the smooth Si melted surface. This suggested that the Si grains were melted, recrystallized, and coalesced each other by the RTA at 1200°C even within 1 s. Both Fig. 3.5 (c) and (d) show the cross-section part of Si paste annealed at 1200°C for 2 s. In the Fig. 3.5 (c), a clear big melted part in the center is observed, 10 nm-sized Si particles become less than the sample annealed for 1 s as showed in Fig. 3.5 (b). Fig. 3.5 (d) shows the intermediate part of the melting process at 1200°C for 2 s. There are two different structures observed in Fig. 3.5 (d). A-region seems to be formed with many small particles melted and coalesced into bigger particles with a size of about 500 nm as marked with an arrow A. B-region shows complete melt of big particles with smooth surface which is marked with an arrow B.

It can be speculated that the A-region continued to melt and coalesced to the B-region.

It is well known that the melting point of crystalline Si is about 1410°C, which is much higher than the RTA condition (at around 1200°C) in this chapter. Generally, there are two approaches to lower the melting point, one of which is to increase the surrounding atmospheric pressure, thus decreasing the distance between atoms and increasing the vibration of atoms. The other approach is to adulterate with impurities elements, such as alloys. However, these explanations do not apply very well in the case of Si paste. The mechanism of Si particle melting under the temperature lower than equilibrium melting point of crystalline Si will be discussed.

3.3.4 I-V characteristic of Si paste device

Fig. 3.6 (a) shows dark and illuminated (AM1.5) I-V characteristic of pn-device made with the RTA at 1200°C for 1 s, and an inset of Fig. 3.6 (a) depicts the device structure. The theoretical fitting using eq. (2-5) is shown in Fig. 3.6 (a) with a blue dash line. The measured characteristic is in good agreement by using the fitting with an ideality factor $n = 4.1$, the reverse saturation current density of 1.5×10^{-5} A/cm^2, and the series resistance of 101 Ω. The rectification on/off ratio was 202 at ± 1 V.

It should be noted that the resistance of Si paste device using RTA process is at least one order of magnitude lower than that of the device using low temperature annealing and AIC technology in the Chapter 2. The reasons are: (1) the oxidation is significantly reduced due to abruptly shortened annealing duration; (2) owing to the melting phenomenon as shown in SEM images, the voids inside the Si paste are significantly reduced, thus more conductive channels can be established.

The enlarged photovoltaic characteristic is shown in Fig. 3.6 (b). The short circuit current density is J_{sc}= 10 μA/cm^2, and open-circuit voltage is V_{oc}= 225 mV. The short

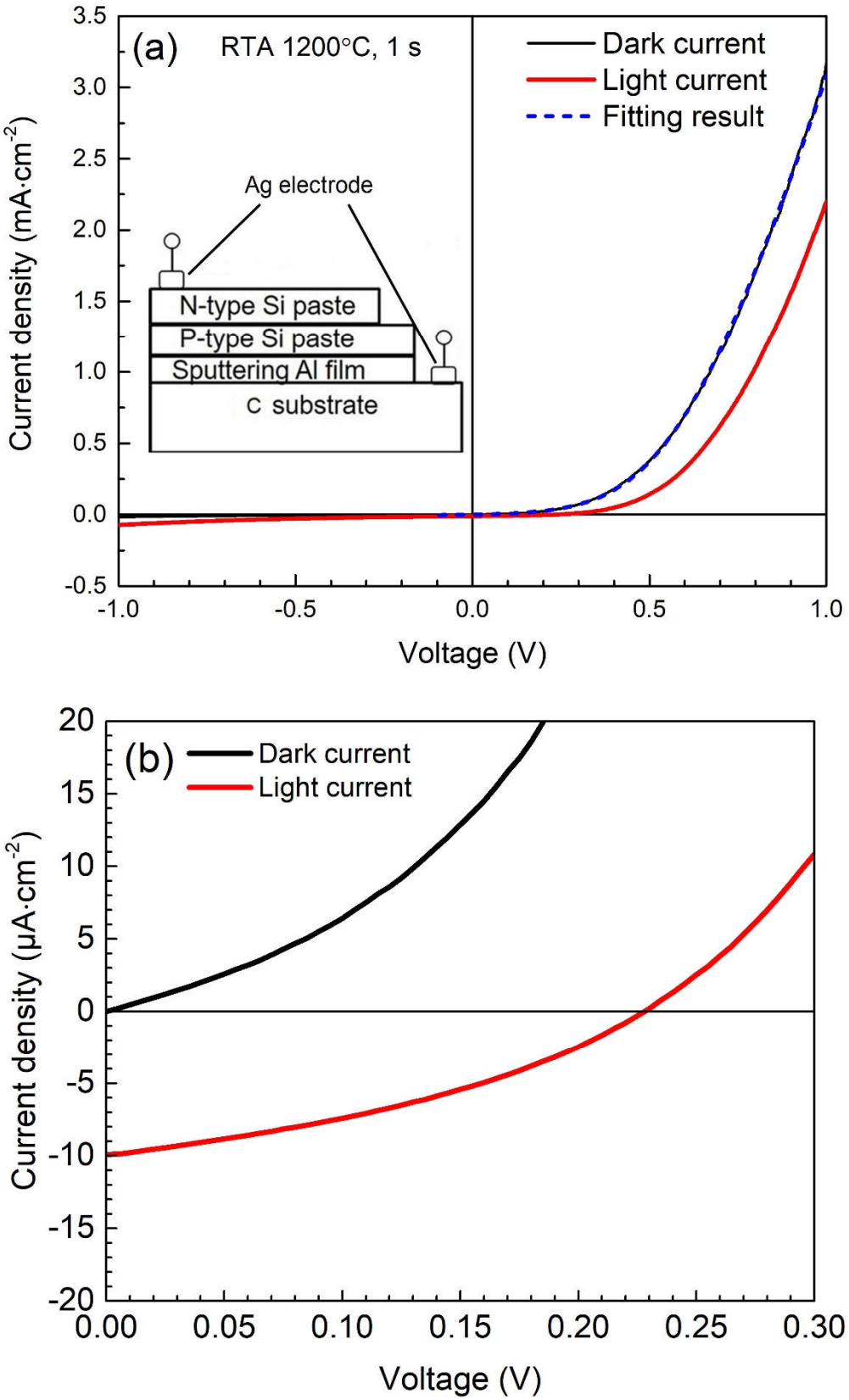


Fig. 3.6 (a) I-V characteristics and fitting results of Si paste pn homo-junction device (RTA at 1200°C for 1 s) with or without AM1.5 illumination, (b) enlarged figure showing photovoltaic characteristics.

circuit current as a solar cell is also much higher than the Si paste device in the Chapter 2, which also indicates the important role of RTA process. However, there is a huge gap in photovoltaic performance compared to conventional solar cells. Since the oxidation still take place as shown by FT-IR spectra, and the Si paste film does not completely melt during the RTA process, this limited output power can be mainly attributed to the still existing pores, defects, and oxides in the Si film. Those pores, oxides and defects in the Si film cause the high resistance and low diffusion length resulting in the small J_{sc} and V_{oc}.

3.3.5 Models of molten Si particles in the Si paste

It is well known that the melting point of bulk Si is about 1410°C; therefore, at the annealing temperature of 1200°C in this study, larger Si chunks should not melt. Even Si is almost transparent to infrared light [22], the C substrate, a black body, can absorb the infrared light [23]; therefore, Si particles can be heated up from the Si paste/C substrate interface even within one second. On the other hand, the lowered melting point of Si can be investigated as discussed below.

In 1910, Lindemann [24] states that melting process starts when the atomic vibration amplitude becomes large enough for adjacent atoms to occupy the space of local atom,

$$T_m = \frac{2\pi m c^2 a^2 \Theta_D^2 k_B}{h^2} \tag{3-1}$$

$$\Theta_D = \frac{\hbar \omega_D}{k_B} \tag{3-2}$$

where m is the atomic mass, ω_D is the Debay frequency describing the movement of ions in a crystal lattice, k_B is the Boltzmann constant, T is the absolute temperature, c is

the Lindemann constant, $\hbar$ is reduced Planck constant, and a is the atomic spacing. The Debay temperature for Si is Θ_D=372°C, and the melting temperature is T_m=1410°C. However, this theory is only appropriate for bulk Si, if the Si particle size is in nanometer order, the size effect will be predominant owing to the enormous surface energy. Buffat and Borel [25] found that T_m of a particle with radius r is linearly dependent on r^{-1} as shown below,

$$T_m(r) = T_0\left\{1 - \frac{2}{L\rho_s r}\left[\gamma_s - \gamma_l\left(\frac{\rho_s}{\rho_l}\right)^{2/3}\right]\right\} \tag{3-3}$$

where melting temperature of bulk silicon is T_0=1683 K, heat of fusion is L=1105 J/g, the density of the liquid phase is ρ_l=2.53 g/cm^3, the density of the solid phase is ρ_s= 2.33 g/cm^3, liquid-gas surface energy is γ_l=0.735 J/m^2, and solid (111)-gas surface energy is γ_s=1.74 J/m^2. The existence of Si particles with a radius of 5 nm was confirmed by the peak deconvolution of Raman and SEM figures as shown in Fig. 3.5 (a). The melting point of this 5 nm Si particles can be estimated as low as 1180 °C according to eq. (3-3), as shown in Fig. 3.7.

When the Si particle sizes decrease after the PBM procedure, the specific surface area will increase drastically. Higher surface area to volume ratio means that the particles have more chances to interact with those oxygen atoms existing in the surrounding environments, making the particles vulnerable to be oxidized. Basically, native oxides are not desired in this study, since SiO_x is an insulator and strongly impacts the conductivity of Si pastes. Although the major steps of Si paste preparation were conducted in the ambient of inert N_2 or Ar gases, the Si crystallites in the pastes are still oxidized to some degree and form the so-called core-shell structure. This core-shell structure consists of a crystalline core of Si with a surrounding amorphous SiO_x

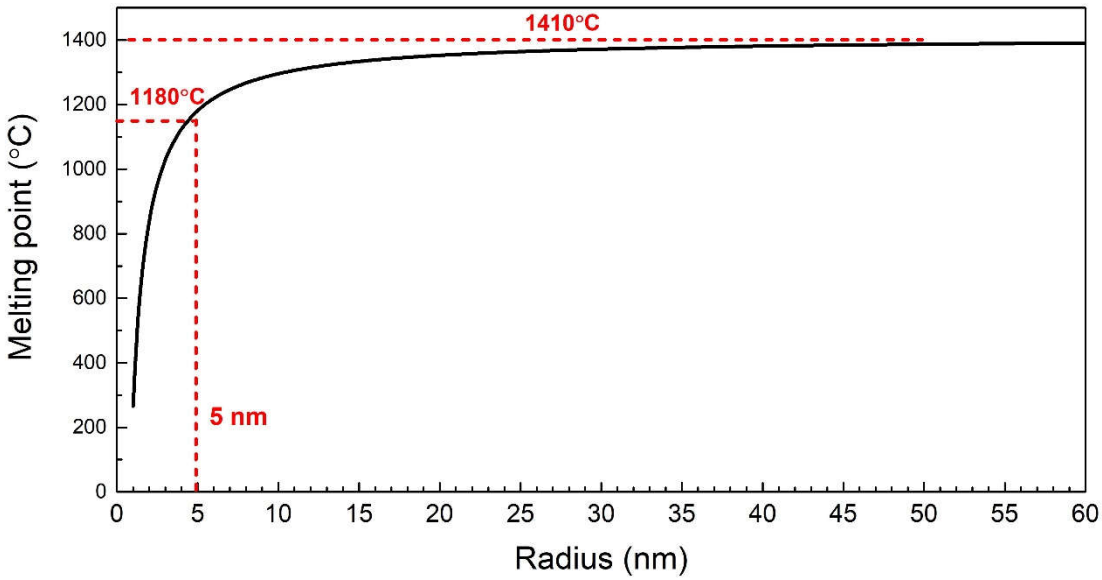


Fig. 3.7 Size effect on melting point of Si particles.

shell with a thickness of a few nanometers [26].

Since the melting point of amorphous SiO_x is around 1713°C [27], which is much higher than that of bulk Si (1410 °C), in order to have Si nanoparticles molten and coalesce with each other, the amorphous SiO_x shell needs to be removed. If there is no oxygen, it is proved that above 900°C, the disproportionation:

$$SiO_x \rightarrow \frac{x}{2}SiO_2 + \left(1 - \frac{x}{2}\right)Si \tag{3-4}$$

becomes kinetically relevant, and the changes induced in the surface chemistry may allow the coagulation of Si particles [28].

Although the 10 nm-sized Si particles melt at the first step of the melting process, it should be noticed that the melting point of particles larger than 20 nm is almost same as that of bulk Si (1410°C) according to eq. (3-3). As it was mentioned above the average grain size of non-annealed Si paste was about 63 nm from the XRD results using Scherrer equation. Moreover, according to the Raman peak deconvolution result,

about 10 nm-size Si particles seem to occupy around 50%; therefore, it implies that the average grain size of other remaining particles could be about 120 nm. It is obvious that the melting point of these particles is almost same as bulk Si (1410°C); therefore, it is supposed to be no melting process if there are only these larger particles existing during the annealing.

A possible mechanism model is proposed to explain that how these large Si particles continue to melt and coalesce each other even at lower temperature than Si bulk melting point. For the model calculation, according to the above XRD and Raman results, intermediate size Si particles in non-annealed Si paste with a radius of r_3= 60 nm surrounded by many r_1= 5 nm Si particles are presumed as shown in Fig. 3.8. When the temperature reaches around 1180°C, the smallest r_1(5 nm) Si particles start melting, and these molten droplets wrap up the surface of the r_3(60 nm) particle. Due to the reduction of the free surface in this process, the exothermal energy is gained and will trigger the melting of r_3 particles. Then further coarsening process proceeds and forms r_2(180 nm) Si particles which is presumed from the above FWHM XRD results of the Si (111) peak that showed that the average grain size of annealed sample was around 360 nm.

In this model the number of r_1(5 nm) particles *n* can be calculated from the volume difference of the final r_2(180 nm) particle and the prior melting r_3(60 nm) particle divided by the volume of r_1(5 nm) particle as following eq. (3-5),

$$n = \frac{V_2 - V_3}{V_1} = \frac{r_2^3 - r_3^3}{r_1^3} \approx 45000 \qquad (3\text{-}5)$$

where V_1, V_2 and V_3 are the volumes of r_1, r_2 and r_3 particles, respectively.

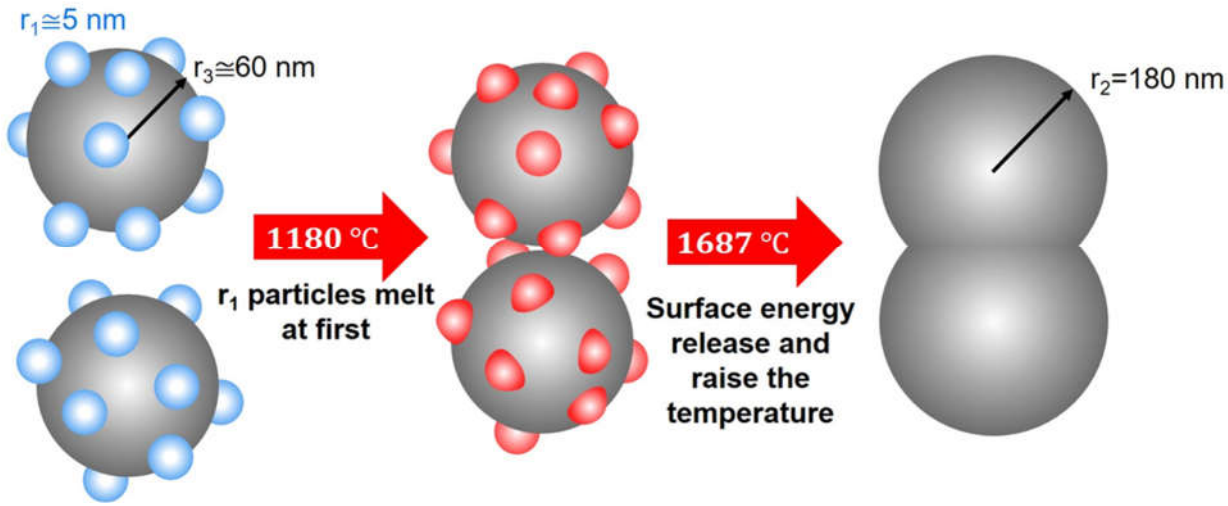


Fig. 3.8 Schematic diagram of the melting and clumping process of Si nanoparticles. A schematic diagram of the smaller $\boldsymbol{r_1}$ particles melt and attach to larger neighboring $\boldsymbol{r_3}$ particles giving exothermal contributions are shown.

It was confirmed that such large numbers of r_1 particles can exist according to the following three phenomena; (I) Raman peak deconvolution of non-annealed Si paste showing possibly 10 nm-sized particles occupy roughly around 50% of paste as showed in Fig. 3.2 (c); (II) observation of thousands of 10 nm-sized particles covering the surface as shown in Fig. 4 (b); and (III) estimation of the average grain size of non-annealed Si paste to be around 63 nm from the FWHM of XRD pattern as showed in Fig. 3.3. However, the SEM figure of non-annealed samples in Fig. 3.5 (a) did not show large amount of around 10 nm size Si nanoparticles. The reason might result from that the binding force of the small Si particles is too weak to stay during the braking process of the cross section.

For calculating the temperature raise in case of the above model is that, particles with a mean radius of r_1(5 nm) melt and wrap up the neighboring particle of r_3(60 nm) in liquid phase, then they solidify and form a particle of r_2(180 nm). Since the free surface area of r_1 particles plus r_3 particle is bigger than final r_2 particle, excess energy comes from the reduction of surface energy during coagulation. This energy is

considered to be calculated from the free surface area change ΔA times surface tension γ_s of Si as following:

$$\Delta E = \Delta A \times \gamma_s = [-(n \times r_1^2 + r_3^2) + r_2^2] \times 4\pi \times \gamma_s \approx -2.4 \times 10^{-11}\ \mathrm{J} \quad (3\text{-}6)$$

Such free surface energy release can heat up the surrounding temperature of r_2 particle and make the particle temperature higher than that of the RTA furnace setting. For calculating the temperature rise due to the free surface energy release, the volume of the final r_2(180 nm) particle should be considered as following:

$$V_2 = \frac{4}{3}\pi r_2^3 \approx 2.4 \times 10^{-14}\ \mathrm{cm}^3 \quad (3\text{-}7)$$

Thus, the temperature rise due to the release of surface energy is calculated as following:

$$\Delta T = \frac{\Delta E}{\rho V_2 C} \approx 487°\mathrm{C} \quad (3\text{-}8)$$

where C is the heat capacity of Si, ρ is the density of Si. Therefore, the r_2 particles are heated up for 487°C excessively, and the particle temperature reaches above the melting point of bulk Si (1200+487=1687°C), as a result, the r_2 particles can start melting.

It is still at the initial development stage of Si paste device process; therefore, the conversion efficiency of device fabricated by Si paste is not yet comparable to the commercial ones. Nevertheless, in order to improve the solar cell performance, further optimization in thermal annealing process is necessary to eliminate the oxidation and have entire Si particles to melt and coalesce during the RTA process. It should be

noticed that the purpose of this study is in introducing the Si paste as an inexpensive technology in order to lower the solar cell cost. On the other hand, it is desired that power conversion efficiency of the solar cells fabricated with this RTA process will reach closer to that of polycrystalline Si solar cells in future.

3.4. Conclusions

The RTA process was successfully performed on the PBM Si paste in order to form a Si film. It was found that the Si particles can be melted at 1200°C even in 1 s duration. This lowering of Si melting temperature appears to be due to the size effect of Si nanoparticles that cause exothermal energy from the surface energy release during the melting process, thus caused melting of larger micro-sized Si particles. The melting process played a significantly role in the closure of pores between the Si particles and the recrystallization process of Si grains, which would contribute to the crystallization improvement. From the FTIR measurement of the annealed Si paste it was found that the oxidation after the 1s RTA was much less than that after a longer conventional thermal annealing for 30 min due to the abruptly shortened annealing duration. Raman spectra revealed that the tensile stress from the ball milling was also relieved after the RTA process. A pn junction fabricated with the RTA at 1200°C for 1s exhibited a rectification characteristic of 202 @ ±1 V, the series resistance of 101 Ω which was more than one order of magnitude smaller than the sample in Chapter 2 (1.8 kΩ), and a much higher photo current density of 10 μA/cm^2 than that of the sample in Chapter 2 (0.058 μA/cm^2). It was considered that both the melting process and sharply reduced oxidation made contribution to much lower resistance and higher photocurrent than that of the Si paste device using low temperature annealing and AIC technology as performed in the Chapter 2.

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CHAPTER 4:

TiO_2/p-Si Paste Heterojunction Fabricated by Rapid Thermal Annealing

4.1. Introduction

Since Si paste device developed in our lab needs to undergo an annealing process to enhance the crystallization and conductivity before use as a semiconductor devices. It has been found in the previous studies [1–3] that the Si paste is seriously oxidized, even though the whole annealing process is conducted in ambient high purity inert gas. The reasons are the high surface to volume ratio of nano-crystal Si in the Si paste and residual oxygen in the voids. Some attempts have been made to reduce the oxidation, for instance, lowering the annealing temperature [2] as written in the Chapter 2, adopting the RTA process to shorten the annealing duration [3] as written in the Chapter 3, and so on. These methods indeed have some effects on inhibiting oxidation, it will be also desired to further reduce the oxidation by combining other methods. It is considered that by introducing other elements that can be more likely to react with oxygen than Si or even reduce SiO_x, the oxidation level of post-annealed Si paste devices may be further reduced. Along with the introduction of this kind of elements, the structure of Si paste device is required to be redesigned to replace the previous pn homo-junction Si paste device. According to the Ellingham diagram [4], Ti has attracted attention. Ti reacts with oxygen more preferentially than Si. When the Ti layer is deposited on the surface of the Si paste film, the Ti layer will react with oxygen instead of the Si paste as an oxidation sacrifice layer during the annealing process. Furthermore,

it has been discovered that Ti has a substantial reduction reaction with SiO_2 at high temperatures [5]. On the other hand, after the oxidation process of the Ti layer, TiO_2 can form a heterojunction with p-type Si. Some studies [6–8] suggest that the TiO_2 deposited on c-Si forms a hole-blocking, electron-transparent interface. Namely, at the interface between TiO_2 and p-type Si, there exists a small conduction band barrier ($\Delta E_C \approx 0$ eV), which allows electrons to pass through the TiO_2 and the significant valence band barrier ($\Delta E_V \approx 3.4$ eV) [6], which results in holes being blocked. Therefore, the TiO_2/p-Si heterojunction structure can also be employed in the application of Si photovoltaics instead of the conventional Si homo-junction structure.

In this chapter, the Ti layer was deposited on the surface p-type Si paste to reduce the oxidation of Si paste. At the same time, a diode with the TiO_2/p-Si heterojunction structure was formed during the annealing process. The effect of annealing conditions on the structure and performance of TiO_2/p-Si paste has been studied.

4.2. Experimental methods

4.2.1 TiO_2/p-Si paste heterojunction device preparation

The first part of the experiment is to prepare the p-type Si paste, the procedure of which has been described in section 2.2.1 of Chapter 2. As for the substrate preparation, the same carbon (C) substrates (Toyo Tanso, IG-43) used in the Chapter 3 was first ultrasonically cleaned with ethanol. An Al layer with a thickness of around 100 nm was deposited on the C substrate by RF sputtering as both the back electrode and back surface field (BSF) [9]. Before the Al sputtering process, the main vacuum chamber was pumped to a base pressure of 4×10^{-4} Pa. Next, an Al film was deposited by RF magnetron sputtering at a working pressure of 3.0 Pa with an Ar flow rate of 30 sccm. Finally, the 20 μl p-type Si paste was drawn by a transfer pipette, coated on the Al

sputtered C substrate at once, and dried naturally in the glove box filled with N_2 (6N: 99.9999%). Next, a Ti layer with a thickness of 30 nm was sputter deposited on the p-Si paste film. Considering that Ti is easily oxidized, during the process of vacuuming, the sputtering chamber should be heated by the electric heating wire wound through the outer wall of the chamber. So that the water vapor and other gases adsorbed by the inner wall of the chamber are evaporated. Therefore, it took more than ten hours to reach the base pressure of 4×10^{-4} Pa for the Ti deposition process. The working pressure was controlled as 3.0 Pa with an Ar flow rate of 30 sccm, while the sputtering power was 50 watts. Since the deposition rate of Ti layer was found to be around 10 nm/min at the center of sample holder, the sputtering time was set to 3 min to obtain a Ti layer with thickness of 30 nm. The reasons for choosing a Ti layer thickness of 30 nm lay in: (1) to ensure that the Ti layer can be completely oxidized in the short duration annealing process, such as RTA, especially considering that the whole annealing process is performed in a quartz tube flowing with the inert Ar gas; (2) it has been found that with the thinner Ti layer, the TiO_2/p-Si heterojunction device will show more photocurrent under AM1.5 illuminations due to the higher transmittance of a thinner TiO_2 layer. The previous long time annealing experiments (1100°C/30 min) showed that the transmittance of the thicker TiO_2 film (original thickness of Ti film is around 50 nm) is around 60%, while the transmittance of the thinner TiO_2 film (original thickness of Ti film is around 30 nm) was about 80%. Another series of Ti layers were deposited on the quartz substrates for the transmittance measurement.

All the RTA treatment was performed in an infrared heating tube furnace (Yonekura: IR-QP1-4-S) where four IR lamps were symmetrically place at the top and bottom corners inside the furnace. The samples were placed in the center of a quartz tube which was placed in the middle of four IR lamps. The schematic diagram of IR heating furnace is shown in the Fig. 4.1. During the annealing process, Ar gas (6N:

99.9999%) was continuously flowing through the quartz tube (0.5 L/min). Then the samples were annealed in this furnace at 1200–1300°C for 1–5s. The heating-up rate was about 150°C/s during the heating process, while during the cooling process, the temperature abruptly dropped from peak temperature to 200°C within 10s. An R-type thermocouple was placed as close as possible on the top right of the samples

During the RTA process, the Ti-Si binary system needs to be discussed. The Ti-Si binary phase diagrams are shown in Fig. 4.2 [10]. As for the RTA condition in this chapter, the annealing temperatures were set as 1200~1300°C (below the eutectic temperature 1330°C), a small amount of Si atoms may diffuse into the Ti layer since the diffusion rate of Si atoms is much higher than Ti atoms in the Ti-Si system [11], so only the left region of the Ti-Si phase diagram is needed to be discussed. It is found that under RTA process conducted in this chapter, Ti silicide phases and the solid solution of Ti will be formed at the interface between Si paste and Ti layer whether in the heating or cooling stage. The Ti silicide is considered to be a conductive alloy phase [12], and

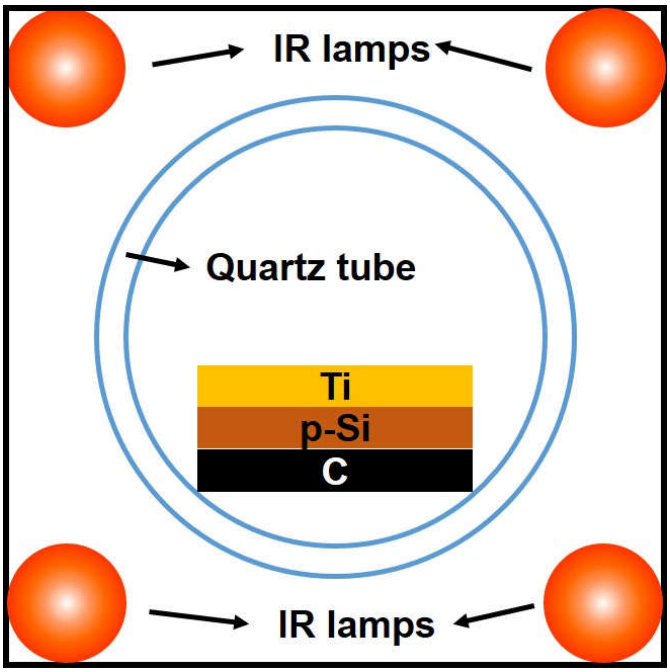


Fig. 4.1 Schematic diagram of the cross section of IR heating furnace.

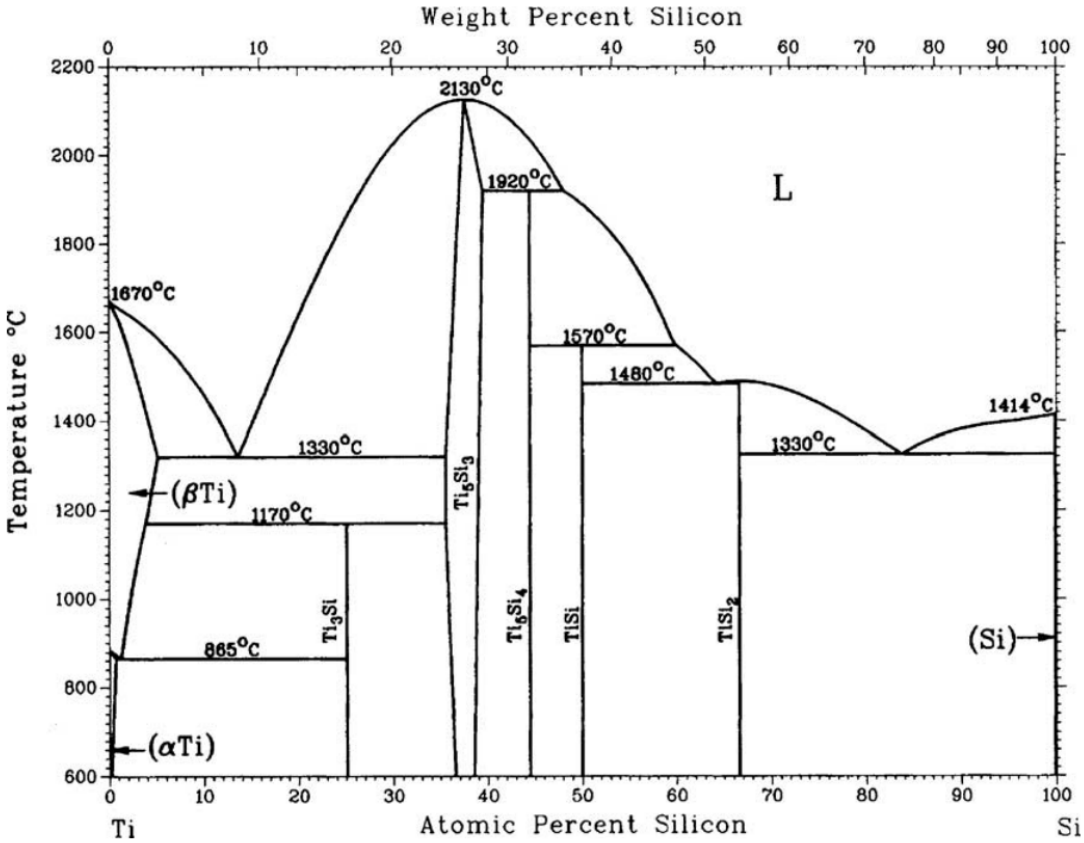


Fig. 4.2 Ti–Si phase diagram (from ref. [10]).

a small amount of Ti silicide rarely has the influence on the TiO_2/p-Si paste device performance.

4.2.2 Optimization of ITO contact preparation

As for the TiO_2/p-Si paste device used to test the current-voltage (I-V) characteristics, an indium tin oxide (ITO) layer was deposited on the post-annealed samples as a top contact in order to keep the transparent appearance and collect the photo generated carriers, the ITO contacts were controlled in circles with a diameter of 1.5 mm by covering a mask, as shown in the Fig. 4.3, with many holes on the samples during ITO sputtering process. In order to prepare the ITO contact with the lowest resistance, the preparation steps are required to be optimized. It has been studied [13–

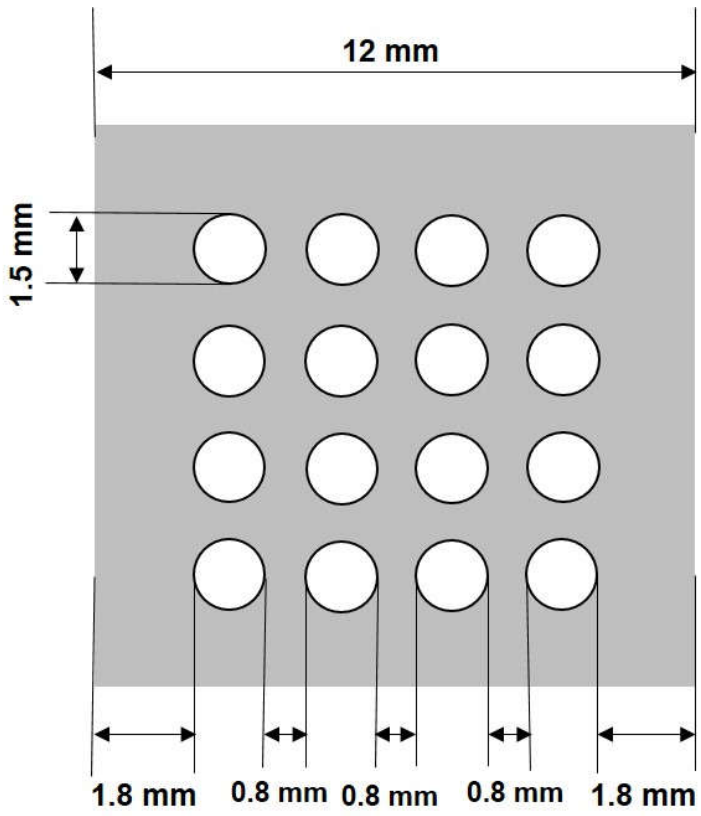


Fig. 4.3 Schematic diagram of sputtering mask used for ITO contacts deposition.

15] that the sputtering power would affect the resistance of ITO films. It was found that in the sputtering power range of 0~100 watts, the resistance of ITO films gradually decreased with the increase of the power, while the variation in resistance of ITO films was not obvious when sputtering power exceeded 100 watts. Therefore, in this chapter, the sputtering power was controlled in the range of 50 to 100 watts to prevent the instrument from being damaged by excessive power. In addition, a post annealing treatment was found to be necessary for ITO films to reduce the resistivity and increase the transmittance in visible light region [16–17]. It was also necessary for eliminating the internal stress at the interface between ITO contacts and the TiO_2 layer during ITO sputtering. Therefore, in this chapter, the post annealing treatment parameters of ITO films has been also optimized.

For the optimization of the ITO films, the ITO films were deposited on quartz

substrates with a size of 10×10×1 mm using a ITO target (oxygen-saturated composition with a formulation of 74% In, 18% O_2, and 8% Sn by weight) and the sputtering powers of 50, 70, 90, and 100 watts, respectively. For the ease of ITO films resistance comparison, the sputtering time was precisely controlled to keep the films thickness almost uniform. As a consequence, the ITO deposition parameters were set as follows: 50 watts/30 min, 70 watts/21.4 min, 90 watts/16.6 min, and 100 watts/15 min. After ITO films deposition, the thicknesses of ITO films were measured by a color 3D laser scanning microscope using violet laser (Keyence, VK-9700). Then, the ITO films were annealed at 200°C, 300°C, 400°C, and 500°C for 1 h, respectively. The rate of temperature change is set to 30°C/min in both the heating and cooling stages. The post annealing treatment of as-deposited ITO films was performed in the same IR heating furnace described in section 4.2.1. During the annealing process, the pure Ar gas (6N) was also continuously flowing through the quartz tube (0.5 L/min). Next, the resistance of non-annealed and post-annealed ITO films was measured by the power device analyzer/curve tracer (Agilent Technologies B1505A). During the resistance measurement, the distance between the two contact needles was kept constant and fixed at diagonal positions on the ITO film surface.

4.2.3 Characterization of TiO_2/p-Si paste heterojunction device

The final part of the experiment was the characterization of the fabricated samples. The X-ray diffractometer (XRD) patterns in the ranges of 20°–90° were obtained with a multi-purpose XRD (Rigaku Ultima IV, Cu Kα radiation, λ=1.54 Å) by using normal scanning mode. Besides, considering that the Ti layer was too thin to collect XRD signals, small-incident angle scanning mode with a fixed incident angle of 1.5° was conducted in the 2θ range of 33°– 42°. Raman spectra were measured by a Laser-Raman

microscope (Nano-photon RAMAN touch) with a 532 nm-wavelength excitation laser to analyze the crystallinity of the samples. The oxidation degrees of the samples were evaluated by the FT-IR (PerkinElmer: Spectrum Two). The cross-sectional microstructure and element distribution of the samples was observed by field emission scanning electron microscopy (FE-SEM) (Hitachi SU8000) equipped with an energy dispersive X-ray spectrometer (EDX, Apollo XLT SDD). Finally, the I-V characteristics of the samples covered with ITO contacts were measured by a power device analyzer/curve tracer (Agilent Technologies B1505A). The performance of the TiO_2/p-Si heterojunction device as a solar cell was also tested by using a solar simulator (Asahi Spectra, LAX-C100, AM1.5). All of the above instrument structures and principles are explained in detail in the section 2.2.3 of Chapter 2.

The transmittance spectra of the Ti layers on the quartz substrates varying different RTA conditions were performed using an ultraviolet (UV) - visible (vis) - near infrared (NIR) spectrophotometer with a model QEPro, from Ocean Photonics, as shown in Figure 4.4 [18]. The transmittance test system consists of five main components: a light source, a sample cell, a spectrophotometer, and a recording device. The light source used in the system is a point light source, and the light emitted from this source is white

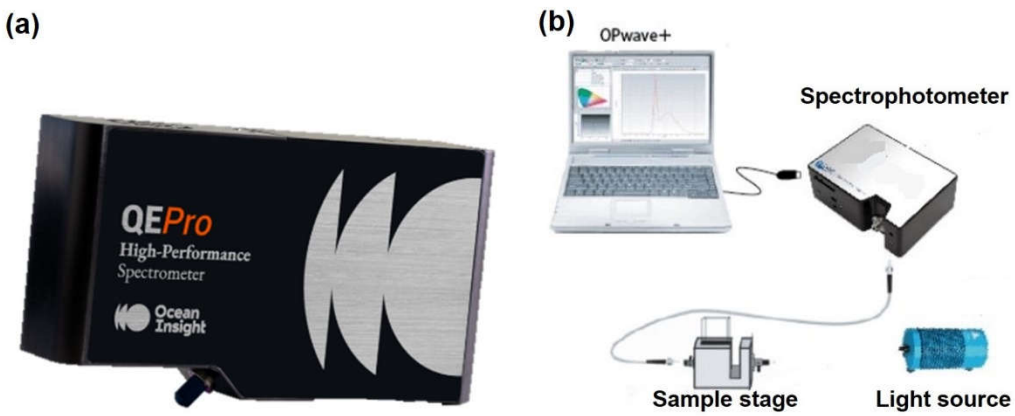


Fig. 4.4 (a) Photo of the UV-VIS-NIR spectrophotometer (Ocean Photonics, QEPro) and (b) the schematic diagram of transmittance measurement [18].

light, while the light used in the test is monochromatic light with continuous wavelength. When the monochromatic light is separated, it is fed into the sample cell through a cutter, and then the final output intensity is read by the detector.

4.3. Results and Discussion

4.3.1 Properties of ITO films

The thickness of ITO films using different sputtering power is shown in the Table 4-1. It is found that the thickness of ITO film does not change so much with the controlled deposition conditions, and they are all around 550 nm. With the higher sputtering powers (90 and 100 watts), the thickness becomes a little bit thinner which may attribute to the re-sputtering effect [19]. That is, the high energy plasma bombardment to the deposited film may cause the deposited atoms to peel off, resulting in slowing down the deposition rate.

The variation of ITO films resistance with sputtering power and post annealing temperature is shown in the Fig. 4.5. It is shown that the resistance of all the as-deposited ITO films decreases with the increase of the post-annealing temperature from 200°C to 400°C, which may be resulted from the relaxation of internal stress during the deposition process and the growth of ITO crystals. However, the resistance of the ITO film annealed at 500°C for 1 h slightly increases compared with 400°C. All the ITO films show the minimum resistance at the post-annealing condition of 400°C. Among them, the ITO film deposited with a sputtering power of 100 watts showed the least resistance of 64 Ω. In the end, the ITO contacts with a thickness of about 100 nm was deposited on the TiO_2/p-Si paste device after RTA treatment as a top contact, and the post-annealing condition of 400°C/1 h was selected to eliminate the internal stress at

Table 4-1 ITO films thickness varying different deposition conditions.

Deposition conditions	50 watts 30 min	70 watts 21.4 min	90 watts 16.6 min	100 watts 15 min
ITO Thickness (nm)	560	570	546	541

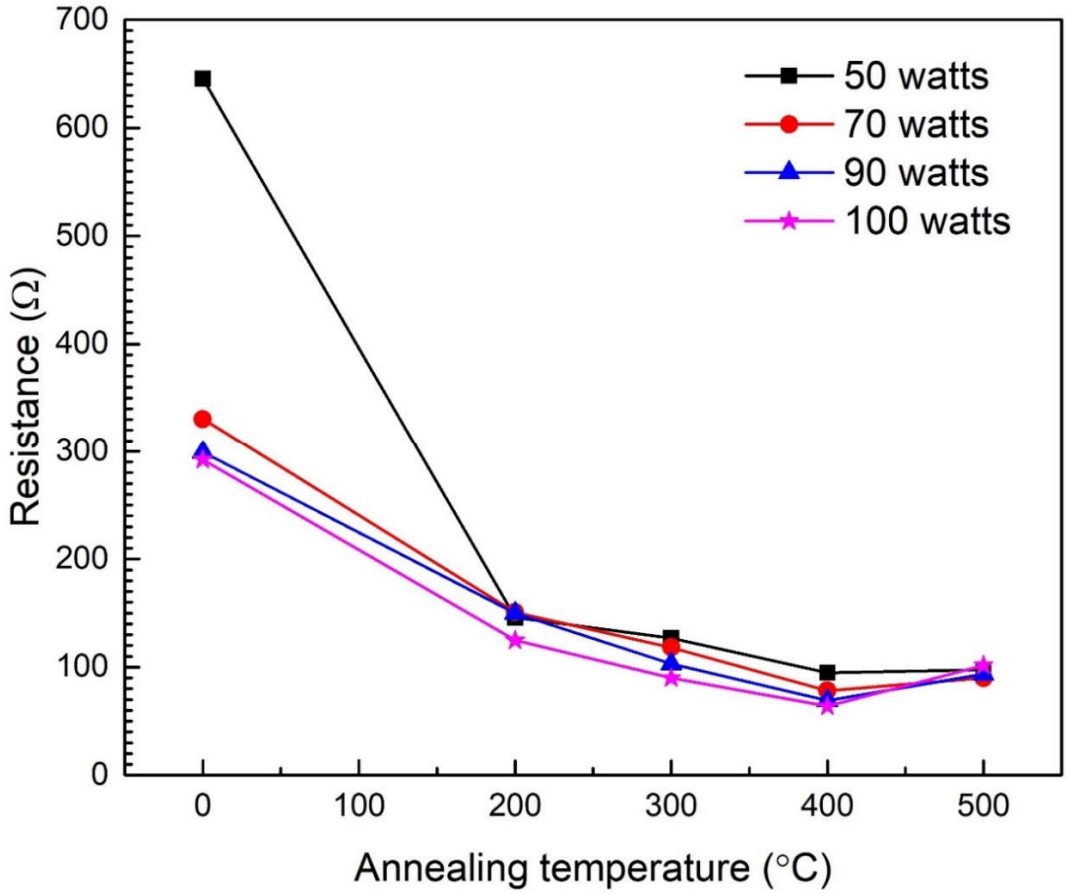


Fig. 4.5 Resistance of ITO films as a function of sputtering power and post-annealing temperature.

the interface between ITO film and the TiO_2 layer and to reduce the ITO contact resistance.

4.3.2 Crystal structure of TiO_2/p-Si paste device

Fig. 4.6 (a), (b), and (c) show the XRD patterns of the p-type Si pastes covered with Ti layer before and after different RTA conditions in the ranges of 20°– 90°, 27.0°–30.0° and 33.0°– 42.0°, respectively. Three typical Si peaks, Si (111), Si (220), and Si (311) are observed in the Fig. 4.6 (a), which indicates the polycrystalline structure in the Si paste. During RTA treatment, Si crystallites oriented preferentially along the (111) plane. Hence the Si (111) peak centered at around $2\theta = 28.6°$ shown in Fig. 4.6 (b) is selected to compare the crystallization conditions.

All the post-annealed samples show sharper Si (111) peaks and stronger peak intensities than that of the non-annealed samples. On account of the high-temperature thermal treatment, the Si particles in the Si pastes recrystallize and grow bigger, eventually enhancing crystallization. Among all the post-annealed samples, the sample annealed at RTA 1200°C for 2 s shows the least FWHM value of 0.08°, thus confirming the best crystallization. However, the previous experiment in Chapter 3 suggests that the Si paste annealed at RTA 1200°C for only 1 s already shows the best crystallization. This difference is considered to be have resulted from the existence of the surface Ti layer. The Ti layer is not transparent to infrared light [20]; therefore, when the p-Si paste covered with Ti layer samples is annealed inside the infrared furnace, the Ti layer reflects a portion of infrared light. The Si paste layer underneath the Ti layer absorbs less heat than Si paste without the Ti layer.

When the annealing temperature becomes higher than 1200°C or duration becomes longer than 2 s, the Si paste will be more oxidized, then the X-ray intensities of the Si (111) peaks decrease slightly. Even so, the Si peak intensity of the sample annealed at RTA 1200°C for 5 s is surprisingly weakened compared with other post-annealed samples. This phenomenon can be explained by Fig. 4.6 (c). Fig. 4.6 (c) shows

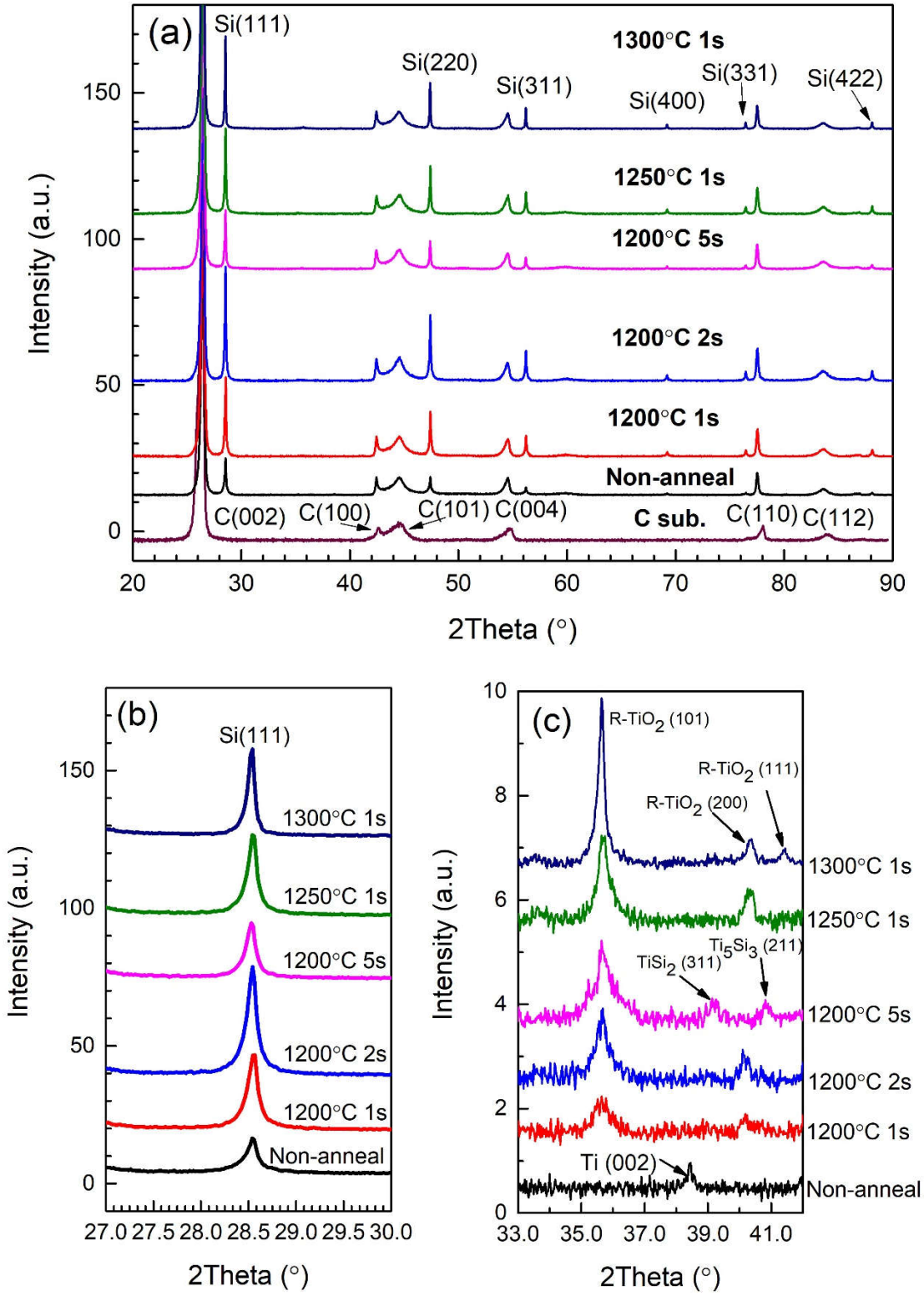


Fig. 4.6 XRD patterns of the p-type Si pastes films on C substrates covered with 30 nm Ti layer before and after the different RTA conditions. 2 theta angles ranges are (a) 20°–90°; (b) 27.0°–30.0° and (c) 33.0°– 42.0°.

that the metallic Ti phase of the post-annealed samples transforms into the TiO_2 phase, which indicates that the Ti layer is actually oxidized even after rapid annealing in an inert atmosphere. Since one phase of TiO_2 (anatase TiO_2) is a metastable phase and easily converts into the rutile TiO_2 phase at above 800°C [21], only the rutile phase TiO_2 exists in the post-annealed samples above 1200°C. It should be noted that only the sample annealed at RTA 1200°C for 5 s shows the $TiSi_2$ and Ti_5Si_3 phases, while the samples annealed at higher temperatures do not show these silicide phases. Considering the sharp heating (~150°C/s) and cooling (~ -120°C/s) rates in the RTA process, the sample annealed at 1200°C for 5 s experiences a longer annealing duration than the sample annealed at 1300°C for 1 s. Thus Ti atoms in the sample annealed for 5s will diffuse more into the solid Si and form these silicide phases. These silicide alloy phases may work as conductive metal and invalidate the TiO_2/p-Si paste heterojunction structure [12]. The existence of these silicide phases also explains why the Si (111) peak intensity of the sample annealed at RTA 1200°C for 5 s weakens so dramatically. as shown in the Fig. 4.6 (b).

The Raman spectra of the p-type Si pastes covered with Ti layers with varying RTA conditions are shown in Fig. 4.7 (a). The spectrum for a c-Si wafer is selected as a reference to evaluate the crystallinity of samples. The Si Raman peaks of all the samples undergoing the RTA process shift towards higher wavenumbers towards 520.5 cm^{-1} for the reference c-Si wafer; in contrast, the peak position of the non-annealed Si paste is located at 518.6 cm^{-1}. This shift of Si peaks can be interpreted as the relaxation of tensile stress in the Si paste, which results from the distortion of the Si lattice by the ball milling process [22]. Therefore, the peak shape of the films after annealing becomes sharper as its FWHM actually becomes closer to that of the reference c-Si, indicating an increase in crystallinity by annealing. In addition, the Si peak of the sample annealed at RTA 1200°C for 1 s is broader and located at a lower wavenumber

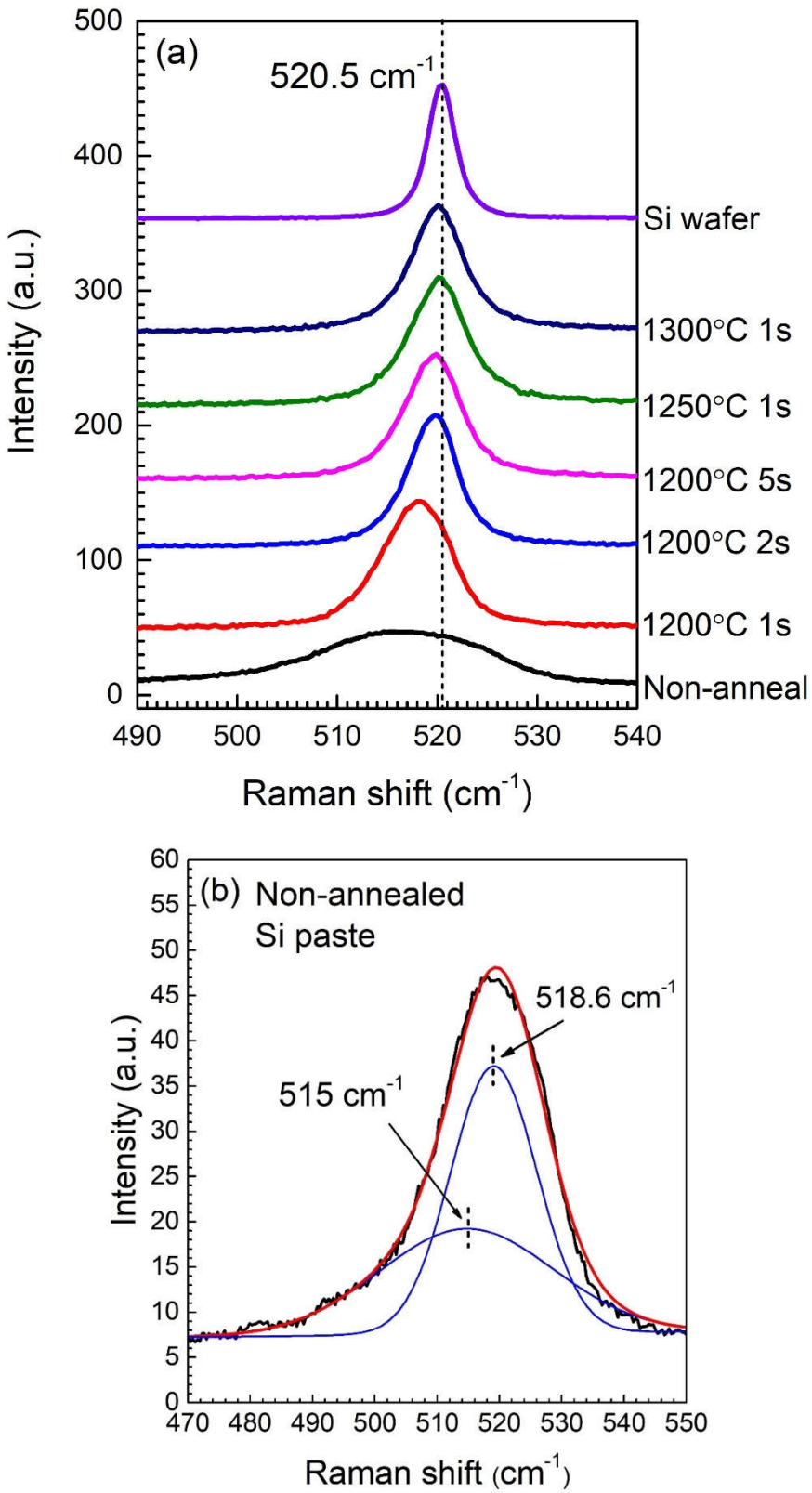


Fig. 4.7 Raman spectra of (a) the Si wafer and the p-type Si pastes films on C substrates covered with 30 nm Ti layer under various RTA conditions, and (b) the deconvoluted peaks of non-annealed Si paste showing the existence of Si nanoparticles with a size less than 10 nm.

compared with other post-annealed samples (RTA 1200°C for 2 s~5 s, RTA 1250°C/1 s, and RTA 1300°C/1 s), which can be explained by the sample not absorbing enough heat for recrystallization. This phenomenon is consistent with the XRD results as shown in the Fig. 4.6 (b): the sample annealed at RTA 1200°C for 1 s shows poorer crystallization condition. The deconvolution of the 518.6 cm^{-1} peak for the non-annealed Si paste using two Gaussian distribution functions is shown in Fig. 4.7 (b). The broad peak centered at a lower wavenumber of 515 cm^{-1} is attributed to small crystallites with diameters below 10 nm [23], thus suggesting the inclusion of a number of Si nano-crystals, as also shown later by SEM.

4.3.3 Oxidation of TiO_2/p-Si paste device

Figure 4.8 gives the FT-IR spectra of the p-type Si pastes with and without Ti layer undergoing various RTA conditions to evaluate the degree of oxidation. As for the non-annealed Si paste, since the present FTIR instrument can only measure the samples with one reflection, the sensitivity is not enough for detecting the native oxide shell, which is thinner than 1 nm, of Si nanoparticles in the Si paste [24]. After the RTA treatment, the peaks located at around 800.0 cm^{-1} become much bigger. Generally, three absorption peaks correspond to various Si-O transverse-optic (TO) vibrational modes, as shown in the Fig. 2.7 of section 2.2.3 in the Chapter 2. Among them, the 800.0 cm^{-1} absorption peak attributes to the symmetrical stretching mode (SS) [25]. The sample with a more prominent oxidation peak directly indicates more oxidation in the Si paste. Compared with the Si paste without Ti layer annealed at RTA 1200°C for 1 s, all the Si pastes covered with Ti layer annealed at RTA 1200°C from 1 s to 5 s show much less oxidation peak areas which reveals that the Ti layer can effectively reduce oxidation. On the other hand, the samples annealed at the higher temperatures (RTA 1250°C, 1300°C) even for

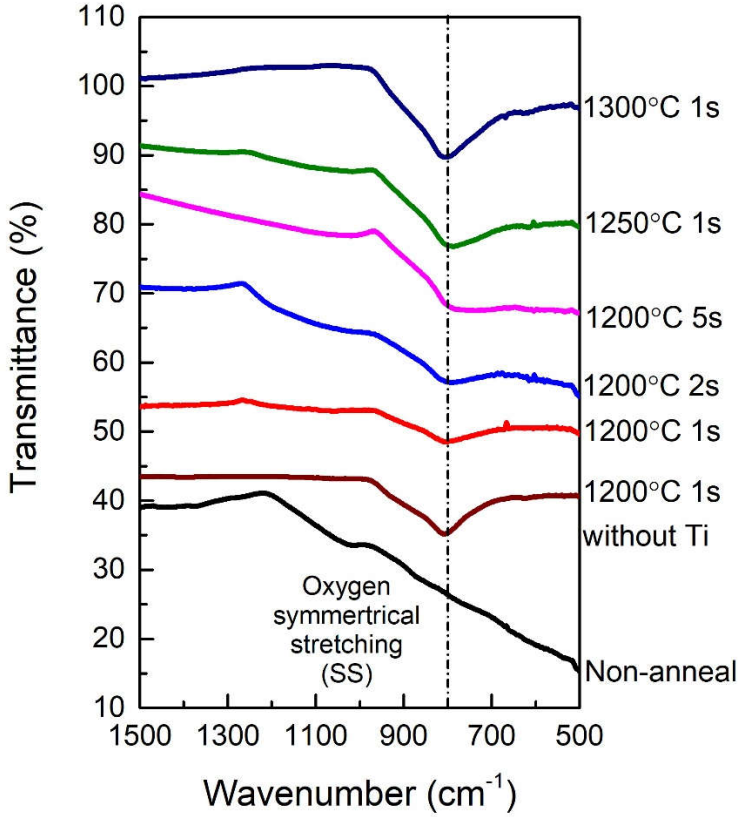


Fig. 4.8 FT-IR spectra of the symmetrical stretching Si-O bond peaks of the p-type Si pastes with and without the Ti layer before and after the different RTA conditions.

1 s, the oxidation peaks become somewhat more significant than RTA 1200°C samples. Besides, rutile phase TiO_2 is also infrared-active and can be detected by FT-IR. However, the Ti-O bond vibrations, which should be observed in the ranges of 493–579 cm^{-1} and 594–639 cm^{-1} [26], maybe too weak to be detected due to the very thin Ti layer. It should be also noted that there are no other bonds involving other impurities in the whole range of FTIR spectra (450~4000 cm^{-1}) for all Si paste samples

4.3.4 Transmittance of TiO_2 films

The transmittance spectra of the Ti films deposited on quartz substrates undergoing different RTA conditions are shown in the Fig. 4.9. Optical transmittance spectra have been measured at a normal incidence in the spectral ranges of (430–1200) nm using a

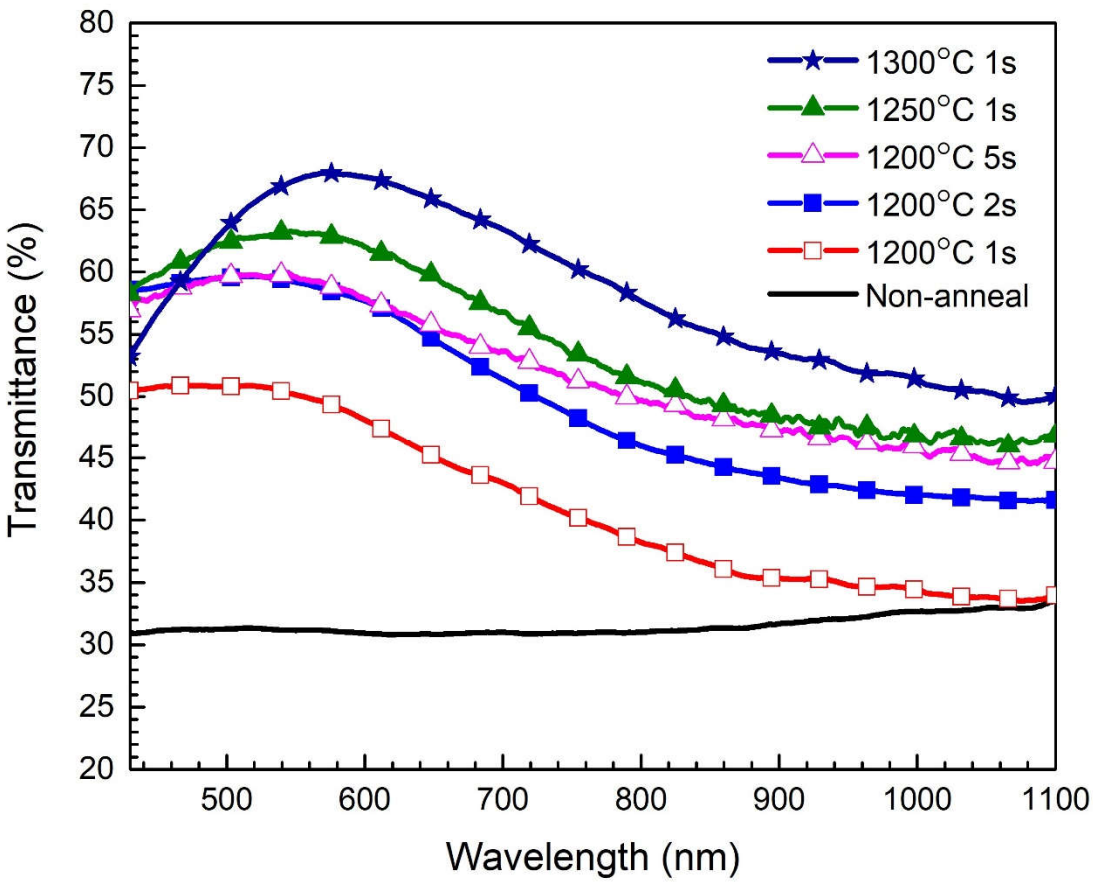


Fig. 4.9 Transmittance spectra of the Ti films deposited on quartz substrates undergoing different RTA conditions.

reference bare quartz substrate. All the post-annealed samples were more transparent than non-annealed Ti film, implying that the metallic Ti phase transforms into a transparent TiO_2 phase. In addition, the transmittance of the post-annealed samples increases with the increase of annealing duration and the annealing temperature. For example, the sample annealed at RTA 1300°C for 1 s shows the highest transmittance, which can be explained by its best crystallization condition, as shown in XRD result of Fig. 4.6 (c). During grain growth, the grain boundary decreases, thus weakening the scatter effect of the incident light.

All the post annealed samples show their highest transmittance as well as the first interference fringes at the wavelength of around 500 nm where the constructive interference occurs. Then the transmittance decrease with the increase of the incident

light wavelength. This phenomenon can be explained by the increased reflectance in the longer wavelength range (500~1100 nm), since there is a relationship between the transmittance T and reflectance R:

$$T = 1 - R \tag{4-1}$$

Besides, the reflectance can also be estimated by the Fresnel equation:

$$R = \frac{a-b+c\cos\varphi}{a+b+c\cos\varphi} \tag{4-2}$$

$$a = (n_0^2 + n^2)(n^2 + 1) \tag{4-3}$$

$$b = 4n_0n^2 \tag{4-4}$$

$$c = (n_0^2 - n^2)(n^2 - 1) \tag{4-5}$$

$$\varphi = \frac{4\pi nd}{\lambda_0} \tag{4-6}$$

where n_0 and n represent the refractive indices of quartz substrate and TiO_2 film, as shown in the inset of Fig. 4.10 (a), respectively, d stands for the thickness of TiO_2 film, and λ_0 is the wavelength of incident light. It should be noted that although the initial thickness of Ti film is around 30 nm, after RTA process, this thickness significantly increases due to the phase transformation of metallic Ti into rutile TiO_2 [27]. However, the thickness of TiO_2 films cannot be accurately measured by SEM observation in this research. Therefore, d is set from 40 nm to 70 nm during the theoretical calculation of reflectance. Furthermore, it has been found that the refractive indices of quartz and rutile TiO_2 do not vary much in the wavelength range of 400 to 1100 nm, the average $n_0 \approx 1.45$, $n \approx 2.60$ [28] can be used to estimate the reflectance. At last, the theoretically estimated reflectance and transmittance spectra can be obtained in Fig. 4.10 (a) and (b),

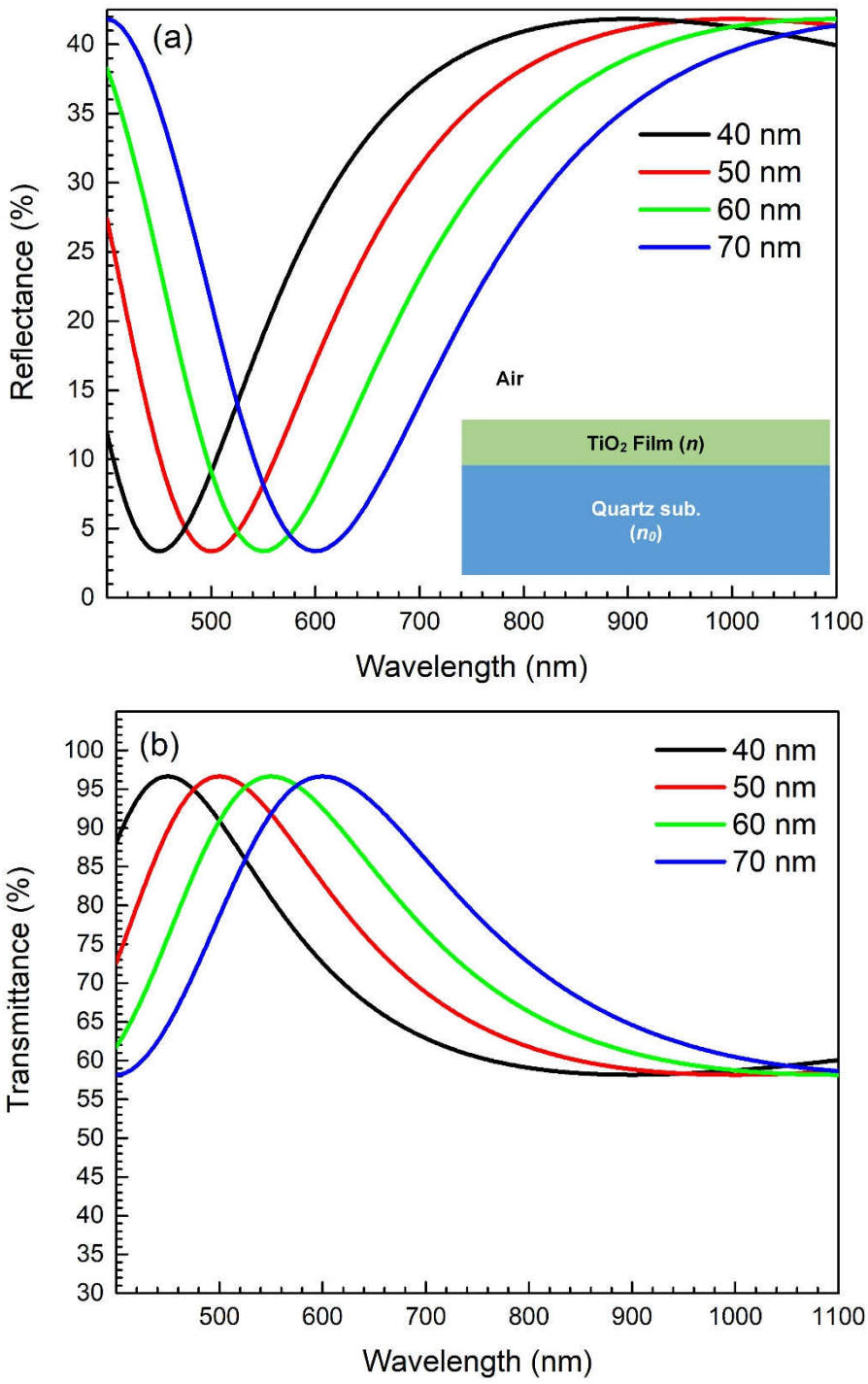


Fig. 4.10 Theoretically estimated (a) reflectance and (b) transmittance of TiO_2 films with different thickness.

respectively.

It is shown that all the interference fringes peaks are observed located in the wavelength range of 400 to 600 nm, which is consistent with the transmittance spectra.

Besides, according to the locations of these interference fringes peaks, the TiO_2 film thickness can be also estimated. It is found that the interference fringes shift towards longer wavelength with the increase of RTA temperature and RTA duration, as shown in Fig. 4.9. Therefore, the thickness of these TiO_2 films after RTA process can be estimated in the range of 45 to 70 nm that Ti thickness of 30 nm had increased after the oxidation.

4.3.5 SEM observation of TiO_2/p-Si paste device

Figures 4.11 (a)–(f) show the cross-sectional morphologies of the Ti/p-Si paste samples under various annealing conditions and Ti distribution in the film. The morphology of the Si paste film before thermal treatment is shown in Fig. 4.11 (a). The Si grains appear to be not tightly bound to each other; therefore, it is challenging to form conductive channels for carrier conduction. Meanwhile, it could be observed that there are some Si particles with both small sizes (~10 nm) and larger sizes (~100 nm) existed in the Si paste. The Ti layer with a thickness of 30 nm on the surface of Si paste is too thin to be observed by SEM on the rough Si paste surface. On the other hand, Ti can be detected on the surface of the Si paste film by using EDS analysis, as shown in Fig. 4.11 (b). It should be also noted that there are no other significant impurities contained in the Si paste as shown by the EDS spectra.

The cross-sectional view of the Si paste film annealed at RTA 1200°C for 1 s is shown in Fig. 4.11 (c). The annealing conditions are similar to the previously reported procedure in the Chapter 3, however, Si paste with Ti layer on the top does not show the similar melting phenomenon, it is more likely still at the intermediate step: small size Si particles have already melted and bonded to surrounding Si particles to form an agglomerate, however, these agglomerates do not continue to melt and then combine to

form large Si grains. The Si paste layer is nearly transparent to IR light during the RTA process while the C substrate strongly absorbs the IR light from the top and bottom of the lamps in the furnace, as shown in the furnace profile diagram Fig. 4.1. Then, the Si paste is heated by the C substrate. Finally, the Si paste is heated by the C substrate. However, in this study, the Ti layer on top of Si paste may reflect a portion of the IR light from the top lamps. Thus the C substrate doesn't provide enough heat to the Si paste layer for a complete melting process within only 1 s as previously reported in Chapter 3.

However, in the sample annealed at RTA1200°C for 2 s, many molten Si grains start to appear on the sample surface. These melted, recrystallized Si grains look like bumped droplets only embedded in the samples' surface. The same melted Si grain was observed for the sample annealed at RTA1200°C for 5 s, as shown in Fig. 4.11 (d). However, the Chapter 2 showed that for the post-annealed Si paste samples without Ti layer on the surface, the largely melted Si grains exist in the middle region of the film cross-section. The differences in the areas where the largely molten Si grains exist will be discussed later. Fig. 4.11 (d) shows that the smaller Si particles are melted and coalesced on the large Si grain lumps. The contrast of the smaller Si particles which wrap the Si lump is much brighter than the molten Si lump due to the higher secondary electron yield on the small protruding particles than the smooth molten surface [29]. It is also clear that the contact angle between these molten Si grain lumps to the underlying Si paste is about 110°. However, the surface Si lumps in the 5 s sample are much less than those of the 2 s sample due to the further melting process. The flatter molten Si grains caused by longer RTA duration were also observed in the other part of the sample annealed at 1200°C for 5 s, as shown in Fig. 4.10 (e). It is shown that the underlying Si particles can continue to melt and coalesce with the surface Si lumps until the melting process reaches the C substrate, then all the Si paste forms a whole, and the

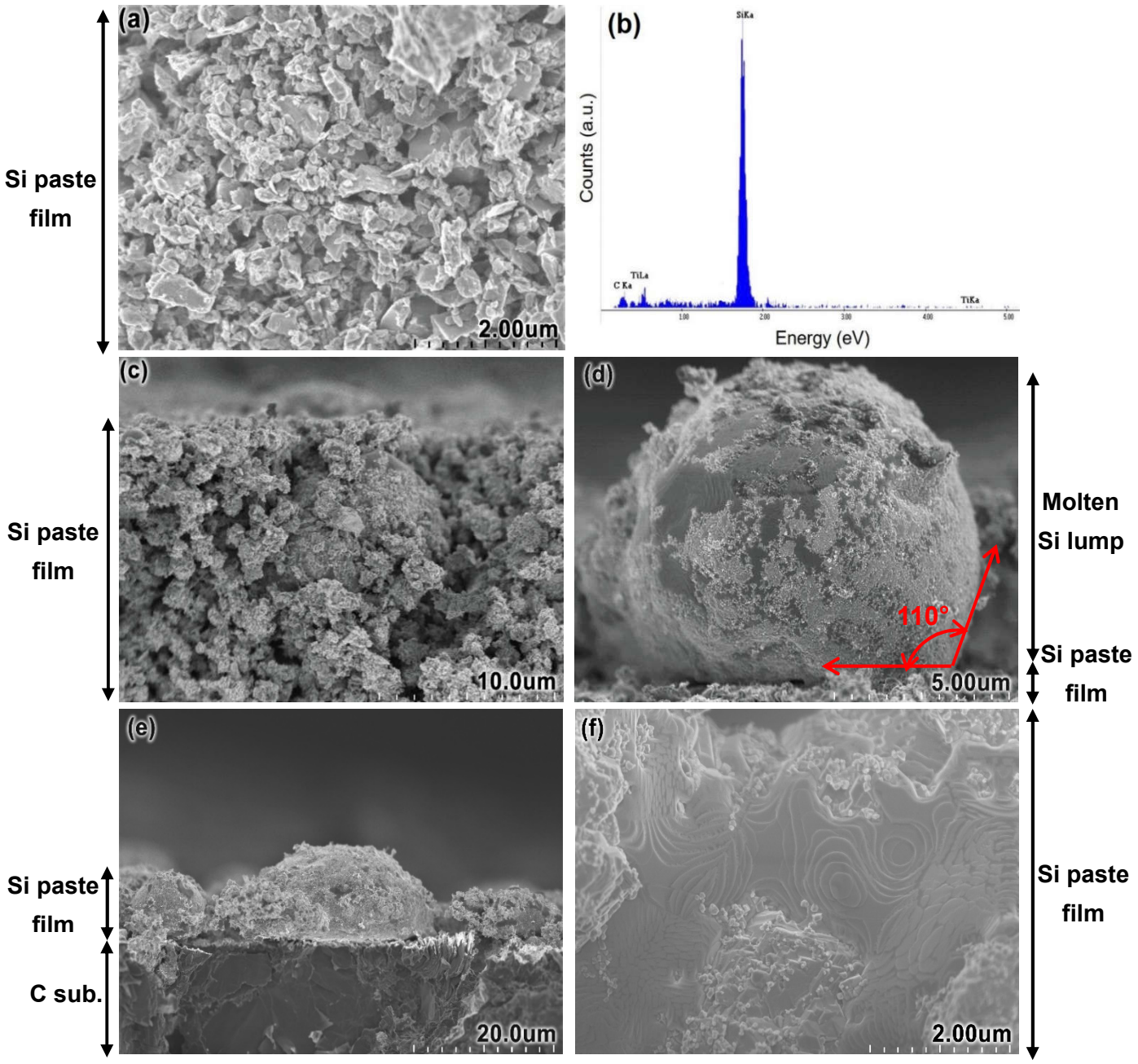
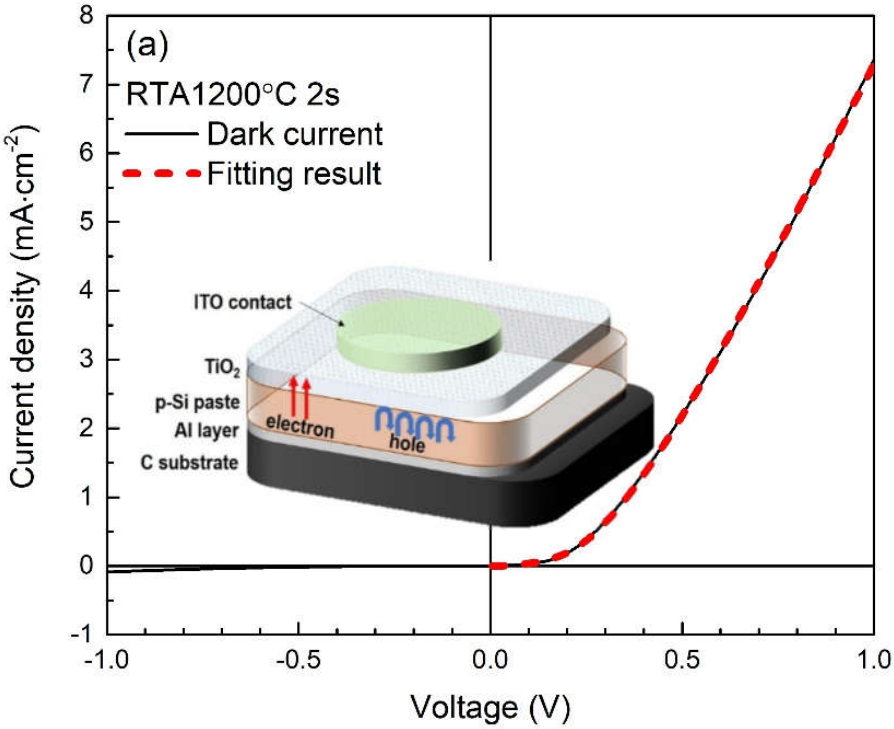


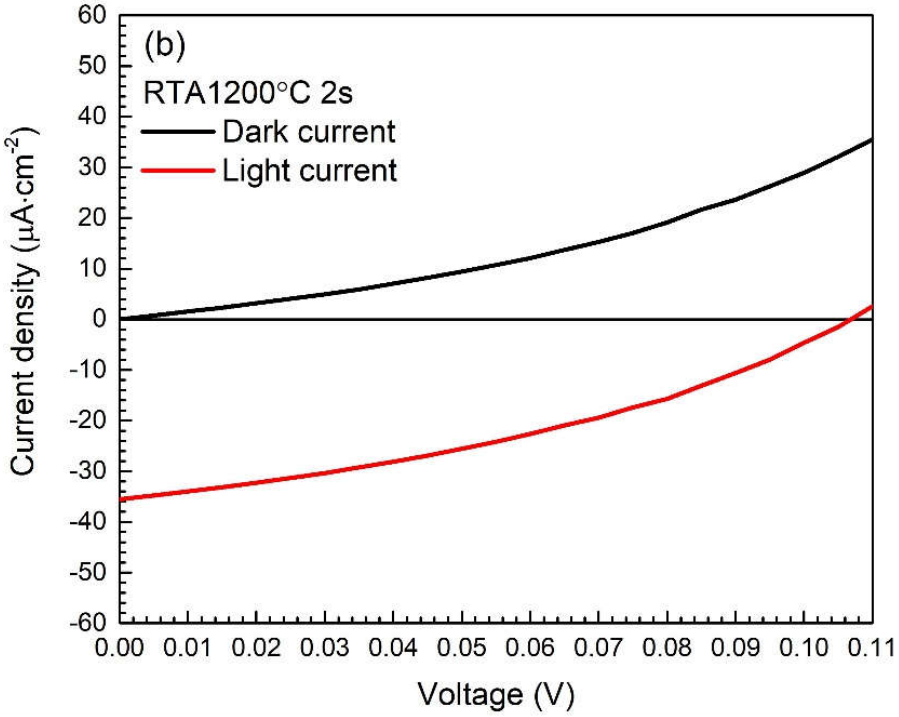
Fig. 4.11 SEM images of the cross-sectional morphology of the p-type Si pastes films on C substrates covered with 30 nm Ti layer. (a) is the middle part of the non-annealed sample; (b) is EDS result of the surface part of the non-annealed sample; (c) is the surface part of the annealed sample at RTA 1200°C for 1 s; (d) is the annealed sample at RTA 1200°C for 5 s showing the large molten Si lump on the surface; (e) is further melting surface of Si lumps observed in the RTA 1200°C/5 s sample; and (f) is the high magnification image of the melting surface [(e)] of RTA 1200°C/5 s sample showing the rippled patterns.

surface Si lumps gradually spread out and become flat. It is also interesting that some rippled patterns appear on the melting surface of the Si paste film annealed at RTA 1200°C for 5 s, as shown in the Fig. 4.11 (f). It can be speculated that due to the short annealing time (only 5 s), the step growth of Si grains occurs on the molten surface, namely, when the Si grains of the first layer have not yet grown completely to cover the whole molten surface, other Si grains attach to the first layer and start to grow, forming a series of undulating steps.

4.3.6 I-V characteristic of TiO_2/p-Si paste device

The I-V characteristic of the TiO_2/p-Si paste heterojunction device is shown in Fig. 4.12 (a) with the device structure depicted in the inset. RTA 1200°C/2 s is selected as the optimal condition to fabricate the device. Under this thermal treatment condition, the Si paste shows the best crystallinity and the most negligible oxidation. Moreover, the rutile phase TiO_2 layer can be maintained to some degree. The device presents a rectification ratio of about 83 at ±1 V. The Shockley equation eq. (2-5) is used for the theoretical fitting of I-V characteristic [30]. The red dash line referring to the curve fitting results using eq. (2-5) are in agreement with the actual experimental data. As the fitting result shows, the ideality factor n is estimated to be about 2.1 with a series resistance R_s =85 Ω. The smaller R_s compared with the best result in the Chapter 3 (101 Ω) proves that Ti layer plays a significant role in the oxidation reduction during thermal treatment. Besides, the illuminated (AM1.5) I-V characteristic is shown in Fig. 4.12 (b). The short circuit current density is calculated as J_{sc}= 36 μA/cm^2, and the open-circuit voltage is V_{oc}= 107 mV. The short current density is more than 3 times greater than best result in Chapter 3. This may be explained by the thin transparent TiO_2 layer and the transparent ITO contact instead of the previous n-/p-type Si paste structure device, let


(a)
RTA1200°C 2s
Dark current
Fitting result
ITO contact
TiO2
p-Si paste
Al layer
C substrate
electron
hole
Current density (mA·cm-2)
Voltage (V)


(b)
RTA1200°C 2s
Dark current
Light current
Current density (μA·cm-2)
Voltage (V)

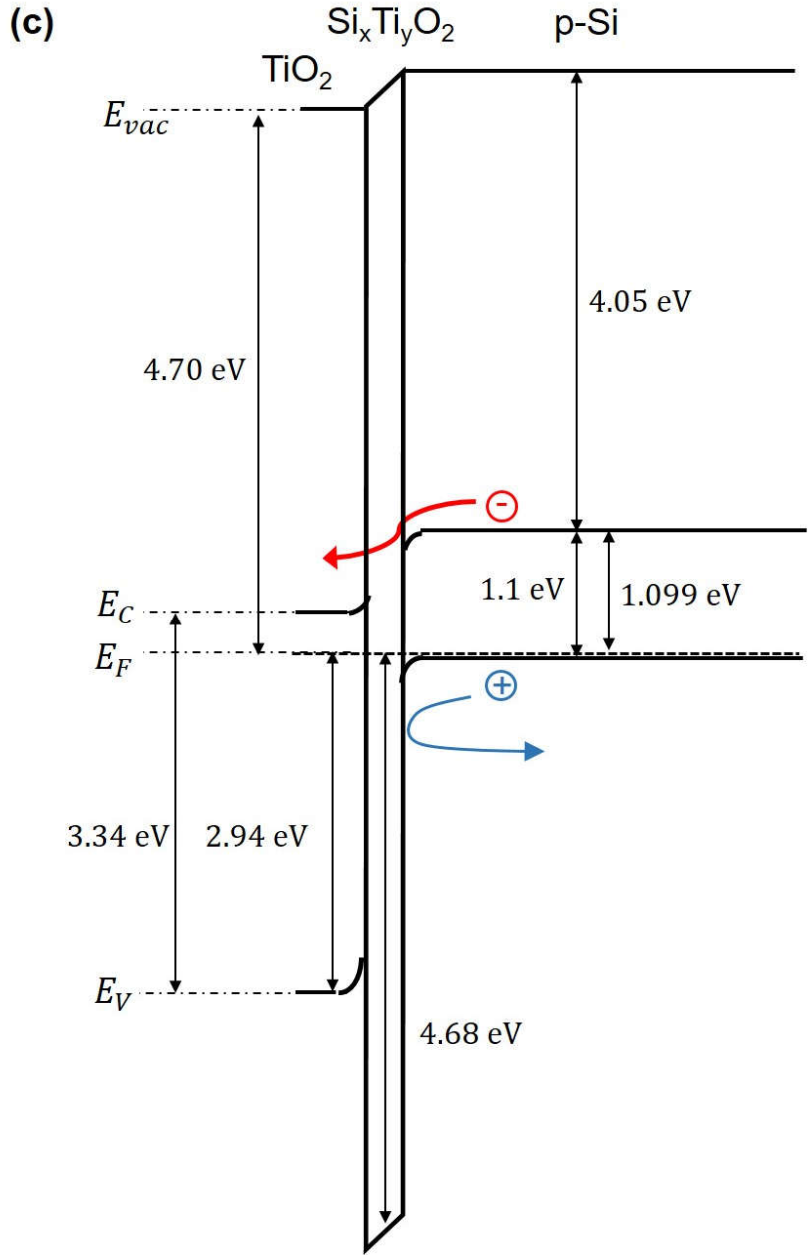


Fig. 4.12 (a) I-V characteristics and fitting results of TiO_2/p-Si heterojunction device (RTA at 1200°C for 2 s); (b) enlarged figure of IV characteristics with and without AM1.5 illumination showing the photovoltaic performance; and (c) the band diagram of TiO_2/ $Si_xTi_yO_2$/p-Si paste device showing the hole-blocking structure.

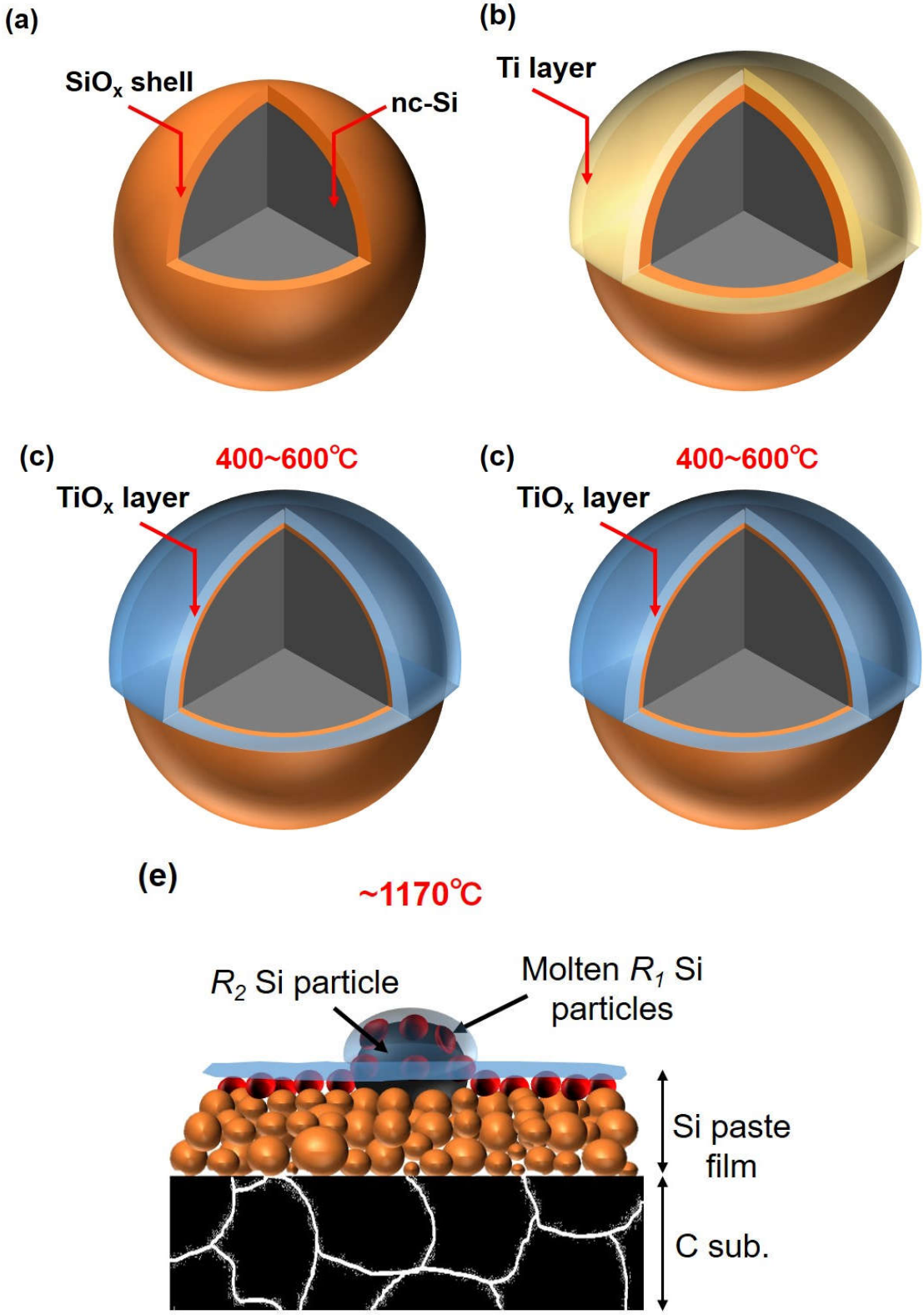
more light incidents into the junction and ITO contacts and collect photogenerated carriers effectively. The electronic band structure of TiO_2/p-Si paste is illustrated in Fig. 4.12 (c) [31]. Due to a big energetic difference (~2.9 eV) between the valence band maxima of the p-Si paste and TiO_2, the holes cannot transport to TiO_2 side. In contrast,

the electrons can be easily transported to the TiO_2 side, forming a hole-blocking rectification structure. During the formation of TiO_2, especially in the low oxygen partial pressure (the annealing process in this Chapter is performed in the ambient 6N Ar gas), many oxygen deficiency areas which are called oxygen vacancies [32] can be formed within the TiO_2. Each fixed oxygen vacancy itself has two positive charges and will release two free electrons. Therefore, TiO_2 is naturally considered to be n-type conductive material. Besides, with the prolonged RTA duration (RTA1200°C/5 s), the inter-diffusion of Ti atoms and Si atoms occurs at the interface between Ti layer and Si paste. The diffusion of Si atoms into the Ti layer is predominant since the diffusion rate of Si is much higher than that of Ti in the Ti-Si binary system [11]. The Ti silicide phase (as shown in Fig. 4.6 (c)) is formed at the interface during the inter-diffusion process. Furthermore, the oxygen atoms from the ambient atmosphere and Si nanoparticle paste diffuse through the Ti film and Ti/Si interface, respectively. As a result, this ultrathin $Si_xTi_yO_2$ interlayer [31] is formed and works as a dielectric layer at the interface of TiO_2 film and p-Si paste as shown in Fig. 4.12(c). Since the work function of p-Si paste (4.05+1.099≈5.15 eV) is larger than that of TiO_2 (4.70 eV), the electrons tend to flow from TiO_2 to p-Si. Therefore, an electric field directed towards the p-Si is formed at the interface, causing the tilted $Si_xTi_yO_2$ interlayer band. Electrons in the conduction band of p-Si paste film can conduct though the $Si_xTi_yO_2$ dielectric layer by tunneling effect [33].

4.3.7 Models for the melting of Ti/p-Si paste system

To show the possible mechanism and the melting phenomenon of the large Si grain lumps formation on the surface of Ti/p-Si paste during RTA treatment, simple nanoscale sphere models are introduced and illustrated in Figs. 4.13 (a)–(g). At the beginning of

the model explanation, the structure of Si particles of non-annealed Si paste is shown in Fig. 4.13 (a). During the high-energy PBM process, the Si particle sizes are crushed into nanometer scale. With the decrease of the Si particle sizes, the specific surface area increases drastically. The higher ratio of surface area to volume means that the Si particles are more likely to interact with oxygen atoms in the surrounding atmosphere, even though the whole Si paste preparation process is carried out in inert atmospheric gas, rendering them prone to oxidation. Thus, the surface of nano-crystalline Si (nc-Si) particles is always accompanied by a shell layer of oxides. This kind of nc-Si/SiO_x core/shell nanostructure illustrated by Fig. 4.13 (a), has also been studied by other researchers [34]. It should be noted that the amorphous Si (a-Si) shell discussed in the Chapter 2 is not considered in this Chapter. The temperature of solid phase crystallization for amorphous is above 700°C, and an a-Si film with a thickness of more than 600 nm can be fully crystallized by using RTA process (700°C for less than 3 min) [35]. Therefore, the a-Si shell with a thickness of only several nanometers can be immediately crystallized during the RTA process (1200–1300°C, 1–5 s). While in the Chapter 2, the Si paste is annealed at low temperature (400–550°C), the a-Si shell cannot be neglected. The substoichiometric SiO_x shell with $x < 2$ is typically only a few nanometers thick [24], but it still has a significant influence on the performance of the sample. This SiO_x shell layer acts as an insulator barrier. If present, a conductive channel for carriers cannot be established between Si particles, consequently increasing the resistance of the semiconductor device. Furthermore, the oxide shell layer can also hinder the coalescing process between Si particles during RTA treatment. Thus causing poor crystallization condition and low structural densification due to its high melting point [36].


(a)
SiOx shell
nc-Si
(b)
Ti layer
(c)
400~600℃
TiOx layer
(c)
400~600℃
TiOx layer
(e)
~1170℃
R2 Si particle
Molten R1 Si particles
Si paste film
C sub.

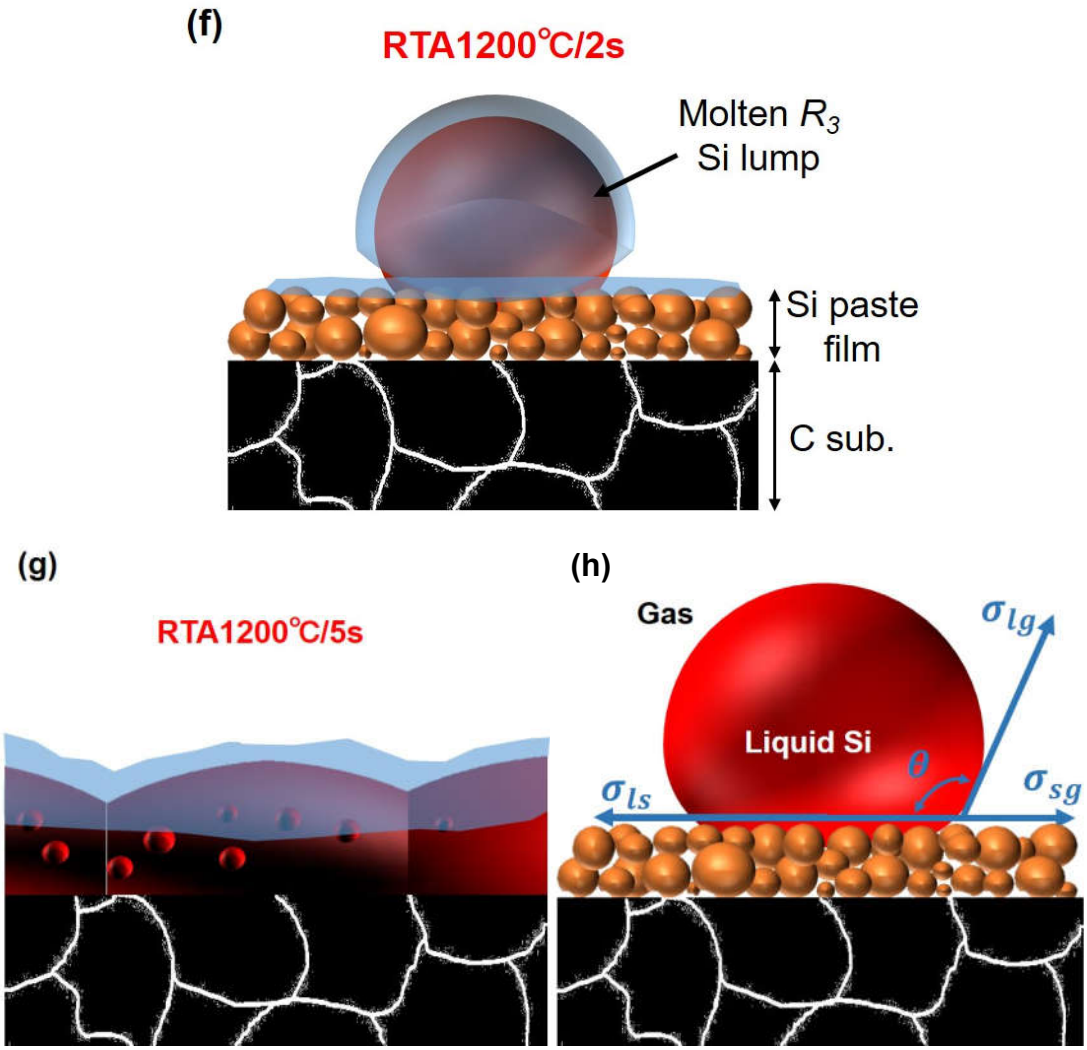


Fig. 4.13 Schematic diagram of (a) a Si particle structure of the non-annealed Si paste; (b) surface of a Si particle covered with Ti film on the top; (c) the first step of the RTA process: the reduction of the SiO_x shell by the Ti layer; (d) the second step of the RTA process: the disproportionation of rest of the SiO_x shell; (e) the third step of the RTA process: the melting and coalescing process of the R_1 Si particles on the surface of R_2 Si particle; (f) the fourth step of the RTA process: the formation and continuous melting process of the R_3 Si lumps; (g) the final step of RTA process: the melting phenomenon reaches to C substrate and surface molten Si grains spread out; (h) the force analysis of the large surface Si grain lumps on the Si paste film.

After the Ti deposition process, the upper surface of the SPS (Si particles at the surface of Si paste film) is covered with a thin layer of Ti. The schematic diagram of the SPS is shown in Fig. 4.13 (b). Then the Ti/p-Si paste samples undergo RTA treatment. In the first stage of the thermal treatment process, it has been reported that

the thin SiO_x shell is reduced by Ti layer when annealing temperature reaches 400~600°C [37] due to the Gibbs' free energy for the reaction of $Ti + O_2 \rightarrow TiO_2$ is smaller than that for $Si + O_2 \rightarrow SiO_2$ [38]. During this reduction, the TiO_x layer could be grown on the SPS by a solid-state reaction where Ti atoms substitute Si atoms in the SiO_x shell of SPS, as shown in Fig. 4.13 (c). With further annealing process, due to the oxygen existence in the pores of the Si paste film and ambient atmosphere 6N Ar, the TiO_x layer will continue to be oxidized to TiO_2, as confirmed by XRD results. Note that this reduction only takes place on the top surface of the Si paste film that in contact with the Ti layer, while the bottom surface of the SPS, and the Si particles inside the Si paste film still show the complete SiO_x shell.

In the second stage of the thermal treatment process, when the annealing temperature reaches to around 900°C [39], a disproportionation reaction takes place on the SiO_x shell of Si particles.

$$SiO_x \rightarrow \frac{x}{2}SiO_2 + \left(1 - \frac{x}{2}\right)Si \tag{4-7}$$

The substoichiometric SiO_x shell is expected to be transformed into the stoichiometric SiO_2 shell and release the Si. This disproportionation causes the oxide shell to become discontinuous and even broken, allowing the coagulation of SPS. The new SPS with the upper surface covered with TiO_2 layer and the bottom surface covered with some fragments of the SiO_2 shell as shown in Fig. 4.13 (d). It is also noted that without a SiO_x shell, titanium silicide could be formed at the interface between residual Ti and Si. If the RTA process becomes more extended, this silicide phase will be produced more and can be detected, as confirmed by the XRD result of RTA 1200°C/5 s sample shown in the Fig. 4.6 (c).

The SiO_x shell of SPS will be quickly removed through both the disproportionation reaction in eq. (4-7) and the redox reaction with Ti layer. On the contrary, for the internal Si particles inside the Si paste layer, their oxide shells can only be decomposed by the disproportionation reaction in eq. (4-7) and there are still some SiO_2 portions remaining on the Si particles. Consequently, the SPS's oxide shell is removed faster than that of the internal Si particles. Thus the SPS come into contact with the nearby SPS easily and quicker than the internal Si particles.

In the last stage of the thermal treatment process, SPS's melting and merging phenomena are shown in Fig. 4.13 (e) and (f). Although the melting point of bulk Si (1410°C) is much higher than the annealing condition (1200°C), the melting point of Si particles in nanometer size decreases dramatically owing to the enormous surface energy [40].

Therefore, the relationship between the melting point (T_m) and Si particle radius r could be described in eq. (4-8):

$$T_m(r) = T_0\left\{1 - \frac{2}{L\rho_s r}\left[\gamma_s - \gamma_l\left(\frac{\rho_s}{\rho_l}\right)^{2/3}\right]\right\} \tag{4-8}$$

where T_0 represents the melting point of bulk Si (1410°C), L is the heat of fusion, ρ_l and ρ_s represent the density of the liquid phase and solid phase Si, respectively. γ_l and γ_s stand for the surface energy of liquid and solid Si, respectively [40]. As reported in the Chapter 3, a similar coalescence model can be applied; Fig. 4.11 (a) shows that Si particles of the non-annealed Si paste are not in a uniform size. For modeling purposes, two kinds of Si particles are considered R_1 particles with a smaller radius and R_2 with bigger particles exist in the non-annealed Si paste. According to Raman results and SEM images, Si particles with less than 10 nm exist in the non-annealed Si

paste. For the simplicity of calculation, it is assumed that the radius of the R_1 Si particle is ~4.8 nm and contains about 48% of total non-annealed Si particles according to the Raman peak deconvolution result as shown in Fig. 4.7 (b). Because the FWHM of Si (111) peak of non-annealed Si paste was about 0.18° as demonstrated in Fig. 4.6 (b), it could be estimated that the average Si particle radius $\bar{R}$ of non-annealed Si, paste was about 35 nm by using the Scherrer Equation. Therefore, R_2 can be estimated as follows:

$$R_2 = \frac{\bar{R} - 0.48 \cdot R_1}{1 - 0.48} \approx 63 \text{ nm} \tag{4-9}$$

According to the eq. (4-8), the melting point of R_1 particles are estimated to be around 1170°C, while the melting point of R_2 particles are approximately 1410°C. During the RTA process, the smaller R_1 nanoparticles start melting first and then wrapping up the neighboring R_2 particle as shown in Fig. 4.13 (e), eventually forming a larger R_3 particle as shown in Fig. 4.13 (f). Since the FWHM of post-annealed Si paste is about 0.08°, thus the average Si grain radius R_3 after annealing is calculated to be around 200 nm. The release of the free surface energy in the melting process of R_1 particles can be estimated by:

$$\Delta E = 4\pi \cdot [R_3^2 - (N \times R_1^2 + R_2^2)] \times \gamma_s \approx -3.4 \times 10^{-11} \text{ J} \tag{4-10}$$

where N is the number of R_1 particles needed to form the R_3 particle. Therefore, this free surface energy release heats up the surrounding temperature of the R_3 particle as:

$$\Delta T = \frac{-\Delta E}{\rho_s V_3 C} \approx 480°\text{C} \tag{4-11}$$

where C is the heat capacity of Si. Therefore, the local temperature near the R_1 Si particles are raised to T=1200+ΔT=1680°C, which will exceed the melting point of big Si particles (1410°C) and trigger the following melting process of larger Si particles.

It has been reported that TiO_2 shows high diffuse reflectance of more than 90% in the near infrared region (750~2500 nm) [41]. Therefore, it may take a longer time for Si paste covered with TiO_2 layer to reach the trigger temperature (~1170°C), the melting point of R_1 particle, compared with those without TiO_2 layer. Thus, unlike the phenomenon observed in the Chapter 3, almost no melting phenomenon was observed for the RTA 1200 °C, 1 s annealed Si paste covered with TiO_2 layer. However, the molten Si particles in the Chapter 3 were much smaller than the molten Si lumps covered with the TiO_2 layer in this study, as shown in Fig. 4.11 (d) even after the longer annealing time (5 s~ 1 min). This implies that the TiO_2 layer affected the melting process. Planck's law describes that every physical body spontaneously and continuously emits electromagnetic radiation. If Si paste is considered as an ideal black body, according to Wien's displacement law, the wavelength of the peak radiation of Si particle is given by:

$$\lambda_{peak} = \frac{b}{T} \approx 1500 \text{ nm} \tag{4-12}$$

where b is a constant of proportionality called Wien's displacement constant. Since the peak radiation was in the infrared region, the TiO_2 layer could reflect these electromagnetic waves radiating from the Si particles and prevent heat loss during the RTA process. However, if the Si particle is not covered with the TiO_2 layer, a portion of heat will be lost as electromagnetic waves. Therefore, we conclude that the TiO_2 layer would keep the heat and promote the melting process of Si particles in the Si paste film during the RTA processing. In which case, all the Si particles could continuously melt

under high temperature (~1680°C) with TiO_2 layer on the surface during the RTA process, eventually forming large Si lumps on the surface as shown in Fig. 4.11 (d).

Moreover, it should be noted that the precondition of the overall melting process is the removal of the oxide shell on Si particles so that Si particles can directly contact each other. In this way, the SPS melts much more preferentially than the internal Si particles. As a result, Si in the liquid phase will appear on the sample surface.

Furthermore, Fig. 4.13 (g) shows that the Si particles are further melted with a longer annealing duration (RTA 1200°C/5 s), and there are no Si grain lumps on the surface like Fig. 4.13 (f). The Si particles fuse into a layer laid on the C substrate, as confirmed by the sample annealed at 1200°C for 5 s in Fig. 4.11 (e). This is due to the surface tension effect. The inclination of liquid surface to shrink into the minimum surface area is so-called surface tension. Due to the cohesive forces a Si atom is pulled equally in every direction by neighboring liquid Si atoms, resulting in a net force of zero. The Si atoms at the surface do not have the same atoms on all sides of them and therefore are pulled inward [42]. This creates some internal pressure and forces liquid surfaces to contract to the minimum area [43]. It is found that the contact angle between liquid Si and C substrate is only 35° due to a small amount of SiC formation at the interface [44]. The surface tension between liquid Si and SiC (~1.2 N/m) is smaller than the solid SiC-gas surface tension (~1.8 N/m) [45]. The surface tension between Si (liquid phase) and SiC (solid phase) drives the Si droplet to shrink into a sphere shape to reduce the liquid-solid contact area, while the surface tension of the solid SiC-gas phase drives the droplet to spread out to reduce the contact area between the solid SiC and gas. The directions of these two surface tensions are opposite. Under the combined effect of the two surface tensions, the molten Si can spread out and fuse on the C substrate.

In the end, the large Si grain lumps are formed on the sample surface also due to

the action of surface tension, as shown in Fig. 4.13 (h). The influence of TiO_2 layer is neglected here. By the means of force equilibrium model simulation carried on the bottom edge of molten Si grains, eq. (4-13) can be given below:

$$\sigma_{ls} + \sigma_{lg} \cos\theta = \sigma_{sg} \tag{4-13}$$

where the σ_{lg} is the surface tension between molten Si lump and gas phase, σ_{sg} is the surface tension between the bottom solid Si paste film and gas phase, σ_{ls} is the interfacial tension between molten Si lump and solid Si paste film, and θ is the contact angle. It has been found that liquid Si-gas surface tension is σ_{lg}= 0.721 N/m [46], solid Si (111)-gas surface tension is σ_{sg}= 0.065 N/m [47], and the liquid-solid Si surface tension is σ_{ls}= 0.413 N/m [48]. Since the liquid-solid surface tension σ_{ls} is more than the solid-gas surface tension σ_{sg}:

$$\sigma_{lg} > \sigma_{ls} - \sigma_{sg} > 0 \tag{4-14}$$

Therefore, the large molten Si grains do not spread out on the surface of Si paste film, but instead coalesce into a droplet-like lumps on the sample surface. Besides, the contact angle $\theta \approx 120°$ can be obtained by using eq. (4-13). However, the SEM observation and contact angle results (110°) are slightly smaller than this theoretical calculating value. This difference may be caused by the fact that the σ_{sg}= 0.065 N/m is only used for ideal flat Si (111) monocrystalline surface. Considering our Si paste condition, the surface is rougher, the noise coming from the irregular fluctuations on a rough surface enhances the noise-induced wetting [49], thus the actual solid-gas surface tension σ_{sg} is considered to be a little larger than 0.065 N/m.

It is also considered that the thickness of the initial Si paste film may affect the

formation of Si lumps. Moreover, it has also been reported that this kind of spherical Si lumps with a millimeter level is used for photovoltaic application, reaching 11.3% [50] efficiency. Therefore, the effect of Si paste film thickness on the Si lumps size and the melting process of Si nanocrystals will be studied in the future. Furthermore, with further optimization of the Si paste annealing process, Si lumps can be candidates for future spherical Si solar cells.

4.4. Conclusions

In this Chapter, the TiO_2/p-Si paste heterojunction device was successfully fabricated by RTA of the p-type Si paste covered with Ti layer. It was found that the oxide shell of surface Si particle was decomposed by Ti layer. Then the surface Si particles first melted and coalesced due to significantly decreased melting point by size effect. The large Si grain lumps were formed on the surface of sample annealed at 1200°C for 2 s. When the RTA duration was extended to 5 s, the melting process reached to the C substrate, then large Si lumps spread out and became flatter. From the FT-IR measurement of the post-annealed samples, it was found that the Ti layer played a significant role in reducing the oxidation of the Si paste during annealing treatment. Si pastes annealed at 1200°C were less oxidized than the samples annealed at 1250°C and 1300°C, which in turn improved the electrical conductivity of the devices. Raman spectra indicated that the tensile stress of non-annealed Si paste was relaxed after the RTA process. XRD patterns revealed that crystallization conditions were improved and rutile phase TiO_2 was formed after the RTA process. A TiO_2/p-Si paste heterojunction device fabricated with the RTA condition of 1200°C/2 s exhibits a rectification characteristic as well as a photo generated current density of 36 $\mu A/cm^2$ under AM1.5 illumination which is three times greater than that in Chapter 3 (10 $\mu A/cm^2$) due to the

surface transparent TiO_2 layer. The series resistance of TiO_2/p-Si paste heterojunction device fabricated with the RTA condition of 1200°C/2 s (85 Ω) is also smaller than that in Chapter 3 (101 Ω) due to the accelerated melting process of Si particles by Ti layer.

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CHAPTER 5:

Conclusions and Future Work

5.1. Conclusions

Solar cells, as the core devices of photovoltaic power generation system are considered to be the most promising approach to solve the energy problem which has increasingly become a bottleneck restricting the economic development of the international community. The c-Si wafer based solar cells are the most matured and commercialized photovoltaics (PV) devices. But due to the conventional costly Czochralski ingot growth as well as slicing process, the manufacturing cost of c-Si wafers still remain the significant barrier that prevents further large-scale dissemination. In this research, the Si paste prepared from grinded the n or p-type Si fragments through a planetary ball miller was adopted as the most promising kerf-less approach that could skip all the Czochralski procedures. A pn diode device was directly fabricated by coating p- or n-type Si pastes on substrates instead of using c-Si wafer for the purpose of manufacturing cost reduction. Since the main problems of Si paste were considered to be the serious oxidation during the annealing process and the high defect density, this PhD dissertation reported several important advancements with feasible oxidation reduction and crystallization enhancement methods on Si paste for application to coated c-Si solar cells. This PhD dissertation was divided broadly into three sections. In the following, the original contributions and possible future work for the respective sections were summarized.

At first, the research background of Si paste, the principle of pn junction

semiconductor device, the purpose together with the brief research contents in this dissertation were introduced in Chapter 1.

In Chapter 2, the method combined low temperature annealing treatment with AIC technology was employed to reduce the oxidation and improve the crystallization of Si paste. As a result, a pn homo-junction device was successfully fabricated with a p-type Si paste followed by an n-type Si paste coating on the Al substrate or Al sputtered iron substrate. Even under low annealing temperature (400, 500, 550°C) treatments for 3 h, an improved crystallization condition of Si pastes was observed with XRD and Raman spectra. This low temperature crystallization seemed to be due to the AIC effect. Additionally, according to the FTIR data the oxidation were less compared with previous high annealing temperature treatment (1100°C for 0.5 h). The device using Al substrate annealed at 400°C showed the highest rectification ratio of 3200 at ±1 V, the lowest reverse current density of 1.8×10^{-9} A/cm^2, and a series resistance of 1.8 kΩ. A photo generated current density of 5.8×10^{-5} mA/cm^2 under AM1.5 illumination was observed with the pn device using Fe/Al substrate annealed at 500°C.

In Chapter 3, an alternative attempt, RTA technology that dramatically shortens the annealing duration, was adopted to reduce the oxidation. In this way, the annealing temperature could be higher to further enhance the crystallization. As a consequence, a pn homo-junction device was also successfully fabricated with p-type Si paste followed by n-type Si paste coating on the C substrate. RTA 1200°C, 1 s was proved to be the most optimal RTA parameters for Si paste to obtain good crystallization conditions and the slightest oxidation. The rapid crystallization of sample annealed at RTA 1200°C for only 1 s was explained by explosive crystallization theory. The mechanism of lowering the melting point (from 1410°C to 1180°C) of Si particle was found to be significant size effect and contribution of release of surface energy. At last, pn device annealed at RTA 1200°C for 1 s was confirmed to own a rectification ratio of 202 at ± 1 V, a series

resistance of 101 Ω, and slight photovoltaic performance with a short circuit current density of 10 μA/cm^2.

Finally, in Chapter 4, on the basis of RTA process, a Ti layer was deposited on the p-type Si paste to achieve more preferential reaction with oxygen than Si, and a TiO_2/p-Si paste heterojunction was formed after RTA treatment to replace the conventional Si homojunction structure. From the FT-IR measurement of the post-annealed samples, it was found that the Ti layer actually played a significant role in reducing the oxidation of the Si paste during annealing treatment. XRD patterns revealed that enhanced crystallization conditions together with the rutile phase TiO_2 formation after RTA process. It was also found that the existence of the Ti layer decomposed the oxide shell of the surface Si particles, thus the surface Si particles melted and coalesced much more preferentially than the internal Si particles, forming the largely melted Si lumps on the surface of the sample annealed at RTA 1200°C for 2 s–5 s. The sample annealed at 1200°C for 5 s also showed that the further melting process reached to the C substrate, then largely Si lumps spread out and became flatter. The TiO_2/p-Si paste heterojunction device fabricated with the RTA condition of 1200°C/2 s exhibited a rectification characteristic with a ratio of 83, a series resistance of 85 Ω, as well as a photo generated current density of 36 μA/cm^2 under AM1.5 illumination.

This PhD dissertation has explored the feasible methods of oxidation reduction and crystallization enhancement, especially for the melting process, in order to overcome the barriers of Si pastes in the electronics devices application field like c-Si solar cells. In Chapter 2, the low temperature annealing method combined with AIC technology has been tried, in Chapter 3, the RTA process has been selected for another attempt, while in Chapter 4, on the basis of RTA process, Ti layer has been introduced to further improve the Si paste device performance. Among them, it has been found that the Si paste device fabricated by sputtering a layer of Ti on the p-type Si paste and then

rapid thermal annealing at 1200°C for 2 s showed the minimal oxidation of Si paste and the highest photocurrent density. To sum up, the technology combining the Ti layer and RTA condition is an approach for fabricating the Si paste device with a better performance towards the solar cell. It is also expected that by employing this oxidation reduction method for annealing the Si paste, the low-cost coated solar cells fabricated by Si paste will be beneficial for the future installation of photovoltaic system as well as solving the emergency energy crisis of human society.

5.2. Future works

Several feasible approaches to reduce the oxidation and improve the crystallization of Si paste during annealing process have been investigated in this dissertation. These attempts indeed are beneficial to realize the future application of Si paste in fabricating c-Si solar cell device. Nevertheless, the oxidation of Si paste is still difficult to be eliminated, and there still has potential for further improvement in crystallinity of Si paste during RTA treatment. In addition, the structure of the Si paste device could be further designed for the purpose of obtaining better photovoltaic performance. Hence, based on this research work, some future works are suggested:

(1) The RTA treatment conditions should be further optimized. Since the melting phenomenon of Si particles was observed when Si paste was under RTA process, the melting process is considered to be the most promising approach for Si paste to achieve the comparable crystallization condition to the c-Si wafer as well as the least defect density. It is desired that after the RTA treatment is optimized by more precise program-controlled annealing duration, all the Si particles in the Si paste melt and solidify to form a single c-Si layer without any voids inside. Thus the series resistance and carrier recombination will be reduced to minimum.

(2) The IR heating furnace used in this dissertation can be replaced by another furnace with evacuation system as well as better gas tightness in case that oxygen infiltrates into the quartz tube.

(3) It is possible to append an intrinsic Si layer at the interface of p-type and n-type Si layer for pn homo- junction device. On the one hand, adding the intrinsic layer by sputtering method is equivalent to broaden the depletion region, enhance the absorption of light waves of solar cells and increase the density of photon generated carriers; on the other hand, it will reduce the lifetime of minor carriers and increase the recombination probability. Hence, the thickness of intrinsic layer should be carefully optimized.

(4) The Si paste is currently pipetted and dropped on the substrate, this method is a simple and difficult to make a uniform Si paste film. The spin coating could provide highly precise control on the thickness of films, so it may be considered as an alternative approach. However, the problems such as the solution wastes during spinning, insufficient thickness for the formation of Si paste device are required to be studied.

(5) The X-ray photoelectron spectroscopy (XPS) method could be adopted to further detect impurities content in the Si paste, especially for the oxygen. XPS is considered as a surface-sensitive quantitative spectroscopic technique based on the photoelectric effect. Therefore, we can not only quantify the oxygen content to determine the oxidation degree of Si paste more precisely, but we can also identify the chemical state, and the overall electronic structure and density of the electronic states of oxygen in the Si paste.

LIST OF PUBLICATIONS

❖ Journals/Transactions/Letters

1. **H. Zhu,** M. Sakamoto, T. Pan, T. Fujisaki, H. Matsumoto, K. Teii, and Y. Kato, Rapid Thermal Annealing of Si paste film and pn-junction formation, *Nanotechnology*, 31 (2020) 385202.

2. Y. Kuboki, **H. Zhu,** M. Sakamoto, H. Matsumoto, K. Teii, and Y. Kato, Low temperature annealing of nanocrystalline Si paste for pn junction formation, *Material Science in Semiconductor Processing*, 135 (2021) 106093.

3. **H. Zhu,** T. Pan, R. Sato, L. Majula, H. Matsumoto, K. Leonard, and Y. Kato, TiO_2 / p-Si paste heterojunction fabricated by rapid thermal annealing, *Applied Surface Science*, 2021. (Accepted on Aug. 17, 2021)

❖ Conference/Proceedings

1. **H. Zhu,** Y. Kato, and K. Teii, Rapid thermal annealing on Si film and pn-junction formation by Si paste, in *Proceeding of Taiwan Association for Coatings and Thin Film Technology (TACT 2019)*, 17-20, November, Taipei, Taiwan, pp. 120, 2019. Be award "**Poster Award of Excellence**".

2. **H. Zhu,** Y. Kuboki, M. Sakamoto, and Y. Kato, Effect of low temperature annealing on pn junction formation using Si paste, in *Proceeding of IEEE Electron Devices Technology and Manufacturing (EDTM 2021)*, 8-11, April, Chengdu, China, pp. 10–12, 2021. DOI: 10.1109/EDTM50988.2021.9420845.

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