Common-Mode Voltage and Circulating Current Reduction of a Single-Stage Inverter in Renewable Energy Power Systems

モハメド，サラー，モハメド，ハッサン

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氏　　名　：モハメド　サラー　モハメド　ハッサン

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(再生可能エネルギー電力システムに用いられる単段インバータのコモンモード電圧と循環電流の低減に関する研究)

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論 文 内 容 の 要 旨

Common-mode voltage (CMV), caused by prevalent high-frequency pulse width modulated (PWM) inverters, is a significant issue for several applications such as motor drives, transformerless photovoltaic (PV) systems, and grid-tied inverters. For example, the induced high amplitude, high frequency, and large step change of the CMV induces motor bearing currents, which significantly influence the aging rate of the bearing and lead to bearing failure, and as a consequence affects the overall system reliability. Moreover, it brings undesirable conducted and radiated electromagnetic interference (EMI) issues, motor insulation breakdown, common mode (CM) leakage current, mechanical vibration, and also malfunction of surrounded electronic equipment. Therefore, the CMV issue is seen as a striking area of research, especially in the aforementioned applications.

Since the conventional voltage-source inverters (VSIs) have only the buck capability during the inversion mode, an additional boosting stage either in the dc side or in the ac side, has to be utilized for several applications. On the other hand, single-stage solutions, with buck and boost capabilities, represent an interesting alternative with reduced cost, complexity and converter volume. Among the possible single-stage solutions, split-source inverter (SSI), which has been recently proposed, has several merits over its counterparts. One of the questionable aspects concerning this topology is the CMV, which has not been investigated yet. This thesis examines the induced CMV with the SSI. This is done by examining the CMV waveforms for VSI and SSI topologies, and then, comparing each other under different PWM schemes. After that a discontinuous PWM (DPWM) strategy has been proposed to mitigate the instantaneous CMV amplitude and its related issues.

Moreover, paralleled configuration of such inverters, shared the same dc and ac sides, suffer from a major challenge related to the excessive circulating currents due to the difference in the induced CMV in each inverter. This voltage difference is due to the instantaneous potential difference between paralleled phase-legs, which results in zero-sequence circulating current (ZSCC) as well as differential-mode circulating current (DMCC). Such currents are generated due to the mismatching between circuit and control parameters in paralleled inverters. This mismatch causes unbalanced output currents, output current distortion, increased power loss, and also failure of switching power module. Moreover, it significantly influences the filter design for circulating current suppression, which may lead to inductance saturation. Consequently, the peak as well as RMS values of these circulating currents must be considered.

Motivated by the abovementioned CMV and circulating currents (ZSCC and DMCC) problems of Power Electronic converters in renewable energy applications, the scope of this thesis is concerning to

comprehensively analyzing and considerably reducing the CMV and circulating currents induced from a single-stage inverter in renewable energy power systems. The thesis comprises five chapters that can be summarized as follows:

In chapter one, an introduction to the CMV issues in renewable energy power systems, and the excessive circulating currents in paralleled converters/inverters are presented. Furthermore, problem definition, research objectives, methodology, and thesis outlines are introduced as well.

In chapter two, a discontinuous space vector PWM strategy for the CMV reduction in three-phase three-leg SSI, considering the inherent constraint of the SSI, is presented. The feasibility of the proposed modulation strategy has been verified theoretically and compared to previously addressed modulation strategies, in which six modulation strategies were studied, programmed, analyzed and experimentally investigated. By applying the proposed modulation strategy to the SSI topology, a reduced instantaneous CMV amplitude with lower number of switching transitions in the CMV profile has been achieved, which further attenuates the CM noise spectra. In order to validate the introduced analysis, simulation model has been designed using MATLAB/Simulink environment, and simulation results are presented. Moreover, a prototype has been built-up for testing the proposed concepts and the obtained experimental results are provided.

In chapter three, a further reduction (50% reduction) in the CMV amplitude of the SSI has been achieved through the control of a four-leg-based configuration of this converter. The proposed four-leg-based SSI topology utilizes a simple, yet-efficient DPWM strategy based on imaginary switching times (ISTs). Moreover, the effect of output filter inductance on the CMV pulse profiles, based on the applied modulation strategy, has been also introduced. To verify the effectiveness and demonstrate the performance of the proposed inverter topology with the associated modulation strategy, a Simulink model has been designed, evaluated and then verified with experiments. The obtained results show that the proposed four-leg-based SSI with the proposed modulation strategy not only restrains the instantaneous peak-to-peak CMV but also reduces the number of switching transitions in the resultant CMV.

In chapter four, a new interleaved DPWM strategy has been proposed to suppress the circulating currents associated with the paralleled operation of the SSIs. The literature considering the circulating currents problem have been extensively reviewed, and he mechanism of producing such currents has been carefully analyzed. Based on the analysis, the proposed modulation strategy has been introduced mathematically and interpreted graphically as well. Moreover, the effect of changing the interleaving angle on the overall system performance has been investigated. A simulation model has been established and the proposed concepts have been verified. The obtained results show that the proposed modulation strategy exhibits the best converter performance in terms of CMV, circulating currents (ZSCC and DMCC). In addition to that, it also produces a reduced CM current (CMC), dc-link ripple current, lower total harmonic distortion (THD) either in the output current or voltage.

In chapter five, the contributions of this thesis are concluded, and the recommendations for extended future research opportunities are presented.