Development of Low-Power and High-Speed On-Chip Clock Distribution System

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https://doi.org/10.15017/4060191

出版情報：九州大学, 2019, 博士（工学）, 課程博士
バージョン：
権利関係：

（別紙様式２）

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論 文 名：Development of Low-Power and High-Speed On-Chip Clock Distribution System
（低消費電力、高速オンチップクロック分配システム開発に関する研究）

区　　分：甲

論　文　内　容　の　要　旨

This dissertation investigates on the development of low-power, high-speed on-chip clock distribution architecture in VLSI systems. Digital products such as smartphone, tablet, laptop, camera etc. are vital to modern societies. The integrated devices such as microprocessors, memories, transceivers and image sensors etc., operate based on some fundamental clocks. Hence, it is not too much to say that the fundamental clocks determine the overall performance of these digital devices. An on-chip clock distribution system is one of the most important function in the chip since it distributes the fundamental clocks to the whole chip. For instance, a global tree structure distributes the system clock to the whole chip and a differential signaling structure which is main scope of this dissertation distributes the I/O clock for high-speed serial links. However, with the recent increase of bandwidth and chip area, an on-chip clock distribution is becoming the power-hungry block as well. A large portion (25%~70%) of the total power can be dissipated in the case of microprocessors due to the large swing and capacitive load according to the recent researches. With the increase of operating speed and length in recent digital systems, low-power and high-speed operation is becoming further challenging task due to the increase of jitter and power caused by multiple repeater stages.

Many works have been investigated for on-chip clock distributions such as inverter chain, small swing, transmission line and *LC* resonance. The repeater-based structures such as inverter chain, small swing are suffering from a huge amount of power and jitter with the increase number of repeater stages. Transmission line structure can potentially reduce the power and jitter due to the absence of the repeaters. However, the design methodology becomes complicated to extract the parasitic inductance which requires time-consuming Elector-Magnetic (EM) simulation. *LC* resonance structures can achieve a good power efficiency owing to the charge recycling mechanism. However, some buffer stages are still required due to the high frequency sensitivity of conventional *LC* oscillators. Hence, conventional on-chip clock distribution structures have not completely solved the fundamental tradeoff between low-power and high-speed operation yet. A new innovative structure has been desirable.

The goal of this dissertation is to propose the innovative solutions to overcome the above stated existing problems of on-chip clock distribution systems. In this dissertation, we propose a new bufferless on-chip clock distribution architecture which makes full use of both transmission line and *LC* resonance. The proposed structure can directly drive a 10-mm on-chip clock distribution line at 3-GHz from a *LC* oscillator without any buffers and repeaters in 0.18-μm fabrication process. The length of 10-mm covers existing large chips and allows us to consider the transmission line effects. The frequency of 3-GHz is selected due to the limited bandwidth of internal logic circuits in 0.18-μm fabrication process. Thanks to the bufferless structure, the performance of the proposed clock distribution is determined by the *LC* oscillator only. The following two major problems must be solved to realize the proposed system. First, the frequency sensitivity of *LC* oscillator must be reduced to directly drive a large capacitive load on the clock distribution line. Second, a simple methodology for on-chip transmission line modeling and optimization are necessary to find the best interconnect parameters and to avoid the time-consuming EM-simulations. To achieve this goals, the proposed

architecture is composed of three key features.

1. A high-frequency, high-symmetry and low-coupling differential inductor

The performance of *LC* oscillators is mainly determined by inductors. Although conventional differential inductors are high-symmetry and low-coupling, the difficulty of high-frequency operation is the major drawback. The proposed differential inductor can achieve almost twice self-resonant frequency while keeping the high-symmetry and low-coupling features. The PGS (Patterned Ground Shielding) structure maximizes Q-factor and improves EM-simulation time owing to the reduced components. The experimental results showed good match with EM-simulation.

2. A simple methodology for on-chip transmission line modeling and optimization

A simplified *RLC*-distributed model and optimization methodology without EM-simulation have been desirable for on-chip transmission line design. The proposed modeling methodology converts a five-wire of GSGSG physical structure to single-ended *RLC*-distributed model. This simplification makes an adoption of basic transmission line theory possible. The proposed optimization methodology can find the smallest metal width, space and structure that achieves the lowest power consumption from the given target specifications such as propagation delay and output swing which significantly improves design time and quality. According to Excel-VBA programming, the proposed methodology can find the optimized transmission line parameters within one minute from 150 combinations which is much faster than conventional EM-simulation-based design methodologies.

3. A low frequency sensitivity *LC* oscillator

Conventional *LC* oscillators have a fundamental tradeoff between low-power and high-frequency operation due to the high frequency sensitivity. The proposed *LC* oscillator can mitigate this tradeoff owing to the shared *LC* resonance mode between frequency tuning capacitor and the load of on-chip clock distribution line. This low frequency sensitivity feature makes bufferless on-chip clock distribution system possible. The proposed theory showed good match with SPICE simulation. The system comparison between the conventional repeater-based and the proposed structure is also discussed. It revealed that advanced processes at least 90nm are preferable for the proposed bufferless structure to reduce the power consumption at the level shift stages.

These three key features are integrated to the proposed bufferless architecture which is directly connected to a 10-mm on-chip clock distribution line fabricated in TSMC 0.18-μm 1-poly 6-metal CMOS process. The experimental results showed good agreement with both theoretical calculations and simulations. It also achieved 2.8-GHz oscillation frequency, 3.3-mA current consumption, -112.8 dBc/Hz phase noise which is comparable to the other state-of-the-art *LC* oscillators in spite of the absence of buffers and repeaters according to the Figure-of-Merit (FoM) analysis. Although both process and frequency are not the most up to date due to the limited available options in our laboratory, the proposed architecture can be applicable to advanced processes and even higher frequencies.

The dissertation is comprised of seven chapters to define and explain on the development of low-power, high-speed on-chip clock distribution line system. Chapter 1 provides the background, motivation and objectives for this research. Chapter 2 presents a brief introduction of existing on-chip clock distribution line systems for high-speed serial links such as inverter chain, low output swing, transmission line and *LC* resonance. Chapter 3 proposes a novel high-frequency, low-coupling differential inductor with patterned ground shield. Chapter 4 proposes a fully calculation-based on-chip transmission line modeling and optimization methodology. Chapter 5 proposes the theory of low frequency sensitivity *LC* oscillator. Chapter 6 presents an experimental implementation of integrated system by organizing a bufferless *LC* oscillator. Chapter 7 concludes the research works. Finally, the contributions and future works are summarized.