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Muroyama, Masanori
Department of Computer Science and Communication Engineering Graduate School of Information Science and Electrical Engineering Kyushu University

Ishihara, Tohru
VSLI Design and Education Center(VDEC) University of Tokyo

Hyodo, Akihiko
Department of Computer Science and Communication Engineering Graduate School of Information Science and Electrical Engineering Kyushu University

Yasuura, Hiroto
Department of Computer Science and Communication Engineering Graduate School of Information Science and Electrical Engineering Kyushu University

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A Power Minimization Technique for Arithmetic Circuits by Cell Selection

†Masanori Muroyama ‡Tohru Ishihara †Akihiko Hyodo †Hiroto Yasuura
†Department of Computer Science and Communication Engineering
Graduate School of Information Science and Electrical Engineering Kyushu University
‡VSLI Design and Education Center(VDEC) University of Tokyo
Email: { *muroyama,akihiko,yasuura* } @c.csce.kyushu-u.ac.jp
ishihara@silicon.u-tokyo.ac.jp

Abstract

As a basic cell of arithmetic circuits, a one-bit full adder and a counter are usually used. Minimizing power consumption of these components is a key issue for low-power circuit design. This paper proposes a new design method, in which basic cells are selected from a set of circuits with different structures (symmetrical and asymmetrical) and connections to their terminals are exchanged, according to input-patterns to minimize power consumption. Experimental results for a parallel multiplier demonstrate average 30% power reduction.

Keywords: low power, cell based design, input patterns, arithmetic circuits

1. Introduction

Considerable advancement of deep sub-micron technology has enabled the manufacturing of large scale complex systems in a single chip. However, this situation makes it more difficult to satisfy short turn around time, high performance computation, low cost, and low power consumption simultaneously. Especially for high performance portable devices, it is difficult to implement high performance computation with low power consumption, because high performance and low power are sometimes incompatible demands in CMOS VLSI circuits. This paper proposes a new cell-based design method to reduce power consumption with little performance degradation.

Many low power techniques in various levels have seem proposal to reduce power consumption[1]. We propose a low power technique on the circuit design level.

The cell-based approach which reuses previously optimized cells is widely applied in VLSI design where the design cost and the time to market are more important than performance and power consumption. In the cell-based design, the quality of the each cell have great impact on the quality of final products. In our approach, the designer selects basic cells considering the behavior of the final circuits. This can reduce more power than conventional logic synthesizer does.

The arithmetic circuits are important components in various LSIs including the microprocessor, DSP and so on. The arithmetic circuits are usually constructed by combining basic cells such as full adders and counters. Therefore, the selection of applicable basic cells is important. In this paper, we propose a new method which reduce the power consumption of arithmetic circuits as follows: (i) we prepare several cells with different circuit structures by considering the input signal patterns of each cell of the arithmetic circuit and we select the most suitable cell from among them and (ii) rearrange a permutation of the input terminal so as to minimize the power consumption. In addition, a simulation technique which can reduce computation time for power estimation is proposed as well.

The rest of the paper is organized in the following way. In Section 2, we explain the input signal patterns of the cell, and a power consumption model of CMOS circuits. In Section 3, we describe the conventional cell-based approach for designing arithmetic circuit and report its problem, and proposes the power reduction technique by considering the input signal patterns. Experimental results are shown in Section 4. In Section 5 we conclude this paper.

2. Preliminaries

2.1. Power Dissipation Model and Related Works

The dominant source of power dissipation in CMOS circuits is the charging and discharging of the node capacitances, and is given by:

$$P = \sum_{k=1}^{N} CL_k \cdot Swit_k \cdot V_{DD}^2 \quad (1)$$

where N is the number of gates, CL_k is the load capacitance of a gate g_k, $Swit_k$ is the switching count of g_k, and V_{DD} is the supply voltage.

Reducing each parameter of expression (1) makes total power dissipation low. V_{DD} reduction are very efficient for low power. According to [2], assigning suitable supply voltage from two type voltages for each cell in order to get low power makes a chip low power. However voltage control technique is very costly in terms of hardware. Gate sizing of transistor [3] is used for reducing CL_k. This method needs to consider various parameters. We explore the switching activity of different circuit implementations in order to reduce power consumption. Many $Swit_k$ reducing methods are proposed [4, 5, 6, 7]. References [4, 5] present switching activity reduction method by adding redundancy cells

and wires to original circuits. Reference [6] suggests low switching activity by technology mapping. These methods do not reduce the internal switching activity of cells.

We propose a technique, which reduces internal switching activity of cells. Besides this method do not need special hardware cost and consider various parameters, it is possible to combine conventional low power methods.

In this paper, it is assumed that CL_k and V_{DD} are fixed.

2.2. Input Patterns

We define an $IPP(InputPatternsPair)$ that is a pair of consecutive input signal values on input terminals. An IPP represents output signal status of $a\ gate$. Signal changes (that is, $Switching$) cause power dissipation. It is important to consider the pairs of consecutive input signal values. $Uniform$ IPPs are a set of IPPs with equal probability of occurrence of each IPP. On the other hand, $biased$ IPPs are a set of IPPs in which probability of occurrence of each IPP is not uniform.

The example in Figure 1 shows the switching count of input terminals in a 1-bit full adder (FA) composing a 3-bit array type multiplier. When we give all kinds of IPPs (4096 patterns) with the multiplier, a set of IPPs of FA are $biased$ IPPs. For instance, in a set of IPPs of FA3 input A switches as many as four times the switch count on input C_{in}.

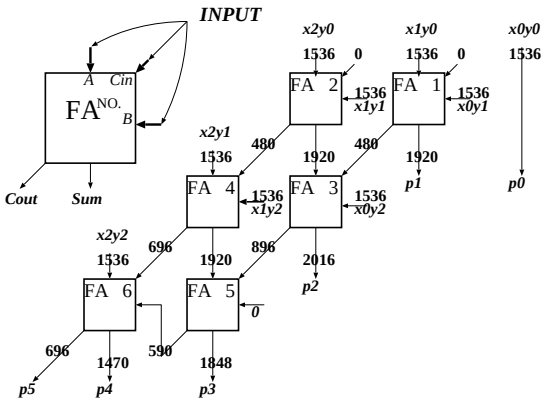

Figure 1. The numbers of switching activity of input terminals of FAs in a 3-bit array type multiplier

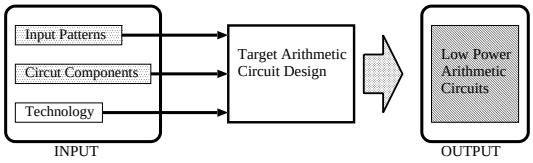

Figure 2. Design flow

3. Conventional Design Method and Our Approach

An arithmetic circuit is usually composed of basic cells (several kinds of function blocks): full adders, parallel counters, multiplexers, shifters, and so on. Circuit structure of a basic cell is usually identical. In addition, designers of the cells focus on uniform IPPs. It is difficult to satisfy severe constraints for area, delay, and power of arithmetic circuit with only one regular circuit structure. In Figure 1, even though a set of IPPs of the arithmetic circuits are uniform, the set of IPPs of each basic cell are not uniform.

3.1. A New Design Method for Low Power Arithmetic Circuits

Figure 2 presents a proposed design flow for low power arithmetic circuits. When we design an arithmetic circuit, we consider three factors: input patterns of the arithmetic circuit , circuits components and process technology. In this paper, we assume following factors.

- Target arithmetic circuit: Parallel Multipliers
- Input patterns for the arithmetic circuits: Probability of each IPP in multiplier is equal
- Circuit components: Two types of FAs (symmetrical and asymmetrical structures)
- Technology: Hitachi Hokkai Semiconductor $0.5\mu m$

The multipliers are important circuits for various LSIs: microprocessors, DSPs, motion video processors, and so on. A multiplier is composed of many FAs, which greatly affect multiplier area, performance and power. We propose a design method for low power multipliers considering characteristics of a set of IPPs. Our basic ideas are as follows:

1. Most suitable FA selection for low power (a FA for uniform IPPs, and a FA for biased IPPs)
2. Rearranging a permutation of the input terminals for low power

Next, we describe two types FAs, which circuit structures are symmetrical(for uniform IPPs) and asymmetrical(for biased IPPs). We reduce power consumption by rearranging permutation of the input terminal of FA.

3.2. Cell Structure for Power Reduction

The standard product sum forms of logical function FA are given expression (2) and (3). Where A and B are adders, C_{in} is carry from lower digit, S is the sum of A, B, and C_{in}, C_{out} is carry to higher digit.

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + AB\bar{C}_{in} + A\bar{B}\bar{C}_{in} \quad (2)$$

$$C_{out} = AB + BC_{in} + C_{in}A \quad (3)$$

An ordinary FA, which was included ordinary cell library, is a low power cell for uniform IPPs. The FA is assumed as FA_u. The FA_u structure is a symmetrical to input A, B, and C_{in} (Figure 3). Expressions (4) and (5) are formed original expressions (2) and (3). Based on the expressions (4) and (5), the circuit structure of FA_u is composed.

$$C_{out} = A \cdot B + C_{in} \cdot (A + B) \quad (4)$$

$$S = A \cdot B \cdot C_{in} + (A + B + C_{in}) \cdot \bar{C}_{out} \quad (5)$$

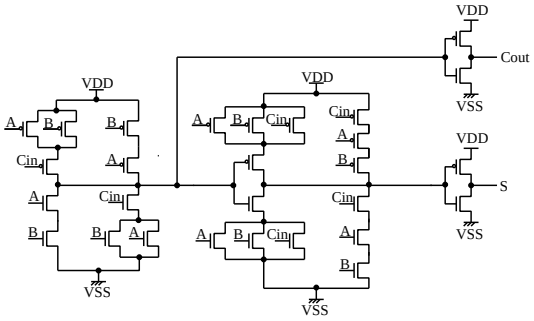

Figure 3. Circuit diagram of FA_u (3 inputs are mostly symmetric)

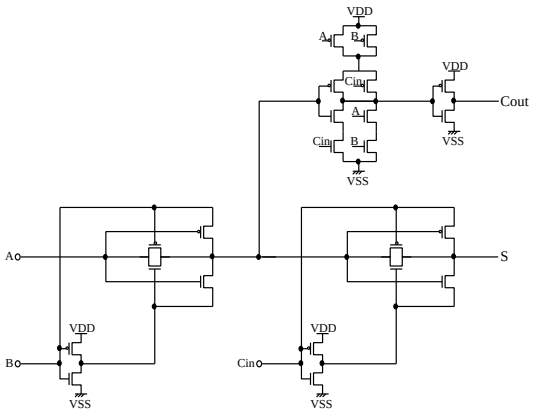

Figure 4. Circuit diagram of FA_b (3 inputs are not symmetric)

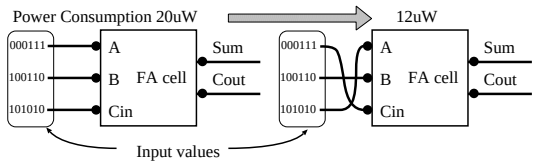

Figure 5. An example of power reduction by exchanging input terminals

On the other hand, we designed a FA that is a low power cell for biased IPPs (Figure 4). The FA is assumed as FA_b. The FA_b circuit structure is asymmetrical (Figure 4). Expressions (6) and (7) are formed original expressions (2) and (3). Based on the expressions (6) and (7), the circuit structure of FA_b is composed. FA_b is composed by using practical $2XOR$ (EXclusive OR).

$$S = A \oplus B \oplus C_{in} \tag{6}$$

$$C_{out} = A \cdot B + C_{in}(A \oplus B) \tag{7}$$

3.3. Exchange Input Terminals for Power Reduction

Both S and C_{out} are symmetrical logical functions. As a result, interchanging variable A, B, C_{in} does not influence the original function. According as the connection change, the power dissipation of FA may be different (Figure 5).

4. Experiments

4.1. Parallel Multipliers

A multiplier multiplies an n-digit multiplicand X by an n-digit multiplier Y. Each x_i and y_i is an unsigned binary digit.

$$X = \sum_{i=0}^{n-1} x_i 2^i, \;\; Y = \sum_{i=0}^{n-1} y_i 2^i, \;\; (x_i, y_i \in \{0,1\})$$

Expression (8) shows the product $P(= XY)$ of X and Y.

$$\begin{aligned} P &= \sum_{i=0}^{2n-1} p_i 2^i, \;\; (p_i \in \{0,1\}) \\ &= XY = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} (x_i \cdot y_j) 2^{i+j} \end{aligned} \tag{8}$$

Partial product $x_i \cdot y_j$ is arranged into matrix form with the weight of 2^{i+j}. Parallel multipliers are composed of the following three parts.

1. Partial product generation part
2. Partial product reduction part
3. Addition part

We evaluate only the partial product reduction part in this paper, because this part is dominant in area, delay and power consumption.

The array type with Carry Save Adder and the Wallace tree type are popular composition methods of the partial product reduction part. The array type which is regular layout can be implemented with small area. The Wallace tree type is somewhat high-speed than the array type.

In our experiments, all transistors size is assumed constant. Hitachi Hokkai Semiconductor $0.5\mu m$ design rules was used.

4.2. 1bit full adders

Power consumption of a FA_u and a FA_b are shown Table 1. Each FA is given uniform IPPs or biased IPPs. The ratio of A to B to Cin of FA which was given in biased IPPs is 4 to 3 to 1. We evaluated power consumption, which are average power of one cycle (unit is μW), by circuit simulator SPICE. Where the output load capacity of a FA is $0.3fF$, transition time of input voltage is $10n\ sec.$ Hereafter we experimented under the same condition.

The experiment results show that the FA_u is suitable for uniform IPPs, while the FA_b is suitable for biased IPPs.

Table 1. Comparison of power consumption of FA_u and FA_b(unit : μW)

FA	Uniform	Biased A:B:Cin = 4:3:1
FA_u	22.4	17.5
FA_b	29.6	15.8

Table 2. The power consumption of 3-bit array type multiplier(unit : μW)

Components of Multiplier	Input terminals	
	no exchange	exchange
FA_u only	**72.277**	66.735
FA_b only	75.222	**49.053**

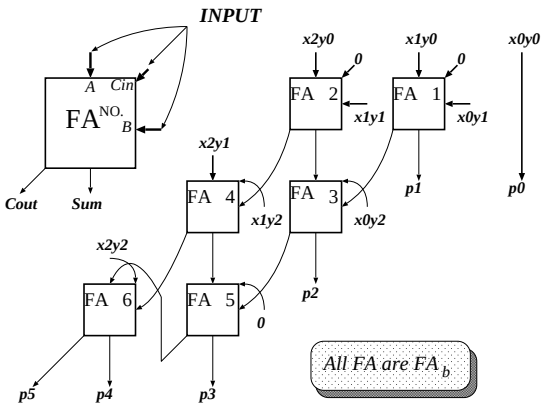

Figure 6. A low power 3-bit array type multiplier

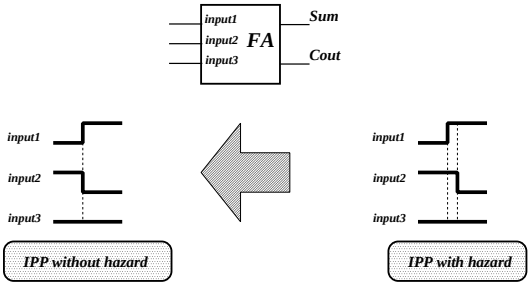

Figure 7. The approximate circuit simulation

4.3. Evaluation of the Proposed Method

We confirmed the proposal method in Section3 with a 3-bit parallel multiplier. We assume that a set of IPPs for the multipliers are uniform. The combination of FA type (FA_u or FA_b) and how to connect input terminals of the FA for low power are determined each FA. FAs of the multiplier minimized in order (from FA1 to FA6). We calculated the average power consumption per IPP. We simulated power consumption when given all IPPs of multiplier. This simulation takes power of hazards account. Table 2 compares the conventional multiplier to optimized multiplier using the proposed method. Figure 6 shows a low power 3-bit array type multiplier construction by using proposed technique. We see that the proposed method reduce 32.1% power dissipation of multiplier than conventional one. However the optimization time took about 271 hours. To reduce the computation time, we need some techniques. In the following 4.4, we propose an optimization time reduction method.

4.4. Computation Time Reduction

There are two reasons for much time consumption for the optimization in 4.3. Firstly, since we evaluate power consumption of multipliers every combination of FAs and input exchanges, simulation takes much time. Since we consider hazard effects, we need to simulate power consumption every combinations. Next, the multiplier was given all IPPs. Count of all IPPs with $n\text{-}bit$ multiplication are 2^{4n}. We propose two methods for reduction of computation time as follows:

1. Approximate circuit simulation
2. Random IPPs to multiplier

We define the approximate circuit simulation, which does not take hazards into account. We assume that arrive time of input signals of FA are equal (Figure 7). We measured power with random IPPs.

Figure 8 shows a low power multiplier by using approximate circuit simulation. We gave all IPPs to the multiplier. The connections of input terminals by using approximate circuit simulation (Figure 8) are different from connections of power minimized multiplier (Figure 6). The comparison of power consumption is shown in Table 3. Since the power in Table 3 are approximate, we evaluate accurate power consumption of the multiplier considering hazard effects (Table 4). Compared with conventional multiplier, optimized one with the approximate circuit simulation achieved 22.5% power reduction. The optimizing time (3.3 sec) is short about 300,000 times as many as the method of Section 4.3.

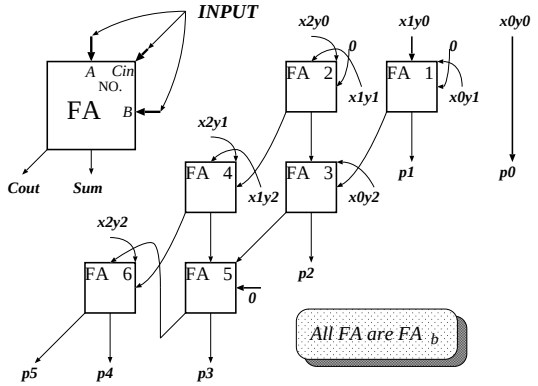

Figure 8. A low power 3-bit array type multiplier designed with the approximate circuit simulation

Table 3. The power consumption of 3-bit array type multiplier by the approximate circuit simulation(unit : μW)

Components of multipliers	Input terminals	
	no exchange	exchange
FA_u only	**83.046**	78.550
FA_b only	85.449	**72.036**

Table 4. The power consumption by precise circuit simulation (unit : μW)

Considering hazard effects	**56.031**

4.5. Experimental Results

We verify the proposed methods by other multipliers. The power consumption of 4-bit array type and 4-bit wallace tree type multipliers optimized by using approximate circuit simulation and random IPPs (1024 IPPs). Figure 9 and 11 show conventional multipliers design, and the numerical values are the switching count of each terminal. Figure 10 and 12 show low power multipliers with the proposed methods. The 4-bit array type multiplier consists of FA_b only, on the other hand the 4-bit wallace tree type multiplier consists of mixture of FA_u and FA_b. As a result, FA_u was assigned the part of uniform IPPs, and FA_b was assigned the part of biased IPPs.

Table 5 and 7 show the power consumption by the approximate circuit simulation. Since of the power consumption in Table 5 and 7 is not considered the hazard ,we evaluate power consumption of power minimized multipliers (Figure 10 and 12) by taking the power of hazard account. Table 6 and 8 compare the power of conventional multipliers with the power of low power multipliers using proposed method. The power of a low power 4-bit array type multiplier reduce 31.1%. The power of a low power 4-bit wallace tree type multiplier reduce 6.97%. Computation time for power reduction of 4-bit array type and 4-bit wallace type are 29 sec and 45 sec, respectively.

Table 5. The power consumption of 4-bit array type multiplier by the approximate circuit simulation(unit : μW)

Components of multipliers	Input terminals	
	no exchange	exchange
FA_u only	**177.87**	165.21
FA_b only	185.82	**145.31**

From the results, we have the following observations.

1. Power consumption of 3-bit and 4bit array type multipliers can be reduce about 30% by combination of FA_b and input terminal changing for low power considering IPPs of each FA.

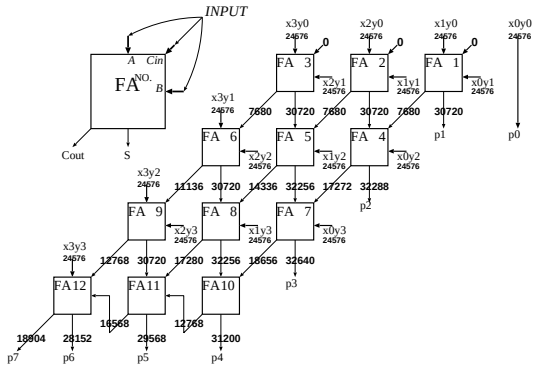

Figure 9. A 4-bit array type multiplier

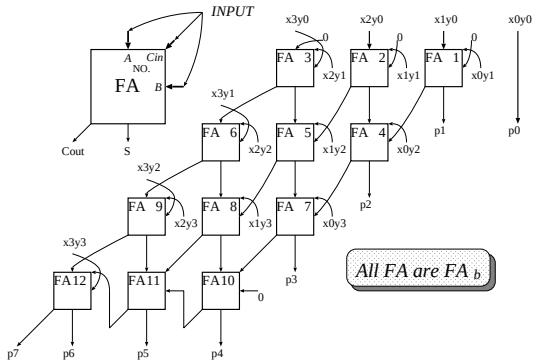

Figure 10. A low power 4-bit array type multiplier

Table 6. The power consumption of 4-bit array type multiplier by precise circuit simulation(unit : μW)

Conventional	**130.50**
Proposal	**91.250**

Table 7. The power consumption of 4-bit Wallace tree type multiplier by the approximate circuit simulation(unit : μW)

Components of multipliers	Input terminals	
	no exchange	exchange
FA_u only	**108.80**	105.91
FA_b only	110.82	101.26
FA_u+ FA_b	—	**98.951**

2. Power consumption of 4-bit Wallace type multiplier

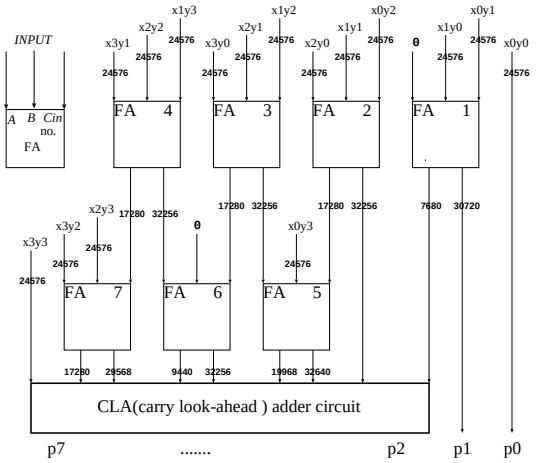

Figure 11. A 4-bit Wallace tree type multiplier

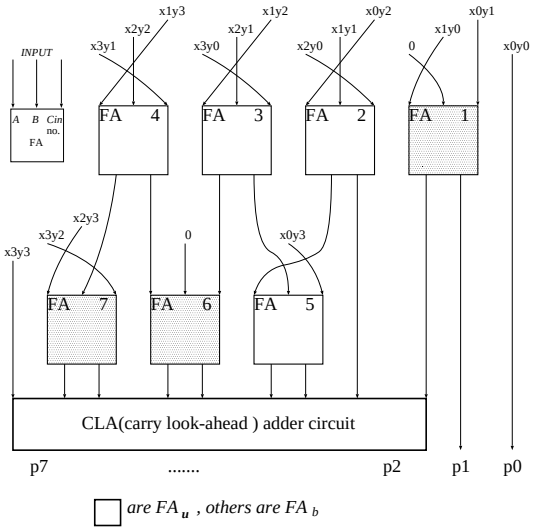

Figure 12. A low power 4-bit Wallace tree type multiplier

Table 8. The power consumption of 4-bit Wallace tree type multiplier by precise circuit simulation(unit : μW)

Conventional	**95.220**
Proposal	**88.586**

can be reduce with combination of two kinds of FA and input terminal changing for low power considering IPPs of each FA.

3. Even if computation for power optimization time is increase and simulation is somewhat inaccurate , we can reduce the power quite degree.

5. Conclusion

In this paper, we proposed a new design method for low power arithmetic circuits considering the characteristics of a set of IPPs. Experimental results illustrated power reduction by using two methods as follows: (i) we prepare several cells with different circuit structure by considering characteristics of a set of IPPs and (ii) rearrange a permutation of the input terminals so as to minimize the power consumption. In addition, we propose a simulation technique which can reduce computation time for power estimation.

Delay of a FA_b takes more than a FA_u. If performance constraint of a part is severe, you must assign the part FA_u.

In the future work, we will study a generation method of power minimized circuit considering characteristics of a set of IPPs.

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