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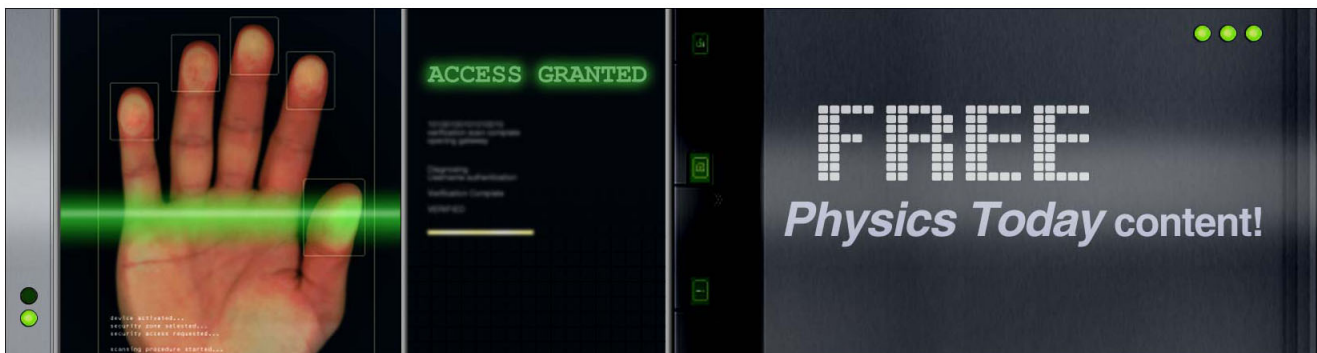
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## ADVERTISEMENT



# Epitaxial all-perovskite ferroelectric field effect transistor with a memory retention

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All-perovskite ferroelectric field effect transistors (FET) are proposed, and switching behaviors of the prototype devices having a  $(\text{Pb,L a})(\text{Zr,Ti})\text{O}_3$  as a gate insulator and a  $\text{La}_{1.99}\text{Sr}_{0.01}\text{CuO}_4$  as a channel layer were demonstrated. Marked improvements in device performances were obtained as compared with the previous ferroelectric FETs. Namely, the present device was written and erased at an operating voltage of 7 V with a pulse width of less than 1 ms, yielding resistance modulation up to about 10% and retaining its memory for more than 10 days at room temperature. Examinations show that the switching speed was limited by a delay constant and can therefore be improved up to 1  $\mu\text{s}$ , and that the memory retention may not be limited by an intrinsic ferroelectric instability as previously suggested. © 1995 American Institute of Physics.

Research on the high-temperature superconductors (HTSC)<sup>1</sup> has revealed a rich physics in the perovskite oxides exhibiting the metal-insulator transition as well as their potential importance in electronics. They also have provided bases for approaches to the perovskite based electronics, e.g., by developing large substrates and deposition technologies suitable for them. In this letter, an approach which uses the normal state properties of the HTSC is reported to significantly improve a long unsolved problem in semiconductor electronics. Namely, a novel ferroelectric field effect transistor (FET) is proposed, and switching behaviors of the prototype devices having a  $(\text{Pb,L a})(\text{Zr,Ti})\text{O}_3$  as a gate insulator and a  $\text{La}_{1.99}\text{Sr}_{0.01}\text{CuO}_4$  as a channel layer are demonstrated for the first time.

The ferroelectric field effect transistor (FET) which uses ferroelectricity as a gate insulator is expected to possess fast write/erase and read-access speeds and a nonvolatile memory feature. While ferroelectric FETs have been studied for a long time after their initial proposals in 1957,<sup>2-8</sup> an acceptable memory retention together with a reasonable write/erase speed has not yet been demonstrated. This difficulty was interpreted by the depolarization field instability.<sup>9</sup> The reported memory retention time was usually less than an hour in thin-film ferroelectric/semiconductor FETs except by Sugibuchi *et al.*<sup>6</sup> which showed an exceptionally slow switching speed difficult to understand as a simple ferroelectric switching. By using a nonoxide ferroelectric  $\text{BaMgF}_4$ , the retention time was reported to increase up to several hours.<sup>8</sup> Additionally, the write-erase voltage in the reported FETs has been too large to be incorporated in standard semiconductor circuits.

From our point of view, the interface between ferroelectricity and the semiconductor was not well controlled in the previous studies. The results of Wurfel and Batra<sup>9</sup> are usually regarded to be against the feasibility of a ferroelectric FET. However, using their formulation, we have concluded that thermodynamically stable ferroelectric domains should form on a semiconductor by choosing a ferroelectric material, but

that an existence of even a 10 Å thick insulating layer should destabilize the ferroelectricity. The latter result is a severe constraint, if conventional combinations of a ferroelectric and semiconductor are used. The use of  $\text{BaMgF}_4$  is an approach to employ a ferroelectric compatible with common semiconductors. Another possibility could be the use of a perovskite semiconductor compatible with common ferroelectrics. To reduce the trap density under the gate, use of an epitaxial heterostructure is inevitable. For this purpose, we proposed an all-perovskite ferroelectric/semiconductor structure and discussed a possibility of the high density integration of more than 1 Gbit.<sup>10</sup>

There are numerous semiconductive perovskites such as  $(L,S)\text{TO}_3$  system ( $L$ :rare earth element,  $S$ :alkaline earth element,  $T$ : $3d$  metal element),  $L(T,T')\text{O}_3$  system ( $L$ :rare earth element or alkaline earth element,  $T$ : $3d$  metal element,  $T'$ : $4d$  or  $5d$  metal element), and HTSC's. Many of them have no rigid band but a charge transfer gap formed by an electronic correlation.<sup>11</sup> Indeed, a drastic change of the electronic structure by chemical doping was observed in the HTSC systems and their related materials using infrared spectroscopy.<sup>12,13</sup> This property provides an enhanced change of resistivity by carrier doping<sup>10</sup> and may compensate for the reduction of field-induced resistance modulation due to their defects. In  $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  (LSCO) system, a good control of conductivity, and a good process stability were achieved. Therefore, we report here on the results using  $\text{La}_{1.99}\text{Sr}_{0.01}\text{CuO}_4$  as a FET channel material. The device structure was similar to that of the superconducting FETs,<sup>14,15</sup> and  $\text{Pb}_{0.95}\text{La}_{0.05}\text{Zr}_{0.2}\text{Ti}_{0.8}\text{O}_3$  (PLZT) was used as a ferroelectric gate insulator. All measurements were done at room temperature.

PLZT/ $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  multilayers were grown *in situ* on  $\text{SrTiO}_3$  (STO) (100) single crystals by a pulsed laser deposition using an ArF excimer laser. Details of the deposition condition and the crystallographic properties were described elsewhere.<sup>16</sup> Ferroelectric hystereses were measured by using a Sawyer-Tower circuit, where a high resistance of  $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  layers was compensated by a 11  $\Omega$  resistor serial to a reference capacitor. The remnant polarization was  $\pm 8 \mu\text{C}/\text{cm}^2$ . The dielectric constant decreased as the resis-

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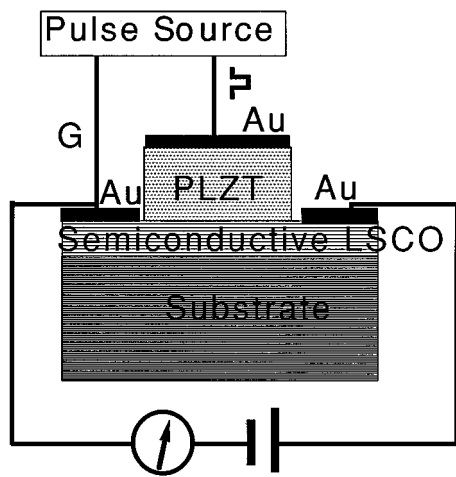


FIG. 1. Structure of the prototype ferroelectric FET and the measurement circuit. The lateral dimension of the gate was typically  $200\ \mu\text{m}$  long along the channel and  $50\ \mu\text{m}$  wide.

tance of  $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  layer increased and as the frequency of the applied voltage increased. Nevertheless, the dielectric constants of the samples having a heavily doped thin  $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  ( $x=0.10$ ,  $800\ \text{\AA}$ ) and those having a lightly doped thick  $\text{La}_{2-x}\text{Sr}_x\text{CuO}_4$  ( $x=0.01$ ,  $2100\ \text{\AA}$ ) were nearly the same at  $100\ \text{Hz}$ . Additionally, the dielectric constant of the latter slightly decreased as the frequency increased from  $100\ \text{Hz}$  to  $1\ \text{kHz}$ . These behaviors can be understood using a  $RC$  time constant ( $R$ : resistance,  $C$ : capacitance), and the related results will be reported elsewhere. The reported depolarization instability<sup>17</sup> was likely to be at least partially due to this effect.

Prototype ferroelectric FETs as schematically shown in Fig. 1 were fabricated by a standard photolithography process. Thicknesses of the semiconductive  $\text{La}_{1.99}\text{Sr}_{0.01}\text{CuO}_4$  (LSCO) and the PLZT layers of the multilayers used in the FETs were  $100\text{--}200\ \text{\AA}$  and  $4000\ \text{\AA}$ , respectively. An excellent three-dimensional alignment of the PLZT, the LSCO and the substrate was confirmed by the x-ray  $2\theta\text{--}\theta$  scan and the pole figure measurements. No interdiffusion of the element was detected in the compositional depth profiles. The resistivity of  $200\text{-\AA}$ -thick LSCO in the multilayers was typically  $0.1\text{--}1\ \Omega\ \text{cm}$ .

The memory characteristics of ferroelectric FETs were measured using the two terminal measurement. Figure 2 shows that the source/drain current was repeatedly reduced by a positive gate pulse (off-state) and was repeatedly enhanced by a negative gate pulse (on-state), where the pulse width and the pulse height were  $10\ \text{ms}$  and  $\pm 7\ \text{V}$ , and the source/drain voltage was  $2\ \text{V}$ . The inset shows the results obtained using  $\pm 5\ \text{V}$   $10\ \text{ms}$  pulses. The modulation in this device was  $9.5\%$ , while its theoretical estimation was  $20\%$  by assuming a remnant polarization of  $\pm 8\ \mu\text{C}/\text{cm}^2$ , a carrier density of LSCO of  $2 \times 10^{20}\ \text{cm}^{-3}$ ,<sup>18</sup> zero carrier trap density, zero contact resistance, and a conventional band picture. This agreement was rather surprising in view of expected imperfections in the present heterostructure and the contact resistance, which was thought to be comparable to the channel resistance. The obtained modulation was low as

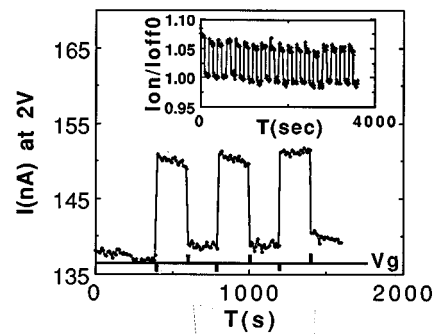


FIG. 2. Write/erase repeatability (main figure and inset) and short period memory retention (main figure) of the FET No. 1 at room temperature. The symbols show the data points. The spikes on the straight line near the abscissa denoted as  $V_g$  show the timing and the polarity of write/erase pulses, where the upward and the downward spikes show the positive and the negative polarities, respectively.  $I_{\text{on}}/I_{\text{off}}$  is the ratio of the on-state current to the initial off-state current.

a FET but was comparable to the on/off ratio of the dynamic random access memory (DRAM) cell.

The highest write/erase speed, i.e., the switching speed, of this device was  $1\ \text{ms}$ . However, the switching speed of several devices increased as the total resistance, being the sum of the source/drain contact resistances and the channel resistance, decreased. The  $RC$  time constant (resistance  $\times$  capacitance) of each FET estimated from its gate capacitance and its total resistance of the FET agreed with the observed switching speed. This explanation is consistent with the above observation of the frequency dependence of the dielectric constants and the hystereses. The highest switching speed obtained in the present devices having a gate area of  $200\ \mu\text{m} \times 50\ \mu\text{m}$  was  $100\ \mu\text{s}$  at  $\pm 7\ \text{V}$ , when the total resistances at  $1\ \text{V}$  were  $3\text{--}4\ \text{M}\Omega$ . Since the  $RC$  constant was found to scale linearly with device dimension as long as contact resistance is negligible, switching speed can be below  $1\ \mu\text{s}$  for devices having a  $2\ \mu\text{m}$  long channel.

Examining dependence of the source/drain current on gate pulse polarity, its magnitude, its width, and source/drain voltage, we have concluded that the observed conductance changes were based on the field effect caused by ferroelectric polarization. Some of the main reasons for that conclusion were that the results were basically unchanged when the gate was short circuited to the ground via a  $1\ \text{M}\Omega$  resistor, and that little increase of modulation was observed when the switching pulse width and its amplitude were increased beyond a threshold. Namely, these observations exclude mechanisms of the modulation of the source/drain conductance dominated by a charge injection or a charge-up. Additionally, the source/drain current characteristics did not change within  $10^4$  write/erase cycles.

The memory retention of ferroelectric FETs were measured using a constant source/drain bias of  $2\ \text{V}$  for  $24\ \text{h}$  in the air at  $20\ ^\circ\text{C}$ . No change was observed as shown in Fig. 3(a). For longer periods of time, the source/drain current at both on- and off-states was observed to a decrease by  $10\%\text{--}20\%$  per month, since the part of the ultrathin channel was directly exposed to the air of  $40\%\text{--}60\%$  humidity at  $20\ ^\circ\text{C}$ . If this change was due to the instability reported by Lampe *et al.*<sup>8</sup>

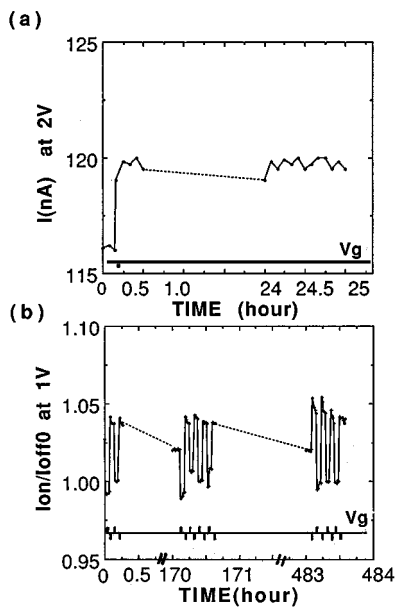


FIG. 3. (a) Retention of an on-state of the FET No. 2. The write/erase pulse voltage and width were  $\pm 7$  V and 10 ms. (b) Retention of an on-state of the FET No. 3. The write/erase pulse voltage and width were  $\pm 7$  V and 1 ms, and the source/drain voltage and its current were 1 V and typically 250 nA. A similar result was obtained for FET No. 2, and the off-state was stable in both FETs. The meanings of the spikes on the straight line near the abscissa denoted as  $V_g$  and  $I_{on}/I_{off0}$  are the same as in Fig. 2.

the off-state current should have increased while the on-state current decreased. Furthermore, the change was suppressed when the channel area exposed to the air was reduced. Therefore, we conclude that this change was due to the chemical change of the channel directly exposed to the air. To exclude this effect from source/drain current modulation, the current values were normalized by one of the typical off-state current values measured on the same day. In this evaluation, the off-state was found to be very stable and not to change for 13 days. However, the on-state was found to be less stable as shown in Fig. 3(b). Nonetheless, the on-state was clearly distinguishable from the off-state, having about 40% of the initial modulation. More importantly, the modulation amplitude were unchanged, which suggests that this memory loss was not likely due to the intrinsic instability.<sup>9</sup> The origin of the switching mechanism in LSCO and the cause of the partial memory loss require a further study.

The present results show that the epitaxial all-perovskite heterostructure can markedly improve the performances of

ferroelectric FET, though the optimization of the fabrication process and the film composition are still on the way. The circuit for the present FET may allow a quite different design which will be discussed elsewhere. However, it is worth noting that such a circuit may not require ultrapure and defect-free films and substrates even in the high density integration contrary to the present all-Si technology.

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