Defect control by Al deposition and the subsequent post-annealing for SiGe-on-insulator substrates with different Ge fractions

Yang, Haigui

Art, Science and Technology Center for Cooperative Research, Kyushu University

Wang, Dong

Art, Science and Technology Center for Cooperative Research, Kyushu University

Nakashima, Hiroshi

Art, Science and Technology Center for Cooperative Research, Kyushu University

Hirayama, Kana

Interdisciplinary Graduate School of Engineering Sciences, Kyushu University

他

<http://hdl.handle.net/2324/26588>

出版情報 : Thin Solid Films. 518 (9), pp.2342-2345, 2010-02-26. Elsevier

バージョン :

権利関係 : (C) 2009 Elsevier B.V.

Defect control by Al-deposition and the subsequent post-annealing for SiGe-on-insulator substrates with different Ge fractions

Haigui Yang^a, Dong Wang^a, Hiroshi Nakashima^a, Kana Hirayama^b,

Satoshi Kojima^b, Shogo Ikeura^b

^a*Art, Science and Technology Center for Cooperative Research, Kyushu University,*

6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

^b*Interdisciplinary Graduate School of Engineering Sciences, Kyushu University,*

6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

Abstract

SiGe-on-insulator (SGOI) substrates with different Ge fraction (Ge%) were fabricated using Ge condensation technique. High acceptor concentration (N_A) in SGOI layer and interface-trap density (D_{it}) at SGOI/buried oxide (BOX) interface were found by using back-gate metal-oxide-semiconductor field-effect transistor method. For the reduction of high N_A and D_{it} , Al deposition and the subsequent post-deposition annealing (Al-PDA) was carried out. As a comparison, a forming gas annealing (FGA) was also performed in H_2 ambient. It was found that both Al-PDA and FGA effectively reduced N_A and D_{it} for low-Ge% SGOI. However, with an increase in Ge%, FGA became less effective while Al-PDA was very effective for the reduction of N_A and D_{it} .

1. Introduction

Mobility enhancement using new materials has become one of key technologies for boosting future complementary metal-oxide-semiconductor (CMOS) performance because of the on-current saturation trend in conventional bulk Si device. Ge-rich SiGe-on-insulator (SGOI) is a promising substrate material for mobility enhancement. Recently, it was reported that Ge condensation by dry oxidation of SiGe layer on Si-on-insulator (SOI) substrate is an attractive method for Ge-rich SGOI or even pure Ge-on-insulator (GOI) fabrication [1]. By using this method, it is very convenient to fabricate both strained and relaxed SGOI's with a wide range of Ge fraction (Ge%), of which the relaxation ratio can be controlled by the thickness of initial SGOI and SOI layers [2]. As a result, hole-mobility enhancement factor of up to 10 has been successfully demonstrated in the condensed SGOI substrate [3].

However, strain relaxation may occur accompanied by the generation of stacking-fault (SF) defects during the structural change from SiGe-on-SOI to SGOI at the initial stage of Ge condensation [4]. With an increase in Ge%, defects such as threading dislocations [5], SFs and microtwins [6,7] were also observed owing to the strain relaxation. As a result, a critical problem related to such acceptor-defect generation is the unintentionally induced hole concentrations as high as 10^{16} – 10^{18} cm⁻³ in Ge-rich SGOI [6]. Therefore, it becomes crucial to reduce acceptor concentration (N_A) from the viewpoint of the suppression of leakage current and the threshold voltage control of p-channel Ge-rich SGOI metal-oxide-semiconductor field-effect transistor (MOSFET). However, so far there is still no effective method to reduce N_A .

In this work, we proposed an effective method of Al deposition and the subsequent post-deposition annealing (Al-PDA) to reduce N_A , as well as the back interface-trap density (D_{it}) at SiGe/buried oxide (BOX) interface, both of which were evaluated by using back-gate MOSFET method. As a comparison, a forming gas annealing (FGA) was also performed in H₂ ambient.

2. Experimental

The processes of back-gate MOSFET fabrication and the treatments with Al-PDA and FGA are schematically shown in Fig. 1. All of SGOI substrates were conveniently fabricated using Ge condensation by the dry oxidation. The SGOI's with $\text{Ge}\% \geq 20\%$, which is hereafter referred to as SGOI-H, was fabricated using 10 nm Si/62 nm $\text{Si}_{0.78}\text{Ge}_{0.22}$ /BOX/Si substrate, which was used in our previous work and the detailed condensation method was given by elsewhere [7]. The SGOI's with $\text{Ge}\% < 20\%$ (referred to as SGOI-L) were fabricated by condensation of 10 nm Si/160 nm $\text{Si}_{0.9}\text{Ge}_{0.1}$ /70 nm SOI/BOX/Si substrate at 1200 °C. The thickness (t_s) and Ge% of the condensed SGOI were measured by spectroscopic ellipsometry. After the Ge condensation, we fabricated back-gate n-channel MOSFET structure on SGOI substrates. First, 400-nm-thick SiO_2 was deposited on SGOI without removal of thermally grown SiO_2 by magnetron sputtering, and windows were opened in source/drain (S/D) areas. Second, a thin film mainly consisting of P_2O_5 -doped SiO_2 was spin-coated on the sample surface, and then solid state diffusion (SSD) was carried out at 1000 °C for 10 min in N_2 ambient to form n^+ S/D, of which concentrations were as high as approximately 10^{20} cm^{-3} . After that, Al film was deposited and patterned as S/D electrodes, and top SiO_2 on the channel area was removed. Then 100 nm Al film was deposited again and Al-PDA was subsequently performed at 400 °C for 30 min in N_2 ambient. After Al-PDA, Al film was removed except that on the electrode areas. As a comparison, FGA was also performed in H_2 ambient ($\text{H}_2/\text{Ar}=1:10$) at 400 °C for 30 min. Finally, mesa etching was performed for SGOI layer for isolation of the MOSFETs, and In-Ga alloy was rubbed onto back Si to form an ohmic contact.

3. Results and discussion

3.1. Extraction of N_A and D_{it} by back-gate MOSFET method

The drain current (I_D) versus gate voltage (V_G) characteristics of back-gate MOSFET were measured, from which the threshold voltage (V_T) and subthreshold swing (S) could be determined. According to Ref. 8 and 9, V_T and S can be expressed by

$$V_T = V_{FB} + \psi_S + \frac{\sqrt{2\varepsilon_s q N_A \psi_S}}{C_{ox}} + \left(1 + \frac{C_D}{C_{ox}}\right)(2\psi_B - \psi_S) + \frac{qD_{it}\psi_B}{C_{ox}} \quad (1)$$

$$S = \ln 10 \cdot \frac{kT}{q} \left(1 + \frac{C_D + qD_{it}}{C_{ox}}\right) \quad (2)$$

where V_{FB} is the flat-band voltage; ψ_S the band bending in SGOI layer; ψ_B the energy difference between the intrinsic Fermi level (E_i) and the Fermi level (E_F); C_{ox} and C_D the BOX- and depletion-layer capacitances, respectively; ε_s the permittivity of SGOI; q the unit electronic charge; kT the thermal energy. There are two-type modes of partially depletion (PD) and fully depletion (FD) at $V_G = V_T$, depending on t_s and N_A . If ψ_{SS} is defined as $(qN_A/2\varepsilon_s) \cdot t_s^2$, the modes are PD and FD in the cases of $\psi_{SS} > 2\psi_B$ and $\psi_{SS} < 2\psi_B$, respectively.

For PD, ψ_S in Eq. (1) is given by $\psi_S = 2\psi_B$, and C_D in Eq. (2) is given by $C_D = \varepsilon_s/W_d$, where W_d is the depletion-layer width at $\psi_S = 1.5\psi_B$ in the subthreshold region. On the other hand, ψ_S and C_D for FD are given by $\psi_S = \psi_{SS}$ and $C_D = \varepsilon_s/t_s$, respectively.

In Eq. (1), V_{FB} is mainly caused by the fixed positive charges (Q_f) in the BOX layer and the work-function difference (ϕ). The contribution of ϕ to V_{FB} can be ignored because both SGOI layer and back-Si gate are p-type. To evaluate V_{FB} from the contribution of Q_f , we performed the same I_D - V_G characterization for SOI substrate with the residual boron concentration of approximately $1 \times 10^{15} \text{ cm}^{-3}$, which has the same BOX layer fabricated by the separation-by-implanted-oxygen (SIMOX) technique. As a result, $V_{FB} = -0.75 \text{ V}$ was obtained, which corresponds to $Q_f = +1.2 \times 10^{11} \text{ cm}^{-2}$. By using Eqs. (1) and (2), and the obtained values of V_T and S , we can extract N_A and D_{it} .

3.2. The dependence N_A and D_{it} on Ge% for SGOI without any treatment

Fig. 2 shows the dependence of N_A on Ge% extracted by back-gate MOSFET method. It is very clear that N_A drastically increase from 10^{16} to 10^{18} cm⁻³ with an increase in Ge%. These high N_A 's should come from the generation of acceptor-type defects due to strain relaxation during Ge condensation [6].

Fig. 3 shows the dependence of D_{it} on Ge%. It can be seen that the D_{it} 's of SGOI with Ge%≤50% are approximately $1\text{--}2\times 10^{12}$ cm⁻²eV⁻¹, which are consistent with those measured by deep-level transient spectroscopy (DLTS) method [10], implying the validity of the back-gate MOSFET method in this work. For SGOI with Ge%=75%, a very high D_{it} of approximately 2×10^{13} cm⁻²eV⁻¹ was found, which is similar to that at Ge/SiO₂ interface, implying that interface quality of SGOI/BOX became worse when Ge% is very high. The poor interface quality should come from the fact that weak Ge-O bonds are easily detached resulting in high dangling-bond (DB) density [11].

To fabricate high-quality SGOI, the reduction of high N_A and D_{it} are desired. In this work, we tried two passivation methods, i.e., Al-PDA and FGA. To clarify the availability of these two methods, in the following section, we used the N_A (Fig.2) and D_{it} (Fig. 3) as reference data.

3.3. The Al-PDA and FGA for the reduction of N_A and D_{it}

We characterized the $I_D\text{--}V_G$ in the linear region of I_D versus drain voltage (V_D) region after Al-PDA and FGA treatments. Fig. 4 shows the results, from which the V_T and S were obtained and summarized in Table 1.

It is very clear that V_T drastically increased with an increase in Ge%, in particular, for no annealing samples. Generally, V_T and S are closely related to N_A and D_{it} , respectively. Therefore, increasing V_T should mainly come from the contribution of increasing N_A .

N_A and D_{it} were obtained using the Eqs. (1) and (2), and the values of V_T and S listed in Table 1. Figs. 5 and 6 show the evaluation results of N_A and D_{it} , respectively. For low-Ge% SGOI with Ge%=20%, it is clear that both Al-PDA and FGA effectively reduced N_A and D_{it} .

More than 1 order decrease of N_A and approximately 1 order decrease of D_{it} were found after both method treatments. With an increase in Ge%, for SGOI with Ge%=50 and 75%, FGA became less effective for the reduction of both N_A and D_{it} . However, after Al-PDA treatment, N_A drastically decreased to $4 \times 10^{15} \text{ cm}^{-3}$ for SGOI with Ge%=50%. It is close to the residual boron concentration of approximately $1 \times 10^{15} \text{ cm}^{-3}$, which implies that N_A induced by acceptor-type defects was effectively reduced by Al-PDA. Simultaneously D_{it} also decreased to $1.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, which is as good as that at SOI/BOX interface [10]. For SGOI with Ge%=75%, although very high D_{it} can not be effectively reduced, approximately 2 order decrease of N_A could be achieved after Al-PDA treatment. Therefore, Al-PDA treatment still effectively reduces N_A even though the Ge% is very high.

It is well known that hydrogenation can be used to significantly reduce D_{it} at Si/SiO₂ interface mainly from DB defects through the formation of Si-H bonds. However, theoretical calculation has demonstrated that in Ge both DB and H are negatively charged, and interstitial H is electrostatically repelled from negatively charged DB defects, thus cannot effectively passivate DB defects [12]. Experimental results also showed that high D_{it} was still observed at Ge/oxide interface in Ge CMOS structure after hydrogenation [13]. Therefore, in this work, it is reasonable that FGA became less effective to reduce D_{it} from DB defects with an increase of Ge%. For low-Ge% SGOI with Ge%=20%, FGA has the same effect on both N_A and D_{it} . Thus, high N_A should also originate from the DB's induced by the structural defects of SF generated during the structural change from SiGe-on-SOI to SGOI at the initial stage of Ge condensation due to strain relaxation [4].

In contrast to FGA, Al-PDA treatment significantly reduced N_A and D_{it} not only for low-Ge% SGOI, also for high-Ge% SGOI. These phenomena suggest that interstitial Al diffused in SGOI during Al-PDA acts as a defect terminator. It exists as positive charge state (Al⁺). On the other hand, the origin of N_A and D_{it} are the acceptor defects in SGOI layer and

DB defects at SGOI/BOX interface, respectively. Both of these defects exist as negative charge state. Therefore, Al-PDA can effectively reduce both N_A and D_{it} .

4. Conclusion

By using back-gate MOSFET method, we evaluated N_A and D_{it} for SGOI with different Ge%. Unintentional acceptor with high concentration of 10^{16} – 10^{18} cm⁻³ were found due to defect generation induced by strain relaxation. The effect of Al-PDA and FGA on the reduction of N_A and D_{it} was clearly demonstrated. We found that FGA could only reduce N_A and D_{it} for low-Ge% SGOI. By contrast, Al diffused in SGOI during PDA acts as a defect terminator and consequently significantly reduced N_A and D_{it} , not only for low-Ge% SGOI but also for high-Ge% SGOI.

Acknowledgements

This study was supported in part by STARC and a Grant-in-Aid for Science Research on Priority Areas (20035011) from The Ministry of Education, Culture, Sports, Science and Technology of Japan.

References

- [1] T. Tezuka, N. Sugiyama, T. Mizuno, M. Suzuki, S. Takagi, Jpn. J. Appl. Phys. 40 (2001) 2866.
- [2] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Hirashita, E. Toyoda, T. Numata, T. Irisawa, K. Usuda, N. Sugiyama, T. Mizuno, S. Takagi, Semicond. Sci. Technol. 22 (2007) S93.
- [3] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, S. Takagi, IEEE Electron Device Lett. 26 (2005) 243.
- [4] D. Wang, S. Ii, H. Nakashima, K. Ikeda, H. Nakashima, K. Matsumoto, M. Nakamae, Appl. Phys. Lett. 89 (2006) 041916.
- [5] T. Tezuka, Y. Moriyama, S. Nakaharai, N. Sugiyama, N. Hirashita, E. Toyoda, Y. Miyamura, S. Takagi, Thin Solid Films 508 (2006) 251.
- [6] N. Hirashita, Y. Moriyama, S. Nakaharai, T. Irisawa, N. Sugiyama, S. Takagi, Appl. Phys. Express 1 (2008) 101401.
- [7] H. Yang, D. Wang, H. Nakashima, H. Gao, K. Hirayama, K. Ikeda, S. Hata, H. Nakashima, Appl. Phys. Lett. 93 (2008) 072104.
- [8] S. M. Sze, Kwok K. Ng, Physics of Semiconductor Devices, Third Edition, John Wiley & Sons, New Jersey, 2006, Chap. 6.
- [9] HK. Lim, J.G. Fossum, IEEE Trans. Electron Devices 30 (1983) 1244.
- [10] D. Wang, S. Ii, K. Ikeda, H. Nakashima, M. Ninomiya, M. Nakamae, H. Nakashima, Thin Solid Films, 508 (2006) 107.
- [11] C.G. Ahn, H.S. Kang, Y.K. Kwon, S.M. Lee, B.R. Ryum, B.K. Kang, J. Appl. Phys. 86 (1999) 1542.
- [12] J. R. Weber, A. Janotti, P. Rinke, C. G. Van de Walle, Appl. Phys. Lett. 91 (2007) 142101.
- [13] V. V. Afanas'ev, Y. G. Fedorenko, A. Stesmans, Appl. Phys. Lett. 87 (2005) 032107.

Table 1. The values of V_T and S obtained from I_D – V_G characteristics for SGOI with different Ge%.

Ge%	20%		50%		75%	
	V_T	S	V_T	S	V_T	S
No annealing	15.3	1.2	42.5	2.0	~110	~10
FGA	4.6	0.5	28.6	2.3	64.5	9.0
Al-PDA	4.2	0.6	7.3	0.9	32.1	5.8

Units. V_T : V; S : V/decade

Figure captions

Fig. 1. The processes of back-gate MOSFET fabrication and the treatments with Al-PDA and FGA.

Fig. 2 Dependence of N_A on Ge%. ●: obtained from SGOI-L samples; ■: from SGOI-H samples.

Fig. 3 Dependence of D_{it} on Ge%. ●: obtained from SGOI-L samples; ■: from SGOI-H samples.

Fig. 4. The I_D-V_G characteristics for SGOI with different Ge% with different treatment.

Fig. 5. The dependence of N_A on Ge% for SGOI with different treatment. The data represented by broken lines is from Fig. 2.

Fig. 6. The dependence of D_{it} on Ge% for SGOI with different treatment. The data represented by broken lines is from Fig. 3.

Figure 1

Figure 2

Figure 3

Figure 4

Figure 5

Figure 6