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Chaitanya Nunna, Krishna  
Department of Advanced Informatics, Kyushu University

Mehdipour, Farhad  
E-JUST Center, Kyushu University

Yoshimira, Masayoshi  
Department of Advanced Informatics, Kyushu University

Murakami, Kazuaki  
Department of Advanced Informatics, Kyushu University

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# Methodology for Early Estimation of Hierarchical Routing Resources in 3D FPGAs

Krishna Chaitanya Nunna

Department of Advanced Informatics  
Kyushu University  
Fukuoka, JAPAN  
krishna@soc.ait.kyushu-u.ac.jp

Farhad Mehdipour

E-JUST Center  
Kyushu University  
Fukuoka, JAPAN  
farhad@ejust.kyushu-u.ac.jp

Masayoshi Yoshimura and Kazuaki Murakami

Department of Advanced Informatics  
Kyushu University  
Fukuoka, JAPAN  
{yosimura, murakami}@ait.kyushu-u.ac.jp

**Abstract**—Power becomes an ever-increasing concern due to the growing design complexity and the shrinking process technology. Power estimation at an early stage of electronic design automation (EDA) flow is essential in order to handle the design issues much earlier. Also power due to the routing resources is a dominant in field-programmable gate arrays (FPGAs). In this paper, we introduce a methodology for early estimation of hierarchical routing resources targeting power-aware EDA flow for three-dimensional FPGAs. We analyze the behavior of wire segments on a two-dimensional plane to derive a model for estimating the required number of routing segments in a 3D FPGA for a given circuit. For a number of MCNC benchmark circuits, the proposed methodology is validated against the output of TPR, an academic 3D place and route tool for FPGAs. We achieved a mean error of 29.04% for segmented wires; single-length, double-length and hex-length segments among all 14 selected benchmark circuits.

**Keywords**- 3D FPGA, hierarchical routing resources, routing segments, early estimation

## I. INTRODUCTION

Three-dimensional integration is one of the promising innovations which can provide benefits like increasing transistor density, reduced form factor, low power consumption, heterogeneous architectures and improvement in delay by significantly reducing the wirelengths of integrated circuits. Particularly for field-programmable gate array (FPGA), it is useful for solving the problems pertaining to longer wire delays [1]. Compared to application-specific integrated circuit (ASIC), power consumption in FPGA is most critical due to its large number of resources. Each of the available resources (logic, routing, IO, clock etc.) will have significant contribution to the overall power consumption. Although area and speed have been the main research focus on FPGA architecture and electronic design automation (EDA) tool to date, power is likely to be a key consideration in the design of future FPGAs especially in 3D platforms. Fast growing industry requirements result in rapid increase of design complexity and put challenges to EDA tool developers for reducing the design time that can help make design decisions early in the process.

Power in FPGA comprises of dynamic and static components in which dynamic power depends on switching activities of the logic and static power is due to the leakage pertaining to the transistor structure. Earlier work in [2] and [3] shows that the dynamic power consumption in FPGA due

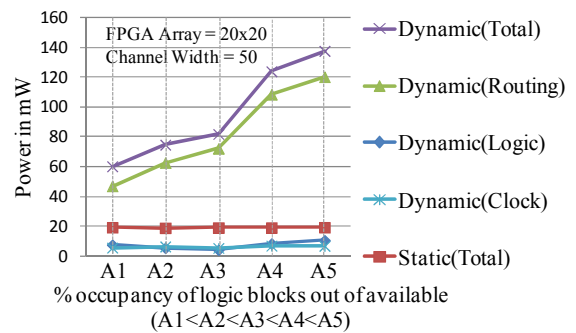


Figure 1. Power analysis for MCNC benchmark circuits

to routing resources is much higher than others because of their large share in chip area. To get the knowledge on power distribution among FPGA resources, we have conducted experiments on five MCNC benchmark circuits [4] using VPR [5] with the power model proposed by Poon *et al.* [6]. Our results are shown in Fig. 1. We can see that the power consumed by routing resources is much higher than the other and it is growing with the increase in circuit size. On the other side, power due to logic is low and almost unchanged. From this we have observed that the role of routing fabric in FPGA power is momentous.

In conjunction with reducing FPGA power, efficient power-aware design will require new estimation tools that gauge power dissipation at the early stages of the design process. It is proved that the early estimation would allow design trade-offs to be considered at a high level of abstraction, reducing design effort and cost. The work presented in this paper is aimed towards estimating power consumption in 3D FPGA (Fig. 2) at an early stage of the design cycle namely before placement. As it is evident from the above discussions that the routing resources have significant role in power consumption, our target needs an early estimation of such resources. Currently several routing estimation techniques are available which are targeting for the wirelength requirements, but none take into account the segmented routing resources. And also for the accurate power calculations, it is observed that the wirelength probability is not enough due to the unknown number of associated switching elements for each net. The hierarchical routing resources feature in FPGA gives us the opportunity to estimate the net length in terms of the segments used by routing that net. As each segment on FPGA plane terminates at switch boxes (SBs), it is easy to find the

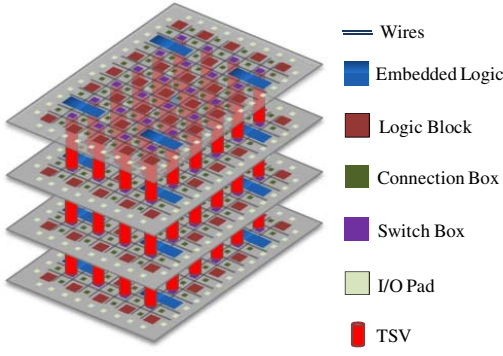


Figure 2. Schematic of 3D FPGA

number of switches associated with each segment. In this paper, we propose a method for estimating the fraction of routing segments used by a given circuit on 3D FPGA. In the rest of paper, section II surveys the related work. Section III explains about the hierarchical routing resources in FPGA. Our methodology is proposed in section IV. Experiment setup and results will be discussed in section V and finally section VI concludes the paper with future work.

## II. RELATED WORK

We have done survey for earlier work on routing estimation at various stages of design cycle. The highly successful Donath's technique [7] gives the estimation of wirelength by performing a hierarchical pre-placement. In this technique, each level of hierarchical placement is treated separately without any knowledge about interactions with the other levels of hierarchy and also no external net consideration. Stroobandt [8] introduced an extended work of [7] for both two and three-dimensional systems. The work presented in [9] depends on approximating the geometrical layout of real wiring nets of FPGA. The same model may not be applicable to 3D. Zhibin *et al.* [10] proposed a methodology for estimating the number of segments that can be used by the given circuit on FPGA with hierarchical routing architecture well before the placement stage but the given net can be routed by only one type of segment and combination of segments is not possible. They have not considered nets related to IOs. In [11], the authors proposed a model for wirelength requirement for 3D FPGAs to show the benefits of 3D integration. And also they have obtained the results by considering each type of routing segment separately. Up to our knowledge there is no direct work on early estimation of hierarchical routing resources for 3D FPGA.

## III. HIERARCHICAL ROUTING RESOURCES IN FPGA

The hierarchical routing resources provide a greater flexibility for routing the target design. In commercial FPGAs, for example, a Xilinx Virtex II device [12] has fully buffered programmable interconnections, with a number of resources counted between any two adjacent SBs at which each vertical and horizontal routing channel interacts. The widely used academic tool VPR [5] has similar resources with a combination of single-length (SL), double-length (DL), hex-length (HL) segments and long length (LL) wires. An example

of horizontal routing channel having a width of 50 on a 20 x 20 FPGA array is shown in Fig. 3.

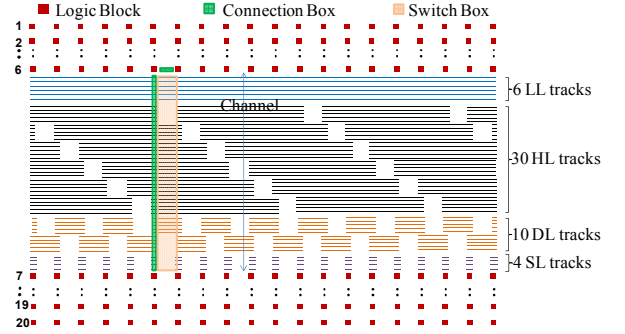


Figure 3. Typical horizontal routing channel in 2D FPGA

On a FPGA plane, the length of a wire can be represented in terms of the logic block (LB) hops that means whenever a signal passes by a LB then distance will be increased by one hop. Each wire can be categorized into two classes: segmented (SL, DL and HL) and non-segmented (LL) wires. Here a segment is defined as a metal wire that can span over a specific number of LBs and terminate at SBs. SL segments intersect at each SB to form a grid of interconnections. An example connection between a source LB and a sink LB routed by SL segments is shown in Fig. 4(a). DL segments are twice as long as SL ones and run past two LBs before entering a SB. Similarly HL segments run past six LBs. And example connection using DL and HL segments is shown in Fig. 4(b). LL wires bypass all the SBs and form a grid of connections that runs vertically and horizontally the entire length and width of the FPGA array. Nets that are distributed over long distances can be routed through LL.

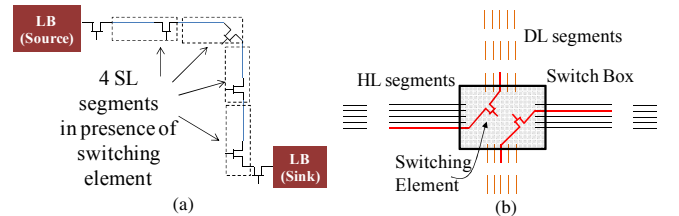


Figure 4. Example connection using (a) only SL segments (b) combination of HL and DL segments

3D FPGA array size = 20 x 20 x 4, routing channel width = 50  
 Number of SL tracks /channel,  $N_{w,SL} = 4$   
 Number of SL segments /track,  $N_{sg,SL} = 20$

Total number of channels for the given 4-layer 3D FPGA,  
 $N_{ch,T} = 4 * (19+19+4) = 168$

Total number of SL segments for the given 4-layer 3D FPGA,  
 $N_{SL,T} = N_{w,SL} * N_{sg,SL} * N_{ch,T} = 13440$

Figure 5. Example calculation for number of SL segments available

For each horizontal and vertical routing channel, the share of each type of segments is fixed by the architecture definition. For example, the total number of available SL segments in a 4-layer 3D FPGA can be obtained as shown in Fig. 5 (with reference to Fig. 3). Each layer consists of 19 horizontal channels, 19 vertical channels and 4 separate

channels for each side of the IO banks. Table I gives a typical share of all four types in a 4-layer 3D FPGA with an array size of 20 x 20 and a routing channel width of 50 for each layer.

TABLE I. SHARE OF EACH SEGMENT TYPE IN 4-LAYER 3D FPGA

Segment Type	Length of segment (in terms of LB hops)	Max available tracks/channel	Total number of segments ( $N_{seg}$ )
Single-Length (SL)	1	4	13440
Double-Length (DL)	2	10	17640
Hex-Length (HL)	6	30	21000
Long-Length (LL)	long	6	1008

#### IV. ESTIMATION METHODOLOGY

Typical routing estimation requires geometrical information of the nets that need to be routed which is available only after the actual placement. Our methodology works before the placement and immediately after the partitioning of the circuit. At this stage, available information is only the number of nets and LBs in the circuit.

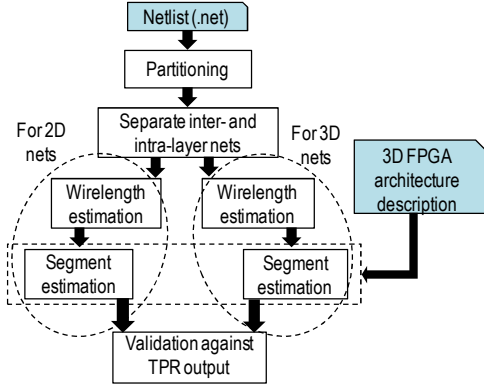


Figure 6. Proposed estimation methodology

As shown in Fig. 6, our proposed methodology takes the technology-mapped netlist of the given circuit as input and performs the multi-level hypergraph partitioning using hMeTiS [13]. We then separate the obtained nets into 2D and 3D nets. By using Stroobandt's model [8], we get the probability of each net to have a specific length (wirelength distribution) for both 2D and 3D nets separately. Depending on these values, segment estimation routine calculates the number of segments used by the given circuit. Here the actual geometry of the nets is predicted depending on the possible combinations of routing the nets in different directions (X, Y and Z) separately for 2D and 3D nets. We extended the work proposed in [10] by incorporating the combination of segments for connecting a given net between any two LBs and also between LB and IOs. For this, we have made few assumptions in our methodology as given below:

- All the four types of segments are internally unpopulated which means it is not possible to make connections from the middle of a segment to other. Indirectly, the segments terminating at SB will be able to connect to other segments while the segments that pass through SB cannot connect to other segments.

- Partitioning result contains the nets assigned to each layer such that a 3D net will pass through any two layers, but not passing through several layers.
- Multi-terminal nets are treated as separate two-terminal nets.
- Design uses less number of LL wires which means that during the next stage (placement), the logic will be placed as close as possible.

From our observations on segmented routing in FPGAs, above assumptions are necessary with respect to the unavailability of most of the required information for the estimation purpose. Validation on the methodology is done by comparing the estimated values against the results generated by TPR [14] which is a 3D place and route tool for FPGAs.

##### A. Wirelength distribution

For estimating the routing segments it is also required to know the wirelength distribution of the given circuit. We obtained this distribution based on Stroobandt's model [8]. He derived the model by satisfying the Rent's rule [15]. In his work, Stroobandt first partitions the given circuit and the 3D Manhattan grid into equal parts. Then each sub-circuit is placed into the sub-block of the grid with the help of hierarchical placement. This is repeated until each cell in the circuit is mapped to exactly one block of the grid. In his model, wirelength distribution is obtained by generating a set of parameters separately for the circuit and for the grid. The target parameter defined as the normalized wirelength distribution,  $P(L_l)$  is obtained by multiplying the structural distribution,  $S_T^{3D}(l)$  generated for the grid by the occupational probability,  $q_l$  calculated depending on the Rent's exponent  $r$  of the given circuit. A typical value for  $r$  can be obtained using top-down partitioning with hMeTiS like with the method described in [16]. For a specific length of  $l$ ,

$$P(L_l) = S_T^{3D}(l) * q_l \quad (1)$$

Where,

$$q_l = C(l^{3r-6}) \quad (2)$$

Here  $C$  is the normalization constant which depends on circuit parameters like the number of nets and  $r$ . In (1),  $S_T^{3D}(l)$  is obtained separately for 2D and 3D nets as the enumeration of all pairs in which each pair is at a distance of  $l$  apart in the Manhattan grid having a size of  $\lambda$ . For 3D nets, the connection paths are assumed in three different combinations: adjacent (A-combinations), diagonally opposed located at a near diagonal (N-combinations) and diagonally opposed located at a remote diagonal (R-combinations) as shown in Fig. 7(a), 7(b) and 7(c), respectively.

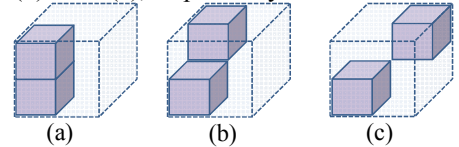


Figure 7. (a) A-combinations (b) N-combinations (c) R-combinations for 3D nets [8]



The combined structural distribution for these combinations is given by,

$$S^{3D}(l) = \frac{1}{30} S_{k,i} \quad \text{where } i\lambda \leq l \leq (i+1)\lambda, \quad (3)$$

with  $i = 0, \dots, 5$

$S_{k,i}$  is obtained by generating polynomials (detailed information on this can be found in [8]). Here  $k$  is the level of hierarchy and ranging from  $(K-1)$  to 0 in which  $K$  is related to the number of LBs,  $G$ , in the input circuit using the relation  $G = 8^K$ . And the structural distribution of the entire Manhattan grid is given by,

$$S_T^{3D}(l) = \begin{cases} (2l^2 + 1)\lambda^2(\lambda - l) + \frac{l^2(l^2 - 1)\lambda}{2} - \frac{l(l^2 - 4)(l^2 - 1)}{30} & (0 < l \leq \lambda) \\ \frac{\lambda(7l\lambda + 1)(3\lambda^2 - 1)}{2} - \lambda^3(2\lambda^2 + l^2) + 5l^2(l - 2\lambda)\lambda^2 - (l^2 - 1)^2\lambda + \frac{l(l^2 - 4)(l^2 - 1)}{15} - \frac{11\lambda(\lambda^4 - 1)}{10} & (\lambda < l \leq 2\lambda) \\ \frac{1}{30} \prod_{i=-2}^2 (3\lambda - l + i) & (2\lambda < l \leq 3\lambda) \end{cases} \quad (4)$$

Then structural distribution for 2D nets is generated as,

$$S^{2D}(l) = S_T^{3D}(l) - S^{3D}(l) \quad (5)$$

#### B. Probability of using each segment type by 2D nets

The next part of the methodology is to find the probability of using different types of segments by a given net which is having a specific length  $l$ . The idea proposed by [10] aimed at finding the possible combinations in routing a net on X-Y plane which motivates us to do separate analysis for 2D and 3D nets. As shown in Fig. 8, let us consider a net  $q$  having a specific length  $l$ , that needs to be connected between A (source) and B (sink). Note that in case of a multi-terminal net, the number of sinks will be larger and we are assuming each multi-terminal net as separate two-terminal nets.

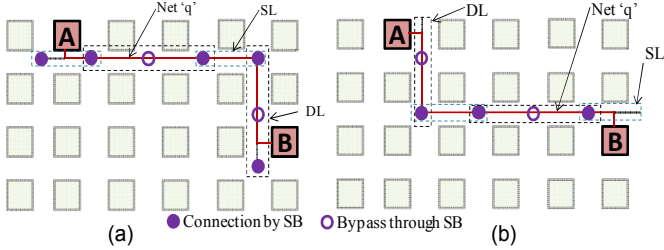


Figure 8. Example connection using combination of SL and DL segments

On the X-Y plane (combination of  $(+x, +y)$ ,  $(+x, -y)$ ,  $(-x, +y)$  and  $(-x, -y)$ ), there will be  $4 * l$  possible combinations in routing the net  $q$ . In each combination, the possibility of connecting  $q$  using different segments can be analyzed by carefully looking at the length in the X and Y directions. The probability of using HL segment by net  $q$  which is having a length of six hops is examined below. Note that while calculating the possible combinations we are taking care of minimizing the usage of switches by choosing the segments depending on the length. From Table II it is clear that there are

four possible combinations of using the HL out of available 24 combinations. For the remaining combinations we can use the other segments (SL or DL or both). Hence these combinations can be added to the respective segment usage calculations. Here  $(\pm 5, \pm 1)$ , for example, means there is five LB hops distance from source LB to sink LB in X-direction and one LB hops distance from source LB to sink LB in Y-direction. And '+' or '-' represents the possible direction of routing the net in all four co-ordinates on an FPGA XY-plane.

TABLE II. POSSIBLE COMBINATIONS FOR A NET OF LENGTH 6 HOPS

Possible combinations	Segment type usage
$(\pm 6, 0), (0, \pm 6)$	HL, SL
$(\pm 5, \pm 1), (\pm 1, \pm 5)$	DL, SL
$(\pm 4, \pm 2), (\pm 2, \pm 4)$	DL, SL
$(\pm 3, \pm 3)$	DL

As shown in Table II, after finding the similar kind of possible combinations for different lengths in an FPGA of array size  $N$ , we have determined the probability of using the HL segments as,

$$P_{HL}^{2D} = \frac{P(L_6)}{6} + \frac{2P(L_7)}{7} + \frac{2P(L_8)}{8} + \sum_{l=8, j=1,3,5..}^N \frac{j P(L_l)}{l} \quad (6)$$

Here  $P(L_l)$  is the probability of a net to have length  $l$  which we found in (1) for 2D nets in sub-section A of section IV. A similar approach is applied to find the probabilities of the other segments as given in (7), (8) and (9). For SL segments,

$$P_{SL}^{2D} = P(L_1) + \frac{P(L_2)}{2} + \frac{2P(L_3)}{3} + \frac{P(L_4)}{4} + \frac{3P(L_5)}{5} + \frac{2P(L_6)}{6} + \frac{5P(L_7)}{7} + \frac{3P(L_8)}{8} + \sum_{l=9}^N \frac{(l-1)P(L_l)}{l} \quad (7)$$

For DL segments,

$$P_{DL}^{2D} = \frac{P(L_2)}{2} + P(L_3) + \frac{3P(L_4)}{4} + 2 \frac{P(L_5)}{5} + \frac{P(L_6)}{6} + \frac{5P(L_7)}{7} + \frac{3P(L_8)}{8} + \sum_{l=9}^N \frac{(l-1)P(L_l)}{l} \quad (8)$$

For LL wires,

$$P_{LL}^{2D} = \frac{P(L_7)}{5} + \sum_{l=8}^N \frac{3 P(L_l)}{l} \quad (9)$$

#### C. Probability of using each segment type by 3D nets

Difference between a net in 2D plane and a net in 3D plane comes from the possible ways of routing the net. It is easy to find the combinations if the net is routed in two directions (Fig. 9(a)). Prediction in Z direction depends mainly on the variable

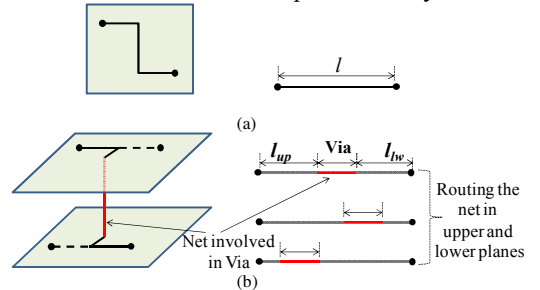


Figure 9. Connection of a net in (a) 2D and (b) 3D planes

length of the TSV. Fortunately, the length of TSV is fixed for a given architecture which will gives us the opportunity to think about only the remaining length of the net occupied by both upper and lower planes as shown in Fig. 9(b). Given 3D net can be divided in to three parts: upper plane net  $l_{up}$ , lower plane net  $l_{lw}$  and via. It is clear from the figure that the routing a net exists in upper and lower planes and obviously in only two directions, X and Y.

Hence the methodology for finding the possible combinations of connecting 2D nets (derived in previous subsection) can also be applied for finding the possible combinations of moving the nets  $l_{up}$  and  $l_{lw}$ . Since the length of via is only one hop, we can add the number of combinations equal to the cut size of the circuit to the combinations related to SL segments. We are assuming that the LL wires are not involved for 3D nets which is a fair assumption from the algorithmic point of view. The probability for a 3D net to have a specific length explained in the first part of section IV will be used in the calculations. Due to space limitation, an example calculation for only SL segments is given below and is valid for both  $l_{up}$  and  $l_{lw}$ .

$$P_{SL}^{3D} = P(L_1) + \frac{P(L_2)}{2} + \frac{2P(L_3)}{3} + \frac{P(L_4)}{4} + \frac{3P(L_5)}{5} + \frac{2P(L_6)}{6} + \frac{5P(L_7)}{7} + \frac{3P(L_8)}{8} + \sum_{l=9}^{N/2} \frac{(l-1)P(L_l)}{l} \quad (10)$$

And the total probability for SL segment usage is given as,

$$P_{SL} = P_{SL}^{3D} + P_{SL}^{2D} \quad (11)$$

Fraction of each segment type used by the given circuit is then calculated depending on the equation similar to (11) for each type of the segment, number of nets in the circuit and the available number of segments for each type.

#### D. Segment Usage Calculation

After parsing the technology-mapped input netlist, the number of nets represented by the circuit consists of both two-terminal and multi-terminal nets. Multi-terminal nets are separated by finding the number of sinks that each net is associated with. And finding the sinks associated with the nets belong to input and output pins gives rise to number of wires related to IO pads. Our methodology implicitly considers this during the segments usage calculation. The fraction of segments used by a given circuit is calculated as,

$$U_{type}^e = \frac{P_{type} N_{net}}{N_{type,T}} \quad (12)$$

This represents the estimated number of utilized routing segments out of available resources. Here  $P_{type}$  is obtained similar to (11) for each type of segments,  $N_{net}$  is the total number of nets including the multi-terminal nets in the circuit,  $N_{type,T}$  is the available number of segments for each type in the architecture. This calculation holds good for both the nets connected between any two LBs and connected between IOs and LBs.

#### V. EXPERIMENTAL RESULTS

We have implemented our methodology in C++ on an Ubuntu Linux based machine. We have considered a 4-layer

3D FPGA with an array size of 50 x 50 and a routing channel width of 65 for each layer such that all the selected 14 MCNC benchmark circuits will be successfully placed and routed. The share of each type of segment in the channel is similar to the Xilinx Virtex II device. We then partitioned each circuit using hMeTiS and separated the 2D and the 3D nets. The probability of each wire having a specific length is found separately for 2D and 3D nets using (1). By feeding these values along with input nets, our estimation methodology has been successfully applied for all the circuits. Validation has been performed against results obtained from TPR ( $U_{type}$ ) and respective results are shown in Table III. The mean error ( $\mu$ ) is calculated as the average of the absolute ratios  $|U_{type} - U_{type}^e|/U_{type}$ . As shown in the table we achieved 29.04% mean error for segmented wires (SL, DL and HL) among all 14 circuits.

From Fig. 10, except for LL wires, it is clear that the estimation follows the expected values. And nearly 80% of the circuits are having SL, DL and HL segment estimations with a mean error of around 20% and nearly 50% of them are having around 15% mean error. This is important because the segmented wires will have higher number of switching elements and hence we can surmise that the estimation with an acceptable error rate for such resources results in better analysis of power at an early stage of the design cycle. For the estimation purpose, we assumed that the circuit will be placed as close as possible and hence requires less number of non-segmented wires. This kind of assumption is a general case for the routing estimation which targets for reducing power consumption at the early stage of the design cycle. And also this assumption is valid due to the objectives derived for place and route algorithms [17] and the smaller share of non-segmented wires for each channel. Because of this, our methodology underestimates the usage of LL wires compared to the TPR values. For the circuits that are large enough, this has no real influence on the average because the number of longer interconnections is relatively small. In real case the usage of LL wires purely depends on the performance of place and route algorithms.

#### VI. CONCLUSION

We presented a methodology for estimating the required routing segments for a given circuit in a 3D FPGA immediately after the partitioning stage and validated against TPR. We achieved an acceptable error rate on average for different sizes of the circuits. We believe that individual routing segment estimation gives opportunity to designers to accommodate extra space in solving complex tasks and while taking design decisions during the architecture and EDA development. The immediate future work would be to use this methodology for early estimation of power and thermal values considering different FPGA architectures on 3D platforms.

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TABLE III. COMPARISON OF ESTIMATED VALUES AGAINST REAL VALUES OBTAINED FROM TPR

Benchmark Circuit	CLBs	Nets including multi-terminal nets	Rent's Exponent (r)	Fraction of segments used (values from TPR)				Fraction of segments used (estimated values)				% Mean error for segmented wires ( $\mu$ )
				$U_{SL}$	$U_{DL}$	$U_{HL}$	$U_{LL}$	$U_{SL}^e$	$U_{DL}^e$	$U_{HL}^e$	$U_{LL}^e$	
alu4	1522	5408	0.77	0.10	0.04	0.03	0.28	0.06	0.02	0.03	0.06	36.03
apex2	1878	6692	0.61	0.15	0.05	0.04	0.37	0.07	0.02	0.02	0.06	58.79
bigkey	1707	6537	0.87	0.06	0.03	0.05	0.25	0.07	0.03	0.04	0.07	16.45
clma	8383	30495	0.51	0.38	0.12	0.21	0.56	0.31	0.10	0.16	0.18	19.93
des	1591	6110	0.77	0.06	0.05	0.07	0.27	0.07	0.02	0.03	0.07	38.97
diffeq	1497	5673	0.71	0.06	0.03	0.03	0.28	0.06	0.02	0.03	0.06	18.54
elliptic	3604	13756	0.84	0.14	0.06	0.07	0.46	0.15	0.06	0.09	0.15	16.29
frisc	3556	13658	0.77	0.18	0.06	0.08	0.46	0.15	0.05	0.08	0.16	10.11
pdc	4575	17193	0.67	0.49	0.08	0.11	0.52	0.18	0.05	0.07	0.18	42.47
s298	1931	6959	0.78	0.10	0.03	0.03	0.34	0.08	0.03	0.04	0.08	23.41
s38417	6406	22807	0.65	0.12	0.07	0.12	0.49	0.14	0.07	0.08	0.22	22.32
s38584.1	6447	22100	0.72	0.09	0.08	0.12	0.46	0.15	0.08	0.11	0.24	26.17
seq	1750	6193	0.75	0.15	0.05	0.04	0.37	0.07	0.02	0.03	0.07	39.05
spla	3690	13808	0.70	0.34	0.07	0.08	0.42	0.15	0.05	0.06	0.15	37.98
<b>Average</b>			0.72									29.04

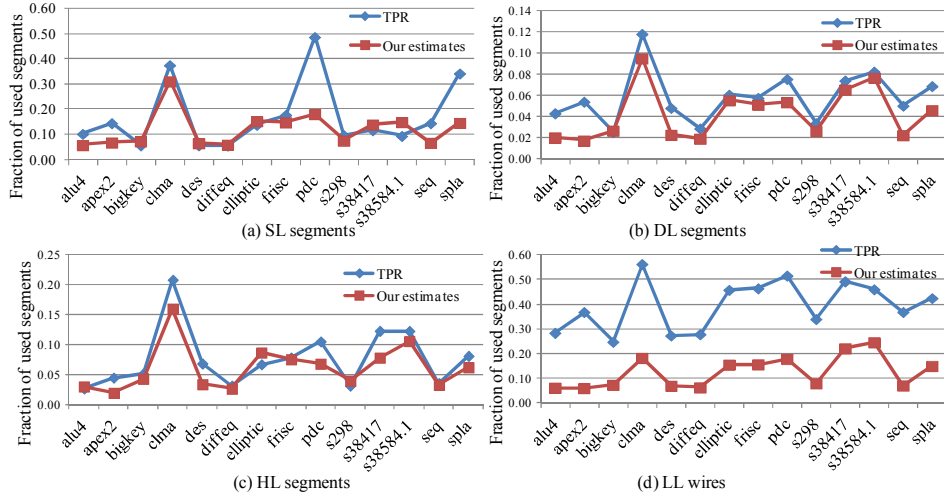


Figure 10. Estimated values versus those of TPR for all four types of routing segments

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