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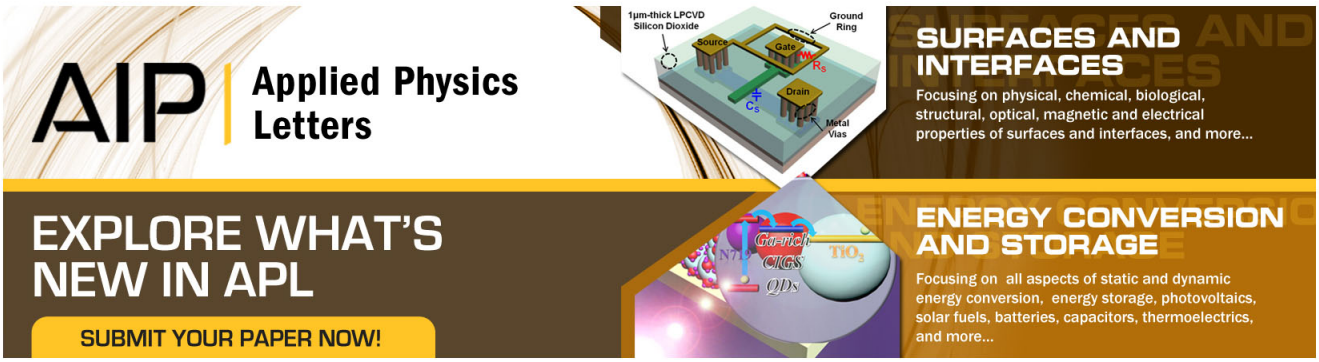

Chip-size formation of high-mobility Ge strips on SiN films by cooling rate controlled rapid-melting growth

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High-quality Ge-on-insulators (GOIs) are essential structures for high-performance transistors on an Si platform. We developed a rapid-melting-growth process for amorphous Ge (*a*-Ge) by optimizing the cooling rate and the underlying insulating materials. The effects of the solidification process for molten Ge on hole generation and spontaneous nucleation in Ge were determined. In addition, nucleation in the *a*-Ge matrix was found to be drastically suppressed by substituting SiO_2 underlayers with SiN underlayers. By combining high cooling rates (10.5–11.5 °Cs^{-1}) and SiN underlayers, we obtained ultra-long single crystal GOI strips (1 cm) with high hole mobilities (> 1000 $cm^2V^{-1}s^{-1}$). This chip-size formation of high-quality GOI will facilitate the development of advanced high-speed Ge-based devices. © *2011 American Institute of Physics*. [doi:10.1063/1.3611904]

Germanium (Ge) is a promising material for advanced high-speed metal-oxide semiconductor (MOS) transistors as it provides much higher carrier mobility than Si.[1–3] Formation techniques for gate stacks and source/drain junctions in Ge devices have been developed and they have enabled the production of high-performance Ge MOS transistors on a Ge substrate.[2,3] To integrate Ge transistors on an Si platform, the formation of single-crystal Ge-on-insulators (GOIs) becomes essential. These GOI structures further improve transistor performance by decreasing the parasitic capacitance and the leakage current.[4,5]

Recently, the seeded rapid-melting growth of amorphous Ge (*a*-Ge) has been investigated, which has enabled the production of defect-free single crystal (100) Ge strips (length, 20–40 μm; width, 1–3 μm) on insulators.[6–8] The monolithic integration of GOI transistors with Si transistors on an Si substrate has also been reported.[9] Our past efforts have focused on the mechanism of this growth, which has enabled the production of (100), (110), and (111) oriented GOI strips of 400 μm in length.[10,11] They are over one order magnitude longer than that previously achieved.[6–8] In addition, high hole mobility (~ 1000 $cm^2V^{-1}s^{-1}$)[12] and GOI networks with mesh-patterned Ge films[13] have been obtained.

If the lateral growth length can be extended to centimeters (cm) in size, i.e., 25 times longer than that in our previous work,[10–13] we can obtain a single-crystal GOI equivalent to the chip size of an integrated circuit. This enables us to remove wasted areas in a chip by arranging the Si seeding areas in scribe lines, which is a significant step toward achieving high-density Ge transistor circuits. In this paper, we examine the influence of cooling rates and underlying insulating materials on the seeded rapid-melting growth of Ge. Ultra-long single-crystal GOI strips (~ 1 cm) with high hole mobilities (> 1000 $cm^2V^{-1}s^{-1}$) were obtained.

In our experiments, Si (100) substrates (600 μm thickness) that were covered with SiO_2 (50 nm thickness) or SiN films (50, 100 nm thickness) were used. These films were patterned using wet etching to form seeding areas (20×25 μm^2). The edges of the seeding areas were formed perpendicular to the ⟨011⟩ direction. Subsequently, 100-nm-thick *a*-Ge layers were deposited using a molecular-beam epitaxy system at a base pressure of 5×10^{-10} Torr. They were patterned into strips (length: 400 μm and 1 cm, width: 3 μm). Then, bilayer capping films of SiO_2/SiN (800 nm/30 nm thickness), which had been used for the zone-melting growth of Si films,[14] were deposited to suppress agglomeration in the molten Ge films. A sample structure is shown in Fig. 1(a). Finally, these samples were heat-treated at 950 °C (1 s) and subjected to various cooling rates (0.8–11.5 °Cs^{-1}) using rapid thermal annealing (RTA). The sample temperatures during growth were monitored by a thermocouple (TC). By changing the temperature falling program of the RTA system, the cooling rates of the samples were controlled over a wide range (0.8–4.3 °Cs^{-1}). This is shown in Fig. 1(b) using solid lines. To control the cooling rates in a rapid-cooling region (10.5–11.5 °Cs^{-1}), pre-heating (PH) at 400 °C and 800 °C (1 min) was carried out followed by high-temperature RTA (950 °C,

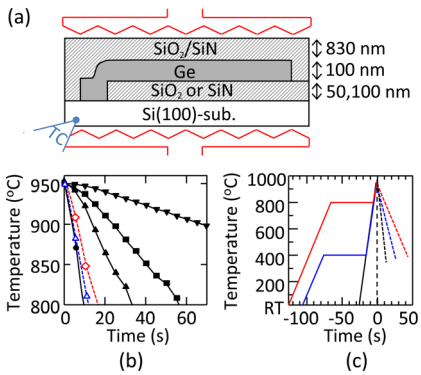

FIG. 1. (Color online) (a) Schematic diagram of the sample structure and (b) temperature falling profiles of the samples after reaching the highest temperature (950 °C) as monitored using a TC. (c) Temperature increase and falling profiles without and with pre-heating (400 and 800 °C: 1 min).

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1 s), as shown in Fig. 1(c). These cooling profiles are replotted in Fig. 1(b) as dashed lines.

After removing the capping layers, the crystal orientations and crystal qualities of the grown layers were characterized using electron backscattering diffraction (EBSD) and cross-sectional transmission electron microscopy (X-TEM). The lateral distributions of Si atoms along the growth direction were measured by micro-probe Raman spectroscopy (spot diameter: 1 μm), where the Si concentration was estimated using the equation proposed by Mooney *et al.*[15] The electrical characteristics of the grown Ge strips were determined by the four-terminal method, where aluminum electrodes were formed on Ge strips by vacuum evaporation after dilute HF (1.5%) cleaning. The carrier concentrations and mobilities were obtained by measuring the temperature dependence of the electrical conductivities. The details of this process have been described in previous work.[10,12]

We examine the electrical properties of the grown Ge strips (length: 400 μm) as a function of the cooling rate. A typical Ge strip with aluminum electrodes is shown in Fig. 2(a). EBSD measurements show that all the Ge strips of 400 μm in length are single-crystallized with a (100) orientation, which is identical to the Si substrates. In addition, the thermo-electromotive force measurement revealed that the majority of carriers are holes. Many researchers have reported that holes are generated in thin film Ge crystals during growth.[16,17] These are attributed to the formation of complex defects, which are stable at room temperature.

Hole mobilities and hole concentrations at the center of the grown Ge strips are shown in Fig. 2(b) as a function of cooling rates. This clearly indicates that RTA with higher cooling rates can provide lower hole concentrations, which results in higher hole mobilities because of a reduction in the impurity scattering. In a thermal equilibrium process such as zone melting, a lower cooling rate usually leads to higher crystallinity.[18] However, the present growth process using RTA is a non-equilibrium solidification process. When the cooling rate of molten-Ge is high, the chance to form complex defects because of agglomerating point defects is reduced. Consequently, high crystallinity at a temperature slightly below the solidification temperature is considered to be quenched by rapid cooling. Therefore, high hole mobilities exceeding 1000 $cm^2V^{-1}s^{-1}$ are obtained when using RTA at high cooling rates (>10 °Cs^{-1}). The thermal stabilities of electrical properties in the Ge grown using the highest cooling rate (~11.5 °Cs^{-1}) are also examined. Figure 2(c) shows the electrical conductivities after post-annealing, i.e., 400 °C (65 h), 800 °C (5 h), 900 °C (5 h), and 920 °C (5 h), which indicates stable electrical properties for the grown Ge strips. A detailed analysis revealed that both the hole mobility and the hole concentration did not change after high temperature post-annealing (920 °C, 5 h). This guarantees device stability during high temperature processing. In addition, these results suggest that holes that originate from complex defects are generated during the solidification of molten Ge. Therefore, the important role of high cooling rates (>10 °Cs^{-1}) to achieve high mobilities (>1000 $cm^2V^{-1}s^{-1}$) by suppressing hole generation is clarified.

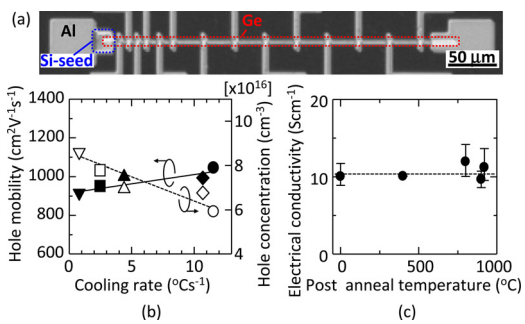

FIG. 2. (Color online) (a) Nomarski optical micrograph of the grown Ge strip with Al electrodes. (b) Cooling rate dependence of hole mobilities and hole concentrations at the center of the grown Ge strips. (c) Electrical conductivities of the grown Ge layers after post-annealing.

To examine the maximum growth-length of Ge, rapid-melting growth using ultra-long *a*-Ge strips of 1 cm in length is investigated. An EBSD image of a Ge strip grown using the highest cooling rate (11.5 °Cs^{-1}), i.e., with an SiO_2 underlayer and RTA without pre-heating, is shown in Fig. 3(a). The resolution of the crystal orientation in the color mapping is about 5°. Epitaxial growth in the lateral direction stops at 0.5 mm from the Si seed. This clearly indicates that spontaneous nucleation occurs in the amorphous matrix and prevents lateral growth. When the cooling rate is reduced to 10.5 °Cs^{-1} by pre-heating at 800 °C (1 min), the growth length extends to 4.4 mm, as shown in Fig. 3(b). Similar results were obtained by Im and Kim[19] and Lee *et al.*[20] while investigating laser annealing induced melting growth for a Si-on-insulator. They found that the degrees of the super-cooling state decrease by lowering the cooling rates, which results in longer Si lateral growth by suppressing spontaneous nucleation.

Therefore, we are confronted by the fact that a further reduction in the cooling rate is necessary to achieve cm size growth, which also causes a reduction in carrier mobility, as discussed above. A possible solution for this dilemma is the use of a new underlying insulator that will reduce spontaneous nucleation by modulating the interfacial energies between Ge and the insulators.

We therefore employed an SiN film as a new underlying insulator. To adjust the cooling rate of the Ge/SiN/substrate structure to that in the Ge/SiO_2 (50-nm-thick) substrate, a

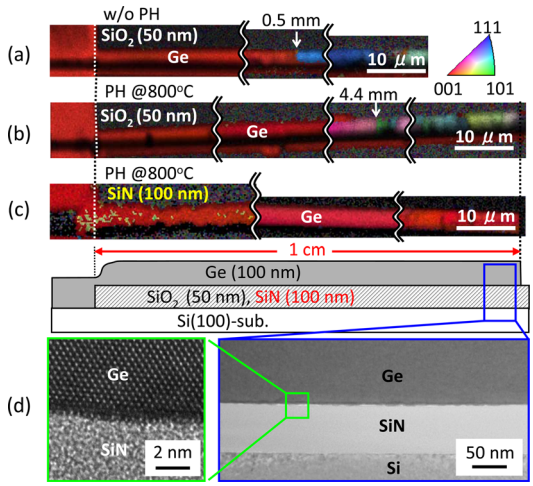

FIG. 3. (Color) EBSD images of the grown Ge strips on SiO_2 layers (50 nm thickness) without (a) and with PH (800 °C, 1 min) (b), and on an SiN layer (100 nm thickness) with PH (800 °C, 1 min) (c). Cross-sectional TEM images of the Ge strip on an SiN layer (d).

thick SiN layer (100 nm) was used to compensate for the different thermal conductivities between SiO_2 (0.014 $Wcm^{-1}K^{-1}$) and SiN (0.032 $Wcm^{-1}K^{-1}$).[21,22] The sample was annealed at 950 °C (1 s) following pre-heating (800 °C, 1 min). The cooling rate was approximately the same (10.5 $°Cs^{-1}$) as that shown in Fig. 3(b), i.e., lateral growth for 4.4 mm over the SiO_2 film. Figure 3(c) shows an EBSD image of a Ge strip grown on an SiN layer, which shows the complete crystallization of Ge from Si seed to the end of the Ge strip pattern. Recently, Appapillai *et al*. reported that spontaneous nucleation can be suppressed by increasing the interfacial energy.[23] In addition, Kaiser *et al*. reported that the interfacial energy between liquid-Ge and SiN is larger than that between liquid-Ge and SiO_2, as judged from contact angle measurements.[24] These results explain our experimental results well, where spontaneous nucleation was suppressed by substituting the SiO_2 underlayer with an SiN underlayer. In this way, a chip-size single crystal GOI of 1 cm in length is achieved even at a high cooling rate (10.5 $°Cs^{-1}$). In addition, the X-TEM shown in Fig. 3(d) reveals that no dislocations or stacking faults are present even at the edge of the GOI.

To demonstrate the effect of the SiN underlayer, RTA (950 °C, 1s) without pre-heating was carried out. Even though limited lateral growth of 0.5 mm was obtained on the SiO_2 layer under a high cooling rate (11.5 $°Cs^{-1}$), 1 cm lateral growth was achieved on the SiN layer. In addition, even on a thin SiN layer (50 nm), 1 cm growth was confirmed after RTA (950 °C, 1s) without pre-heating. These results clearly indicate the important role of the underlying insulating material in suppressing spontaneous nucleation.

Finally, we evaluate the Si concentrations and the electrical properties of the chip-size single crystal Ge strip (sample shown in Fig. 3(c)). This is summarized in Fig. 4. The Si concentration profile shown in Fig. 4(a) indicates that the Si fractions in the seeding area and the seeding edge are 8% and 4%, respectively. This gradually decreases along the growth direction and becomes zero where the lateral growth length exceeds 100 μm. Consequently, a pure single crystal Ge strip almost 1 cm in length is achieved. The results shown in Fig. 4(b) indicate a high hole mobility ($\sim$1000 $cm^2V^{-1}s^{-1}$) and a low hole concentration ($< 7 \times 10^{16}$ cm^{-3}) over the entire growth region of the 1 cm crystal length.

In summary, the influence of cooling rate and the underlying insulating material on the seeded rapid-melting growth of Ge were studied. High cooling rates (>10 $°Cs^{-1}$) during the solidification process of molten Ge were found to suppress hole generation, which enables high hole mobility (>1000 $cm^2V^{-1}s^{-1}$). However, super-cooling because of high cooling rates enhanced spontaneous nucleation in the amorphous matrix, which limited the lateral growth length to less than 1 mm. This dilemma was solved by substituting the underlying SiO_2 with SiN, where the nucleation that was generated on the underlying insulator decreased drastically. By combining the high cooling rates (10.5–11.5 $°Cs^{-1}$) and an SiN underlayer, we obtained ultra-long single crystal GOI strips (1 cm) with high hole mobilities (>1000 $cm^2V^{-1}s^{-1}$). This chip-size formation of a high-quality GOI will enable the production of Ge-based devices on an Si platform.

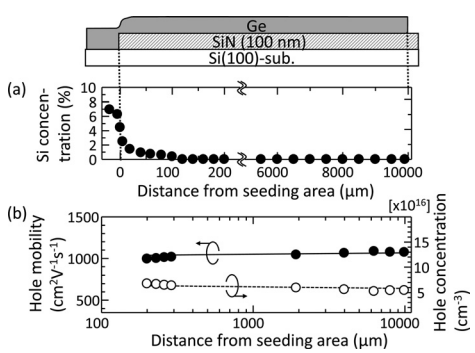

FIG. 4. Si concentration profile obtained from Raman spectra (a) and hole mobility as well as hole concentration (b) of a single-crystal Ge strip (1 cm length) on an SiN layer as a function of distance from the Si seed.

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