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Fabrication of Ge-MOS capacitors with high quality interface by ultra-thin SiO_2/GeO_2 bi-layer passivation combined with the subsequent SiO_2-depositions using magnetron sputtering

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Abstract

Ge-MOS capacitors were fabricated by a novel method of ultra-thin SiO_2/GeO_2 bi-layer passivation (BLP) for Ge surface combined with the subsequent SiO_2-depositions using magnetron sputtering. For the Ge-MOS capacitors fabricated by BLP with O_2, to decrease oxygen content in the subsequent SiO_2 deposition is helpful for improving interface quality. By optimizing process parameters of the Ge surface thermal cleaning, the BLP, and the subsequent SiO_2 deposition, interface states density of 4×10^{11} $cm^{-2}eV^{-1}$ at around midgap was achieved, which is approximately three times smaller than that of non-passavited Ge-MOS capacitors. On the contrary, for the Ge-MOS capacitors fabricated by BLP without O_2, interface quality could be improved by an increase in oxygen contents during the subsequent SiO_2 deposition, but the interface quality was worse compared with BLP with O_2.

1. Introduction

To maintain Moore's Law, it is desired to continuously improve performance of complementary metal-oxide-semiconductor (CMOS) devices, for which mobility enhancement has become a key technology. Since germanium (Ge) has superior intrinsic carrier mobility than that of silicon (Si), it is of great interest as a candidate channel material for future. So far, Ge-CMOS technology has not been realized because of many difficulties associated with different physical and chemical properties of Ge compared with Si. One of the most challenging issues is to achieve good interface property for a Ge metal-oxide-semiconductor (MOS) capacitor, which attracted many studies on passivation technology for interface between gate dielectric film and Ge substrate. One of the attractive interface passivation methods is to grow Ge compounds such as GeO_2, Ge_3N_4, and GeO_xN_y, on Ge surface [1-3]. In particular, GeO_2/Ge structure has superior interface property. From a simple calculation on the basis of viscoelastic properties of GeO_2, a good interface property of as-oxidized GeO_2/Ge (100) interface at above 500 ^oC was predicted [4]. Experimentally, Matsubara et al. have reported very low interface state density (D_{it}) of 1×10^{11} $cm^{-2}eV^{-1}$ for GeO_2/Ge structure, which were formed by dry oxidation of Ge substrate at around 575 ^oC [5].

Unfortunately, GeO_2 has poor thermal stability and high water solubility. It has been reported that thermal decomposition of GeO_2 is caused by GeO molecule desorption by furnace annealing at above 425 ^oC [6]. Abstracting Ge from Ge substrate at a GeO_2/Ge structure is essential for GeO molecule formation, causing to serious degradation of GeO_2/Ge interface property [7]. In addition, it has been also pointed out that not only water but also hydrocarbons are easily infiltrated into GeO_2 layers during air exposure,

causing to unusual negative shift of flat band voltage (V_{fb}) and large increase in hysteresis (*HT*) in capacitance-gate bias voltage (C-V_G) curve [8]. Therefore, it is difficult to integrate GeO_2 into conventional MOS fabrication process.

Thus, to passivate Ge surface by GeO_2, it is necessary to fabricate GeO_2 on Ge surface without exposure in air, and the fabricated GeO_2 layer should be also protected by a stable material, such as SiO_2, to prevent thermal decomposition and unintentional reaction with subsequently deposited gate dielectric film. If this kind of SiO_2/GeO_2 bi-layer can be very thin, it should be very useful as interlayer (IL) between insulating film and Ge substrate, because high-k film such as HfO_2 or ZrO_2 can be deposited on Ge substrate passivated with the bi-layer, for which low EOT (effective oxide thickness) and low D_{it} are expected.

In this paper, we demonstrate the fabrication of ultra-thin SiO_2/GeO_2 bi-layer for electrical passivation of Ge surface. A novel method is proposed to fabricate the bi-layer using a physical vapor deposition (PVD) system through the thermal etching of GeO_2 by vacuum annealing and the subsequent SiO_2 deposition at 350 ^oC. During the SiO_2 deposition, oxygen flow rate is an important parameter, which dominates the growth of ultra-thin GeO_2 film on Ge substrate. After Ge surface passivation, SiO_2 was deposited as gate dielectric film by magnetron sputtering followed by post deposition annealing (PDA). To validate the effect of SiO_2/GeO_2 bi-layer passivation (BLP), D_{it} was measured for all the MOS capacitors by deep level transient spectroscopy (DLTS). By optimization of the BLP and the subsequent SiO_2 deposition processes, Ge-MOS capacitor with high quality interface was successfully fabricated.

2. Ge surface passivation process

To fabricate high quality passivation layer on Ge, surface cleaning is essential. If a Ge substrate with clean surface is exposed in air, the Ge surface can be naturally oxidized, simultaneously water and hydrocarbons are easily infiltrated into the naturally oxidized GeO_2 layer during air exposure [8]. Therefore, it is better to prevent air exposure between Ge surface cleaning and surface passivation, which can be realized by a vacuum annealing for sacrificially oxidized GeO_2 combined with the subsequent passivation process in the same vacuum chamber. Figure 1 shows the process flow of the surface cleaning and passivation. A *p*-type (100) Ge substrate with a resistivity of 0.2-0.3 Ωcm was used. After cleaning by acetone and the subsequent cyclic cleaning by 10% HF dip and deionized water rinse, the sacrificial oxidation was done at 450 ^{o}C for 30 min in O_2 ambient with pressure of 1 atmosphere, resulted in GeO_2 thickness of 3 nm, as shown in Fig. 1b. The sample without sacrificially oxidized GeO_2 was also prepared for investigation. The oxidized Ge substrate was then loaded in a PVD chamber, which was subsequently pumped down to base pressure of less than 2×10^{-5} Pa. Then the Ge substrate was immediately heated by a step mode heating by lamp heater with total time of 30 min, as shown in Fig. 1c, by which the sample temperature increased up to around 550 °C at the beginning and decreased down to 350 °C during approximately 5 min. This vacuum annealing led to complete volatilization of GeO_2 layer, which was confirmed by ellipsometry measurement that GeO_2 layer disappeared completely after the step mode heating. Without breaking the vacuum, 1 nm-thick SiO_2 IL deposition was performed at deposition temperature (T_D) of 350 °C in the same chamber using PVD (radio frequency (RF) magnetron sputtering) with a SiO_2 target, where the ambient pressure *p* was 1 Pa. There are two ways to passivate Ge surface. One is to introduce O_2 in the gas ambient

during SiO_2 IL deposition, resulting in a simultaneous growth of GeO_2, as shown in Fig. 1d. Another way is to deposit SiO_2 IL without the addition of O_2 in the gas ambient, by which only SiO_2 layer was deposited on Ge surface, as shown in Fig. 1e. For this kind of passivation, a subsequent growth of Ge-oxygen compound between SiO_2 and Ge should be performed by adjusting oxygen contents in the later steps of MOS capacitor fabrication. The gas flow rates of Ar and O_2, as well as RF power P_{RF}, are also shown in Figs. 1d and 1e. P_{RF} is slightly different from each other to maintain the same deposition rate of 0.11 nm/min for above two deposition methods.

In order to clarify the structures after SiO_2 IL deposition, X-ray photoelectron spectroscopy (XPS) measurements using an Al Kα line were carried out for the samples with and without the addition of O_2 during SiO_2 IL deposition. Figure 2a shows the Ge 3*d* XPS spectra at a photoelectron take-off angle of 90°, where all measured spectra were calibrated using an Ge $3d_{3/2}$ core-level (29.3 eV). The SiO_2 signals with binding energy (BE) of 103.6 eV were clearly observed for both samples, as shown in the inset of Fig. 2a. For the sample without the addition of O_2, oxidized Ge 3*d* peaks could not be observed. This implies that initial GeO_2 layer was completely removed by vacuum annealing and the subsequent GeO_2 formation did not occur. On the other hand, the sample with the addition of O_2 showed clear oxidized Ge 3*d* peak, which shifts to higher BE by 3.2 eV relative to the Ge bulk peak (29.3 eV) [9], implying that the signal with BE of 32.5 eV is mostly originated from GeO_2. In Fig. 2b, the spectra of thermally grown GeO_2/Ge samples with thicknesses of 1.0, 1.5, and 2.4 nm, which were prepared at 400 °C for 21 min, 450 °C for 9 min, 450°C for 18 min, respectively, were used as reference for thickness of GeO_2 underlying SiO_2 IL. The signal intensity ratio of GeO_2 to Ge bulk for the sample with O_2 is close to that for 1.5 nm-thick GeO_2/Ge sample. Thus, the thickness

of GeO_2 underlying SiO_2 IL should be less than 1.5 nm, because 1 nm-thick SiO_2 IL should cause to decrease the intensity of Ge bulk XPS signal, which was confirmed by the following TEM measurement.

The sample with the addition of O_2 was prepared for the TEM observation under the same condition as 1.0 nm-thick SiO_2 IL deposition, followed by 50 nm-thick Zr deposition. Figure 3 show cross-sectional TEM image. It can be seen from the image that there is white-contrasted layer between Zr and Ge substrate, corresponding to SiO_2/GeO_2 layer with the thickness of 1.9 nm. This suggests that the thickness of GeO_2 was 0.9 nm.

3. Fabrication flow of Ge-MOS capacitors and DLTS measurement

Figure 4 shows the details of fabrication flow for Ge-MOS capacitors. The fabrications were continued from the samples with structures in Fig. 1d and 1e. Since oxygen content is an important parameter for improving interface quality of GeO_2/Ge, we performed gate SiO_2 depositions with different oxygen contents. Figures 4a and 4b show fabrication parameters of 10 nm-thick SiO_2 deposited by magnetron sputtering with (2 sccm) and without (0 sccm) the addition of O_2, respectively, in the same PVD chamber as that of BLP process. Both of them were performed at *RT* with Ar flow rate of 20 sccm and gas ambient of 1.0 Pa. P_{RF} in Figs. 4a and 4b were 50 and 42 W, resulted in SiO_2 deposition rate of 2.54 and 0.91 nm/min respectively. The explanation of the electron cyclotron resonance (ECR) sputtering is described in Sec. 4.3. Then PDA was performed at 550 ^{o}C in 1 atmosphere N_2 for 30 min to eliminate damage caused by SiO_2 deposition, as shown in Fig. 4d, which was followed by 200 nm-thick Al deposition using thermal

evaporation, as shown in Fig. 4e. Finally, Al gate electrode with area of 4.52×10^{-4} cm^{-2} was patterned by lithography and etched by H_3PO_4 solution at 40 ^oC.

D_{it} for all the MOS capacitors was measured by DLTS using DLS83D (SEMILAB Co.), which was performed according to a procedure given in Refs. [10] and [11]. During the DLTS measurement, an essential issue is to balance the enough band-bending (ϕ_s) for complete hole emission from interface states and the small ϕ_s for minimizing minority carrier generation. Based on *EOT* and V_{fb} calculated from C-V_G result measured at 220 K, a certain V_G could be determined for achieving ϕ_s equal to ϕ_B (the potential difference between Fermi level and the intrinsic Fermi level) at the maximum experiment temperature (220 K), which is the critical ϕ_s for complete hole emission from interface state. In this study, we set V_G corresponding to ϕ_B + 0.05 eV to make a margin for complete hole emission. With this V_G, D_{it} could be slightly over-estimated in the range near to mid-gap due to the contribution of minority carrier generation. Note that minority carrier generation is usually slow when $\phi_s < 2\phi_B$, but not negligible.

4. Electrical characterization of fabricated Ge-MOS capacitors

In this section, we present the three-type results classified by the BLP and subsequent gate-SiO_2 deposition methods. The type-I results are obtained from the combination of Fig. 1d and Fig. 4b. The type-II results are from the combination of Fig. 1d and Fig. 4a. The type-III results are from the combination of Fig. 1e and Fig. 4b.

4.1 Electrical characteristics of type-I Ge-MOS capacitors

We labeled the product samples #1-3 according to the BLP in Fig. 1 and SiO_2-gate deposition in Fig. 4. Sample #1 was prepared by the process in Figs. 1a → 1b → 1c → 1d→ Fig. 4b; #2 was Figs. 1a → 1c → 1d→ Fig. 4b; #3 was only Fig. 1a → Fig. 4b. For all samples, this was followed by PDA and Al electrode fabrication in Fig. 4 d and 4f.

Figure 5a shows a normalized C-V_G curve of the MOS capacitor labeled as #1, where the measurement was performed at room temperature (*RT*) and at a frequency (*f*) of 1 MHz. The bias was double-scanned from -3 to +1 V and then +1 to -3 V. *EOT*, hysteresis (*HT*) and V_{fb} were determined to be 12.5 nm, 0.22 V, and −0.73 V, respectively. By using the value of *EOT* and the deposited SiO_2 thickness, *EOT* of GeO_2 underlying SiO_2 IL was estimated to be 1.1 nm, which corresponds to the physical thickness (T_p) of 1.6 nm by taking into account that the *k*-value of GeO_2 is 5.7. Thus, it is suggested that the re-growth of GeO_2 from 0.9 to 1.6 nm occurred during 550 °C-PDA.

The fixed oxide charge density (Q_f) was estimated as $+5.7\times10^{11}$ cm^{-2} from the values of V_{fb} and the work function (4.1 eV) of Al on SiO_2 [12] using the relation of $Q_f = (\phi_{MS}-V_{fb})C_{ox}$, where ϕ_{MS} is the work function difference and C_{ox} the oxide capacitance. This situation leads to the strong inversion of Ge surface underlying GeO_2 in the area without Al electrode, and the induced electron density should be around 2×10^{11} cm^{-2}, because the maximum width W_m of the Ge surface depletion region and corresponding depletion charge were calculated as 0.2 μm and 4×10^{11} cm^{-2}, respectively, from the equation of $2\phi_B = qN_AW_m^2/(2\varepsilon_s)$ [13], where N_A is the acceptor concentration (2×10^{16} cm^{-3}), and ε_s the Ge permittivity. This causes to easy penetration of electrons in the depletion region from periphery of MOS capacitor, leading that frequency dependence of C-V_G curve shows strong inversion response [14], as shown in Fig. 5b.

Figure 5c also shows that the current density (J)–electric field (E: calculated as V_G/EOT) curve of capacitor #1 shows excellent insulating features governed by Fowler-Nordheim tunneling with a high breakdown field (E_b) of 14 MV/cm. By Fowler-Nordheim analysis, a barrier height of 3.27 eV was estimated using an effective electron mass of 0.39m (m: free-electron mass) in thermally grown SiO_2 [15], implying a good quality of the deposited SiO_2. The other MOS capacitors (#2-3) showed properties similar to those of #1, implying that the parameters of MOS capacitors such as HT, V_{fb}, and E_b were not dependent on SiO_2 IL preparation, but rather were governed by SiO_2 gate insulating film deposition and subsequent PDA.

However, D_{it} was strongly dependent on IL preparation. Figure 6 shows D_{it} results for MOS capacitors #1-3. All of the MOS-capacitors tended to show decreases with an increase in the energy position (E_T), which is very similar to the trend seen with a GeO_2/Ge interface [5]. The D_{it} values at around midgap are shown in Fig. 6. Among capacitors #1-3, #1 showed the best D_{it} result, which was 5.8×10^{11} $cm^{-2}eV^{-1}$. The worst D_{it} was observed for the capacitor #3, which was 1.2×10^{12} $cm^{-2}eV^{-1}$. The D_{it} of capacitor #2 was lower than that of #3 and higher than that of #1. Thus, it is clear that the surface thermal cleaning with sacrificial oxidation (in Figs. 1b and 1c) and the BLP (in Fig. 1d) improve interface quality.

4.2 Electrical characteristics of type-II Ge-MOS capacitors

The product samples were labeled as follows: Sample #4 was prepared by the process in Figs. 1a → 1b → 1c → 1d→ Fig. 4a; #5 was Figs. 1a → 1c → 1d→ Fig. 4a. These samples were followed by PDA and Al electrode fabrication.

Figure 7a shows a normalized C-V_G curve of the MOS capacitor labeled as #4, where the measurement was performed at *RT* and at f of 1 MHz. The bias was double-scanned from -3 to +1 V and then +1 to -3 V. *EOT*, *HT* and V_{fb} were determined to be 12.5 nm, 0.12 V, and −1.12 V, respectively. From the value of *EOT* and the same consideration in Sec. 4.1, it was suggested that the re-growth of GeO_2 from 0.9 to 1.6 nm occurred during 550 °C-PDA.

The *HT* of capacitor #4 was smaller than that (0.22 V) of capacitor #1, suggesting the improvement of interfacial layer quality. However, Q_f was estimated as $+1.2\times10^{12}$ cm^{-2} from the V_{fb}-value, which was twice higher than that of capacitor #1. Thus, Ge surface should become stronger inversion compared with capacitor #1, and induced electron density should be 8×10^{11} cm^{-2}. In fact, a C-V_G curve at f = 10 kHz showed complete strong inversion response [14].

Figure 7b also shows that the J–E curve of capacitor #4 shows excellent insulating features governed by Fowler-Nordheim tunneling with a high E_b of 12 MV/cm, for which a barrier height of 3.16 eV was obtained by Fowler-Nordheim analysis, implying a good SiO_2 quality. The capacitor #5 showed *HT*, V_{fb}, and E_b similar to those of #4.

Figure 8 shows D_{it} distribution for capacitors #4 and #5. From the comparison of D_{it} results in Fig. 8, it can be concluded that sacrificial oxidation and subsequent surface cleaning under vacuum are very useful for obtaining a good interface of IL/Ge, which is the same conclusion in Sec. 4.1. The best D_{it} of 3.7×10^{11} $cm^{-2}eV^{-1}$ at around midgap was obtained for the capacitor #4, which is approximately three times lower than that of the capacitor without thermal cleaning and BLP (#3 in Fig. 6). This was confirmed from several fabrication trials, and the obtained D_{it} was in the range of $(4\pm0.5)\times10^{11}$ $cm^{-2}eV^{-1}$.

However, it can not be concluded from the D_{it} comparison between capacitors #1 and #4 that gate-SiO_2 deposition without the addition of O_2 is better than that with the addition of O_2, because the deposition rates were different for both SiO_2 depositions (Fig. 3). Thus, we prepared a MOS capacitor (#6) using the same process as capacitor #4 with gate-SiO_2 deposition rate of 0.91 nm/min instead of 2.54 nm/min. In this case, P_{RF} was 21 W. The D_{it} result of capacitor #6 is shown in Fig. 8, which was the same as that of capacitor #4 at around midgap. Thus, we can conclude that oxygen-rich deposition method of gate-SiO_2 is harmful to interface quality for the capacitors fabricated by BLP with the addition of O_2, implying that excessive oxygen may degrade quality of the GeO_2 passivation layer.

4.3 Electrical characteristics of type-III Ge-MOS capacitors

In the case of BLP without the addition of O_2, gate-SiO_2 deposition with the addition of O_2 is essential because of no-GeO_2 formation between SiO_2 and Ge just after SiO_2 IL deposition. Actually, when the gate-SiO_2 deposition was performed without the addition of O_2, C-V_G curve showed flat line attributable to high D_{it}. Thus, we prepared a MOS capacitor labeled as #7, which was fabricated by the process in Figs. 1a → 1b → 1c → 1e→ Fig. 4b. Figure 9 shows D_{it} distribution for capacitor #7. The D_{it} at around midgap was 8.0×10^{11} $cm^{-2}eV^{-1}$, which is worse than those of capacitors #1 and #4. This is maybe caused by the insufficient supply of oxygen.

Thus, we used ECR sputtering method [16] to supply the abundant oxygen during SiO_2 deposition, as shown in Fig. 3c, which is reactive sputtering from Si target and an oxygen-rich process. The gas ambient was a mixture of Ar and O_2 with flow rates of 16

and 8 sccm, respectively. The ECR sputtering was performed at T_D of 130 ^oC with microwave power (P_μ) and P_{RF} of 300 and 100 W, respectively, and ambient pressure of 0.14 Pa, resulting in a deposition rate of 0.67 nm/min. From the gas ambient pressure and O_2 flow rate, the oxygen pressures were calculated as 0.01 and 0.047 Pa for deposition methods of Figs. 4b and 4c, respectively. Thus, ECR sputtering has longest deposition time and highest T_D, resulted in the large oxygen content introduced into the SiO_2/GeO_2 IL. We prepared two MOS capacitors labeled as #8 with the SiO_2-thickness of 8 nm and #9 with the SiO_2-thickness of 20 nm, which were fabricated by the process in Figs. 1a → 1b → 1c → 1e→ Fig. 4c.

The best D_{it} was obtained from the capacitor #9, which was approximately 6×10^{11} $cm^{-2}eV^{-1}$ at around midgap. It is interesting that D_{it} deceased with increasing SiO_2 thickness. In the case of a thicker SiO_2 deposition, a longer deposition time is needed, during which more oxygen can be introduced into the SiO_2/GeO_x IL. Therefore, after BLP without O_2 addition, an oxygen-rich condition of the dielectric SiO_2 deposition is helpful for the formation of stoichiometric GeO_2 between SiO_2 IL and Ge. However, the interface quality of BLP without the addition of O_2 is worse than that of BLP with the addition of O_2 even though oxygen-rich process was used for gate-SiO_2 deposition. Therefore, BLP with the addition of O_2 is a good candidate for the Ge-MOS gate stack with high quality interface.

5. Summary

Ge-MOS capacitors were fabricated by a novel method of ultra-thin SiO_2/GeO_2 bi-layer passivation (BLP) for Ge surface combined with subsequent SiO_2 deposition using

magnetron sputtering. Good electrical characteristics of C-V_G and J-E were shown for typical Ge-MOS capacitors. For the Ge-MOS capacitors fabricated by BLP with O_2, to decrease oxygen content in the subsequent SiO_2 deposition is helpful for improving interface quality. By optimizing process parameters of the Ge surface cleaning, the BLP, and the subsequent SiO_2 deposition, D_{it} of 4×10^{11} $cm^{-2}eV^{-1}$ at around midgap was successfully obtained for Al-gate Ge-MOS capacitor fabricated by BLP with O_2 and subsequent gate-SiO_2 deposition without O_2, which is approximately three times smaller than that of Ge-MOS capacitor without surface thermal cleaning and BLP. On the contrary, for the Ge-MOS capacitors fabricated by BLP without O_2, interface quality could be improved by an increase in oxygen contents during the subsequent SiO_2 deposition, but the interface quality was worse compared with BLP with O_2. Therefore, BLP with O_2 is a good candidate for the Ge-MOS gate stack with high quality interface.

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Figure captions

Fig. 1 Process diagram of surface cleaning and passivation for Ge substrate. (a) chemical cleaning; (b) sacrificial oxidization for Ge substrate; (c) vacuum annealing in a PVD chamber to completely volatilize the sacrificially oxidized GeO_2; (d) SiO_2 deposition by magnetron sputtering in the same chamber with the addition of O_2, resulting in SiO_2/GeO_2 passivation layer on Ge surface; (e) SiO_2 deposition by magnetron sputtering in the same chamber without the addition of O_2, by which only SiO_2 layer was formed on Ge surface.

Fig. 2 (a) Ge 3*d* XPS signals for the samples shown in Figs. 1d and 1e. A GeO_2 peak was clearly observed for the sample passivated with the addition of O_2. On the contrary, only Ge bulk signal was observed for the sample passivated without the addition of O_2; (b) Ge 3*d* XPS signals for thermally oxidized Ge samples with different GeO_2 thickness.

Fig. 3 Cross-sectional TEM image of 1.0 nm-thick SiO_2/Ge sample prepared using BLP with the addition of O_2.

Fig. 4 Fabrication flow of Ge-MOS capacitors. (a) SiO_2 deposition by magnetron sputtering without the addition of O_2 in the same PVD chamber as that of BLP process; (b) SiO_2 deposition by magnetron sputtering with the addition of O_2 in the same PVD chamber as that of BLP process; (c) SiO_2 deposition by the ECR sputtering method; (d) PDA process to eliminate damage caused by SiO_2 deposition; (e) Al deposition as gate metal. The electrode formation by lithography and wet etching is not shown. SiO_2 thicknesses were 10 nm for all the deposition methods. Other important parameters are also shown in the figure.

Fig. 5 Electrical characteristics for a Ge-MOS capacitor #1. The preparation method for capacitor #1 is described in the text. (a) normalized C-V_G; (b) frequency dependence of C-V_G. (c) J-E; The inset in Fig. 5c is the Fowler-Nordheim plot.

Fig. 6 D_{it} distribution for Ge-MOS capacitors #1, #2, and #3. The preparation method for each capacitor is described in the text.

Fig. 7 Electrical characteristics for a Ge-MOS capacitor #4. The preparation method for capacitor #4 is described in the text. (a) normalized C-V_G; (b) J-E; The inset in Fig. 7b is the Fowler-Nordheim plot.

Fig. 8 D_{it} distribution for Ge-MOS capacitors #4, #5, and #6. The preparation method for each capacitor is described in the text.

Fig. 9 D_{it} distribution for Ge-MOS capacitors #7, #8, and #9. The preparation method for each capacitor is described in the text.

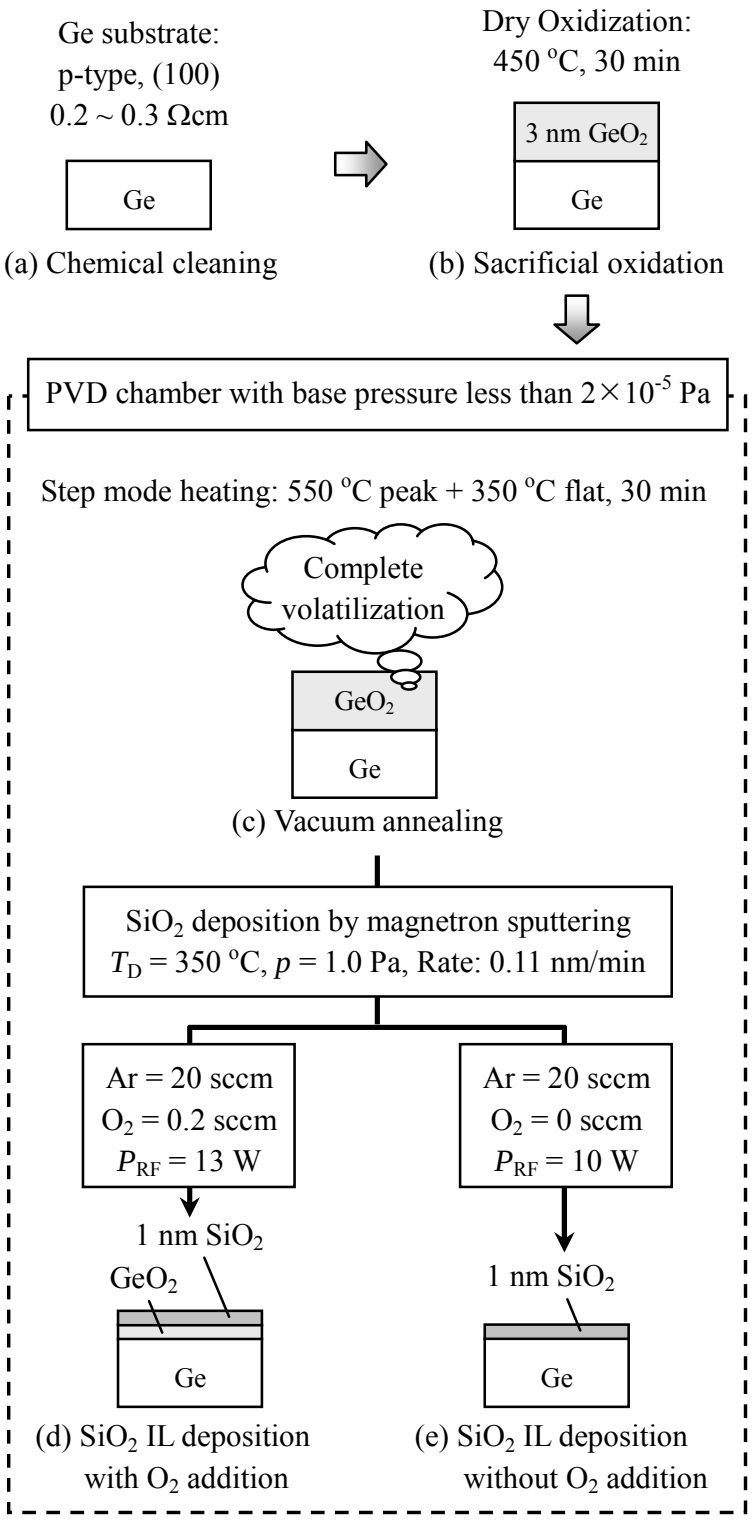

Figure 1. Kana Hirayama *et al*.

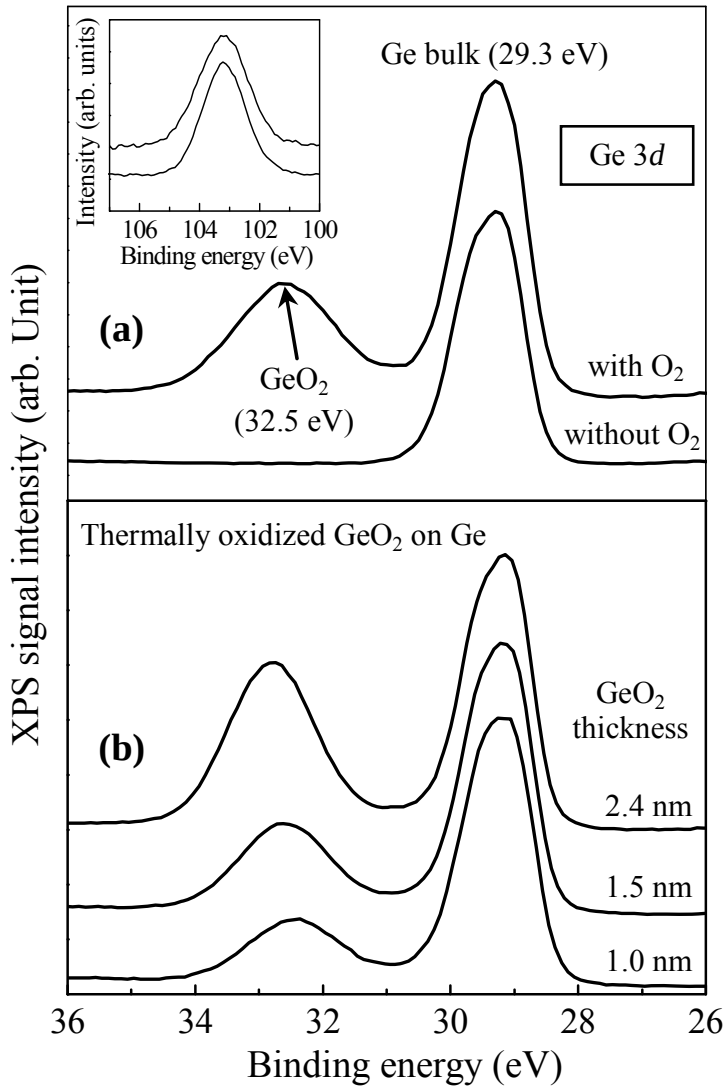

Figure 2. Kana Hirayama *et al*.

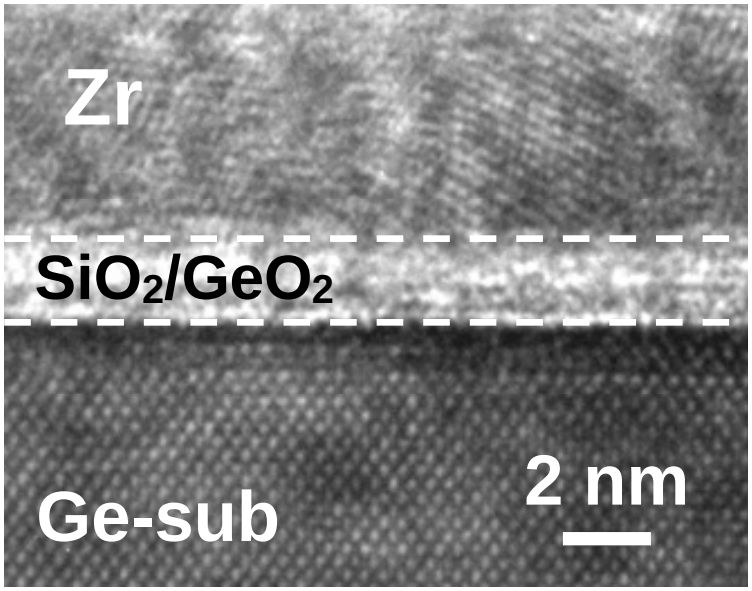

Figure 3. Kana Hirayama *et al*.

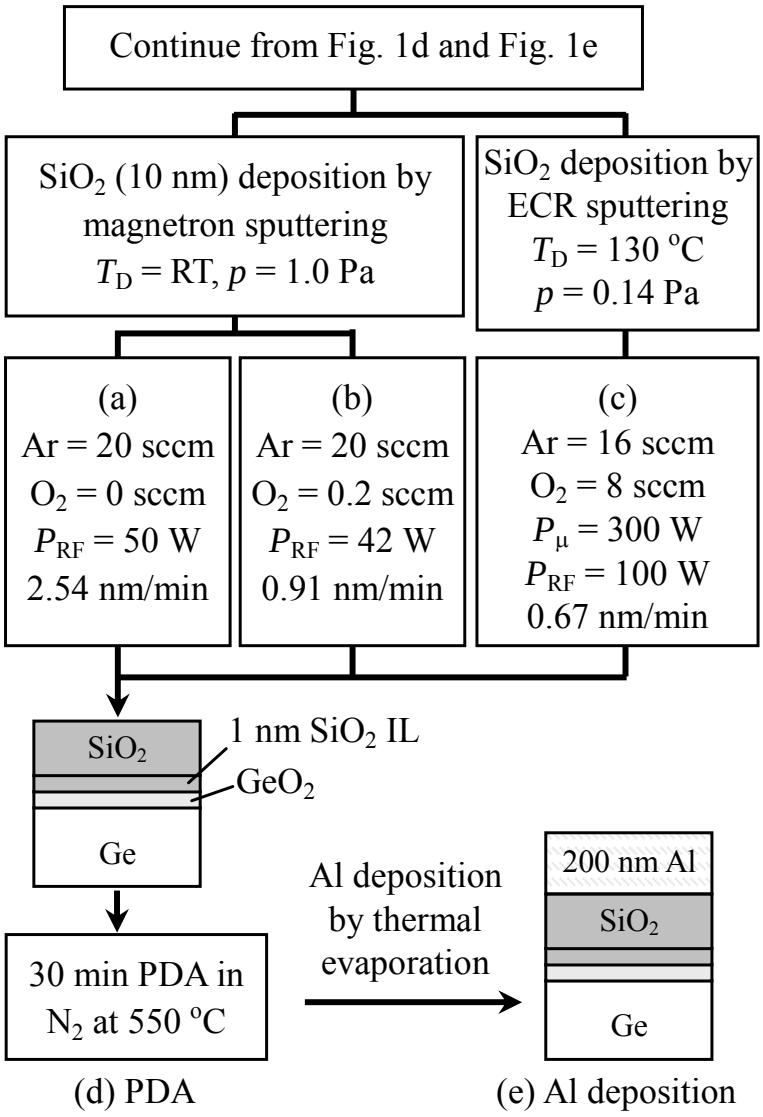

Figure 4. Kana Hirayama *et al*.

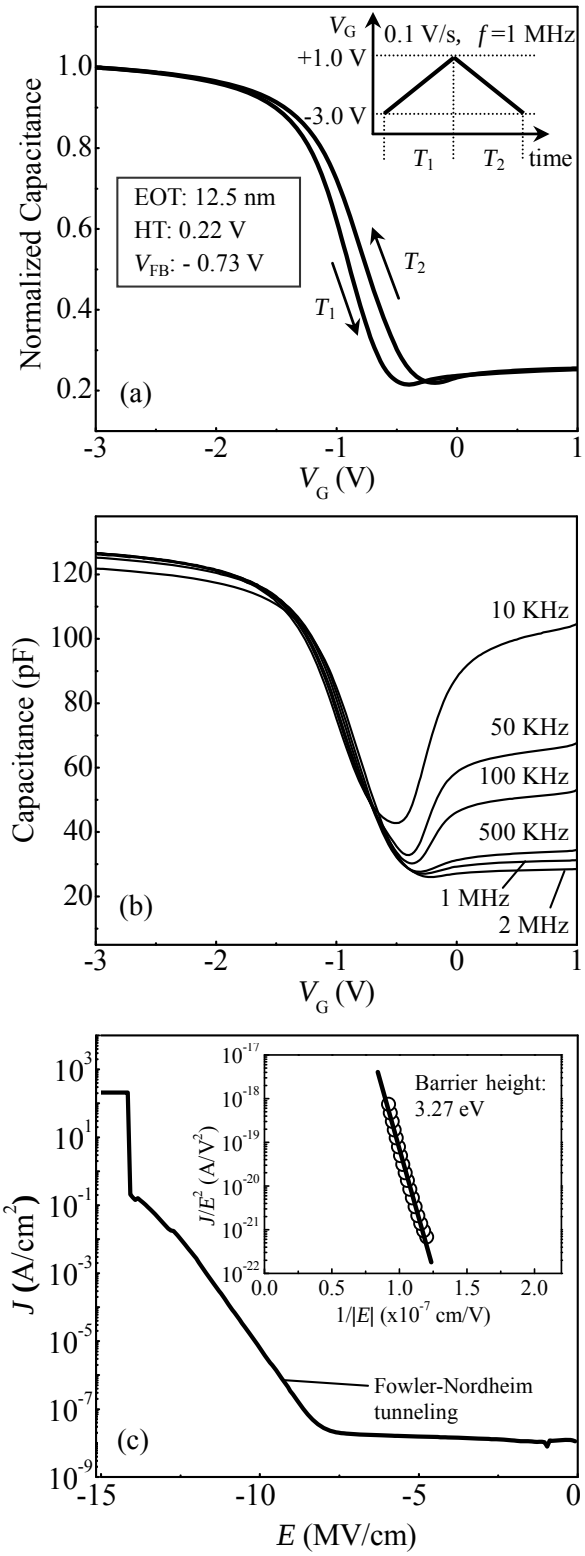

Figure 5. Kana Hirayama *et al*.

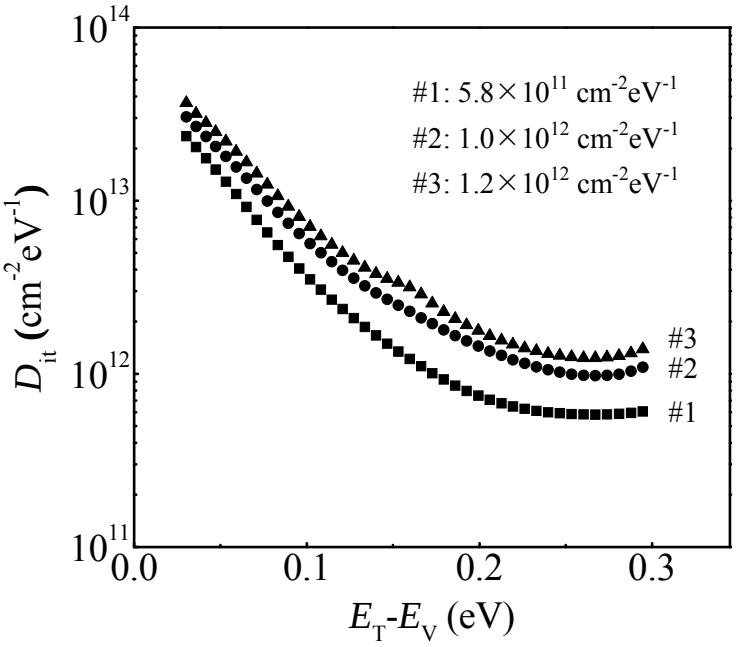

Figure 6. Kana Hirayama *et al*.

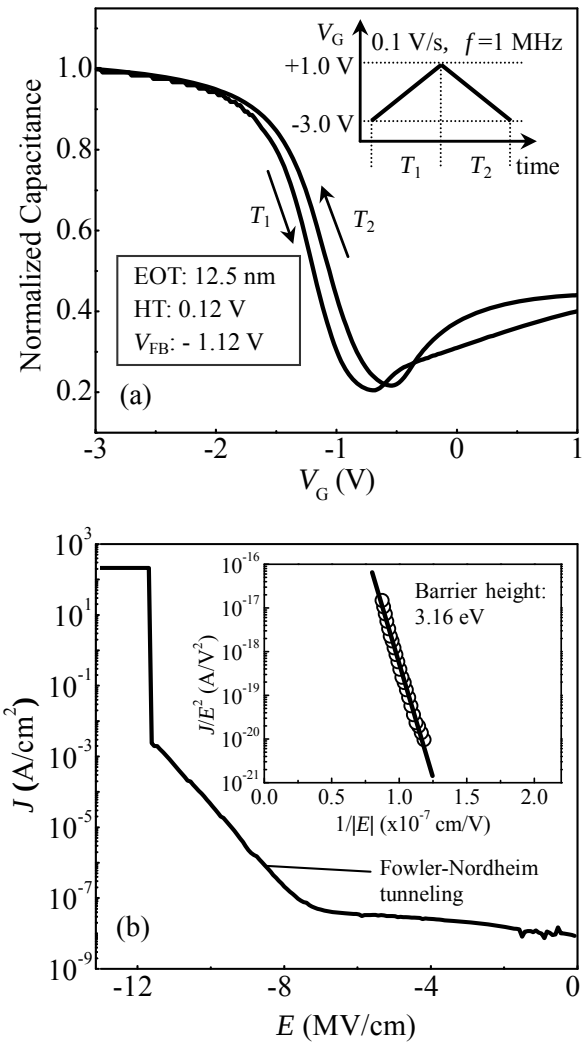

Figure 7. Kana Hirayama *et al*.

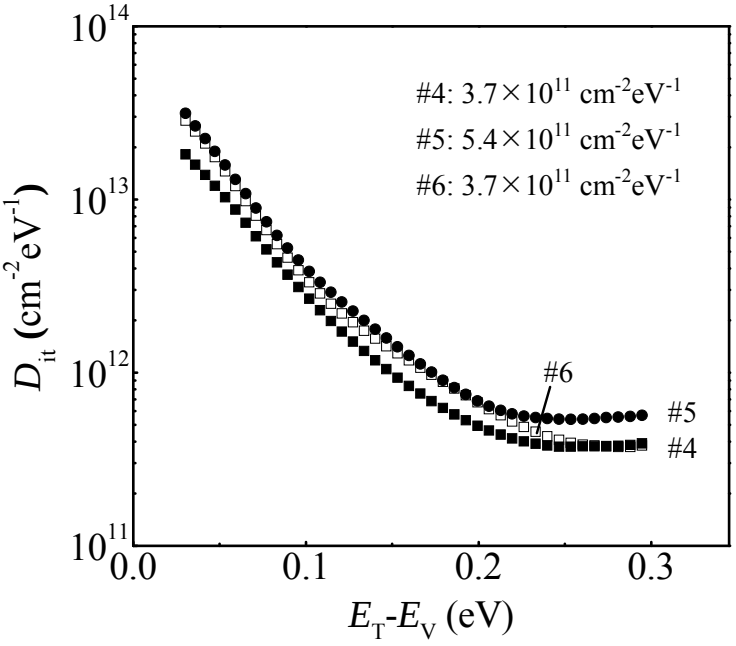

Figure 8. Kana Hirayama *et al*.

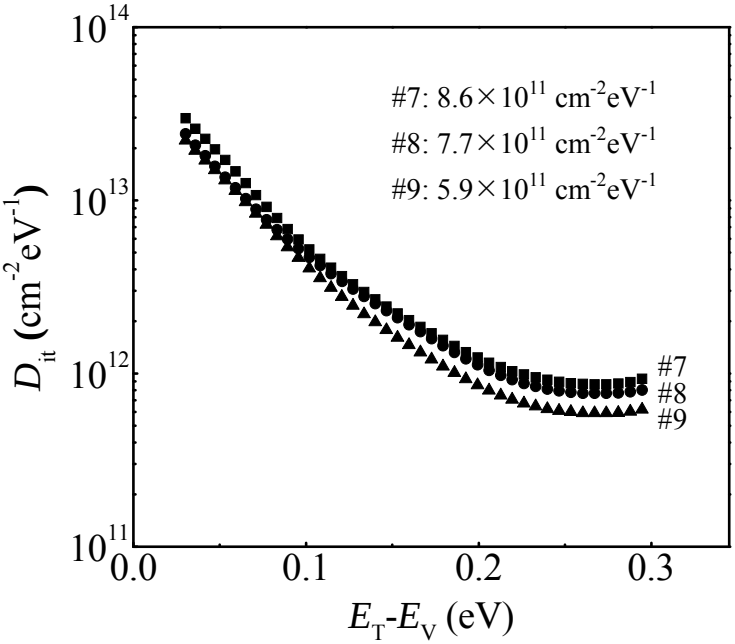

Figure 9. Kana Hirayama *et al*.