Effective passivation of defects in Ge-rich SiGe-on-insulator substrates by Al$_2$O$_3$ deposition and subsequent post-annealing

Yang, Haigui
Art, Science and Technology Center for Cooperative Research, Kyushu University

Iyota, Masatoshi
Interdisciplinary Graduate School of Engineering Sciences, Kyushu University

Ikeura, Shogo
Interdisciplinary Graduate School of Engineering Sciences, Kyushu University

Wang, Dong
Art, Science and Technology Center for Cooperative Research, Kyushu University

他

http://hdl.handle.net/2324/25510

出版情報：Solid-State Electronics. 60 (1), pp.128-133, 2011-06. Elsevier
バージョン：
権利関係：(C) 2011 Elsevier Ltd.
Effective passivation of defects in Ge-rich SiGe-on-insulator substrates by Al₂O₃ deposition and subsequent post-annealing

Haigui Yang¹, Masatoshi Iyota², Shogo Ikeura², Dong Wang¹, Hiroshi Nakashima¹ *

¹Art, Science and Technology Center for Cooperative Research, Kyushu University
6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

²Interdisciplinary Graduate School of Engineering Sciences, Kyushu University,
6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

Abstract

A method of Al₂O₃ deposition and subsequent post-deposition annealing (Al₂O₃-PDA) was proposed to passivate electrically active defects in Ge-rich SiGe-on-insulator (SGOI) substrates, which were fabricated using Ge condensation by dry oxidation. The effect of Al₂O₃-PDA on defect passivation was clarified by surface analysis and electrical evaluation. It was found that Al₂O₃-PDA could not only suppress the surface reaction during Al-PDA in our previous work [Yang et al., Thin Solid Films 2010; 518: 2342], but could also effectively passivate p-type defects generated during Ge condensation. The concentration in the range of 10¹⁶-10¹⁸ cm⁻³ for defect-induced acceptors and holes in Ge-rich SGOI drastically decreased after Al₂O₃-PDA. As a result of defect passivation, the electrical characteristics of both back-gate p-channel and n-channel metal-oxide-semiconductor field-effect transistors fabricated on Ge-rich SGOI were greatly improved after Al₂O₃-PDA.

Keywords: SiGe-on-insulator, Ge condensation, Al₂O₃-PDA, Defect passivation, Hole concentration, Acceptor concentration, MOSFET.

* Corresponding author. Tel.: +81 92 583 7872; fax: +81 92 573 8729.
E-mail address: nakasima@astec.kyushu-u.ac.jp (H. Nakashima).
1. Introduction

Since the scaling of conventional Si devices has confronted many physical problems and limitations, new device technologies such as gate stack engineering, source/drain (S/D) engineering, and mobility-enhanced channel engineering are emerging to overcome scaling issues and further boost the performance of complementary metal-oxide-semiconductor (CMOS) integrated circuits [1]. Especially, mobility enhancement is becoming more important because of the saturation trend of on-current in conventional Si channel. To realize mobility enhancement, one of the most convenient method is using high-mobility Ge-based materials and III-V alloys [2]. In particular, more attention is paid to Ge-rich SiGe-on-insulator (SGOI) or Ge-on-insulator (GOI) substrates because they combine the benefits of high hole mobility from Ge and low parasitic capacitance and leak current from the “on-insulator” structure. High Ge fraction (Ge%) of SGOI is of benefit to improve hole mobility in SGOI. Thus, it is important to fabricate a high quality SGOI substrate with high Ge% and low defect density.

Tezuka et al. have proposed a convenient method of Ge condensation by dry oxidation of SiGe layer on Si-on-insulator (SOI) substrate to fabricate Ge-rich SGOI or even GOI [3]. This method has shown its advantage that SGOI with a wide range of Ge% and a strain-adjusted SiGe layer could be fabricated. As a result, hole-mobility enhancement factor of approximately 10 has been successfully demonstrated in the condensed SGOI [4]. However, it is noticeable that structural defects such as stacking faults and microtwins were unintentionally induced in Ge-rich SGOI due to strain relaxation during high-temperature oxidation [5-7], and defect-free SGOI with Ge% higher than 82% can not be obtained regardless of the initial parameters [7]. Furthermore, these electrically active defects act as acceptors, which cause a hole concentration \(N_p\) and acceptor concentration \(N_A\) as high as \(10^{16}-10^{18}\) cm\(^{-3}\) in Ge-rich SGOI [8,9]. As a result, a p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) on Ge-rich SGOI exhibits a large off current \(I_{\text{off}}\) and is difficult to operate in full depletion (FD) mode [5,10]. nMOSFET on Ge-rich
SGOI exhibits a high threshold voltage ($V_T$) [8]. Efforts thus far with post-gas annealing, such as with H$_2$ and N$_2$, as well as optimization of the Ge condensation process, have had limited effects on passivation for these defects [6,10,11]. Therefore, it is still a big challenge to passivate these defects and improve the electrical properties of Ge-rich SGOI.

Recently, our group developed a method of Al deposition and subsequent post-deposition annealing (Al-PDA) [11]. With this method, Al diffused in the SiGe layer effectively passivated the electrically active defects and consequently reduced the $V_T$ of SGOI nMOSFET. In this case, secondary ion mass spectrometry (SIMS) revealed that Al was present in the SiGe layer at concentration of approximately $10^{18}$ cm$^{-3}$ after Al-PDA. However, a reaction layer due to the solid-state reaction between Al and SiGe was unintentionally formed on the SiGe surface. This could make it difficult to perform gate stack fabrication on SGOI.

In this work, we propose the use of an Al$_2$O$_3$ insulating film instead of an Al film. By using Al$_2$O$_3$ deposition and subsequent post-deposition annealing (Al$_2$O$_3$-PDA) method, we sought to suppress surface reaction-layer formation, passivate p-type defects, and improve the electrical properties of Ge-rich SGOI.

2. Experimental

To fabricate SGOI with a wide range of Ge% using Ge condensation by dry oxidation, two kinds of initial samples were used. The initial sample of 10 nm Si/74 nm Si$_{0.85}$Ge$_{0.15}$/140 nm buried oxide (BOX)/Si substrate was used to fabricate SGOI’s with Ge%≤50%, and 10 nm Si/80 nm Si$_{0.78}$Ge$_{0.22}$/140 nm BOX/Si substrate was used to fabricate SGOI’s with Ge%>50%. Considering the melting point of SiGe, we carried out Ge condensation in a 100% O$_2$ atmosphere at temperatures from 1200 to 1075 °C for Ge%≤50%, from 1075 to 950 °C for 50%<Ge%≤75%, and from 950 to 900 °C for Ge%>75%. To evaluate the electrical properties, we fabricated back-gate pMOSFET and nMOSFET structures on SGOI. Detailed fabrication processes were shown in Fig. 1. In the case of pMOSFET fabrication in Fig. 1a, after thermally grown SiO$_2$ was
removed, 20-nm-thick Al$_2$O$_3$ films were first deposited on SGOI by radio frequency (RF) magnetron sputtering using an Al$_2$O$_3$ target at an Ar flow rate of 30 sccm and an RF power of 60 W. The deposition rate was approximately 3 nm/min, which was measured by spectroscopic ellipsometry (SE) and transmission electron microscopy (TEM). PDA was then performed at temperatures of 500-800 °C for 30 min in N$_2$. After PDA, Al$_2$O$_3$ films were removed by buffered-HF solutions. Then Al films were deposited and patterned as S/D electrodes. After that, mesa etching and subsequent ohmic contact annealing were done. Finally an In-Ga alloy was rubbed onto back Si to form an ohmic contact. Compared with pMOSFET fabrication, the main difference of nMOSFET fabrication, as shown in Fig. 1b, is that n$^+$ S/D was first formed by solid-state diffusion (SSD) of phosphorus at temperatures of 900-1000 °C before Al$_2$O$_3$-PDA. The channel width/length of both pMOSFET and nMOSFET is 40/400 µm. Moreover, the structure and surface analyses were performed by using TEM, x-ray photoelectron spectroscopy (XPS) and optical microscope.

3. Results and discussion

3.1 The structure and surface analysis

Figure 2 shows cross-sectional image of SGOI with Ge\%=45\% after Al$_2$O$_3$-PDA at 700 °C. The Al$_2$O$_3$ layer and a flat interface at Al$_2$O$_3$/SiGe were clearly observed. The thickness of Al$_2$O$_3$ measured by TEM is approximately 20 nm, which is the same as the measured by SE.

Figure 3 shows surface images of SGOI with Ge\%=45\% before and after Al$_2$O$_3$-PDA at 700 °C, which were taken with an optical microscope. As a comparison, the surface image after Al-PDA at 400 °C is also shown. It is noted in Fig. 3 that both top Al and Al$_2$O$_3$ on the surface were removed after PDA. As clearly shown in Fig. 3b, a reaction layer due to the solid-state reaction between Al and SiGe was formed on the surface after Al-PDA. Similar phenomena were also observed for Al-PDA-treated SGOI with other Ge\%. Moreover, we found that these spot-like
patterns on the surface became larger with increasing Ge%. This indicates that the reaction is enhanced as Ge% increases. In contrast to the results with Al-PDA, no change in the surface morphology was observed after Al₂O₃-PDA based on a comparison of Fig. 3a and 3c. These results indicate that Al₂O₃, as an insulator, does not react with the SiGe layer even during high-temperature annealing, and therefore can effectively suppress the formation of a reaction-layer on the SGOI surface.

To further clarify the surface morphology, we carried out XPS measurements using an Al Kα line. Figure 4 shows the Al 2p spectra from the surface of four kinds of samples. After Al-PDA and subsequent top-Al removal, Al 2p peak at 74.2 eV was still detected, and it shifted to higher binding energy (BE) from the position (72.5 eV) of metal Al. This suggests that the solid-state reaction between Al and SiGe occurred during Al-PDA and caused the formation of surface-reaction layer. After Al₂O₃ deposition, the 2p peak at 74.9 eV from Al oxidation state was clear. However, no signal from Al 2p was detected after Al₂O₃-PDA and subsequent top-Al₂O₃ removal. It indicates that the solid-state reaction between Al and SiGe on the surface was completely suppressed by using Al₂O₃-PDA. These XPS results are well consistent with the observation in Fig. 3.

3.2 The effect of Al₂O₃-PDA on the reduction of Nᵣ in Ge-rich SGOI

To clarify the effect of Al₂O₃-PDA on defect passivation, we first evaluated Nᵣ by the Hall effect measurement. Figure 5 shows the dependence of Nᵣ on Ge% for SGOI’s with and without Al₂O₃-PDA treatment. Al₂O₃-PDA was performed at an optimal annealing temperature of 700 °C for Ge%<50%, 600 °C for 50%<Ge%<75%, and 500 °C for Ge%>75%. The optimal conditions were determined by the drain current (Iᵦ) versus back-gate voltage (Vᵦ) characteristics of MOSFET’s, which will be shown in the following sections. Clearly, defect-induced Nᵣ drastically increases from 10¹⁶ to 10¹⁸ cm⁻³ with an increase in Ge% for SGOI’s without Al₂O₃-PDA. For Ge%<50%, Al₂O₃-PDA reduces Nᵣ to a value lower than approximately 1×10¹⁶ cm⁻³ (the detection
limit of the Hall effect system for a very thin sample). When Ge%>50%, a drastic decrease in \(N_p\) of approximately one order of magnitude was obtained after Al\(_2\)O\(_3\)-PDA. While \(N_p\) is as high as \(5.0 \times 10^{18}\) cm\(^{-3}\) for as-fabricated SGOI with Ge%=90%, it decreased to \(5.5 \times 10^{17}\) cm\(^{-3}\) after Al\(_2\)O\(_3\)-PDA. Thus, Al\(_2\)O\(_3\)-PDA is a very effective method for the passivation of electrically active p-type defects in Ge-rich SGOI. The measured resistivity was correspondingly increased by approximately one order of magnitude after Al\(_2\)O\(_3\)-PDA treatment.

### 3.3 The effect of Al\(_2\)O\(_3\)-PDA on the electrical properties of SGOI pMOSFET

The effect of Al\(_2\)O\(_3\)-PDA on the electrical properties of SGOI pMOSFET was evaluated by using the structure in Fig. 1a. The \(I_D-V_G\) characteristics for SGOI’s with Ge%=25, 45, 65 and 90% are shown in Fig. 6, from which the flatband voltage (\(V_{FB}\)), on/off current (\(I_{on/off}\)) ratio, and FD voltage (\(V_{FD}\)) were extracted, and are summarized in Table 1. \(I_{on}\) and \(I_{off}\) are defined as the on-state drain current and off-state leakage current of pMOSFET, respectively. \(V_{FD}\) is defined as the gate-bias voltage at \(I_{off}\). Table 1 indicates that, while there is almost no difference in \(V_{FB}\), there are significant differences in both the \(I_{on/off}\) ratio and \(V_{FD}\) between Ge-rich SGOI’s with and without Al\(_2\)O\(_3\)-PDA.

When Ge%=25%, since \(N_p\) is lower than \(1 \times 10^{16}\) cm\(^{-3}\) regardless of whether Al\(_2\)O\(_3\)-PDA is treated or not (See Fig. 5), both pMOSFET’s with and without Al\(_2\)O\(_3\)-PDA exhibit a well-behaved \(I_D-V_G\) with a high \(I_{on/off}\) ratio and a low \(V_{FD}\). However, with an increase in Ge%, \(I_{off}\) drastically increases for as-fabricated SGOI’s. This phenomena have been observed by other group and our previous work [5,10]. When Ge% increases to 90%, the \(I_{on/off}\) ratio decreases to less than \(10^4\). We think that a high \(N_p\) shown in Fig. 5 is one of the main causes of the low \(I_{on/off}\) ratio besides the impact of band gap narrowing. Another disadvantage induced by a high \(N_p\) is the increasing in \(V_{FD}\). Therefore, the pMOSFET becomes more difficult to operate in FD mode with an increase in Ge%.

Based on a comparison of Ge-rich SGOI’s with and without Al\(_2\)O\(_3\)-PDA (Figs. 6b-6d), we found that Al\(_2\)O\(_3\)-PDA began to become effective when Ge%≥45%. With increasing Ge%, it
greatly improved the electrical properties of SGOI pMOSFET’s with Ge%=65 and 90%. One improvement is that the $I_{\text{off}}$ decreases by more than one order of magnitude and consequently the $I_{\text{on}}/I_{\text{off}}$ ratio is increased to approximately $10^5$, as shown in Table 1. Another is that pMOSFET can be easily operated in FD mode with a low $V_{FD}$ after Al$_2$O$_3$-PDA treatment. These improvements in electrical properties with Al$_2$O$_3$-PDA are consistent with the reduction in $N_p$ shown in Fig. 5.

We also studied the effect of Al$_2$O$_3$-PDA on carrier transport properties. Figure 7 shows the bottom-channel hole mobility for SGOI’s with and without Al$_2$O$_3$-PDA, which were obtained by using the $I_D$-$V_G$ characteristics of pMOSFET [5]. Although Al$_2$O$_3$-PDA can effectively improve the $I_{\text{on}}/I_{\text{off}}$ ratio by decreasing $I_{\text{off}}$, Fig. 7 shows that it has limited impact on the enhancement of extracted hole mobility. In the case of SGOI with Ge%=90%, a decrease in mobility was observed, although a high mobility value of around 400 cm$^2$/V$\cdot$s was expected. This may be attributed to the influence of a top surface without passivation because the SiGe layer is less than 20 nm thick [5,12].

### 3.4. The effect of Al$_2$O$_3$-PDA on the electrical properties of SGOI nMOSFET

The effect of Al$_2$O$_3$-PDA on the electrical properties of SGOI nMOSFET was also studied by using the structure in Fig. 1b. Figure 8 shows the $I_D$-$V_G$ characteristics for SGOI’s with Ge%=25, 45, and 65%, from which the $V_T$ and subthreshold swing ($S$) were determined, and are summarized in Table 2. Since the SiGe layer in S/D region will be evaporated during n$^+$ S/D fabrication using SSD at high temperature annealing when Ge% increases to 90%, we can not obtain the results of SGOI nMOSFET with Ge%=90%.

Obviously different from pMOSFETs, as-fabricated SGOI nMOSFETs exhibit a poor behavior with a high $V_T$ even though Ge% is low. The detailed study for this phenomena was done in our previous work [8]. According to this study, we have found $N_A$ was much higher than $N_p$ for low-Ge% SGOI due to the existence of deep acceptor level, which caused high $V_T$ for low-Ge% SGOI. With an increase in Ge%, $V_T$ drastically increases. By a comparison of SGOI’s with and
without Al$_2$O$_3$-PDA, we found that Al$_2$O$_3$-PDA treatment greatly improved nMOSFET characteristics. The $V_T$’s for all SGOI’s were significantly reduced after Al$_2$O$_3$-PDA. Here it is noted that the change of $I_D-V_G$ characteristics for nMOSFETs due to the Al$_2$O$_3$-PDA is obviously different from that for pMOSFETs in Fig. 6. This is because SGOI nMOSFETs operate under inversion mode while pMOSFETs operate under accumulation mode.

The interface-state density ($D_{it}$) of SiGe/BOX and $N_A$ were extracted from the obtained values of $V_T$ and $S$ in Table 2, and the results are shown in Figs. 9 and 10, respectively. The detailed extraction method has been described elsewhere [8,11]. Although Fig. 9 shows that Al$_2$O$_3$-PDA has limited effect on the reduction of $D_{it}$, it is clear from Fig. 10 that Al$_2$O$_3$-PDA significantly reduced high $N_A$. Furthermore, it becomes more effective with an increase in PDA temperature. The decrease in $N_A$ by approximately two orders of magnitude was achieved for all SGOI’s at the optimal temperatures. In particular when Ge$\%$=65$, N_A as high as 5×10$^{18}$ cm$^{-3}$ was reduced to 9×10$^{16}$ cm$^{-3}$ after Al$_2$O$_3$-PDA treatment. Therefore, the decrease in $N_A$ is responsible for the improved nMOSFET characteristics with low $V_T$.

In principle, Al$_2$O$_3$ has a thermodynamically stable structure. However, in this study Al$_2$O$_3$ films were prepared by RF magnetron sputtering using an Al$_2$O$_3$ target at an Ar flow. The structure of Al$_2$O$_3$ prepared by this method should be not perfect stable because we found that thin SiO$_2$ films was formed somewhere on SiGe surface after Al$_2$O$_3$-PDA by TEM observation. Similar phenomena have also been reported by other group [13]. Therefore, it is possible that Al was diffused in SiGe layer during high temperature annealing of Al$_2$O$_3$. But Al diffusion is difficult during Al$_2$O$_3$-PDA because of its stable structure, which is reflected in the fact that Al$_2$O$_3$-PDA requires a higher temperature than Al-PDA (400$^\circ$C) [11]. Compared with Al-PDA, Al$_2$O$_3$-PDA is somewhat less effective at reducing the $V_T$ and $S$ of nMOSFET, and consequently less effective at reducing $N_A$ and $D_{it}$. Based on this fact, the concentration of Al existed in the SiGe layer after Al$_2$O$_3$-PDA should be less than 10$^{18}$ cm$^{-3}$ after Al-PDA, which was measured by SIMS method.
The effect of Al$_2$O$_3$-PDA suggests that interstitial Al diffused in the SiGe layer exists as positive-charge state (Al$^+$) and therefore can effectively passivate negatively charged p-type defects.

4. Conclusion

We have demonstrated the effect of Al$_2$O$_3$-PDA on the passivation of electrically active defects for Ge-rich SGOI fabricated using Ge condensation by dry oxidation. The surface analysis by optical microscope and XPS indicated that Al$_2$O$_3$-PDA effectively suppressed the formation of a reaction-layer on the surface. From Hall-effect measurements, it was found that Al$_2$O$_3$-PDA reduced $N_p$ by approximately one order of magnitude in Ge-rich SGOI’s, which suggested that the electrically active p-type defects were effectively passivated. As a result of this decrease in $N_p$, Ge-rich SGOI pMOSFET exhibits a well-behaved characteristics with a high $I_{on/off}$ ratio and a low $V_{FD}$ after Al$_2$O$_3$-PDA. Our results also showed that Al$_2$O$_3$-PDA greatly reduced the $V_T$ of SGOI nMOSFET. The decrease in $N_A$ by approximately two orders of magnitude was achieved for all SGOI’s.

Acknowledgements

This study was supported in part by STARC, JSPS, a Grant-in-Aid for Science Research on Priority Areas (20035011) and a Science Research A (21246054) from The Ministry of Education, Culture, Sports, Science and Technology of Japan.

References


Table 1. $V_{FB}$, $I_{on/off}$ ratio, and $V_{FD}$ obtained from the $I_D$-$V_G$ characteristics of pMOSFET with and without Al₂O₃-PDA. The PDA’s were performed at temperatures of 700 °C for Ge% = 25 and 45%, 600 °C for Ge% = 65%, and 500 °C for Ge% = 90%, respectively.

<table>
<thead>
<tr>
<th>Ge%</th>
<th>$V_{FB}$ (V)</th>
<th>$I_{on/off}$ ratio</th>
<th>$V_{FD}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>w/o</td>
<td>w/</td>
<td>w/o</td>
</tr>
<tr>
<td>25%</td>
<td>-4.2</td>
<td>-3.9</td>
<td>7.3×10⁵</td>
</tr>
<tr>
<td>45%</td>
<td>-2.6</td>
<td>-3.0</td>
<td>3.1×10⁵</td>
</tr>
<tr>
<td>65%</td>
<td>-4.3</td>
<td>-4.3</td>
<td>5.1×10³</td>
</tr>
<tr>
<td>90%</td>
<td>-2.2</td>
<td>-2.6</td>
<td>3.3×10³</td>
</tr>
</tbody>
</table>

Table 2 $V_T$ and $S$ obtained from $I_D$-$V_G$ characteristics of nMOSFET with and without Al₂O₃-PDA (Units. $V_T$: V; $S$: V/decade).

<table>
<thead>
<tr>
<th>Ge%</th>
<th>25%</th>
<th>45%</th>
<th>65%</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_T$</td>
<td>$S$</td>
<td>$V_T$</td>
</tr>
<tr>
<td>w/o PDA</td>
<td>29.3</td>
<td>2.5</td>
<td>40.9</td>
</tr>
<tr>
<td>500 °C</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>600 °C</td>
<td>14.1</td>
<td>1.8</td>
<td>16.2</td>
</tr>
<tr>
<td>700 °C</td>
<td>8.6</td>
<td>1.2</td>
<td>11.2</td>
</tr>
<tr>
<td>800 °C</td>
<td>9.6</td>
<td>1.3</td>
<td>11.8</td>
</tr>
</tbody>
</table>
Figure captions

Fig. 1. The fabrication processes of back gate (a) pMOSFET and (b) nMOSFET, and the treatment with Al₂O₃-PDA.

Fig. 2. Cross-sectional TEM image of SGOI with Ge% =45% after Al₂O₃-PDA at 700 °C.

Fig. 3. The surface images of SGOI with Ge%=45% before (a) PDA, after (b) Al-PDA at 400 °C and (c) Al₂O₃-PDA at 700 °C.

Fig. 4. XPS spectra for SGOI with Ge%=45% after (a) Al deposition, (b) Al-PDA at 400 °C and the subsequent top-Al removal, (c) Al₂O₃ deposition, and (d) Al₂O₃-PDA at 700 °C and the subsequent top-Al₂O₃ removal.

Fig. 5. Dependence of $N_p$ on Ge% with (w/) and without (w/o) Al₂O₃-PDA. The PDA’s were performed at an optimal annealing temperature of 700 °C for Ge%<50%, 600 °C for 50%<Ge%<75%, and 500 °C for Ge%>75%, respectively.

Fig. 6. $I_D$-$V_G$ characteristics for SGOI pMOSFET of Ge%= (a) 25%, (b) 45%, (c) 65% and (d) 90% with and without Al₂O₃-PDA.

Fig. 7. Dependence of bottom-channel hole mobility on Ge% with and without Al₂O₃-PDA. The PDA’s were performed at temperatures of 700 °C for Ge%=25 and 45%, 600 °C for Ge%=65%, and 500 °C for Ge%=90%, respectively. The corresponding thickness of SiGe layer was also given.

Fig. 8. $I_D$-$V_G$ characteristics for SGOI nMOSFET of Ge%= (a) 25%, (b) 45%, and (c) 65% with and without Al₂O₃-PDA.

Fig. 9. Dependence of $D_{it}$ on Ge% for SGOI’s with and without Al₂O₃-PDA.

Fig. 10. Dependence of $N_A$ on Ge% for SGOI’s with and without Al₂O₃-PDA.
(a) pMOSFET

- Ge condensation
- Remove top SiO₂
- **Deposit 20 nm Al₂O₃**
- **Post annealing**
- Remove Al₂O₃
- Form Al contact
- Form isolation
- Contact annealing
- Rub In-Ga alloy

(b) nMOSFET

- Ge condensation
- **Fabricate n⁺ S/D**
- **Deposit 20 nm Al₂O₃**
- **Post annealing**
- Remove Al₂O₃
- Form Al contact
- Form isolation
- Contact annealing
- Rub In-Ga alloy

Figure 1
Figure 2
Figure 3

(a) Before PDA  
(b) After Al-PDA  
(c) After $\text{Al}_2\text{O}_3$-PDA
Figure 4
Figure 5
Figure 6
Figure 7

Hole mobility (cm$^2$/V s)

- w/o Al$_2$O$_3$-PDA
- w/ Al$_2$O$_3$-PDA

Ge%
Figure 8
Figure 9
Figure 10