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# Strained Single-Crystal GOI (Ge on Insulator) Arrays by Rapid-Melting Growth from Si (111) Micro-Seeds

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## Abstract

Liquid-phase epitaxial growth of Ge islands on insulator (GOI) using Ni-imprint-induced Si (111) micro-crystal seeds (~1 μmϕ) is proposed. As a result, single-crystalline GOI (111) structures with large area (~10 μmϕ) are realized. The transmission electron microscopy observations reveal no dislocation or stacking fault in the laterally grown regions. Moreover, the Raman measurements show that the tensile strain (~0.2 %) which enhances the carrier mobility is induced in the growth regions. This new method can be employed to realize the multi-functional SiGe large scale integrated circuits.

**Keywords**: Germanium (Ge), Ge on Insulator (GOI), Metal Induced Crystallization (MIC), Liquid-Phase Epitaxial Growth

## 1. Introduction

In order to break through the scaling limit of large scale integrated circuits (LSI), the materials innovation employing new functional materials is desired. Ge is an attractive channel material for high-speed transistors, as it provides much higher carrier mobility compared to Si [1,2]. In addition, high absorption coefficient in infrared region has a potential for application to photodetectors which are necessary for the optical fiber communication [3]. In addition, the band structure modulation into a direct-transition type structure has been reported in tensile-strained Ge [4], which favors the application of Ge to light emitting devices. In order to merge such advanced Ge-devices into LSI, arrays of strained single-crystal Ge with the area of device-size (>5 μm) should be achieved at controlled positions on $SiO_2$/Si structures. Many techniques, such as the oxidation-induced Ge condensation [5], laser annealing [6,7], solid-phase crystallization (SPC) [8,9] metal-induced lateral crystallization (MILC) [10], imprint [11] or indentation [12] induced SPC, and Al-induced crystallization [13], have been developed in recent ten years. However, some of them require very complex process, and others have difficulty in obtaining single-crystal Ge layers with smooth surfaces.

To solve these problems, the Si seeding rapid-melting-growth [14-17] of Ge was proposed. Here, a-Ge layers deposited on $SiO_2$ films were first grown vertically from Si substrates through opening window formed in $SiO_2$ films, and then propagated laterally over $SiO_2$. These efforts achieved defect-free

single-crystal Ge wires (20-40 μm length, 2-3 μm width) on insulating films. To expand the application field of this method, we have examined details of this process, and clarified that the driving force to cause the lateral growth of Ge was not the thermal flow from the molten-Ge to Si substrates through seeding windows, but the spatial gradient of the solidification temperature originating from Si-Ge mixing at seeding areas [18,19].

Based on these findings, we propose a new technique to obtain single-crystal Ge island arrays on insulators, where Ni-imprint-induced Si (111) fine-crystals (~1 μmϕ) are used as growth-seeds for rapid-melting-growth of a-Ge [20]. In this paper, details of this Si-substrate-free process and characteristics of the grown regions are investigated. Defect-free single-crystal Ge island arrays with device-sizes and smooth surfaces are demonstrated at controlled positions on $SiO_2$/Si substrates.

## 2. Experimental procedures

The process flow is schematically shown in Fig. 1. Amorphous Si (a-Si) films (thickness: 100 nm) were deposited on thermally grown $SiO_2$ layers (thickness: 50-160 nm) on Si substrates by the molecular beam technique (base pressure: $5x10^{-10}$ Torr). Ni metals were imprinted on the a-Si films by pressing a tip-array substrate covered with a Ni film (thickness: 3 nm). After removing the tip array, the a-Si films on $SiO_2$ were annealed at 590$^{o}$C (5h) in $N_2$ to grow the imprint-induced small Si crystals (diameter: ~1 μm) with the

(111) orientation, as shown in the insertion of the electron backscattering diffraction (EBSD) image of the grown Si crystals. The EBSD image indicates that the Si crystals were oriented to the (111) direction. The details of the Ni-imprint technique are described in Ref. [21]. Then, amorphous regions of the Si films were removed by wet etching in order to form the Si-seeds for Ge-LPE. Subsequently, circular a-Ge islands (diameter: 15 μm, thickness: 100 nm), covering the small Si (111) crystals, were formed by molecular beam deposition and wet etching. Then, the samples were capped with $SiO_2$ films (thickness: 0-2000 nm) by RF magnetron sputtering, and heat-treated by rapid thermal annealing (RTA) at 1000 $^{o}$C (1 sec) to induce LPE from the Si-seeds.

Morphology, crystal orientation, and crystal quality of the grown layers were characterized by Nomarski optical microscopy, EBSD, energy dispersive X-ray spectroscopy, micro-probe Raman spectroscopy, and cross-sectional transmission electron microscopy (X-TEM).

**3. Results and Discussion**

We investigated the growth morphology of Ge as a function of the capping-$SiO_2$ thickness. Here, the thickness of the bottom-$SiO_2$ layers was kept constant (50 nm). When the cap-$SiO_2$ thickness is 100 nm, Ge islands are dispersed due to local evaporation of Ge from $SiO_2$ cracks. In the case of 800 nm, cap-$SiO_2$ layers on Ge islands are pushed away by Ge, and Ge islands disappear. On the other hand, in the case of the thickness of 2000 nm, cap-$SiO_2$ is so strong that Ge evaporation is suppressed as shown Fig. 2(a),

and Ge islands are agglomerated as shown Figs. 2(b) and 2(c).

We evaluated the yield of residual Ge islands as a function of the capping-$SiO_2$ thickness and bottom-$SiO_2$ thickness, where the yield is defined as the fraction of the Ge islands remaining with circular shapes after RTA. Results are summarized in Fig. 2(d). The yield increases with increasing capping-$SiO_2$ thickness, though it does not depend on the bottom-$SiO_2$ thickness. These results indicate that capping by thick $SiO_2$ layers is very effective to prevent Ge agglomeration and/or breaking. Consequently, high (~ 90 %) yields are obtained for the samples with thick capping-$SiO_2$ (2000 nm) layers.

The crystal orientations of the Ge islands with thick capping-$SiO_2$ (2000 nm) were evaluated by EBSD measurements. The results for the samples with the thin (50 nm) bottom-$SiO_2$ layer and the thick (160 nm) bottom-$SiO_2$ layer are shown in Figs. 3(a) and 3(b), respectively. Ge islands with the (111) orientation, identical to Si-seeds, are obtained for the sample with the thin (50 nm) bottom-$SiO_2$ layer, as shown in Fig. 3(a). This indicates that Ni-imprint induced Si-crystals act as crystal-seeds during melt-back growth of Ge. A few grain boundaries observed in the EBSD image of Fig. 3(a) were identified to be Σ3 coincidence-site-lattice boundaries. Matsuki *et al.* [22] reported that Σ3 grain boundaries scarcely degrade the carrier transport properties. In this way, (111) oriented high-quality Ge islands with device-size diameter (~10 μmϕ) are achieved on $SiO_2$/Si substrates.

By contrast, polycrystalline Ge (poly-Ge) islands are obtained for the

sample with the thick (160 nm) bottom-$SiO_2$ layer, as shown in Fig. 3(b). The observed poly-crystallization of Ge islands can be explained on the basis of the cooling rate. The growth velocity of the molten Ge should become lower with decreasing cooling rate, as Fujiwara *et al.* [23] reported for the melt-growth of Si. Thus, the cooling rate of the molten Ge must be high enough to complete the epitaxial growth before spontaneous nucleation. In this experiment, the cooling rates should depend on the thickness of cap-$SiO_2$ and bottom-$SiO_2$ layers because of the low thermal conductivity of the $SiO_2$ films (~0.02 W/mK) [24]. In this way, molten Ge islands with thick bottom-$SiO_2$ layers are considered to be poly-crystallized. For the sample with thin (800 nm) cap-$SiO_2$, single-crystalline Ge island is obtained, as shown in Fig. 3(c). This result supports our speculation that decreasing cooling rate by thickening $SiO_2$ layers causes the poly-crystallization. However, further study is needed to clarify this.

We examined the detailed characteristics of grown Ge islands by X-TEM observations. The TEM image of the single-crystalline Ge island, shown in Fig. 3(a), are shown in Fig. 4(a). The Si-seed is missing in Fig. 4(a), which is probably due to removal during the sampling process for the TEM observation. The surface morphology of the Ge island is very flat as revealed from Fig. 4(a), which indicates the thick capping-$SiO_2$ layer well prevents the agglomeration of Ge islands during RTA process. The magnified TEM image in Fig. 4(b) indicates no dislocation or stacking fault in the laterally grown region. These defect-necking results well agree with those for the previously

reported rapid-melting-growth of Ge, where Si substrates were used as growth seeds [14,15,18]. In addition, the electron diffraction pattern, as shown Fig. 4(c), confirms the (111) orientation of the Ge island.

To evaluate Si diffusion and crystal-quality of grown Ge islands, micro-probe (spot diameter: ~1 μm) Raman spectroscopy measurements were performed for the sample shown in Fig. 3(a). Raman spectra obtained from the seeding point (A) and the laterally grown region (B), as indicated in Fig. 4(a), of the single-crystal Ge island are shown in Fig. 4(d). In the figure, the spectra of single-crystal Ge (c-Ge) wafer are also shown for comparison. Large peaks are observed at about 300 $cm^{-1}$ in all spectra, which originate from the Ge-Ge bonding. On the other hand, a small peak is observed at 380.9 $cm^{-1}$ at the Si-seeding point (A), which originates from the Si-Ge bonding. Such Si-Ge peak is not observed at the region (B). These results clearly indicate that the Si diffusion originating from Si-Ge mixing at seeding point is limited only in the vicinity of Si-seed (<1 μm). The full width at half maximum (FWHM) of the Ge-Ge peak obtained from laterally grown region (B) is 3.3 $cm^{-1}$, which is very close to that (3.1 $cm^{-1}$) of the c-Ge wafer and much smaller than those (5.0-8.3 $cm^{-1}$) reported in the previous works, which were obtained by using laser annealing [7], SPC [9], and MILC [10] methods. These results indicate the advantage of rapid-melting-growth to achieve high-quality single-crystal Ge islands on insulators.

Moreover, low energy shift of Ge-Ge peak positions by RTA processing is found from the Raman spectra. Here, positions of Raman spectra shown in

the region (A) and region (B) shift about 0.8 $cm^{-1}$ from the Ge-Ge peak of the non-strained c-Ge wafer. This indicates a generation of tensile strains of about 0.2% in grown-Ge islands. We speculate that these tensile strains are caused by the difference in the thermal expansion coefficients between Ge and Si-substrate. Previously, we examined laser annealing [25] of Si on insulator (SOI) structures and achieved strained SOI structures with a tensile strain as large as 0.6% by tuning the sample structures. These results indicate generation of more strong tensile strains will be possible by using melt-back growth. This favors the possible enhancement of carrier mobility [26] and formation of the direct-transition band structure.[4] In order to increase the strain field, the strain-generation mechanism is now under investigation by changing cooling rates after RTA.

**4. Conclusion**

We have developed the rapid-melting-growth method of a-Ge combined with seed-positioning technique, where Ni-imprint-induced Si (111) fine-crystals (~1 μmϕ) are used as the growth seeds. It was found that thick cap-$SiO_2$ suppresses the Ge evaporations. Moreover, it was speculated that control of the cooling rate of the molten-Ge islands by optimizing bottom-$SiO_2$ thickness was very important to achieve single-crystal Ge island arrays on insulating films. As a result, single-crystal Ge island-arrays with device-size (~10 μmϕ) have been achieved on $SiO_2$/Si structures. The TEM observations revealed no dislocation or stacking fault in the grown regions.

This method opens up the possibility of multi-functional SiGe-LSI, where advanced Ge-devices, i.e., high speed transistors and optical devices, are stacked on Si-LSI.

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**Figure captions**

Fig. 1 Process flow of experiment. Si (111) seeds (diameter: ~1 mm) were grown by Ni-imprint-induced SPC (590 $^{o}$C, 5 h), as confirmed by EBSD observation. Subsequently, lateral liquid-phase epitaxial growth of Ge was induced from Si seeds by RTA (1000 $^{o}$C, 1 sec).

Fig. 2 Nomarski optical micrographs of Ge island arrays (a), and SEM image (b) and EDX mapping (c) of a Ge island for the annealed sample with the cap-$SiO_2$ thickness of 2000 nm. The yield of residual Ge islands keeping circular shapes as a function of cap-$SiO_2$ thickness, where the bottom-$SiO_2$ with different thickness (50, 160 nm) was used (d).

Fig. 3 EBSD images for the Ge islands with bottom-$SiO_2$ thickness of 50 nm (a) and 160 nm (b), where the cap-$SiO_2$ with the identical thickness (2000 nm) was used. For comparison, EBSD image for the Ge island with thin cap-$SiO_2$ (800 nm) and thick cap-$SiO_2$ (160 nm) is shown (c).

Fig. 4 X-TEM image for the sample (a), shown in Fig. 3(a), together with magnified image (b), and the electron diffraction pattern of the Ge island (c). Raman spectra obtained from the seeding point (A) and laterally grown region (B) of the single-crystal Ge island shown in Fig. 4(a) and a single-crystal Ge wafer (d). The values of the peak positions due to Ge-Ge bonding and tensile strains in the point (A) and (B) are summarized in the inserted table.

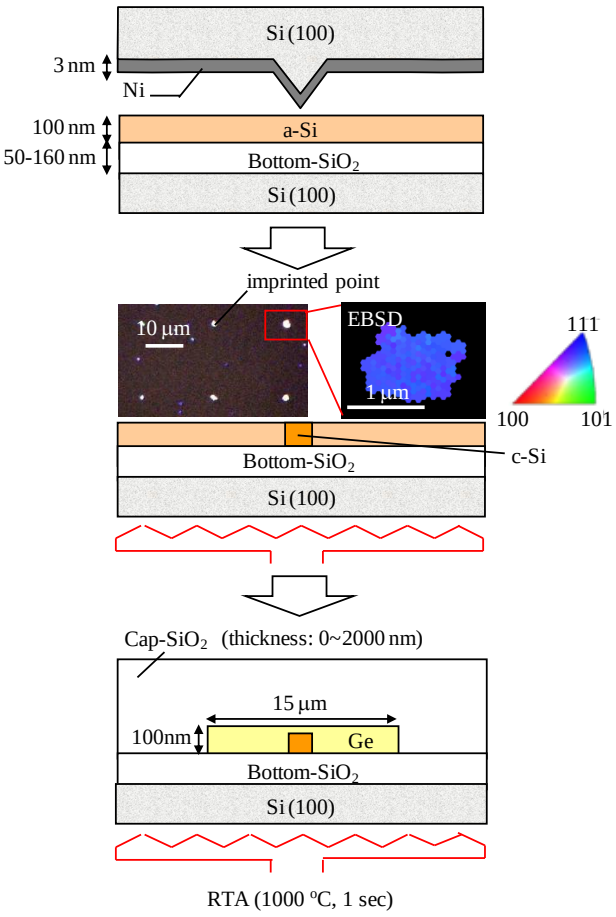



Fig. 1 T. Sakane

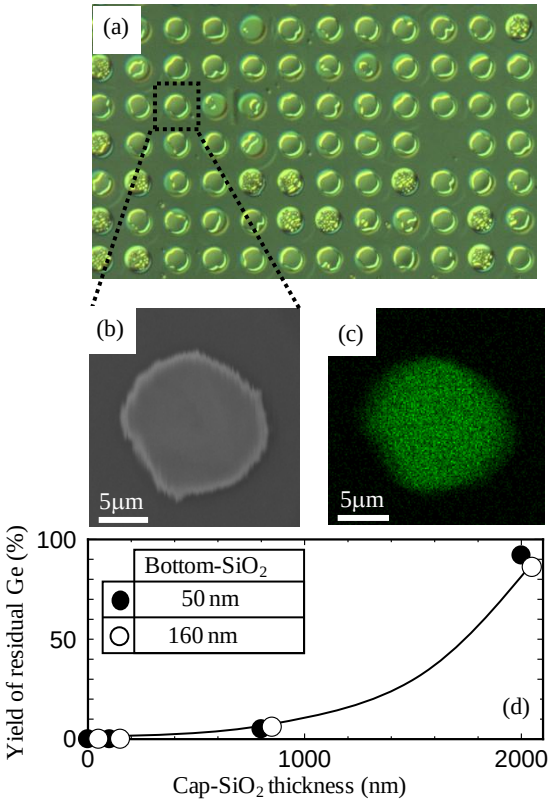



Fig. 2 T. Sakane

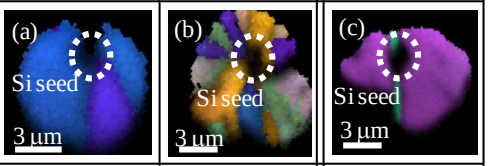
| | | | |
|---|---|---|---|
| Cap-$SiO_2$ | 2000 nm | | 800 nm |
| Bottom-$SiO_2$ | 50 nm | 160 nm | 160 nm |
| EBSD |     | | |
| Yield | ~ 90 % | | ~ 10 % |

Fig. 3 T. Sakane

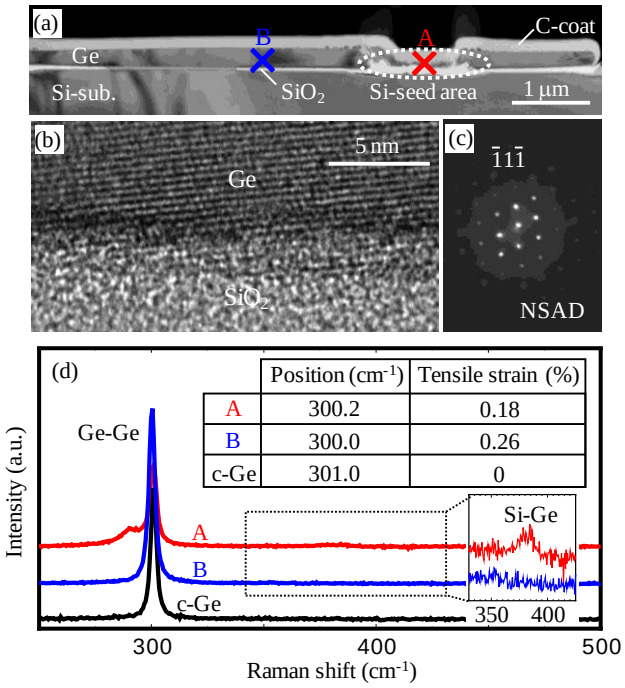



Fig. 4 T. Sakane