Fundamental Research on Waveguide Fabrication for Future Photonic Circuits

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Abstract

The reliance and demand for ever increasing data in the current information age in the field of information and technology (ICT) is ever increasing. With new development and proliferation of connected devices and services such as the internet of things and high definition content, the global internet traffic is expected to surpass 3.2 zettabyte per year in 2021. This extraordinary increase in data consumption however increase the energy footprint of ICT and it is expected to consume 10% of electricity generated worldwide while at the same time contributing to an increase of 5% of direct global CO_2 emissions. This puts a severe strain on the energy and power requirements of ICT devices and systems. Rather than the actual computation of data, more than half of the energy consumed is due to interconnects that transfer data and information from one location to another. Therefore, one of the main research topics to improve energy efficiency is by integrating new logic and device architectures and applying novel integration schemes. Towards this aim, one of the main research topics undertaken and is presented in this thesis is a photonic integrated circuit. Photonic integrated circuit combines the high speed benefits of monolithic integration of photonic devices along with high data processing of electronic devices to realize higher bandwidth, lower footprint, lower power consumption and higher power efficiency to meet the ICT demands.

In this thesis, the research background and the purpose are explained in chapter 1. The photonic integrated circuit is explained along with components and materials to realize the photonic integrated circuit. Two different but interrelated topics for photonic integrated circuits are discussed. The first is a monolithically integrated light source where the novelty of Ge as a material for monolithic integration of light source is discussed. For the second topic, interfacing from the photonic integrated circuit to space division multiplexing techniques through a multi-core fibre is discussed. Furthermore, fabrication issues of both of these topics for photonic integrated circuits and novel fabrication techniques in order to realize these two topics are also explained as the research published in this thesis.

In chapter 2, the structure and design consideration for Ge waveguides are elaborated. The electric field profile and optical field confinement for Ge-on-Si and Ge-on-insulator are calculated and simulated through BPM. The design considerations are then applied to the fabrication of Ge waveguides. A novel fabrication technique for accurate dry etching of Ge is then developed by using a CHF_3 based inductively coupled plasma to achieve a near vertical sidewall with relatively high selectivity with a polymeric photoresist. The accurate dry etching and near vertical sidewall achieved enables precise fabrication of Ge waveguides and can improve the performance of Ge lasers and other devices.

In chapter 3, the issues, mechanism and fabrication method to realize multi-layer stacking of sol-gel SiO_2 for optical waveguide cladding and passivation layers was discussed. A new annealing and O_2 plasma fabrication process was developed to eliminate the issues of cracks and peeling. The surface resistivity and refractive index were measured to characterize the sol-gel SiO_2 layer. Furthermore, different core layer materials stacked on top of the sol-gel SiO_2 were also explored to confirm the sol-gel SiO_2's capability for optical confinement. The results demonstrates that multi-layer stacking scheme of sol-gel SiO_2 layers is suitable to realize cladding and passivation layers for optical waveguides with different core materials on an Si substrate.

In chapter 4, the above results are summarized and the outlook and future view of the novel fabrication technology for implementation in photonic integrated circuits are clarified.

Chapter 1: Introduction

1. 1. Background

In the current information age, the reliance and demand of society on the field of information and communications technologies (ICT) is ever increasing. The demand for data traffic is expected to grow by ~300% from 2016 – 2021 [1] as shown in Fig. 1.1 and this is fuelled by demand for high definition content and growth in the proliferation of the Internet of Things (IoT) devices. With this sustained demand, global internet traffic is set to surpass 3.3 zettabyte (2^{70} bytes) by 2021 [2]. This demand increases the energy footprint of ICT and it is expected to consume 10% of electricity generated worldwide while additionally contributing to an increase of 5% of direct global CO_2 emission, and this puts a severe strain on the energy and power requirements for both devices and systems [3]. Rather than the actual computation of data, more than half of the energy consumed is due to interconnects that transfer data and information from one location to another. Therefore, one of the main topics where research activity is focused on is to improve energy efficiency is by integrating new logic and device architectures and applying novel system integration schemes [4]. One of the main integration schemes proposed is a photonic integrated circuit [5].

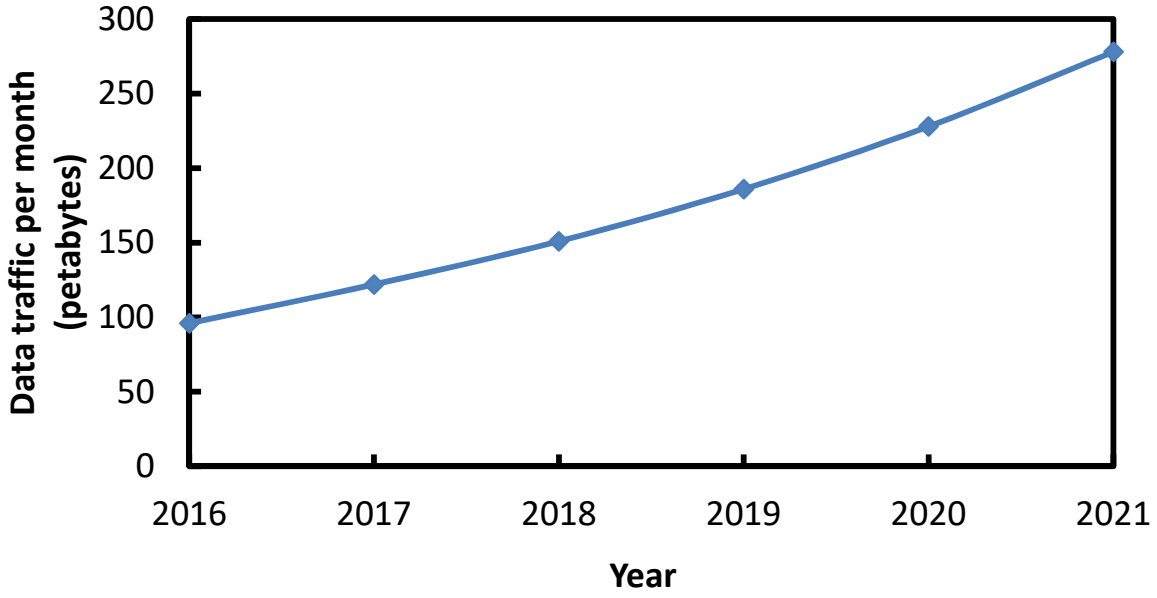


Fig. 1.1: Estimated worldwide monthly consumer data in petabytes from 2016 to 2021 [1].

Research towards electronic-photonic integrated circuits and photonic integrated circuits on silicon (Si) thus are becoming an increasingly appealing solution towards addressing this issue [6],[7]. They combine the benefits of the high speed and bandwidth of photonics with the benefits of high-speed data processing of electronics in a single monolithic device [8]. It is unsurprising then that the monolithic integration of photonic integrated circuits poses the greatest technical challenge and at the same time provides the biggest opportunity for higher bandwidth, lower size footprint, lower power consumption and higher power efficiency to meet the demands of ever increasing data traffic in this communication age [9].

1. 2. Photonic integrated circuits

Photonic integrated circuit is a device that integrates two or more photonic functions similar as to the now ubiquitous electronic integrated circuit which are mainly based on Si. The main difference is that rather than the movement of data and information through the flow of electrons as in the electronic integrated circuit, the photonic integrated circuit provides the movement of data through optical light or wavelengths [10]. Fig. 1.2 below is an example of a photonic integrated circuit. The photonic integrated circuit consists of a laser as a light source, a modulator to encode electrical data onto the light source, waveguides and coupling device to couple the light to a multi-core fibre, a multi-core fibre to transport data to and fro from the external world and a photodetector to re-convert optical data to back to electrical data as illustrated.

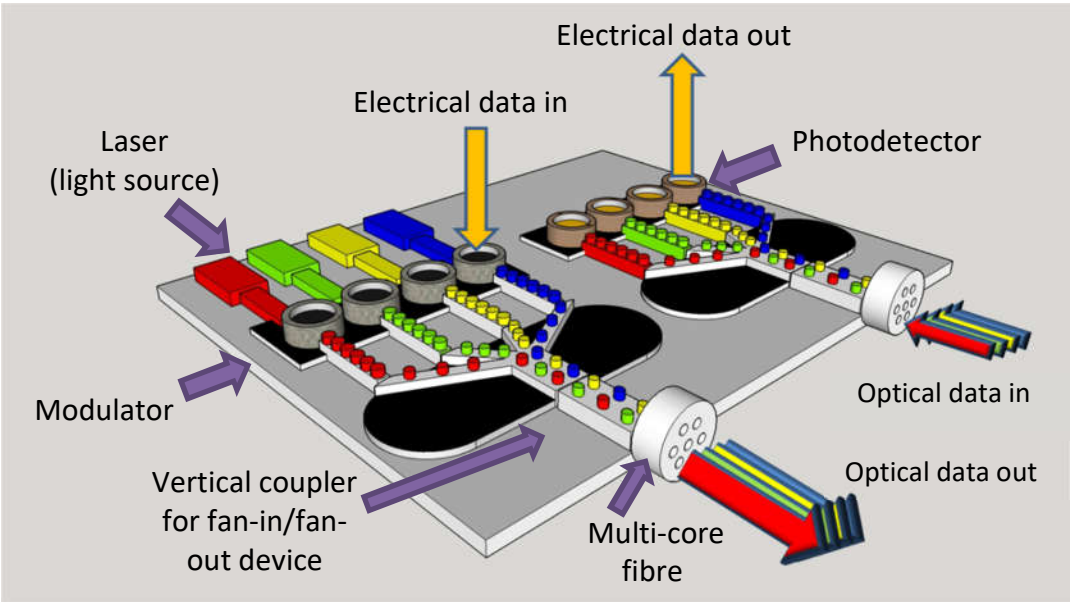


Fig. 1.2: An example of a photonic integrated circuit.

One key aspect of this example of a photonic integrated circuit is that the optical light is generated by an on-chip laser or light source. The modulator converts and encodes electrical data onto the optical light and a coupler is then used to interface between the modulator and the multi-core fibre. The multi-core fibre here is used to transport encoded data from the photonic integrated circuit to the external world and back from the external world to the photonic integrated circuit. Similarly, the photodetector converts the optical light back to an electrical data. It should be noted that an ideal photonic integrated circuit should monolithically integrate all of these photonic components within a signal device.

The development of semiconductor lasers [11], the semiconductor alloy laser [12] and the growth and fabrication of compound semiconductor alloys [13] has led the groundwork for the possibility of extending electronic integrated circuit concepts into the realm of photonics.

Several examples of photonic integration are:

1. Monolithic integrated optical wavelength demultiplexer [14]
2. Monolithic integrated transmitter circuits (lasers) [15]
3. Monolithic integrated repeater chip [16]
4. Hybrid integrated bistable optical device [17]
5. Integrated distributed feedback (DFB) laser and modulator [18]
6. Integrated tuneable receiver [19]
7. Integrated balance heterodyne receiver [20]

The advantages and merits of a photonic integrated circuit are listed below:

1. Increased bandwidth
2. Expanded frequency or wavelength division multiplexing
3. Low-loss couplers
4. Expanded multi-node switching – increase in number of switching nodes and switching speed
5. Smaller size and weight
6. Reduced power consumption
7. Batch fabrication economy
8. Improved reliability
9. Improved optical alignment and immunity to vibration
10. Reduced footprint of photonic circuits
11. Increased density
12. Reduced packaging costs

Meanwhile, the disadvantages of photonic integrated circuits are:

1. The high cost of developing new materials
2. The high cost of developing new fabrication technology
3. The need to leverage the existing fabrication technology available for CMOS fabrication

In terms of materials and processing for developing the monolithic photonic integrated circuit, the case for Si as the dominant material platform is based upon the well-developed infrastructure of the microelectronics industry and

the compatibility of the fabrication process for integration of both photonic and electronic functions [21].

Si and its corresponding dielectrics, silicon dioxide (SiO_2) are a great material system for use in optical confinement and wave transmission in the near infrared range such as the 1.3 – 1.55 µm range used in the optical telecommunication industry [22] as shown in Fig. 1.3 below where the white areas represent optical transparency and the dark areas represent high loss. Si not a good choice for active photonic devices due to its transparency in such wavelength ranges and indirect bandgap which makes it unsuitable for light emitting devices [23]. Despite this, the development of Si laser has been demonstrated [24], however the need for optical pumping negates the capability for integration in photonic integrated circuits. Germanium (Ge) is a material that has been identified as a unifying material for the photonic integrated circuit [25]. Ge is also transparent within the optical telecommunication range and although it is also an indirect bandgap material, band engineering of Ge enables it to be suitable as active photonic devices. The suitability of Ge is further discussed in section 1.4.

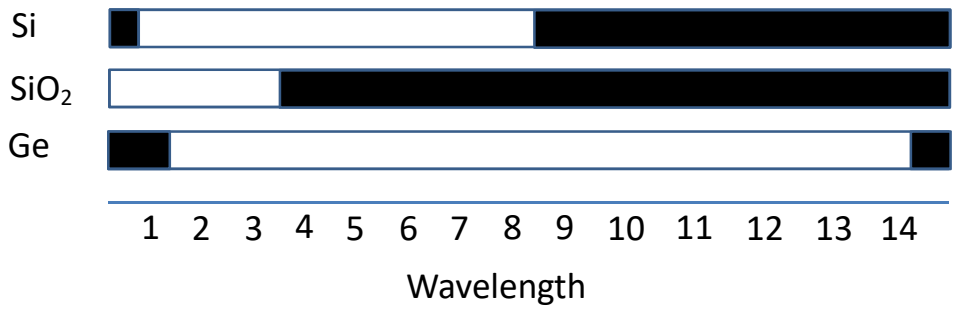


Fig. 1.3: Wavelength range over which waveguide propagation loss is <2dB/cm for Si, SiO_2 and Ge. [22].

1. 3. Components of photonic integrated circuits

The crucial building blocks of a photonic integrated circuit consists or both active and passive devices. Active devices are high performance photodetectors, modulators and an efficient light source. Passive devices are waveguides, array waveguide gratings and couplers.

Monolithic integration of photodetector and modulators have been demonstrated [26][27]. Recent advances showcase significant compatibility and performance optimization to realize low dark current, high responsivity and speed with CMOS compatible fabrication processes.

The main component that is lacking then for a photonic integrated circuit is an efficient light source. Two schemes have been proposed for integrating light source with photonic integrated circuit, the first is an off-chip light source and the second is an on-chip monolithically integrated light source [28].

The advantages and disadvantages of monolithically integrated vs an off-chip light source for optical interconnections has been analysed and discussed [29]. An off-chip light source display high light emission, high efficiency and good temperature stability. On the other hand, an off-chip light source suffers from a relatively large coupling loss between the off-chip light source and other photonic devices. The off-chip light source also incurs a more complex and higher cost for packaging. Therefore, an on-chip light source is an important component to realize photonic integrated circuits. An on-chip

light source could achieve a higher integration density with a smaller footprint [30]. It could also achieve better performance in terms of energy efficiency. Despite these advantages, the development of an on-chip light source has lagged behind that of other photonic components such as photodetector [31], modulator [32] and passive devices [33].

In order to fully utilize the current microelectronic and optical communication technologies, the ideal on-chip light source should satisfy the following requirement:

1. The light needs to be emitted at around 1550 nm to be able to connect to the existing fibre optic network.
2. It must lase under electrical pumping to integrate with other components.
3. It should exhibit a high output power and efficiency for a low energy cost-per-bit data transmission.
4. It should be able to integrate with Si CMOS fabrication techniques for large-scale manufacturing.

Therefore, based on these requirements, the most suitable candidates to enable on-chip light source are (1) III-V laser on Si, and (2) Ge laser. The differences and characteristics of III-V based laser vs Ge based laser is described in the Table 1.1. An overview of Ge photonics in particular its suitability for monolithic photonic integration is described in section 1.3.

Table 1.1: Differences and characteristics of Ge based laser vs III-V based laser

	Ge based laser	III-V based laser
Working mechanism	Enhance emitting efficiency via bandgap engineering	III-V materials as gain medium
Gain material	Ge	InGasAsP quantum well InAs/GaAs quantum dots
Advantages	Large gain spectrum Material and process compatibility with Si technology	High gain and output optical power Good structure design & flexibility
Challenges	Ge materials quality, Ultrahigh threshold current	Fabrication compatibility and cost reduction

In this work, we focus on the accurate fabrication of Ge to enable an on-chip light source and other photonic devices for future photonic integrated circuit.

Similarly, there also exists a need to transmit the data from the photonic integrated circuit to the external world and this can be best done by leveraging the existing fibre optics network [34]. Recent research and development has been directed towards the use of multi-core fibres (MCF) to achieve higher data capacity [35]. There exists then a need to interface between the photonic integrated circuit and the fibre optics network. In this work, we also focus on a novel fabrication technique by using an all sol-gel fabrication technique to enable the interface between a photonic integrated circuit and the fibre optics network though vertical coupling as will be elaborated in section 1.5.

1. 4. Germanium photonics: State of the art

Ge is a group IV semiconductor that has in recent years been highly researched and developed for monolithic integration with CMOS Si based electronic and photonic systems [36]. Ge can be found as a material used in the semiconductor industry in transistors [37], fibre optic systems [38], as well as various other electronic devices. Ge has a historical importance in that the first decade of semiconductor electronics was based entirely on Ge [39]. However, with the abundance of Si and the availability of an easily processed insulating dielectric oxide - SiO_2 along with Si's ability to work at higher temperatures and smaller reverse leakage current compared to Ge, soon made Si the material of choice for the semiconductor industry [40]. A comparison of some of the properties of Ge versus Si is as described in Table 1.2 Even though Ge and Si both belong to the same group IV in the periodic table, several key differences has a large effect on the fabrication of Ge.

Table 1.2: Properties of Ge and Si

	Ge	Si
Crystal structure	Faced centre diamond cubic	Faced centre diamond cubic
Refractive index @ 1550 nm	4.28	3.41
Bandgap (eV) at 300K	0.67	1.11
Lattice constant (Å)	5.64613	5.43095
Thermal expansion coefficient ($°C^{-1}$)	5.8×10^{-6}	2.6×10^{-6}
Melting point (°C)	937	1415
Oxide	GeO	SiO_2

As previous described section 1.2, Si and its corresponding dielectric SiO_2 are a great material system for use in optical confinement and wave transmission, however Si not a good choice for active photonic devices due to its transparency in such wavelength ranges. Ge and silicon germanium (SiGe) alloy, are materials that have recently been adopted to improve the performance of Si transistors and have also been researched and developed to show their potential as the building blocks for monolithically integrated photonic devices [41].

Recently, high-performance Ge active devices have been developed for monolithic integration with Si. The most advance Ge based active device is a Ge based photodetectors with high absorption coefficients, internal quantum efficiencies larger than 90% and bandwidth above 30 GHz at a wavelength of 1550 nm [42]. The Ge photodetectors can be found in telecom application where they are monolithically integrated in active cables and with transimpedance amplifiers [43]. Ge based modulators have also been developed where the best reported performance of Ge modulators was based on a Franz-Keldysh effect with 30 GHz bandwidth [44]. This was achieved without resorting to resonant enhancement as what is required in plasma dispersion based Si microring modulators. Ge photodetectors and modulators have been integrated with Si waveguides that results in very low capacitance [45]. It was reported that if this was directly integrated with analog circuits such as drivers or transimpedance amplifiers, power consumption of the whole systems can be reduced to a few tens of femtojoules per bit [46]. This is an order of magnitude lower than

conventional systems that are based on wire bonding which have a consumption of picojoules per bit.

Ge based lasers are the least advanced Ge based device and more research and development is required to increase its performance and reliability for integration in a photonic integrated circuit. Even though Ge is an indirect bandgap material, the lasing effect in Ge can be band engineered to behave like a direct gap material by using tensile stress and n-type doping [47]. The energy bandgap of bulk Ge, tensile strained intrinsic Ge and tensile strained n-type doped Ge is as shown in the Fig 1.4 below.

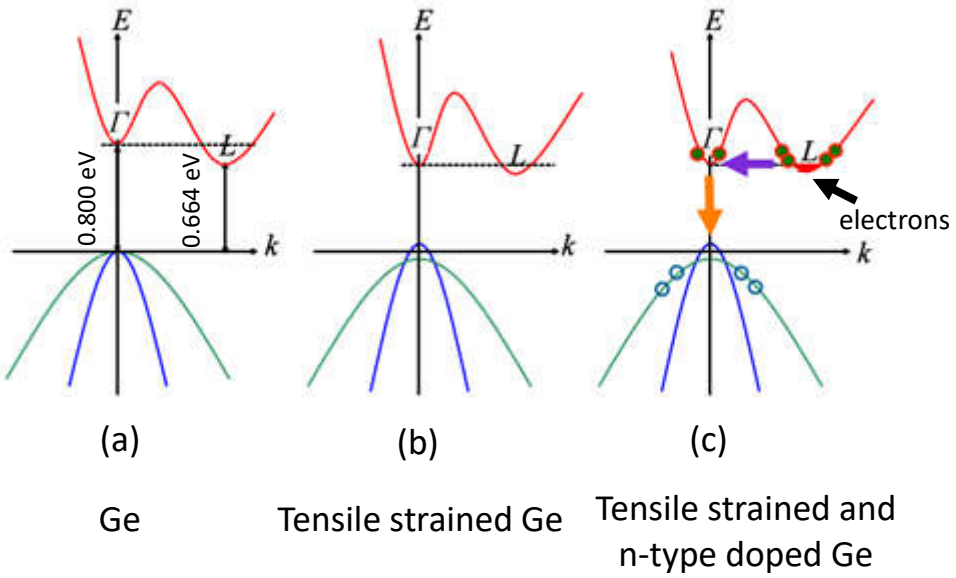


Fig. 1.4: (a) Schematic band structure of Ge showing the difference of 0.136 eV between the direct and indirect gap, (b) the difference between the direct and indirect can be reduced to 0.115 eV by introducing 0.25% tensile strain, (c) equal direct and indirect gap is achieved by 0.25% tensile strain and n-type doping [48].

Efficient light emission in the 1550 nm - 1620 nm region was achieved by inducing 0.2 - 0.3% tensile strain along with n-type doping to compensate for the energy difference between the direct and indirect gap. The performance of the Ge lasing is expected to improve with increasing n-type doping levels.

For practical application and monolithic integration, the ability to achieve lasing or light emission under electrical injection is required. Ge laser was firstly demonstrated indicating the capability of electrical injection causing light emission by employing tensile stress and n-type doping [49].

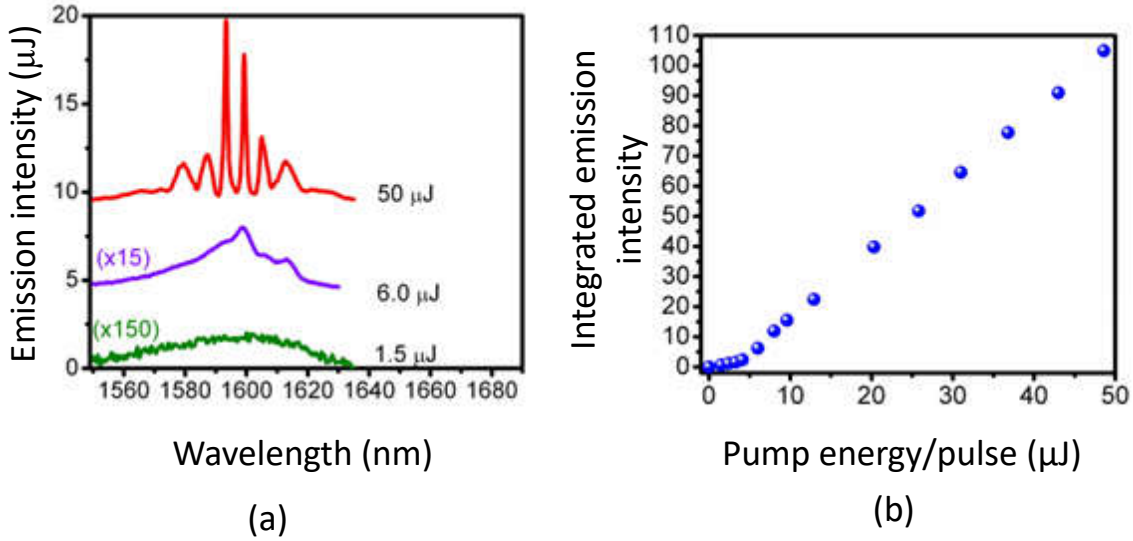


Fig. 1.5: (a) 3 emission spectra of Ge under optical pumping at 1.5, 6.0 and 50 μJ/pulse pumping power corresponding to spontaneous emission, threshold for lasing and laser emission, (b) integrated emission intensity showing the lasing threshold at 6.0 μJ/pulse pumping power [50].

The lasing spectra have been shown to evolve from broad emission band to a sharp Fabry-Perot resonance with increasing pump level. The polarization evolves from mixed TE/TM mode to dominantly TE while a threshold is also observed at ~5 μJ/pulse (30 kW/cm^2) [51].

Ge based passive devices such as waveguides have also been demonstrated. Ge waveguides fabricated on Ge-on-insulator (GeOI) have been reported to be smaller in footprint compared to a Si waveguide with negligible bending loss due to the strong optical confinement [52].

Fig. 1.6 below shows the wavelength performance range for Ge based modulators, photodetectors and laser all within the optical telecommunication range. For Ge modulators, the wavelength performance can be changed by adding 0.7% Si to the Ge during the growth process to tune the modulator response to 1550nm [53].

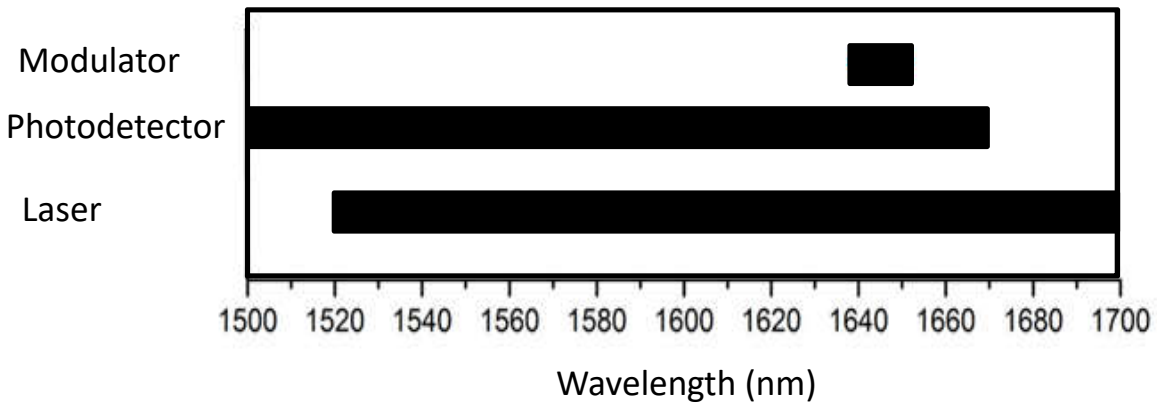


Fig. 1.6: Wavelength performance range for Ge modulators, detectors and lasers.

Integrating the Ge photodiode, modulator, laser and passive devices monolithically in one photonic integrated circuit would require designing a compatible fabrication process flow. The biggest challenge for monolithic integration is to determine the material composition, doping and fabrication process. Highlights from publications stated that the biggest challenges to the fabrication of Ge based devices are wafer polishing and the etching of Ge [54]. With research towards fabrication process compatibility between Si and Ge, it is anticipated that a monolithic photonic integrated system based on Si and Ge can be fully realized.

1. 5. SiO_2 cladding layers for optical waveguides: State of the art

Silicon dioxide (SiO_2) is a great material system for use in optical confinement and wave transmission due to it being an excellent electrical insulator and is transparent and has low optical loss at telecoms wavelength. For optical confinement; SiO_2 is a low refractive index material that can be used as a cladding layer for optical waveguides and photonic circuits. The thickness of the required SiO_2 cladding layer is dependent on the refractive index difference between the core and cladding layers. Therefore, the SiO_2 cladding layer must be sufficiently thick in order to avoid the optical light leakage [55]. Furthermore, the capability of SiO_2 to be stacked on top of different substrate materials such as Si, GaAs, GaN, sapphire is highly desirable in order to fabricate photonic circuits.

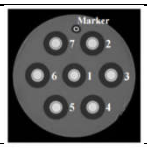
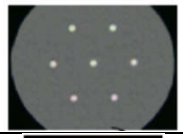
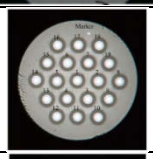
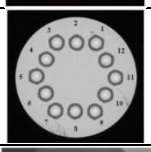
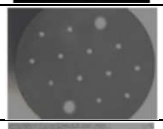
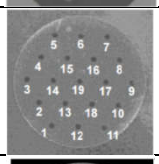
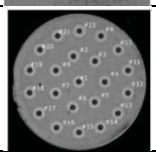
There are a number of different methods to deposit SiO_2 layer which are:

1. Thermal oxidation [56]
2. Chemical vapour deposition (CVD) [57]
3. Plasma enhanced chemical vapour deposition (PECVD) [58]
4. Sputtering [59]
5. Sol-gel method [60]

The main advantages and disadvantages of these different methods are explored later in chapter 3 which highlights the development of multi-layer stacking of sol-gel SiO_2 for cladding and passivation layers.

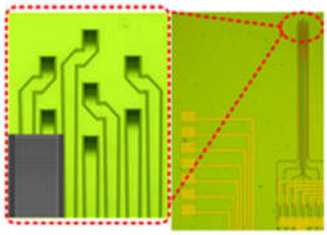
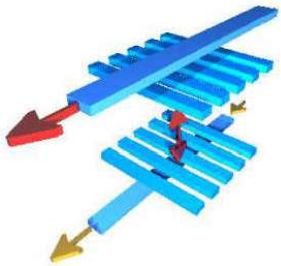
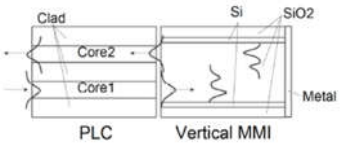
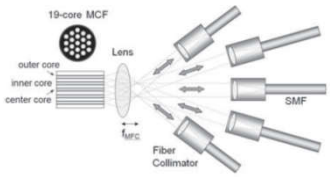
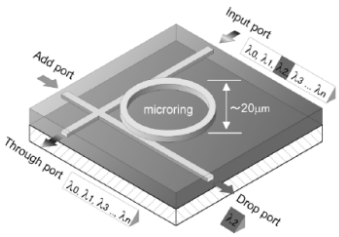
One of the main aims of the SiO_2 as a cladding and passivation layer is to enable space division multiplexing (SDM) which is a technique proposed as one of the candidates to address the issue of ever increasing demand for greater data transmission and this is achieved by exploiting additional channels (e.g. cores) in the spatial domain [61]. SDM promises to deliver higher capacity, smaller footprint, and eventually a lower cost per bit compared to conventional single mode fibre communication [62]. In order to improve the capacity of data transmission bandwidth through SDM, multi-core fibres (MCF) are a major component to realize this scheme [63]. High density MCFs have been developed with the number of cores ranging from 7 to 22 cores and capacities up to 2.15 Pb/s as shown in the table 1.3.

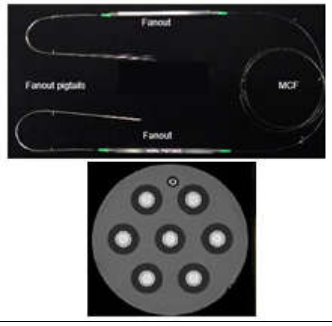
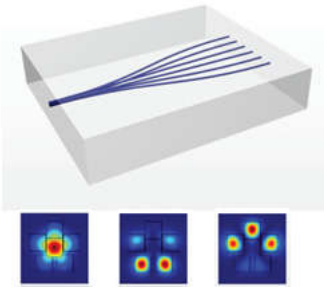
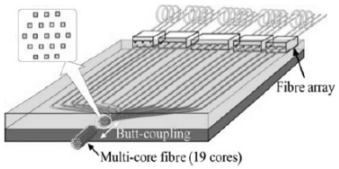
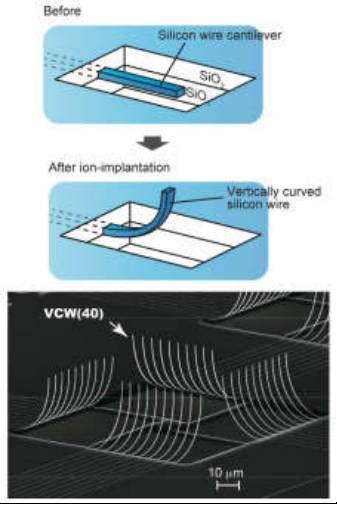
Table 1.3: High capacity multi-core fibre

	Number of cores	Cross sectional view	Capacity	Reference
1	7		109 Tb/s	[64]
2	7		112 Tb/s	[65]
3	19		305 Tb/s	[66]
4	12		1.01 Pb/s	[67]
5	14		1.05 Pb/s	[68]
6	19		2.05 Pb/s	[69]
7	22		2.15 Pb/s	[70]

Due to the fact that the cross sections of the core position of these MCFs are all 3 dimensional, the issue arises then on how to interface from photonic integrated circuits which are planar to these 3-dimensional MCFs. Several schemes have been proposed for interfacing such as fan-in/fan-out device [71], vertical Si waveguide [72], vertical MMIs [73], compact lens coupling [74] and vertical coupled ring resonators [75]. These schemes can be categorized into direct and indirect interface method and a summary is as seen in Table 1.4.

Table 1.4: Summary of various coupling schemes

	Scheme for interfacing	Figure	Comments	Reference
1	Fan-in/fan-out device: Grating coupler array based MCF		Vertical grating coupling connection to a 7-core MCF. Loss of less than 2.5 dB.	[71]
2	Vertical Si waveguide		Theoretical vertical coupling from Si waveguide to photonic crystal microcavity. 90% efficiency.	[72]
3	Vertical MMI		Vertical MMI coupler with insertion loss of 1.2 dB and high return loss of over 30 dB.	[73]
4	Compact lens coupling		Free space coupling to 19-core MCF using optics with total insertion loss of 1.22 dB.	[74]
5	Vertical coupled ring resonator		Vertical coupled ring resonator fabricated using sputtered SiO_2 and Ta_2O_5. Loss of 0.2 dB at cross point.	[75]

6	Multi-core fibre fan-out		2-12 core MCF fibre fan-out with average insertion loss of 0.6 dB, average crosstalk of <40 dB.	[76]
7	Ultra-short pulse laser inscription method		Accurate 3D embedded waveguide from laser inscribed glass with a low insertion loss of 0.9 dB and return loss of <60 dB.	[77]
8	Laminated polymer waveguide fan-in/fan-out device		Stacked polymer waveguide for 19 core MCF with insertion loss of <20 dB and crosstalk of <-40 dB.	[78]
9	Vertically curved Si wire		Vertical curved Si waveguide fabricated via implantation of ions onto Si waveguide with a coupling loss of 3 dB.	[79]

For a direct interface scheme, the optical signal stays completely within the whole interface process. The schemes for direct interface are shown in the Fig. 1.7(a) and Fig. 1.7(b) below.

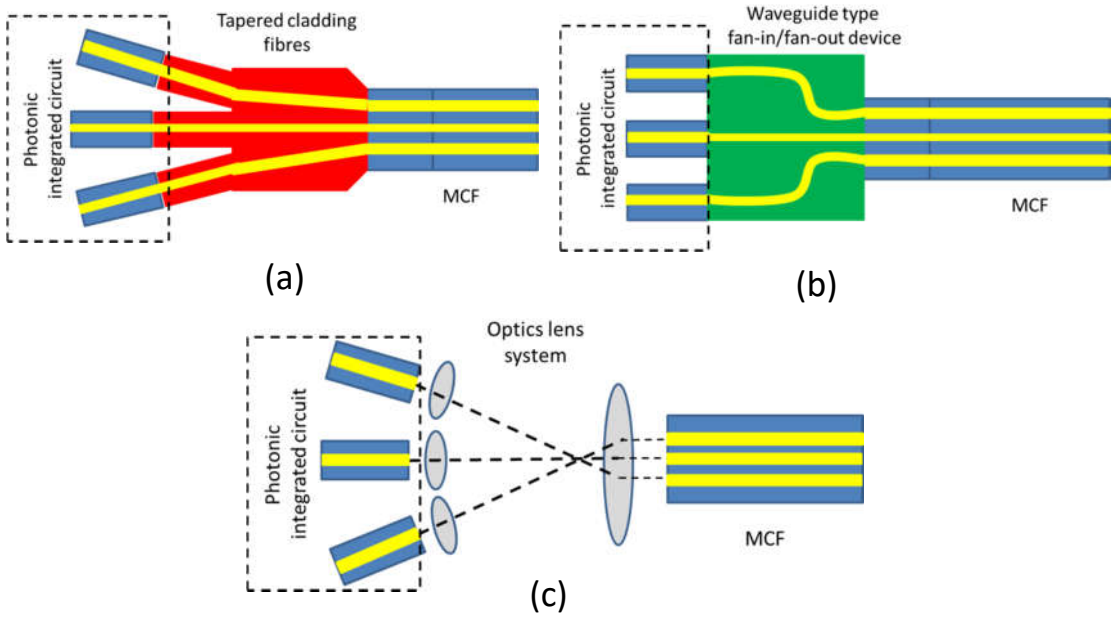


Fig. 1.7: Interface scheme from photonic integrated circuits to MCF through direct interface: (a) Tapered cladding fibres and (b) waveguide type fan-in/fan-out device while indirect interface through free space is shown in (c) optic lens systems [80]**.**

In Fig. 1.7(a), photonic integrated circuits are connected to single mode fibre and the single mode fibre cladding are then tapered or thinned down to the core spacing as shown. The fibre bundle type has been commercialized by Chiral photonics [76] and is well suited for low cost and mass production.

Alternatively, in Fig. 1.7(b), the connection can be provided by a separately fabricated waveguide module. The waveguide module can consist of a small block of glass or polymer where waveguides are either inscribed by ultra-short pulse laser inscription or patterned using photolithography and etched within the stacked polymer layers. The ultra-short pulse laser inscription method has been commercialized by Optoscribe [77] and offers high design flexibility and can be easily combined with photonic integrated circuits. Similarly, a laminated polymer waveguide fan-in/fan-out waveguide device has also been demonstrated to couple to a 19-core MCF [81].

As for indirect interface methods, the optical signal is propagated through free space from one facet to the other using bulk optics such as lenses and prisms as shown in Fig. 1.7(c). Compared to the direct method, the indirect interface method usually results in a less compact design. Despite this, the indirect method has the flexibility to be easily adapted to accommodate slight variations in alignment to the core layout of the MCF. The indirect method also allows the manipulation of the wavefronts of spatially multiplexed signal while it is propagating through free space. Results have shown the indirect method being applied to 7-core, 19-core and 36-core MCFs [82]. These designs have also been commercialized by Optoquest [83].

In our work, we aim to develop a novel interface method from the photonic integrated circuit to the MCF by leveraging a vertical coupler waveguide.

1. 6. Fabrication issues for photonic integrated circuits and novel fabrication techniques

There are two approaches as of how to fabricate a photonic integrated circuit. The first method is a non-monolithic approach where the photonic devices are fabricated separately and at a later stage are bonded or packaged together [84]. Wafer bonding of separately fabricated photonic devices such as in the case of III-V lasers has been demonstrated [85]. Nevertheless, this wafer bonding approach faces challenges in terms of the parasitic capacitance, high temperature required for bonding and difficulty in aligning the separate devices for bonding [86].

The development and growth of Ge crystals on Si has been demonstrated at temperatures ≤ 450°C which is compatible with the CMOS Si processing [87]. Therefore, a monolithic approach to fabricating the photonic integrated circuit using Ge would be the most ideal.

Waveguides are one of the basic building blocks of photonic devices and the width of the waveguide is one of the important design parameters that must be controlled in order to maintain the correct optical mode. Likewise, device performance of other photonic devices also relies on accurate geometry and width, for example the fabricated dimensions of laser diodes affect the performance and far field angle of laser diodes. Further details on waveguide geometries, its effect and fabrication results are discussed in chapter 2 of this thesis.

In order to achieve high fabrication accuracy, the use of chemical etching would have undesirable effect in terms of etch controllability and the isotropic etching of the sidewall profile. Therefore, plasma based dry etching is the only practical way to etch the semiconductor material. Dry etching is one of the key technologies for the processing of semiconductor devices which demand excellent sidewall profile control, etching anisotropy, low ion-induced etch damage, smooth and residual free etch surface, selectivity versus the photo resist and moderate etch rates [88]. This realizes the capability to fabricate very small structures with excellent dimension control. To control the etching process, the pressure, frequency, power, temperature, gas chemistry and gas flow rate are all important parameters that affect the dry etching results. For dry etching, the inductively coupled plasma (ICP) dry etching is the main key technology that is used to for accurate and repeatable etching. It is also one of the main processes that are fully integrated within the CMOS Si process flow. Therefore it is compelling to make use of the ICP to etch the Ge; nevertheless the dry etching parameters are less researched in order to realize accurate dry etching of Ge.

To realize optical waveguides for interfacing from the photonic integrated circuit to a MCF, there are two issues that must be addressed. Firstly is the ability to stack different refractive index materials on top of one another to realize the optical waveguides. Secondly, to ensure optical confinement, the thickness of the cladding layers must be sufficiently thick enough. To address this, we develop a multi-layer stacking scheme using sol-gel SiO_2. The main issue with sol-gel based fabrication is the appearance of cracks and peeling

on the sol-gel SiO_2 layer during the fabrication process. The work presented in thesis seeks to address the fabrication issues by characterizing and optimizing the fabrication process to realize a multi-layer stacking of sol-gel SiO_2 layer with no cracks and peeling. A number of different core materials were also experimented on to realize an optical waveguide. Also, by making use of multi-layer stacking, the second issue of achieving greater thickness can also be addressed.

Due to the highlighted fabrication issues, we explore two novel techniques for fabricating future photonic integrated circuits. Firstly, we make use of CHF_3 based ICP dry etching to accurately etch Ge waveguides and achieve a near vertical sidewall angle profile. Secondly, we explore a multi-layer stacked sol-gel SiO_2 fabrication technique which can be developed towards a optical waveguides to interface between the photonic integrated circuit and a MCF.

1. 7. Thesis construction

In this thesis, the research background and purpose of has been explained in Chapter 1. An overview of photonic integrated circuits has been discussed. Ge as the material of choice for photonic integrated circuits has been explained. The need for coupling to interface between planar circuits to 3-dimensional structures such as a multi-core fibre has also been explained with the need for proper cladding layers. The issues with regard to the fabrication of Ge and coupling have also been highlighted. Furthermore, two novel fabrication techniques have been proposed. The accurate etching of Ge by using a CHF_3 based inductively coupled plasma is proposed and a multi-layer all sol-gel fabrication technique is also proposed for the cladding and passivation layers for fabrication of optical waveguide.

In chapter 2, theoretical calculations on the optical confinement of a Ge waveguide are presented which represents the design requirement for fabricating a single mode Ge waveguide. Then, the accurate dry etching of Ge by using a CHF_3 based ICP presented and discussed [89][90]. Dry etching of Si is a well understood fabrication technique and the use of SF_6 based ICP dry etching is able to produce vertical sidewall with high accuracy. However, when using the same recipe for Ge, under-cut occurs and this produces a sloping sidewall and reduces the accuracy of the etched waveguide. A CHF_3 ICP based dry etching method is proposed and reported for the accurate etching of Ge waveguides. CHF_3 ICP based dry etching produces excellent anisotropy along with good selectivity with regards to regular polymeric

photoresist, which leads to the elimination of the under-cut issue. As a result, an almost vertical sidewall angle of 85° with an etching rate of 190 nm/min was realised with a relatively high selectivity ratio of 5:1 against regular photoresist.

In chapter 3, the issues, mechanism and fabrication method to realize multi-layer stacking of sol-gel SiO_2 for optical waveguide cladding and passivation layers was discussed. A new annealing and O_2 plasma fabrication process was developed to eliminate the issues of cracks and peeling. The results demonstrates that multi-layer stacking scheme of sol-gel SiO_2 layers is suitable to realize cladding and passivation layers for optical waveguides. Furthermore, a number of different core materials on the sol-gel SiO_2 cladding layer were experimented on to realize an optical waveguide.

In chapter 5, the above results are summarized and the feasibility of the novel fabrication techniques is clarified for future photonic integrated circuits.

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Chapter 2: Accurate dry etching for Ge waveguides by using CHF_3 based ICP

2. 1. Germanium wafer structures

Significant research has been devoted to the integration of photonic devices that are compatible with standard silicon (Si) CMOS processing. Germanium (Ge) and/or Ge/Si materials has been demonstrated to be an Si process compatible material for active and passive photonic devices [1]. For both active and passive photonic devices, the structure of the material and wafer is important to determine the device characteristics and performance. Both Ge-on-Si and Ge-on-insulator (GeOI) structures such as the schematic shown in Fig. 2.1 below have been researched as suitable materials for active devices such as Ge lasers [2],[3] and passive devices such as rib waveguides [4].

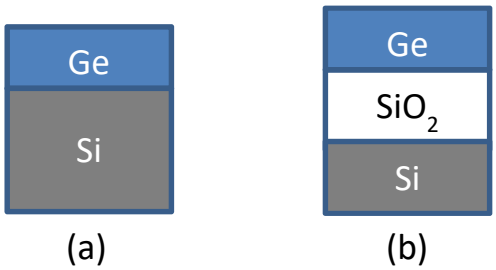


Fig. 2.1: Schematic diagram for (a) Ge-on-Si and (b) Ge-on-insulator (GeOI) structure

Table 2.1 below summarizes the structure and material of Ge wafers and its growth or fabrication process [5] and the explanation on the different growth and fabrication process are elaborated later on.

Table 2.1: Ge-on-Si and GeOI wafers, the respective growth and fabrication techniques and working wavelength for active and passive devices

	Structure	Growth/Fabrication Process	Wavelength (nm)	References
1	Ge-on-Si	2 step growth by UHV-CVD	1400 ~ 2200	[6],[7],[8], [9]
2	Ge-on-Si	2 step growth by MBE	1400 ~ 1700	[10],[11], [12],[13], [14]
3	Ge-on-Si	2 step growth by RP-CVD	1400 ~ 1700	[15],[16], [17],[18], [19]
4	Ge-on-Si	LEPE-CVD	1400 ~ 2200	[20],[21], [22],[23]
5	Ge-on-Si	Cold-wall thermal CVD	1400 ~ 1700	[24],[25]
6	Ge-on-Si	MHAH by RP-CVD	-	[26]
7	Ge-on-Si	Hot-wire CVD	-	[27]
8	Ge-on-Si	Bulk Ge bonding and polishing	-	[28]
9	Ge-on-Si	Oxidation condensation and growth	1400 ~ 1700	[29],[30]
10	GeOI	Layer transfer with SiO_2	1500 ~ 2200	[31],[32], [33]
11	GeOI	Layer transfer with Al_2O_3/SiO_2	1500 ~ 2200	[34],[35]
12	GeOI	LPE on Si_3N_4	-	[36],[37]
13	GeOI	LPE on SiO_2	-	[38],[39]

For Ge-on-Si structures shown in Table 2.1 (1-9), these have most predominantly been fabricated for direct growth of Ge photodetectors on Si [40]. There are a number of different growth techniques but in overall they follow the same strategy. Firstly, a thin buffer of Ge was deposited a low temperature of ~400°C directly on Si, and this layer was reported to contain many defects [6]. Secondly, a second layer of Ge was deposited at a higher temperature of ~700°C with a higher growth rate according to the different methods. After deposition, post-deposition annealing was carried out with the annealing conditions being critical for the improving the quality of the wafer. Multiple hydrogen annealing hetroepitaxy (MHAH) [26] was reported to markedly improve the quality of the wafer. Among all of the reported techniques, remote plasma chemical vapour deposition (RP-CVD) [15-19] is the most widely employed and is a process that is readily used in the industry while ultra-high vacuum chemical vapour deposition (UHV-CVD) [6-9] and molecular beam epitaxy (MBE) [10-14] are most commonly used in universities. Other novel growth methods such as hot-wire CVD [27] and oxidation growth [29-30] have also been reported. For direct bonding of Ge on Si [28], it was recently reported that a Ge photodetector was successfully fabricated at process temperatures of less than 450°C and this process was highlighted as promising for investigating Ge based light source.

A limitation of Ge-on-Si structure is that due to the smaller refractive index difference between Ge and Si, this limits the scaling down of the photonic device footprint. Furthermore, lattice mismatch between the Ge and Si

interface may degrade device performance. Therefore, the GeOI structure in Table 2.1 (10-13) is an alternative that is currently being highly researched.

For GeOI structures, the possibility of using a SmartCut technology on bulk Ge wafers has been reported [41]. The SmartCut technology involves using hydrogen implantation to transfer a Ge layer to a Si wafer using a SiO_2 oxide layer. However, issues reported are weak adhesion between the Ge and SiO_2 layer as well as planarization issues. This weak adhesion makes the structure too fragile for device fabrication. By using Al_2O_3 on top of the SiO_2 layer, the weak adhesion issue can be improved substantially [34-35]. Other novel techniques such as liquid phase epitaxy (LPE) by melting Ge directly onto Si_3N_4 [36-37] and SiO_2 [38-39] have also been reported with excellent result that also makes it a promising candidate to investigate Ge based light source.

2. 2. Design considerations for dry etching of Ge waveguides

Waveguides are basic building blocks of photonic devices and the thickness and the width of the waveguide are some of the important design parameters that must be controlled in order to maintain the correct optical mode. Likewise, both active and passive device performance also relies on accurate geometry and width of the waveguide for example in the far field angle for laser diodes.

The optical confinement factor is an important parameter to determine waveguide structure characteristics. It describes where the light is confined within the structure and furthermore, optical confinement factor also affect laser performance in laser diodes where having a high confinement is crucial for good laser performance.

In this work, we firstly look at the Ge-on-Si and GeOI slab waveguide structure and numerically calculate the confinement factor and its effect on the fabrication requirements.

The confinement factor can be calculated by following the work of Theodore Tamir in Guided-wave Optoelectronics [42] and the numerical analysis is explain in Appendix A.

Firstly, we determine the cut-off for fundamental mode in order to determine the maximum thickness of both the Ge-on-Si and GeOI slab waveguide structure. In all our calculations, we use the Ge refractive index of 4.28 [43], Si refractive index of 3.42 [44] and SiO_2 refractive index of 1.44 [45].

The normalized frequency *V* is determined by the following equation.

$$V = \kappa h \sqrt{\left(n_f^2 - n_s^2\right)} \tag{2.1}$$

Where n_f is the refractive index of Ge as the film core, and n_s is the refractive index of the substrate being either Si or SiO_2 and κ is the dispersion relation.

By designating *V* to be the fundamental mode, the maximum thickness, *h* of the waveguide to support only fundamental mode can be determined.

For the Ge-on-Si slab waveguide structure, the cut-off thickness for fundamental mode was calculated to be 300 nm while for the GeOI slab waveguide structure; the cut-off thickness for fundamental mode is 192 nm.

The electric field profile for a 300 nm Ge-on-Si waveguide is as shown in Fig. 2.2. From the electric field profile, we can determine the optical confinement within the Ge layer as well as the extent of the evanescent field spreading into the substrate, which in this case is the Si substrate.

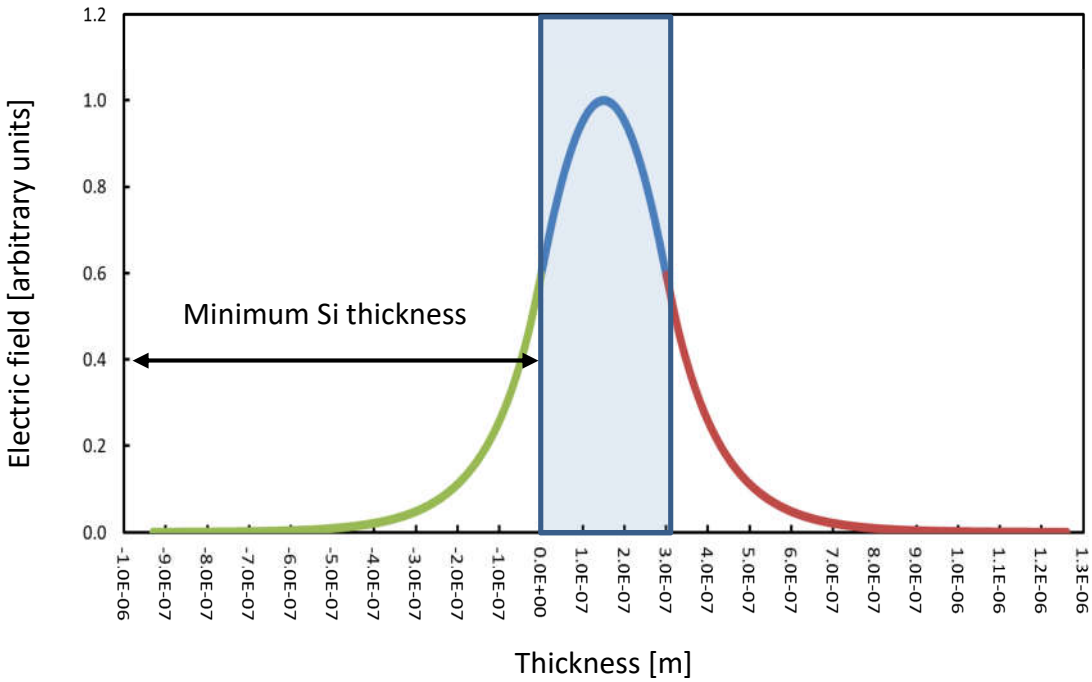


Fig. 2.2: Electric field profile for a 300 nm Ge-on-Si structure with the blue area being the 300 nm Ge core layer with 67% optical confinement. The minimum Si thickness to ensure that 99.9% of the electric field is confined within the structure is calculated to be 1.17 µm.

For a GeOI waveguide, the electric field profile for a 192 nm GeOI is as shown in Fig 2.3. The extent of the evanescent field spreading into the substrate, which in this case is SiO_2 is also shown. The spread of the evanescent field into the substrate determines the thickness of the substrate required to achieve >99.9% optical confinement within the whole slab waveguide structure.

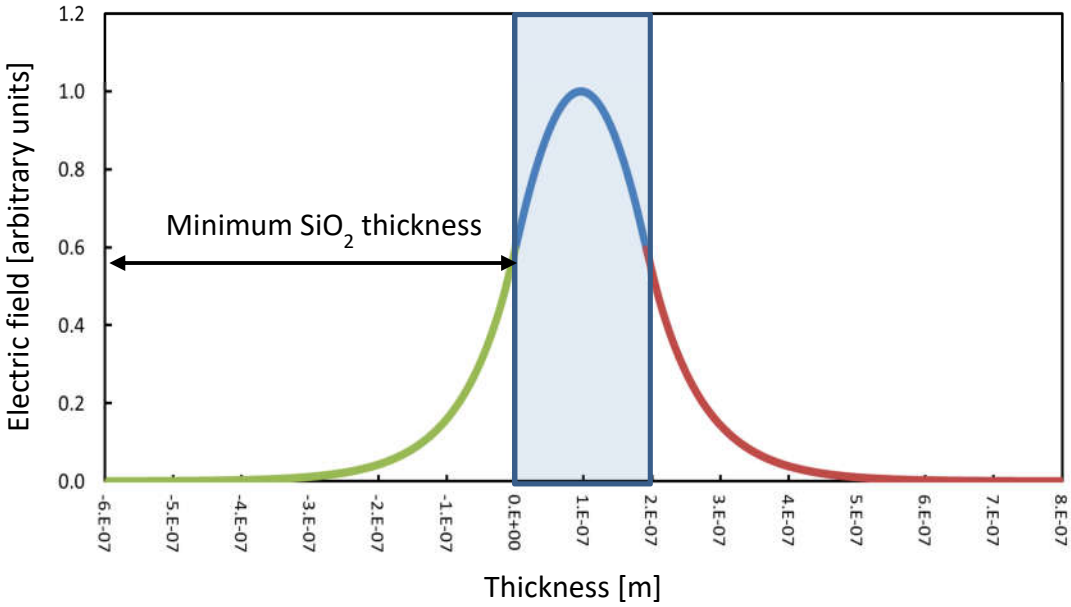


Fig. 2.3: Electric field profile for a 192 nm GeOI structure with the blue area being the 192 nm Ge core layer with 69% optical confinement. The minimum SiO_2 thickness to ensure that 99.9% of the electric field is confined within the structure is calculated to be 0.74 µm.

The optical field confinement calculated for the Ge-on-Si waveguide at cut-off thickness of 300nm is 67% while for the GeOI waveguide at a cut-off thickness of 192 nm is calculated to be 69%. This thickness however can

depend on the growth and fabrication method for the Ge-on-Si and GeOI wafers so as the thickness of the waveguide decreases, the optical confinement also decreases as shown in Fig. 2.4. It shows that for the Ge-on-Si structure, the optical confinement decreases from the maximum of 67% for 300 nm down to 13% with a thickness of 10 nm. Similarly, for the GeOI structure, the optical confinement decreases from the maximum of 69% for 200 nm down to 13% with a thickness of 10 nm. If considering the same thickness of 200 nm for Ge-on-Si and GeOI structures, we see the Ge-on-Si structure has a lower optical confinement of only 49% and this is due to the smaller refractive index contrast between the Ge core and the Si substrate.

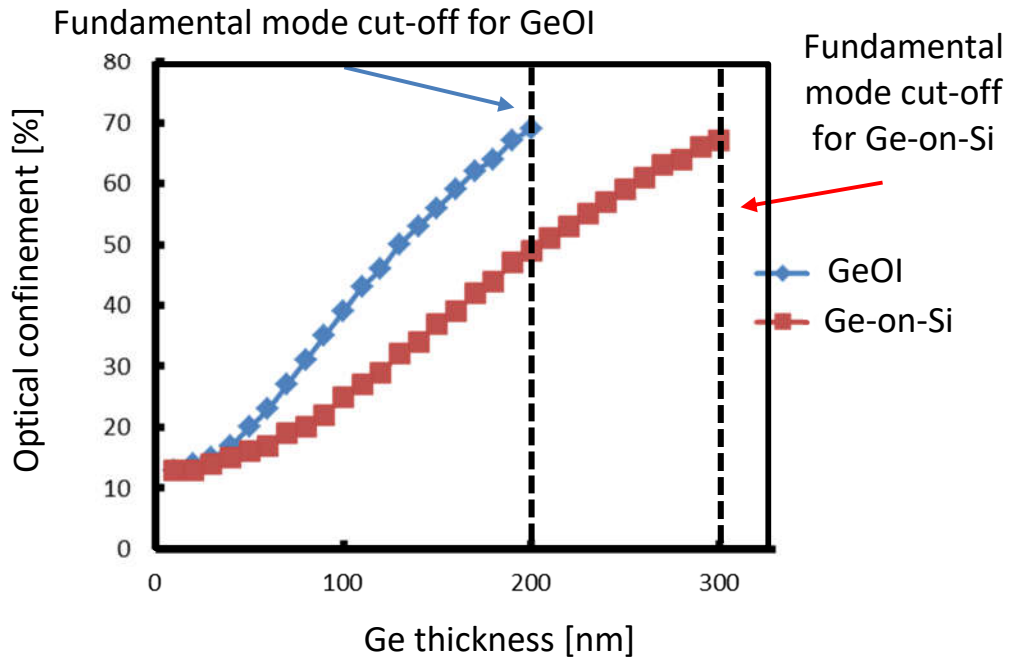


Fig. 2.4: Optical confinemnt as a function of Ge thickness for GeOI and Ge-on-Si structure. The fundamental mode cut-off for GeOI is 192 nm while for Ge-on-SI is 300 nm. Optical confinement decreases as the thickness of the Ge core layer decreases.

The evanescent field spreading into the substrate determines the minimum thickness that is required in order for the optical confinement to be >99.9%. A low optical confinement can lead to loss in the waveguide which is known as radiation loss towards the substrate. As the Ge thickness decreases, the evanescent field spreading into the substrate increases leading to a requirement of thicker substrates to maintain optical confinement. For the Ge-on-Si waveguide, the minimum Si thickness is 1.17 µm for a Ge core of 300nm and increase to 19 µm for a Ge core of 10 nm as shown in Fig. 2.5 below.

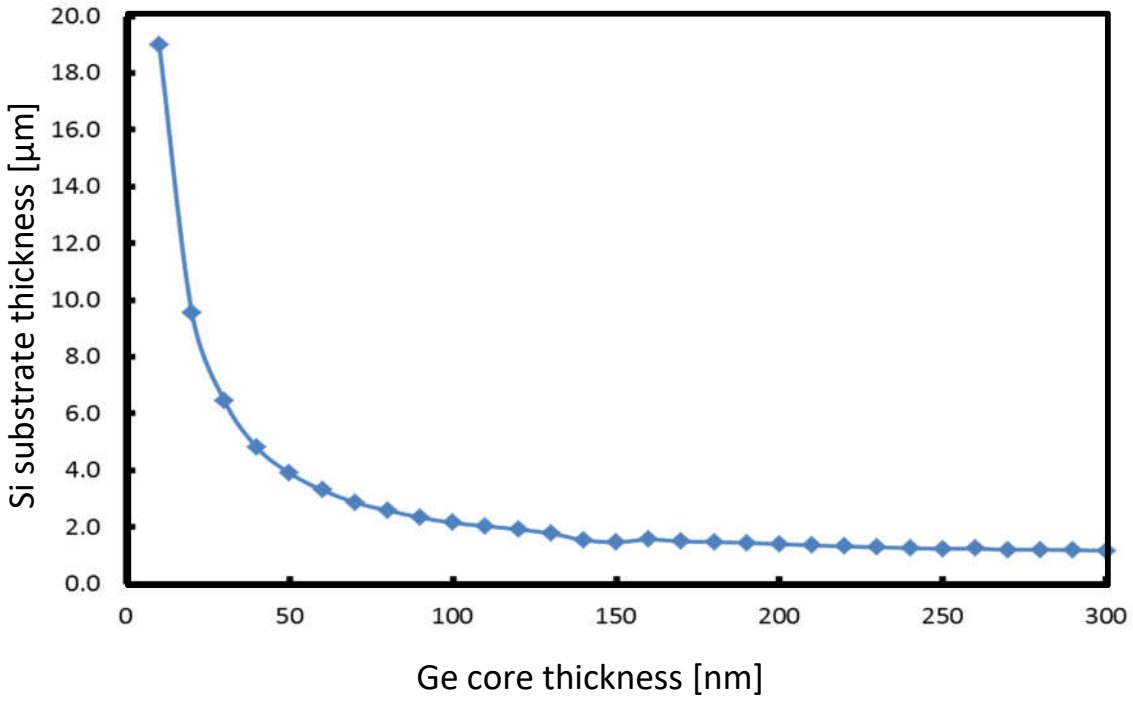


Fig. 2.5: Si substrate thickness required for >99.9% optical confinement in Ge-on-Si structure.

For the GeOI waveguide, the minimum SiO_2 thickness is a lot less with 0.74 µm thickness required for a Ge core of 200 nm and this increases to 8 µm for a Ge core thickness of 10 nm as shown in Fig. 2.6. The SiO_2 layer wafers available from the industry are available in thickness ranging from 0.05 µm to 4 µm [46]. Therefore, the feasibility of having a thick SiO_2 layer complicates the fabrication of the GeOI structure substantially. By limiting the Ge core thickness between 100 – 200 nm, the minimum SiO_2 thickness required is kept at < 1 µm, therefore easing the difficulty in producing a thick SiO_2 layer.

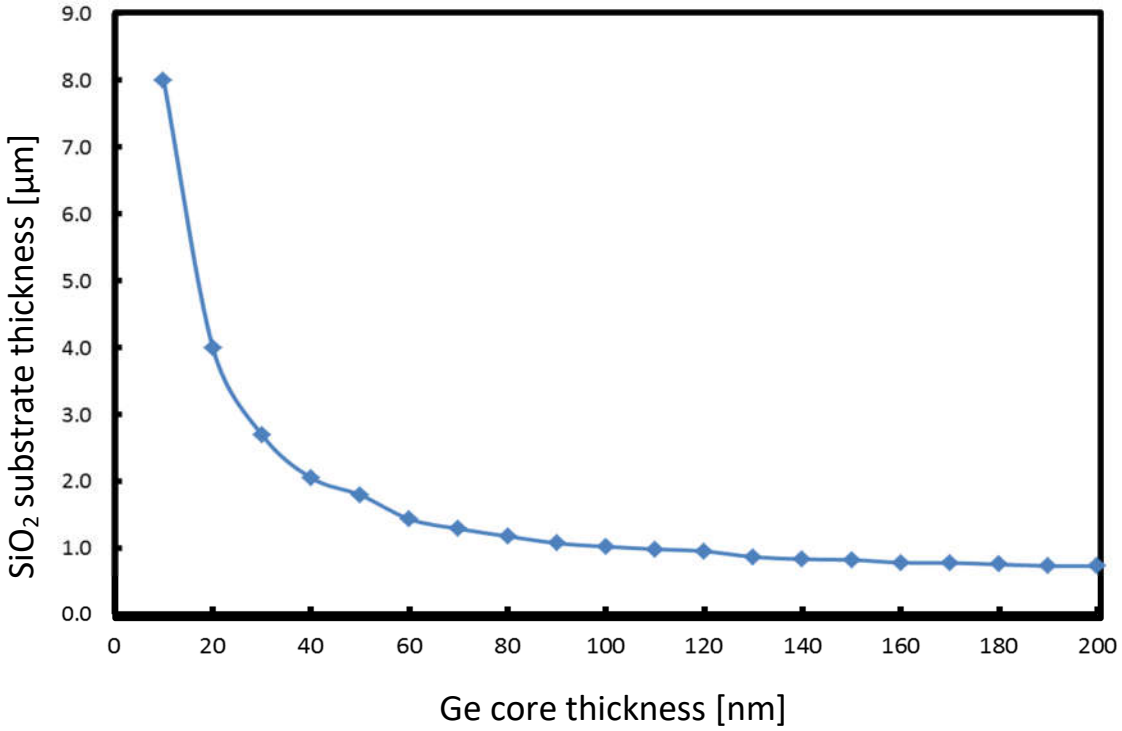


Fig. 2.6: SiO_2 substrate thickness required for >99.9% optical confinement in GeOI structure.

If comparing the same Ge core thickness of 200 nm for both Ge-on-Si and GeOI structures, we can conclude that due to the higher difference in refractive index, the GeOI structure has a better optical confinement at 69% and requires a much thinner SiO_2 substrate layer of 0.74 µm to have >99.9% optical confinement. On the other hand, for a 200 nm Ge-on-Si structure, the optical confinement is only 49% and it requires a thicker Si substrate layer of 1.4 µm for >99.9% optical confinement. With this we can conclude that the thickness of around 200 nm for the Ge core waveguide is suitable to fabricate a single mode waveguide.

The width of the waveguide is also another factor that must be taken into consideration for the optical confinement when designing a waveguide. When looking at the width of the waveguide, we make use of FemSIM simulation to observe the change in the optical field as the waveguide width is reduced. As seen in the Fig. 2.7(a), for the Ge-on-Si structure with a 200 nm Ge core thickness, the optical confinement with a width of 1 µm is confined fully within the Ge core. However, the optical field radiates more towards the substrate as the waveguide width is reduced and at a width of 0.4 µm as shown in Fig. 2.7(b), the optical field is no longer confined only in the Ge core and it radiates substantially towards the Si substrate.

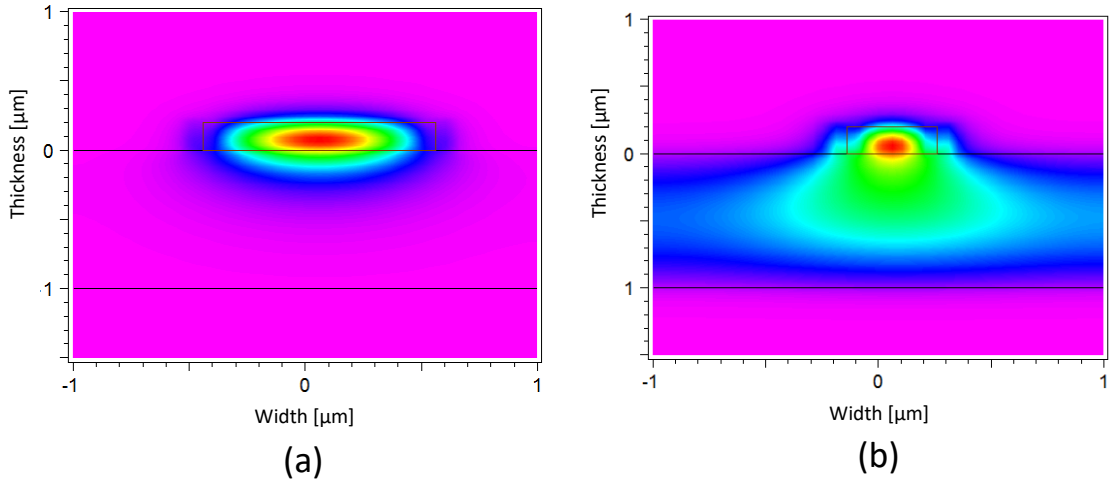


Fig. 2.7: Optical field confinement of a 200 nm thick Ge-on-Si structure with a waveguide width of (a) 1 µm and (b) 0.4 µm

For the GeOI structure, the optical field at a waveguide width of 1 µm is shown in Fig. 2.8(a). In contrast to the Ge-on-Si structure however, even when reducing the waveguide width of 0.4 µm as shown in Fig. 2.8(b), the optical field is still confined within the Ge core. This is attributed to the higher refractive index contrast between the Ge core and the SiO_2 substrate. The optical field was only found to be no longer confined within the Ge core when the waveguide width was reduced to 0.2 µm.

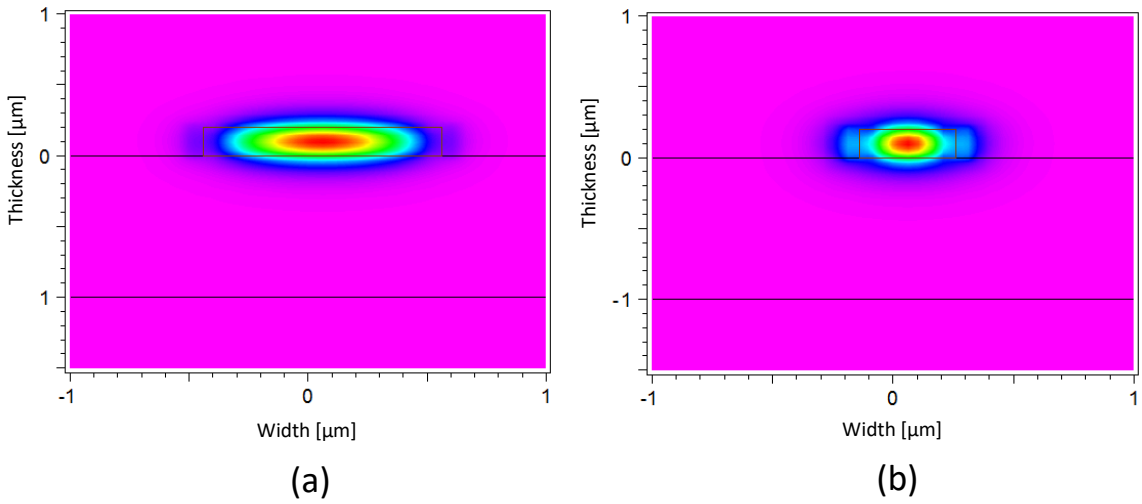
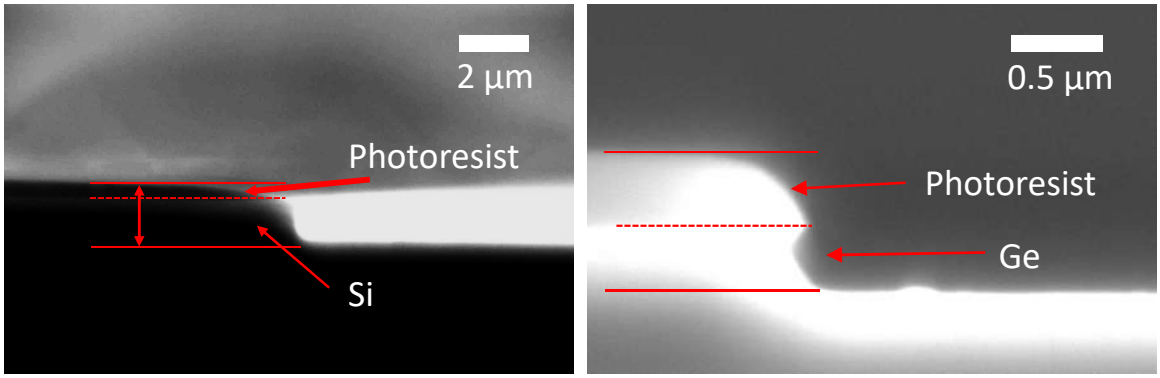


Fig. 2.8: Optical field confinement of a 200nm thick GeOI structure with waveguide width of (a) 1 µm and (b) 0.4 µm

Based on the numerical and simulation results, we can conclude that a Ge core thickness of 200 nm is sufficient for etching down the Ge waveguide and for a GeOI structure, waveguide width of more than 0.2 µm is sufficient for 69% optical confinement. For the Ge-on-Si structure however, the minimum waveguide width has to be more than 0.5 µm for optical field confinement of 67%.

2. 3. Dry etching of Ge

Issues arise where waveguide geometries may change during fabrication caused by under-cut of the sidewall during etching. A change of the waveguide geometry as shown in the previous section such as the thickness and the width will degrade and affect the optical confinement and optical mode [47],[48]. Therefore, anisotropic etching is a key feature in fabricating photonic devices [49]. With regards to the fabrication of waveguides, SF_6 based inductively coupled plasma (ICP) etching has been widely used for etching precise Si based photonic devices [50],[51] as seen in Fig. 2.9(a). Although both Si and Ge belong to the same group IV elements, fabricating precise Ge waveguide width and vertical sidewall has been less investigated. When using the same SF_6 based ICP etching of Si which produced a near vertical sidewall in Fig. 2.9(a), a significant issue of under-cut arises in Ge etching as seen in Fig. 2.9(b). When the under-cut happens, it degrades the precise width control and vertical side wall as shown clearly in Fig. 2.9(b). The under-cut occurs below the photoresist edge producing a sloping sidewall and thereby effectively reducing the width of the waveguide [52] when compared to the desired designed waveguide width.



(a) (b)

Fig. 2.9: Cross sectional view of SF_6 based ICP dry etching for; (a) Si showing a near vertical sidewall and (b) Ge clearly showing the under-cut issue producing a sloping sidewall

In addition to the under-cut issue, selectivity during dry etching is another issue that may reduce the width of the waveguide structure. A photoresist is used as a mask during dry etching to provide a means for transferring patterns and geometries to the Ge. A high selectivity would imply that Ge would be etched at a faster rate compared to the photoresist. On the contrary, a low selectivity would cause the photoresist to be eroded during the dry etching process. The final transferred geometry would then become distorted and less defined and conversely affects the width of the waveguide.

In this section of the study, a dry etching process using CHF_3 for the dry etching of Ge was developed to eliminate the under-cut issue and improve the selectivity. The etching properties, angle of the Ge waveguide's sidewall and accuracy of the etched waveguide width was investigated and discussed in this chapter.

2. 4. Experimental procedures

Throughout the experimental process, n-doped (6.5 x$10^{15}$$cm^{-3}$) Ge wafers with a (100) crystal orientation were used. The wafers were cleaned in warm butanol followed by warm isopropyl alcohol and blow dried in N_2 gas. A polymer based photoresist; 23CP by Tokyo Ohka Kogyo Co. Ltd was used as the photoresist mask and spin coated onto the Ge surface. Line and space periodic patterns forming the waveguide structure were defined and developed using a photoresist developer. Waveguide structures with widths ranging from 2 µm to 4 µm were formed to see the effect of under-cut and accuracy of the final etched waveguide widths. The initial thickness of the photoresist was determined to be around 0.85 - 0.9 µm thick.

An ICP was used to etch the waveguide structures and the ICP operating conditions used were as follows: Background pressure of 1.5x10-4 Pa, bias power (RF ion acceleration power) of 50 W, and CHF_3 flow rate of 10 sccm. The ICP power (decomposition power) was varied from 800 W to 1400 W at a reactor pressure of 2 Pa and the etching results are discussed in the following section. An ICP etching time of 60 seconds was determined to achieve the desired etching depth of approximately 190 nm that corresponds to the depth of a fundamental mode Ge waveguide. Finally all of the samples were cleaved and the facet was observed in a scanning electron microscope (SEM) so as to observe the etched sidewall angle profile.

2. 5. Results and discussion

We examined the selectivity ratio when using CHF_3 based ICP, which was approximately more than 4:1 (Ge:Photoresist) as seen in Fig. 2.10. The selectivity ratio was found to be the best at 5:1 when using an ICP power of 1000 W and 1200 W. Selectivity was 4.2:1 for 800 W and was the worst at 3.9:1 for 1400 W. It should be noted that in this experiment, we only used regular polymeric photoresist mask. No hard mask was required in order to obtain a vertical sidewall as CHF_3 supports polymer covering on top of the photoresist mask.

The etching rate of CHF_3 ICP dry etching was then determined in order to correctly etch to the core thickness of a Ge waveguide. The etching rate was 160 nm/min when using an ICP power of 800 W and increases to 220 nm/min when using an ICP power of 1400 W. For 1000 W and 1200 W of ICP power, a comparable Ge etching rate of 190 nm/min was determined as seen in Fig. 2.11. Therefore, the best conditions were found when using an ICP power of 1000 W and 1200 W in terms of the relative selectivity and etching rate.

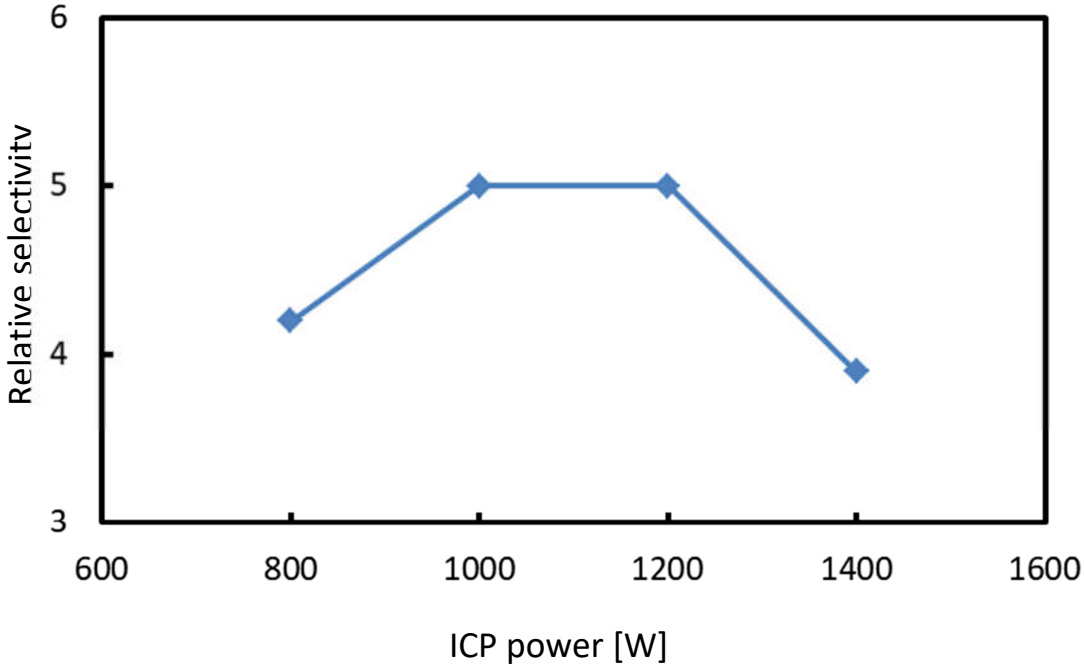


Fig. 2.10: Relative selectivity of Ge:photoresist of CHF_3 based ICP dry etching results as a function of ICP power

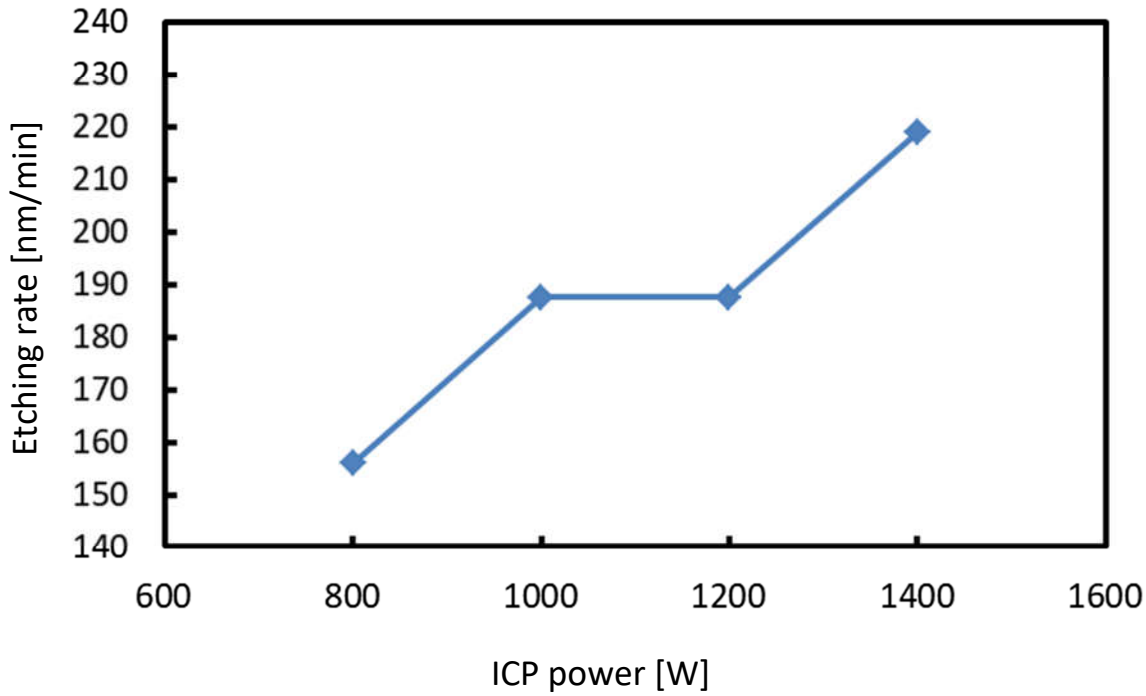


Fig. 2.11: Etching rate of CHF_3 based ICP dry etching results as a function of ICP power

Figure 2.10 shows the cross-sectional views and sidewall angle of dry etched Ge with increasing ICP power from 800 W to 1400 W; Fig. 2.12(a). 800 W (sidewall angle: 50°), Fig. 2.12(b). 1000 W (sidewall angle: 60°), Fig. 2.12(c). 1200 W (sidewall angle: 85°) and Fig. 2.12(d). 1400 W (sidewall angle: 70°). As is shown in Fig. 2.12, almost no under-cut was observed especially between 800 W and 1200 W ICP power even if the side-wall angles are significantly different.

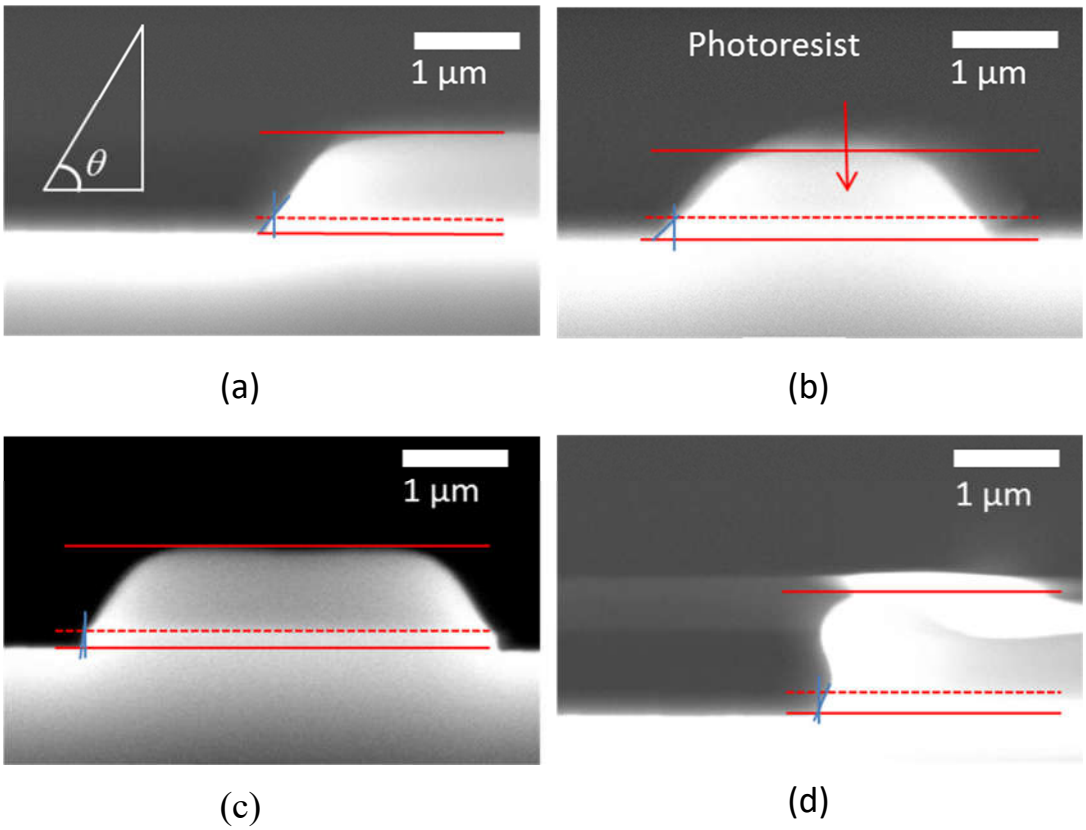


Fig. 2.12: Cross sectional views of CHF3 ICP dry etched Ge. ICP power and corresponding sidewall angle;

(a) 800 W ICP power – 50° sidewall angle

(b) 1000 W ICP power – 60° sidewall angle

(c) 1200 W ICP power – 85° sidewall angle

(d) 1400 W ICP power – 70° sidewall angle

The total kinetic momentum affects the sidewall angle. This is controllable by varying the ICP power even if the acceleration RF is fixed as it changes the total decomposed ion number. For an ICP power of 1200 W, a near vertical sidewall was obtained as shown in Fig. 2.12(c).

It should be noted that the sidewall angle degrades again for higher ICP power of 1400 W as seen in Fig. 2.12(d). This is attributed to the high kinetic momentum of the ions reflecting from the bottom etched surface and thus etches the sidewall. This correlates to the selectivity data where Ge was etched slowly when using 800 W of ICP power, however it was etched faster at 1400 W due to the higher kinetic momentum of the ions that caused the under-cut issue and leads to lower selectivity and higher etching rate as seen in Fig. 2.11.

When measuring the waveguide widths, it was found that the CHF_3 based ICP dry etching with 1200 W of ICP power gave the most accurate etched waveguide width compared to the desired designed waveguide width as seen in Fig 2.7. As the designed waveguide width became narrower, it was observed that the etched waveguide accuracy decreased due to the sidewall angle of photoresist being below 90° which changed the etched waveguide width. However, by using CHF_3 based ICP dry etching with 1200 W of ICP power, even a narrow waveguide width of 2 µm is etched accurately. The accuracy of the etched waveguide widths decreases from ICP power from 1400W to 800W. In comparison, the accuracy of an SF_6 based ICP etching was much lower than CHF_3 as shown in Fig. 2.13.

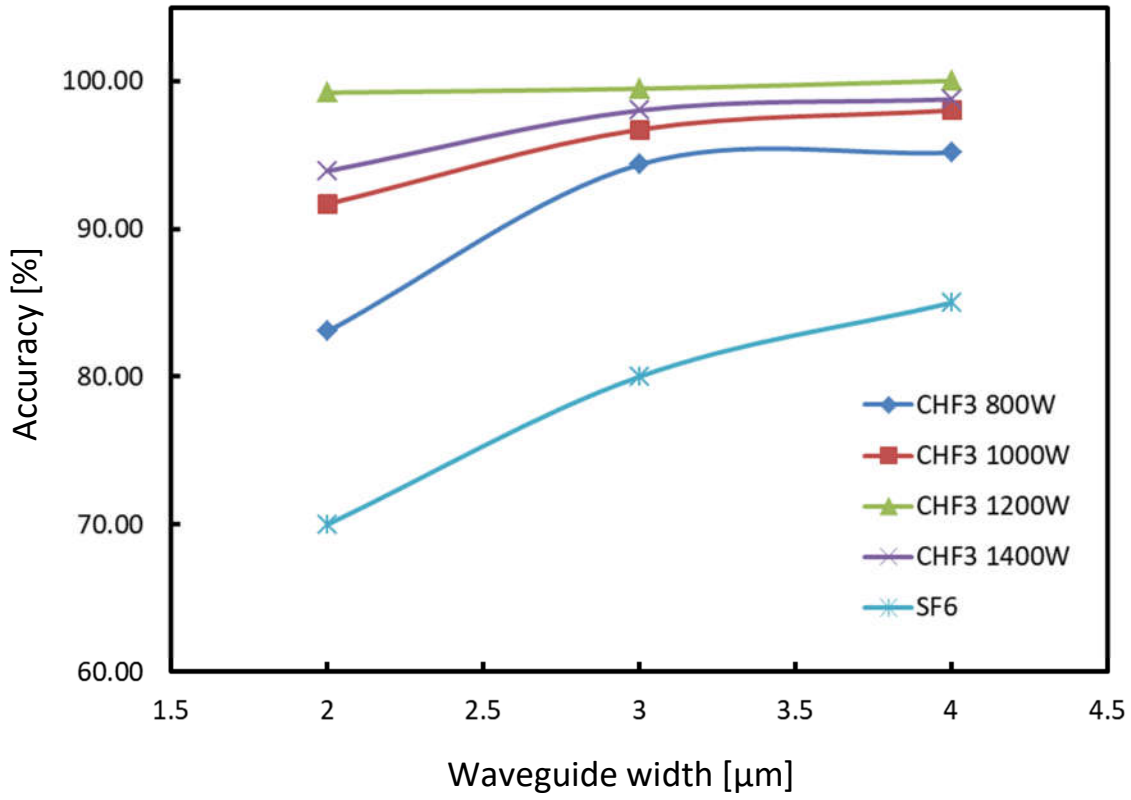


Fig. 2.13: Comparison of etched waveguide widths accuracy with widths from 2 to 4 µm for various CHF_3 ICP power and SF_6 ICP dry etching.

When looking at both SF_6 and CHF_3, the main etching during the dry etching process is through the dissociated F ions. Even though there is less data on dry etching mechanism for Ge, some information can be inferred from the etching of Ge by HF based wet etching. Si and Ge both belong to the same group IV and the crystal structure of Si and Ge are both the same which is in the shape of a diamond cubic crystal structure. The main differences when comparing Si to Ge then are the lattice spacing where Si has a shorter lattice spacing of 0.54209 nm while Ge has a longer lattice spacing of 0.56575 nm. Another difference can be seen when observing the electronegativity of Si

(1.90), and Ge (2.01). When comparing the electronegativity to F (3.98), we can see that that Si-F has a larger difference of 2.08 while Ge-F has a smaller difference of 1.97. This difference in electronegativity affects the bond strength and bond length of Si-F and Ge-F as shown in Table 2.2 below. It is shown that Ge-F has weaker bond strength and longer bond length and this causes the Ge to be etched at a faster rate compared to Si.

Table 2.2: Bond strength and bond length difference between Ge-F and Si-F

	Ge-F	Si-F
Bond strength (KJ/mol)	485	533
Bond length (Å)	1.73	1.58

It has also been reported that when using SF_6 ICP dry etching, Ge was etched faster than Si because the binding energy for Ge (33eV) is lower than Si (105eV) [53]. The lower binding energy for Ge and the reflectance of Ge-F ions at the etched-bottom surface causes severe under-cut of the sidewall as seen in Fig. 2.9(b) when compared to Si in Fig. 2.9(a). Therefore, the lighter mass of CHF_3 dissociated ions does not produce under-cut compared to SF_6 related dissociated ions.

An SF_6 based ICP dry etching was also found to have a low selectivity of 1:1 (Ge:Photoresist) that leads to photoresist erosion at the edges. The effects of further extending the etching time completely removes the photoresist and leads to a sloping sidewall and a reduction in the waveguide width.

Majority of fabricated Ge devices reported tend to make use of an oxide or metal hard mask during the fabrication process due to the faster etching rate of a normal polymeric photoresist mask compared to Ge [54]. The removal of the hard mask can be done through plasma processing. However, exposure to further plasma processing may lead to additional damage to the waveguide's surface [55], the sidewall and can also lead to a reduction in the waveguide width. In this study, we only used a polymer photoresist and by using CHF_3 based ICP dry etching; a relatively high selectivity ratio was achieved. The photoresist used in the experiment can be easily removed with warm photoresist remover.

2. 6. Conclusion

We have researched the ICP dry etching using CHF_3 to fabricate accurate Ge waveguides using photoresist mask [56]. A near vertical sidewall angle of 85° and a relatively high selectivity ratio of 5:1 (Ge:photoresist) were successfully achieved as shown in Fig. 2.14 below. The results suggest that the use of CHF_3 based ICP provides the capability to accurately etch Ge waveguides by eliminating the under-cut issue. We anticipate that the ability to fabricate precise vertical sidewall and width control of Ge waveguides can not only benefit other Ge and/or Ge/Si photonic devices but it can also improve the performance in other applications such as Ge metal-oxide-semiconductor field effect transistors on Si for future CMOS technologies.

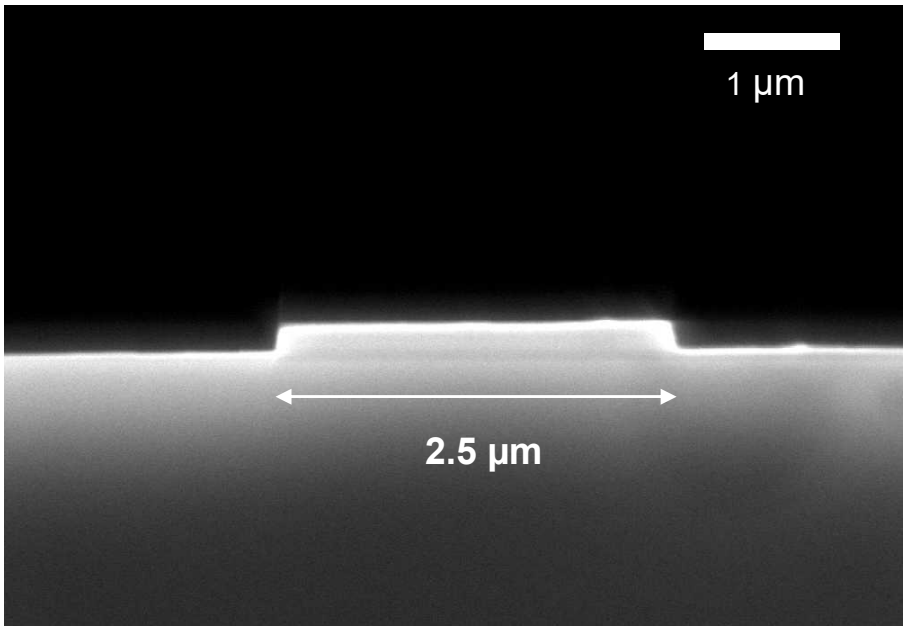


Fig. 2.14: Cross sectional view for a photoresist removed Ge waveguide with a width of 2.5 µm.

2. 7. References

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Chapter 3: Multi-layer stacking of sol-gel SiO_2 fabrication technique for cladding and passivation layers of optical waveguides

3. 1. Sol-gel SiO_2

In chapter 2, we focused on the optical confinement of a single Ge waveguide, the necessary parameters to fabricate a fundamental mode waveguide and the fabrication technique to fabricate a near vertical sidewall for a Ge waveguide. For chapter 3, the topic changes to the sol-gel SiO_2 fabrication technique for cladding and passivation layers of optical waveguides. Silicon dioxide (SiO_2) is a great material system for use in optical confinement and wave transmission due to it being an excellent electrical insulator and is transparent and has low optical loss at telecoms wavelength. For optical confinement; SiO_2 is a low refractive index material that can be used as a cladding layer for optical waveguides. The thickness of the required SiO_2 cladding layer is dependent on the refractive index difference between the core and cladding layers. Therefore, the SiO_2 cladding layer must be sufficiently thick in order to avoid the optical light leaking into the Si substrate [1]. Furthermore, the capability of SiO_2 to be stacked on top of different substrate materials such as Si, GaAs, GaN, sapphire is highly desirable.

The different methods to deposit the SiO_2 layers are thermal oxidation [2], chemical vapour deposition CVD [3], plasma enhanced chemical vapor deposition (PECVD) [4], sputtering [5], electron beam (EB) evaporation [6], atomic layer deposition (ALD) [7] and sol-gel method [8][9]. The advantage of using a sol-gel method is a lower working temperature of around 500°C compared to thermal oxidation method which has a working temperature of >1000°C. Correspondingly, deposition processes such as PECVD, ALD and sputtering requires the use of plasma equipment which increases the processing steps, complexity and cost of fabricating the device. Plasma based deposition also has a disadvantage of introducing damage by reducing electrical isolation [10] and increasing optical loss [11]. Furthermore, CVD and ALD uses silane gas as the main precursor which is explosive and flammable when its density exceeds 1%. Major incidents have occurred where silane gas supplied to a plasma CVD system had exploded leading to deaths and injuries [12].

For sol-gel based SiO_2, the deposition technique mostly used are dip-coating [13] and spin coating [14] which can both be used to control the thickness of the deposited sol-gel SiO_2 layer. Other different fabrication techniques using sol-gel method have also been demonstrated such as spray pyrolysis [15], direct imprinting [16] and recently even 3D printing [17]. In terms of the substrate used, the most commonly used substrate for sol-gel fabrication has been glass substrates due to the comparable thermal expansion co-efficients [18]. Waveguides based on sol-gel have been demonstrated, however majority of fabricated devices were fabricated on glass substrates and at low

temperatures [19]. Nevertheless, to achieve better integration, the ability to stack sol-gel SiO_2 on top of an Si substrate is much more desirable. In this work, sol-gel SiO_2 multi-layer fabrication technique on an Si substrate is demonstrated for the cladding and passivation layers of optical waveguide.

To fabricate optical waveguides, different refractive index materials must be stacked on top of the SiO_2 cladding layer to form the waveguiding core layer. Similarly, there are several techniques of depositing different refractive index materials including CVD [20], pulsed laser deposition [21], magnetron sputtering [22], spray pyrolysis [23] to form the waveguiding core layer. Sol-gel based fabrication has also been proposed for optical devices due to its simpler fabrication methods. SiO_2, ZnO, TiO_2 and GeO_2 are several examples of sol-gel materials used for photonic applications. Thus far, the fabrication of sol-gel based optical devices has been demonstrated as a single photonic layer deposited on glass [19] and Si substrate [24]. Sputtering is also another viable option to form the core layer.

In this chapter, we report and discuss on the main issues of stacking of sol-gel SiO_2, the cracking and peeling mechanism when stacking of the sol-gel SiO_2, the experimental procedures conducted and the results obtained to resolve the issues observed. Moreover, different core layers stacked using sol-gel and sputtering has also been explored.

3. 2. Cracking and peeling issue in stacking of sol-gel SiO_2

Two main issues are present when stacking sol-gel SiO_2. The first issue is the appearance of cracks on the sol-gel SiO_2 layer and the second issue is the peeling of the sol-gel SiO_2 layer. Both issues cause the sol-gel SiO_2 to not be stackable and prevent the fabrication of the cladding and passivation layers. The definition and mechanism for the cracks and peeling issues are addressed separately in the following sections.

3.2.1 Cracking mechanism in sol-gel SiO_2

Cracks in sol-gel SiO_2 are defined as a type of failure where fracture lines occur and break the SiO_2 atomic bonds. Cracks are shown in Fig. 3.1 (a) and (b) which are the side view and top view of cracks, respectively, in a thick single sol-gel layer of 1.9 µm thickness. For Fig. 3.1 (a), it is seen that the cracks appear throughout the thickness of the thick sol-gel layer. As shown in Fig. 3.1 (b), the cracks occur throughout the entire sample in this case (1.9 µm sol-gel SiO_2).

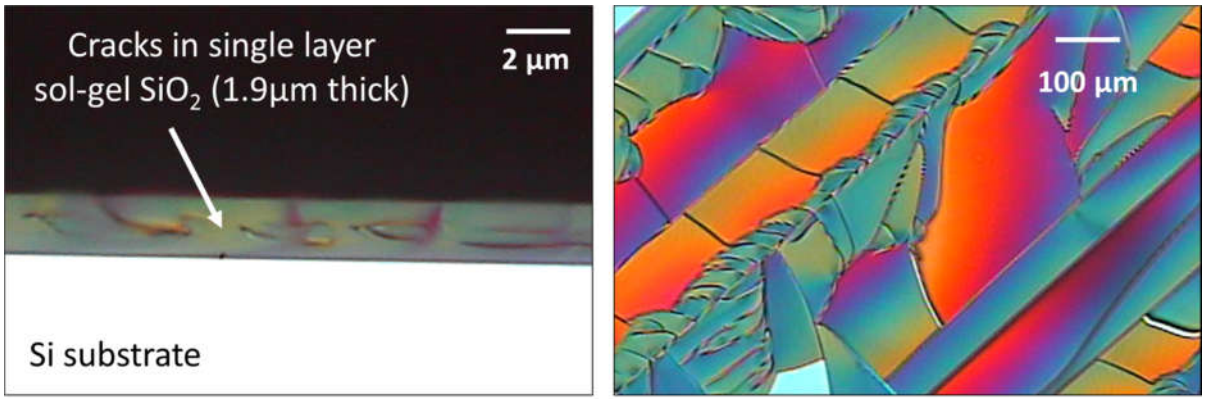


Fig 3.1: Crack issues observed during fabrication of sol-gel SiO_2:
(a) cracks in single layer sol-gel SiO_2 of ~1.9 µm thick,
(b) top view of the cracks across the entire sample.

The stress in the sol-gel SiO_2 layer, which causes the cracks, is due to multiple reasons in general such as external load, interfacial tension, intrinsic stress and mismatch in thermal expansion coefficients between the substrate and the sol-gel SiO_2 layer. When examining these sources of stress, we see that when varying the thickness of the sol-gel SiO_2 layer, the main cause is from the intrinsic stress. The intrinsic stress, σ_i is determined through Stoney's formula [25]:

$$\sigma_i = \frac{E_S t_S^2}{6(1-\upsilon_S)t_f}\Delta\frac{1}{r} \qquad (3.1)$$

where E_s, t_s and υ_s are the Young's modulus, thickness and Poisson's ratio of the substrate, t_f is the thickness of the sol-gel SiO_2 layer while Δ 1/r is the difference of curvature of the substrate before and after stacking of the sol-gel SiO_2 layer. E_s and υ_s are material properties with the ratio of $E_s/(1-\upsilon_s)$ (152 GPa) used in our estimations. From Eq. 3.1, two components affect the

intrinsic stress, namely, 1) the film and substrate thickness, and 2) the difference in curvature of the substrate before and after stacking the sol-gel SiO_2 layer. The influence of film and substrate thickness on the substrate curvature is approximated by the following equation [26]:

$$\Delta\frac{1}{r} = \frac{6\in_m}{t_s}\frac{M_f}{M_s}\frac{t_f}{t_s}\left[1 + \left(\frac{M_s - 4M_f}{M_s}\right)\frac{t_f}{t_s}\right] \qquad (3.2)$$

where $\in_m$ is the mismatch of thermal expansion coefficient of the sol-gel SiO_2 layer with respect to the substrate, M_s and M_f are the ratio of elastic modulus and Poisson's ratio of the substrate sol-gel SiO_2 layer and t_s and t_f are the thickness of the substrate and the sol-gel SiO_2 layer. From Eq. 3.2, and by using the critical thickness of 0.8 µm sol-gel SiO_2 layer where we see cracks starting to occur, the critical curvature of the substrate Δ 1/r is estimate to be 5.41×10^{-4} m^{-1}. From this and the use of Eq. 3.1, the critical intrinsic stress, σ_i where cracks start to occur is estimated to be 4.3 MPa.

From Fig. 3.1, we observe that this estimated stress causes cracks to appear throughout the whole sample because for a 1.9 µm thick sol-gel SiO_2 layer, the estimated curvature corresponds to 1.282×10^{-3} m^{-1} which is ~3 times greater compared to 0.8 µm case that leads to high intrinsic stress of 12.86 MPa. Thick SiO_2 layers of greater than 1.5 µm is occasionally required for optical waveguide cladding layers. Hence, in order to achieve greater SiO_2 thickness, a multi-layer stacking scheme of thinner sol-gel SiO_2 layers is proposed in this work. The difference in the estimated intrinsic stress against thickness for the single thick layer against the multi-layer stacking scheme is elaborated in the later sections.

3.2.2 Peeling mechanism in sol-gel SiO_2

Peeling is another issues observed during stacking of the sol-gel SiO_2 layer. The characteristic of peeling is that the upper sol-gel SiO_2 layer detaches from the lower layer and curls upwards [26]. This is shown in Fig. 3.2 (a) which shows the side view of the peeling between two sol-gel SiO_2 layers and Fig. 3.2 (b) which shows the top view of peeling.

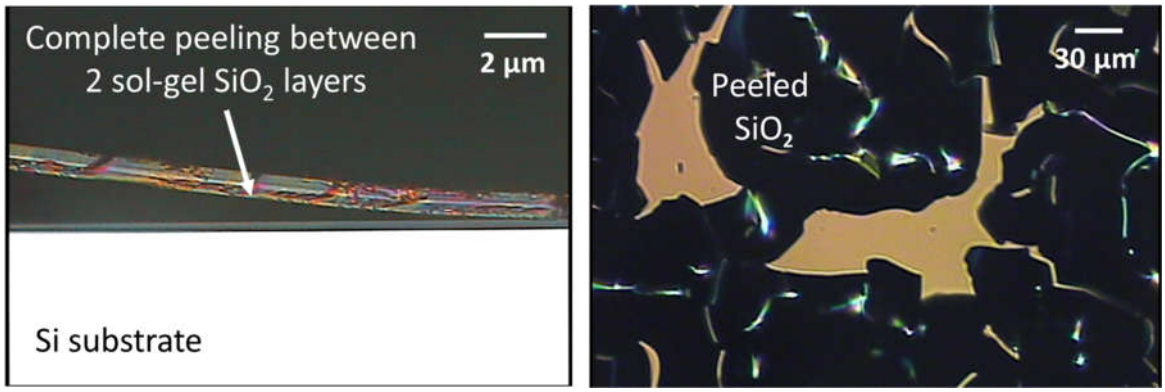


Fig. 3.2: Peeling issues observed during fabrication of sol-gel SiO_2: (a) side view of peeling between the SiO_2 layers in a double layer stacking, (b) top view of the same sol-gel SiO_2 sample showing peeling and cracks.

The main mechanism that we believe to be the cause of the peeling is the low adhesion between the upper sol-gel SiO_2 layer to the bottom sol-gel SiO_2 layer. It has been reported that chemicals used in making the sol-gel produced polymers that migrated to the surface of the layer during the annealing process [27]. When we stack the second sol-gel SiO_2 layer, we observe this polymer layer on top of first sol-gel SiO_2 layer. This polymer layer is what causes low adhesion between the two sol-gel SiO_2 layers and

this is defined in terms of work of adhesion (J/m^2). Work of adhesion is defined as the work which must be done to separate two adjacent surfaces. The work of adhesion is a measure of the strength of contact between these two surfaces. The work of adhesion is defined as:

$$\bar{\omega} = \frac{A}{\beta a_0^n} \tag{3.3}$$

where A is the Hamaker constant and β and a_0^n are related to the geometry of the sample [18]. The Hamaker constant for SiO_2 to SiO_2 is defined as 6.55 $x10^{-20}$J while a SiO_2 to a polymer material is defined as 4.87 $x10^{-20}$J. Assuming that the geometry of the sample is the same, we see that the work of adhesion for a SiO_2 to a polymer layer ($4.87x10^{-20}$ J/m^2) is lower than the adhesion of SiO_2 to SiO_2 ($6.55x10^{-20}$ J/m^2). This lower work of adhesion requires lesser work to peel when there is a polymer layer in between the two sol-gel SiO_2 layers.

Hence, in order to improve adhesion and eliminate peeling, we need to remove the polymer layer completely. Proper surface conditioning is required to ensure the removal of the polymer layer and the process to remove the polymer layer is explained in the following sections.

3. 3. Fabrication procedure for sol-gel SiO_2

In order to produce the sol-gel SiO_2, the following chemicals were mixed together; tetraethyl orthosilicate (TEOS), methyltriethoxysilane (MTES), ethanol, water and acetic acid in the following ratio (0.21:0.49: 0.24:0.29:0.05). If only using TEOS, the thickness of a crack free layer was determined to be only 0.3 µm. The addition of MTES in our experiments enables lower stress and a thicker crack free layer up to 0.7 µm, however the thickness is still insufficient for the purpose of optical confinement. A standard bulk n-type Si wafer is used as the substrate and which was firstly cleaned in a diluted BHF solution for 60 seconds. The solution was spin coated onto the cleaned Si wafer and heated on top of a hot plate up to 145°C to stabilize the sol-gel layer and then it was annealed at 500°C to remove the solvents. In our experiments, the size limitation of our annealer only permits 3.5 cm x 3.5 cm sized samples. Nevertheless, the simplicity of the sol-gel SiO_2 process using spin coating to deposit the sol-gel SiO_2 solution is also applicable for wafer scale processing. To increase the thickness of the sol-gel SiO_2 layer, multiple spin coating was carried out. A summary of the fabrication process is as described in Fig. 3.3. In order to eliminate the cracks and peeling, a number of different processes were carried out as is described in the following section.

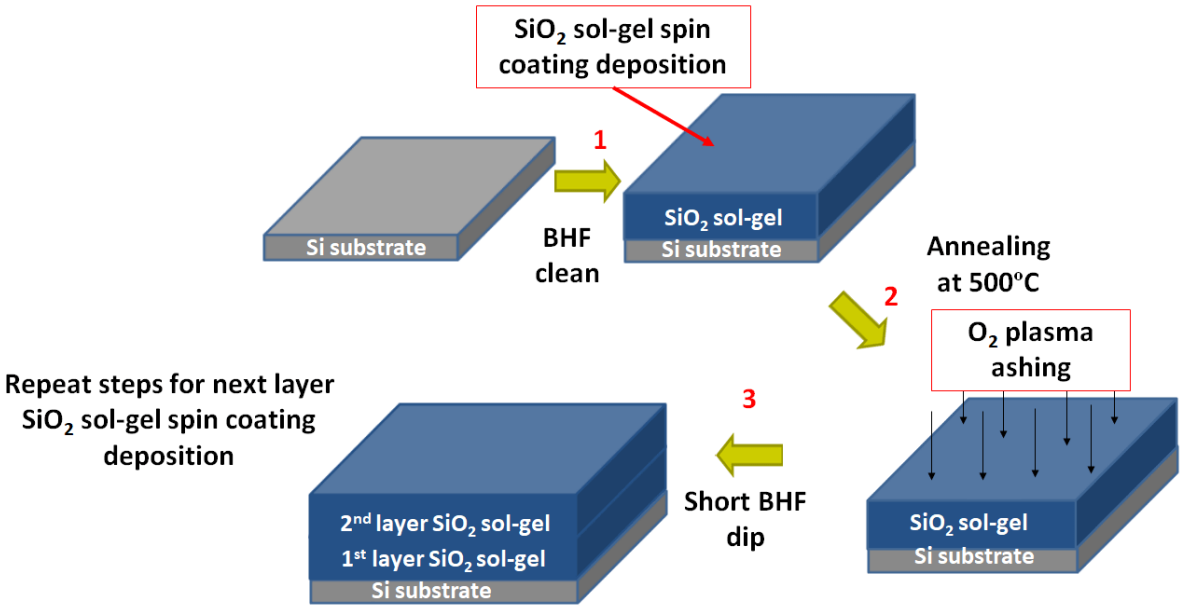


Fig. 3.3: Schematic of the multi-layer sol-gel SiO_2 fabrication process showing Si substrate cleaning by BHF, spin coating deposition of the sol-gel SiO_2, and annealing at 500ºC. This is followed by O_2 plasma ashing and a short BHF dip before stacking on the next sol-gel SiO_2 layer which produces layers that does not peel or crack.

As described in the previous section, two main issues are present when stacking sol-gel SiO_2. The first issue is the appearance of cracks on the sol-gel SiO_2 layer and the second issue is the peeling of the sol-gel SiO_2 layer. Both of these issues causes the sol-gel SiO_2 to not be stackable and prevents the fabrication of the cladding and passivation layers. The methods in order to eliminate the cracking and peeling issues are addressed separately in the following sections.

3. 4. Eliminating issues in multi-layer sol-gel SiO_2 stacking

3.4.1 Eliminating crack issues in sol-gel SiO_2

In order to reduce cracks on a single SiO_2 layer, the thickness of each stacking layer must be controlled to be 0.7 µm by regulating the spin coating rotation speed. From our previous estimations, the critical thickness where we see cracks occurring is around 0.8 µm and from Eqs. 3.1 and 3.2, this relates to an estimated intrinsic stress of 4.30 MPa which is caused by the difference in the thermal expansion of the single layer sol-gel SiO_2 and the Si substrate where the thermal expansion coefficient of sol-gel SiO_2 is much smaller at 0.55×10^{-7} K^{-1} compared to Si which is 3.6×10^{-6} K^{-1}. By terminating the thickness of the 1st sol-gel SiO_2 layer to be 0.7 µm (below the 0.8 µm critical thickness), we control the estimated intrinsic stress to be around 3.4 MPa and then stack the 2nd layer on top of the first layer. When stacking the next sol-gel SiO_2 layer, the intrinsic stress of the 2nd layer is estimated to be 0.8 MPa for a 2nd layer thickness of 0.7 µm. The estimated intrinsic stress is lower because we believe it is due to the similar thermal expansion of the 2nd sol-gel SiO_2 layer and the bottom 1st layer. Similarly, successive stacking of the 3rd, 4th and 5th sol-gel SiO_2 layers stacked on top of one another is illustrated in Fig. 3.4 below which shows the estimated intrinsic stress in each stacked layer. A point to note in our assumption is that the estimated intrinsic stress for each layer starts at approximately 0.47 MPa due to shrinkage of the sol-gel SiO_2 layer during the annealing process which causes an initial stress [28]. Note also that the stress in the first layer may increase

and cracks may occur in the first layer after multi-layer stacking while Fig. 3.4 shows only the stress after stacking. It is also observed in Fig. 3.4 that the maximum stress is different even among the 2nd to 5th layers. This is because as more layers are stacked, the effect of the thermal expansion between the Si substrate and the top most layer becomes less due to the greater distance between the Si substrate and top layer which reduces the maximum stress at the top stacked layer. By using multi-layer stacking of 0.7 μm per layer and stacking 5 layers successively, the total thickness of the sol-gel SiO_2 layer is increased up to greater than 3.0 μm and the estimated intrinsic stress is controlled to ensure that no cracks will occur in the sol-gel SiO_2 layer.

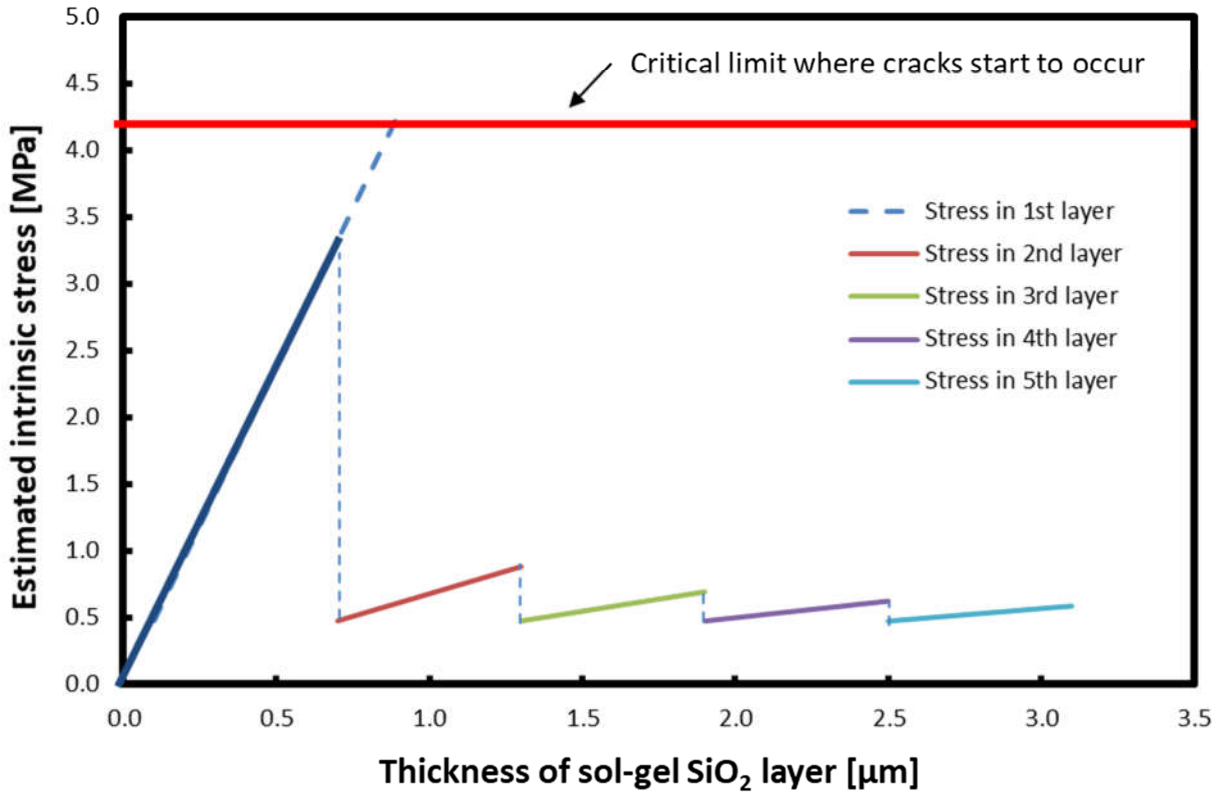
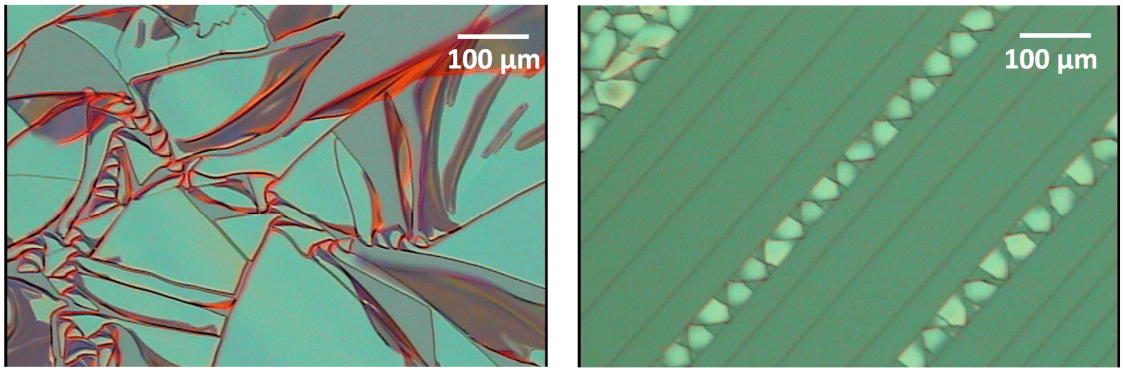


Fig. 3.4: Estimated intrinsic stress at different layers of sol-gel SiO_2. Our initial experiments showed that cracks started to appear for 0.8 µm thick sol-gel SiO_2 layer which corresponds to an estimated intrinsic stress of 4.3 MPa. In order to eliminate cracks, we terminate the 1st layer at 0.7 µm and the estimated intrinsic stress for this 3.32 MPa. The 2nd sol-gel SiO_2 layer has a lower estimated intrinsic stress due to it having a similar thermal expansion coefficient to the lower sol-gel SiO_2 layer. Similarly, the 3rd, 4th and 5th layer stacked on top of one another also has a lower estimated intrinsic stress.

Cracks during fabrication can occur when heating at both low temperature (140°C) and high temperature (500°C). Cracks at low temperature are characterized by non-directional cracks that have no preferred orientation as

shown in an example of Fig. 3.5 (a) below. For the SiO_2 sol-gel on Si fabrication process, we make use of an organic modified precursor, MTES to provide stress relief during the low temperature heating solvent evaporation stage [29]. Meanwhile, cracks at high temperature are directional as shown in Fig. 3.5 (b).



(a) (b)

Fig. 3.5: Example of crack formation on sol-gel layer at (a) low heating temperature (140°C) and at (b) high heating temperature (500°C).

As described in the previous section, the main cause of cracks that appear during the annealing process is due to the difference in thermal expansion coefficient between the sol-gel SiO_2 and the Si substrate. The annealing temperature profile for the high temperature annealing stage is as shown in Fig. 3.6.

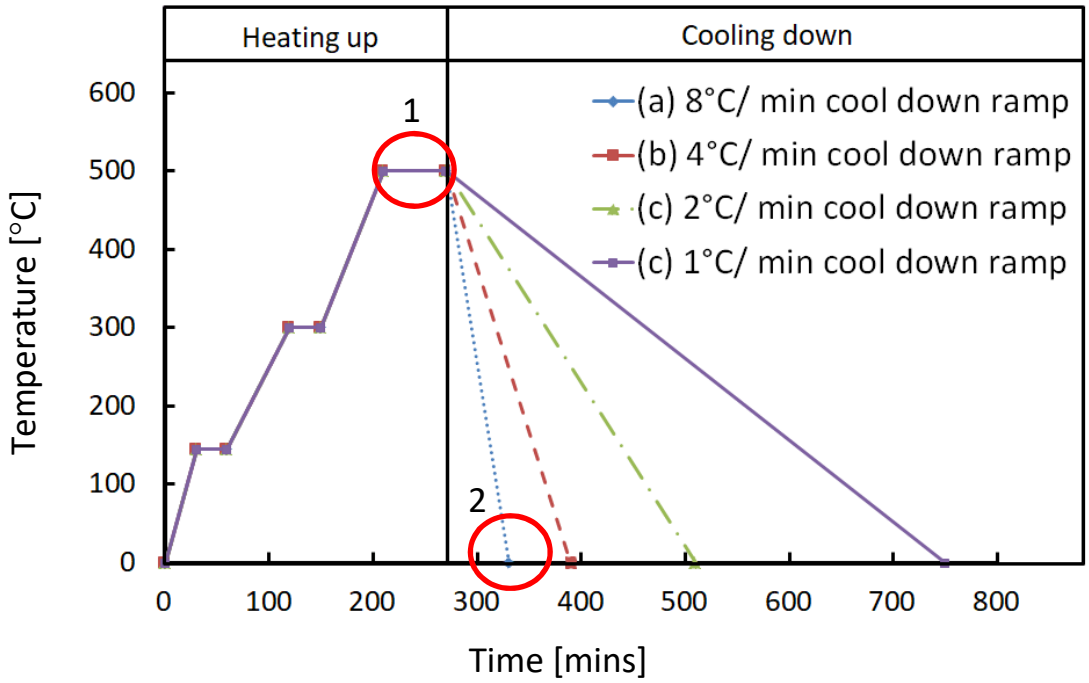


Fig. 3.6: High temperature annealing profile for SiO_2 in the thermal annealer showing the heating up stage and the cooling down stage with cooling down ramps of (a) 8°C/min, (b) 4°C/min, (c) 2°C/min and (d) 1°C/min.

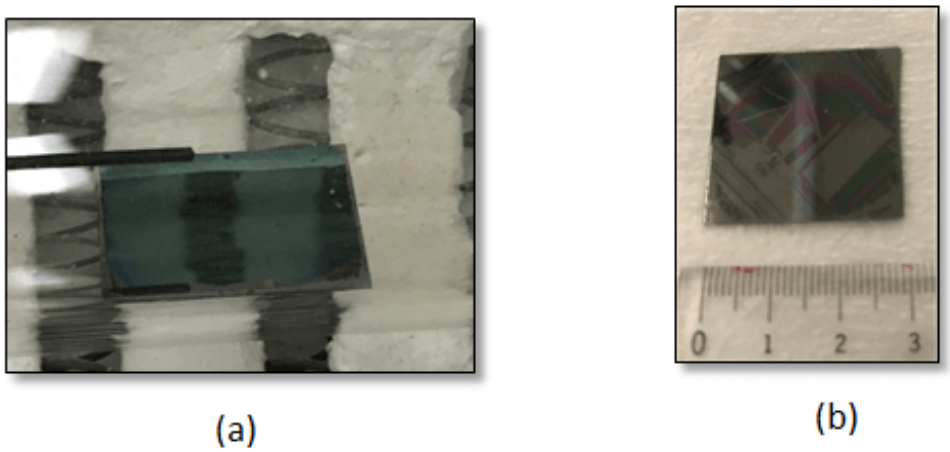


Fig. 3.7: SiO_2 sol-gel on Si substrate sample at (a) maximum annealing temperature (position 1 in Fig 3.5) showing no cracks while (b) sample with 8°C/min cool down ramp (position 2 in Fig. 3.5) showing cracks across the whole sample

During the heating up stage, the sample undergoes stress due to densification. This thermal stress can lead to cracks especially if the layers have a large difference in thermal expansion coefficient [30]. Therefore, in order to minimize and eliminate the cracks, the subsequent layers stacked on top ideally should have a small difference in thermal expansion coefficient compared to the lower layers. We do not observe any cracks during the heating up stage as shown in Fig. 3.7 (a). Images of the sample at the maximum heating temperature do not show any evidence of cracks. This is because during the heating up process, the SiO_2 layer is still not fully cured yet. Therefore, there is no stress on the SiO_2 layer up to the maximum heating up temperature.

Cracks were only observed on the SiO_2 layer when cooling the sample from the maximum annealing temperature down to room temperature. Figure 3.7 (b) shows the appearance of cracks on the sample based on an 8°C cool down ramp. During the cooling down stage, thermal stress that was generated and accumulated in the SiO_2 layer is released, and due to the thermal coefficient difference between SiO_2 and Si gives rise to the formation of cracks. This formation of cracks however can be reduced by controlling the cooling down ramp of the SiO_2 layer. Figure 3.8 shows the microscope view of the cracks on the SiO_2 surface when the sample was cooled down from maximum heating temperature down to room temperature by different cooling down ramps.

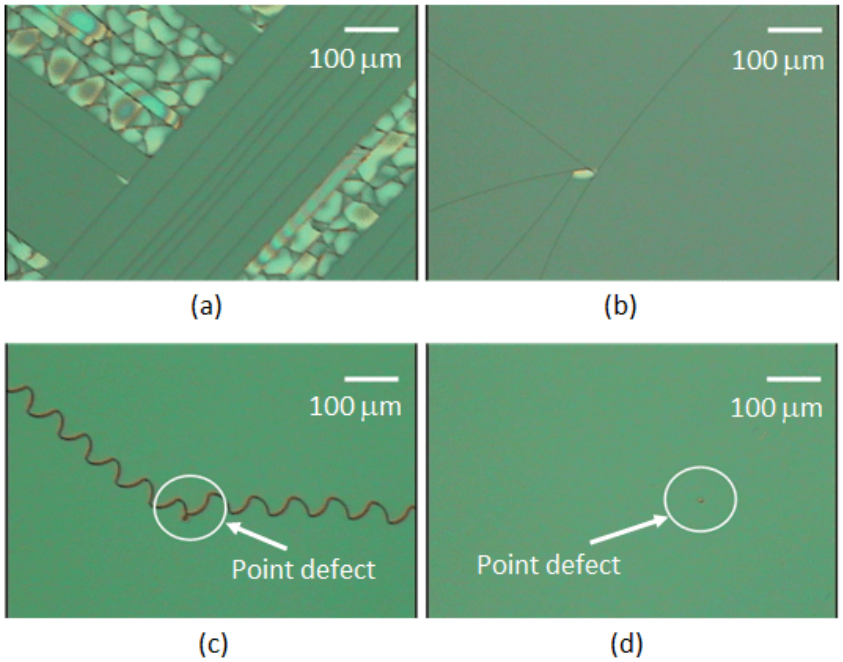


Fig. 3.8: Surface of SiO_2 sol-gel on Si where the cooling down ramp was (a) 8°C/min, (b) 4°C/min, (c) 2°C/min and (d) 1°C/min.

Figure 3.8 (a) shows multiple oriented cracks and delamination of the SiO_2 sol-gel layer when cooling down at a rate of 8°C/min which appears over the whole sample. Slowing the cooling rate down to 4°C/min in Fig. 3.8 (b) produces lesser cracks that still occur over the whole sample but no delamination is observed. Figure 3.8 (c) with a rate of 2°C/min shows only zig-zag cracks that originate from point defects on the SiO_2 surface and is significantly less than in Fig. 3.8 (a) and Fig. 3.8 (b). Finally, Fig. 3.8 (d) with a cooling down rate of 1°C/min shows no cracks on the surface even ones originating from point defects. The appearance of the zig-zag cracks as shown in Fig. 3.8 (c) can be attributed to stress that accumulates at the defect point and then propagates through the sample in order to release the stress during the cooling down stage.

Table 3.1 Results of cracks density for different annealing cooling down ramps

Annealing cooling down ramp (°C/min)	8	4	2	1
Crack density (μm^2)	69.5	14.2	8.6	0.0

3.4.2 Eliminating peeling issues in sol-gel SiO_2 multi-layer stacking

For the peeling issue, it was determined that a polymer layer appears on top of the sol-gel SiO_2 layer during the annealing process which has a lower work of adhesion (4.87×10^{-20} J/m^2) compared to SiO_2 (6.55×10^{-20} J/m^2). In order to eliminate the peeling issue, a number of different experimental processes were carried out to determine the best parameters to achieve two layers stacking with no peeling effect as is elaborated below. The results are as described in Table 3.2.

Process 1: 2nd sol-gel SiO_2 layer spin coated directly on top of the 1st sol-gel SiO_2 layer and both layers were annealed together at 500°C for 120 mins.

Process 2: 1st sol-gel SiO_2 layer annealed at 500°C for 120 mins and 2nd sol-gel SiO_2 layer spin coated on top and then annealed at 500°C for 120 mins.

Process 3: 1st sol-gel SiO_2 layer annealed at 500°C for 120 mins, the layer was then subjected to O_2 plasma ashing for 200 sec before annealing again at 500°C for 120 mins. Similarly, the 2nd sol-gel SiO_2 layer was spin coated and annealed at 500°C for another 120 mins followed by O_2 plasma ashing for 200 sec and annealed again at 500°C for 120 mins.

Table 3.2: Results of processes for two layer stacking of sol-gel SiO_2

	Process 1	Process 2	Process 3
Total annealing time at 500°C (mins)	120	240	480
O_2 plasma ashing between layers (secs)	None	None	200
Crack density (μm^2)	47	18	0
Sample ratio of peeling (%)	100	78	0

The top and side view for process 1,2 and 3 are as shown in Fig. 3.9 (a) - (c) below. The thickness of process 1 is 1.78 µm, thickness of process 2 is 1.28 µm, and thickness of process 3 is 1.15 µm. Cracks and peeling can be seen for process 1and 2 in Fig. 3.9 (a) and (b).

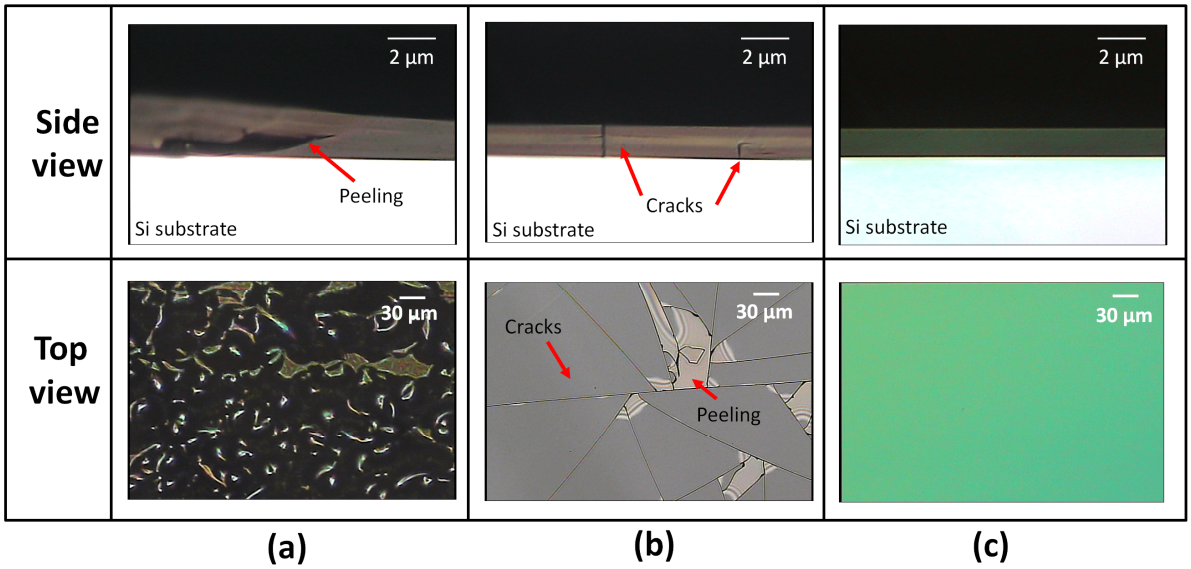


Fig. 3.9: Side and top views of samples with 2 layers of stacked sol-gel SiO_2 fabricated by using: (a) Process 1 showing peeling of both layers across the whole sample, (b) Process 2 showing cracks propagating from the lower layer and (c) Process 3 showing no peeling or cracks on both sol-gel SiO_2 layers

When stacking two layers sol-gel SiO_2, our experiments have shown that a polymer layer appears at the top of the sol-gel SiO_2 layer during the annealing stage. This polymer layer is expected to materialize from the precursor materials used [31] where this layer reduces the surface adhesion due to the lower work of adhesion and is observed in Fig. 3.9 (b) of process 2. The polymer layer is expected to have a lower work of adhesion of 4.87×10^{-20} J/m^2 and this is lower than the SiO_2 work of adhesion of 6.55×10^{-20} J/m^2. Complete removal of this polymer layer is required in order to increase adhesion and eliminate peeling.

The annealing in process 3 was developed to eliminate the peeling issue where it was identified that removal of the polymer layer was required before stacking on the next sol-gel SiO_2 layer. In order to accomplish this, an O_2 plasma step was introduced to remove the polymer layer for surface conditioning. After firstly annealing the sample at 500°C, the sample was then subjected to O_2 plasma ashing in order to remove the polymer layer that has formed on the top surface. Subsequently, the annealing process was then repeated once again in order to completely densify the sol-gel SiO_2 layer and followed by O_2 plasma ashing again to remove any polymer layer that may appear again.

For two layer stacking of SiO_2, the thickness at each step of the process is as shown in Fig. 3.10 (a) - (c). The thickness of the SiO_2 was initially 0.76 µm. It was observed that the thickness of the sol-gel SiO_2 layer was reduced from 0.76 µm down to 0.70 µm after the annealing and O_2 plasma ashing process.

Similarly, Fig. 3.10 (c) shows the thickness of a two layer stacking of sol-gel SiO_2 after the annealing and O_2 plasma ashing which is 1.15 µm. Nevertheless, it is necessary to stack more than 1.15 µm for the purpose of optical confinement to avoid leakage into the substrate. To achieve greater thickness, the multi-layer stacking of sol-gel SiO_2 is shown in the following section.

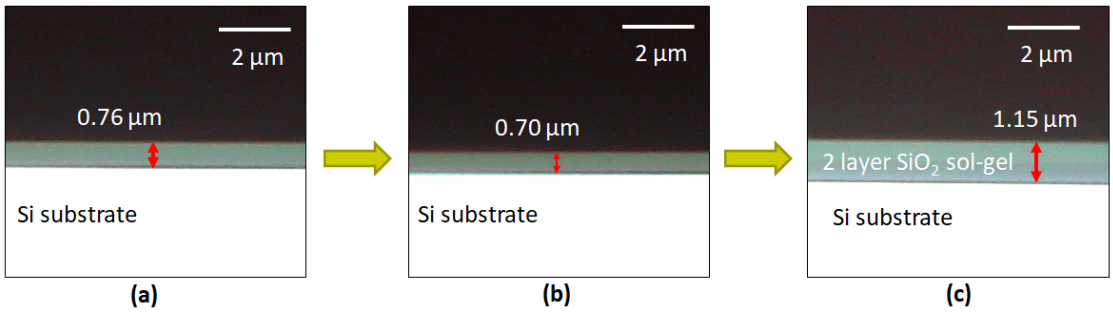


Fig. 3.10: The thickness of a sol-gel SiO_2 throughout the two layers stacking (a) initial thickness of starting at 0.76 µm after spin coating, (b) the sol-gel SiO_2 thickness reduces to 0.70 µm after annealing at 500°C and O_2 plasma ashing, (c) a two layer sol-gel SiO_2 stacking with thickness of 1.15 µm thickness after the same annealing and O_2 plasma.

3. 5. Multi-layer stacking towards thicker sol-gel SiO_2 layer

In order to achieve a thicker sol-gel SiO_2 layer, multiple layers need to be stacked on top of one another. The main issues seen during the stacking process as previously described are peeling and cracks of the deposited multi-layer stacked SiO_2 as was shown in Figs. 3.1 and 3.2. The crack issue

occurs due to the mechanical stress that builds up during the fabrication process when it exceeds the sol-gel's ability to elastically respond. Meanwhile, the peeling issue can completely detach the upper SiO_2 layer from the lower SiO_2 layer and this can happen on any layer during the fabrication process. The previous sections has described the cracking and peeling mechanisms and the steps required to overcome these issues.

In our experiment, by using multi-layer stacking of sol-gel SiO_2, it was successfully confirmed that crack and peeling free layers of 3.5 µm thickness was achieved as shown in Fig. 3.11 below. Fig. 3.11 (a) shows a single layer SiO_2 with 0.7 µm thickness, Fig. 3.11 (b) shows a 2 layer sol-gel SiO_2 with 1.15 µm thickness, Fig. 3.11 (c) shows a 4 layer SiO_2 with 2.31 µm thickness and Fig. 3.11 (d) shows a 6 layer SiO_2 with 3.52 µm thickness.

Compared to the single thick layer sol-gel SiO_2 of 1.9 µm shown previously in Fig. 3.1, we do not observe any cracks and peeling even for the 4 and the 6 multi-layer stacking shown in Fig. 3.11 (c) and 3.11 (d) which has a much thicker layer of 2.31 µm and 3.52 µm. We believe that by limiting the thickness of a single layer to 0.7 µm where we estimate the intrinsic stress to be less than 3.32 MPa, we effectively stack multi-layer sol-gel SiO_2 to achieve an overall greater thickness. There have been other reports that describe a multi-layer stacking having increased strength and rigidity due to the chemical bond formation between thin layers [29] which explains why the multi-layer scheme is able to exceed the crack and peel free thickness of a single layer. Therefore, it has been shown that by employing a multi-layer

stacking scheme, the thickness of the sol-gel SiO_2 is increased to achieve crack and peel free layers to be used as optical waveguide cladding and passivation layers.

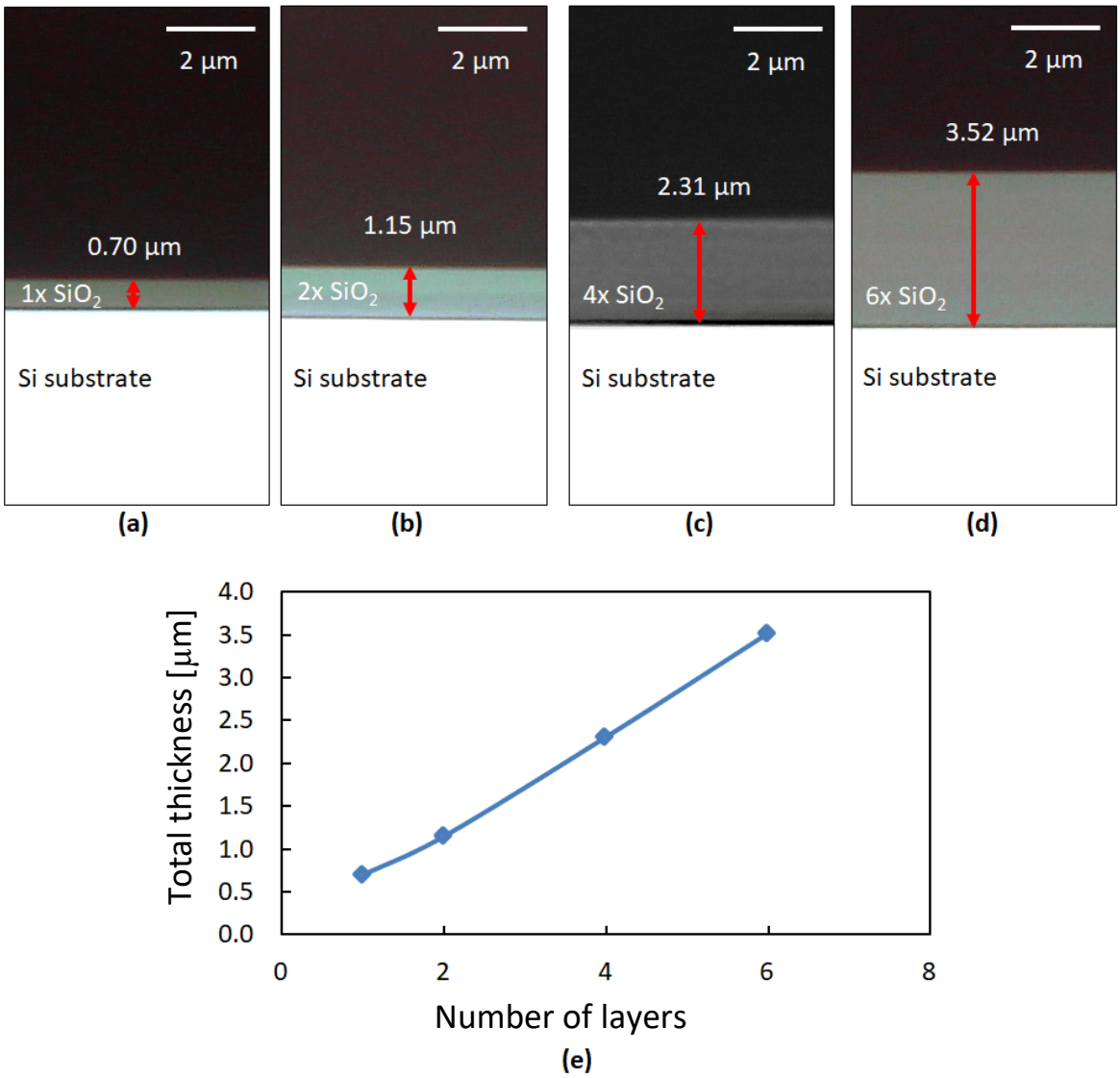


Fig. 3.11: Thickness of the sol-gel SiO_2 for (a) single layer (0.70 µm), (b) two layers (1.15 µm), (c) four layers (2.31 µm), (d) six layers (3.52 µm), and (e) graph showing the total thickness of sol-gel SiO_2 as a function of the number of layers deposited by spin coating.

3. 6. Resistivity measurement and refractive index of sol-gel SiO_2

In order to evaluate the characteristics of the sol-gel SiO_2, the refractive index was measured using an ellipsometer. The ellipsometer available can only conduct measurement at 632.8 nm wavelength. For a six layer sol-gel SiO_2 showed a refractive index of 1.42. This slightly lower refractive index compared to SiO_2 deposited by other methods can be attributed to the porosity of the sol-gel SiO_2 based fabrication process [32].

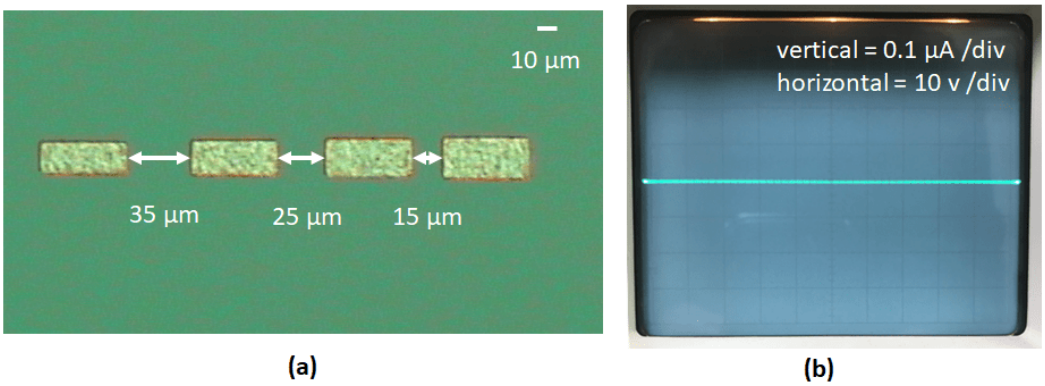


Fig. 3.12: Resistivity measurement of sol-gel SiO_2 (a) TLM structure of metal contacts with varying distances of 15 µm, 25 µm and 35 µm and (b) curve tracer results showing <0.1 µA at 100 V for all metal contact distances even at the closest metal contact of 15 µm indicating resistivity measurement of >6.6×10^{13} Ω.

In order to evaluate the suitability of the sol-gel SiO_2 as a passivation layer, metal contacts were deposited in a transfer length method (TLM) structure as shown in Fig. 3.12 (a) above to measure the resistivity. IV measurements were carried out and Fig. 3.12 (b) shows the IV curve tracer output at the limit of our measurement setup with an obtained resistance of $1x10^9$ Ω.

This high resistivity makes the sol-gel SiO_2 layer suitable as a passivation layer for optical and electronic devices [33]. A summary of the characteristics of a six layer sol-gel SiO_2 is as described in Table 3.2 below.

Table 3.3: Characteristics for a six layer sol-gel SiO_2

	Thickness (µm)	Surface resistivity (Ω)	Refractive index
SiO_2 sol-gel	3.5	$>6.6 \times 10^{13}$	1.42

3. 7. Stacking different materials on sol-gel SiO_2 as core layer

In order to evaluate the suitability of the developed SiO_2 sol-gel layer as a cladding layer, a number of different materials were experimented on as the core layer on top of the sol-gel SiO_2 to realize an optical waveguide. Our initial experiments made use of different sol-gel materials stacked on top of the sol-gel SiO_2 to try to achieve an all sol-gel process to fabricate optical waveguide. Later on, different core materials deposited through the sputtering process were also experimented on. The core materials experimented on were: sol-gel TiO_2, sol-gel ZnO, sputtered SiN and sputtered amorphous silicon and these were all stacked on top of the sol-gel SiO_2 cladding layer. A summary of the materials used, the refractive index, the critical thickness to maintain fundamental mode, the effective index for 100 nm and 200 nm core layer thickness as well as the required thickness of the SiO_2 cladding layer to maintain >99% optical confinement are as described in the following Table 3.4. It can be seen that for lower refractive index core, a thicker cladding layer is required. Similarly, if the core layer is thinner, a much thicker cladding layer is also required to maintain > 99% optical confinement.

Table 3.4: Characteristics of different core layers stacked on top of sol-gel SiO

Material	Sol-gel SiO_2	Amorphous Si	SiN	Sol-gel TiO_2	Sol-gel ZnO
Usage	Cladding layer	Core layer	Core layer	Core layer	Core layer
Refractive index	1.44	3.0	1.99	2.43	1.92
Critical thickness to maintain fundamental mode	-	294 nm	563 nm	395 nm	605 nm
For a core layer thickness of 100 nm					
Effective refractive index		1.87	1.485	1.473	1.473
Cladding layer thickness		1.79 µm	5.94 µm	6.92 µm	6.92 µm
For a core layer thickness 200 nm					
Effective refractive index		2.32	1.579	1.547	1.547
Cladding layer thickness		1.16 µm	3.32 µm	3.80 µm	3.80 µm

3.7.1 Sputtered a-Si as core layer

In order to evaluate the suitability of the developed SiO_2 sol-gel layer as a cladding layer, an amorphous-Si (a-Si) layer with a refractive index of approximately 3.0 was sputtered on top of the sol-gel SiO_2 to form a waveguide core layer.

The parameters for the a-Si sputtering process was as follows:

Main pressure (Torr)	1.6×10^{-2}
Ar gas flow rate (sccm)	20.0
Plasma power (W)	500
Temperature (°C)	250
Sputtering time (mins)	16

For an a-Si core layer thickness of 200 nm, a thin SiO_2 cladding layer will cause light to leak from the core into the substrate. Therefore, simulation as shown in Fig. 3.13 (a) for an SiO_2 cladding layer of 1.9 µm is shown to be sufficiently thick enough to confine all light to within the core with no leakage into the substrate. To achieve 1.9 µm thickness, a 3 layer sol-gel SiO_2 deposition is sufficient. Figure 3.13 (b) shows the facet of the fabricated a-Si core with thickness of 200 nm, waveguide width of 4 µm and 3 layers of sol-gel SiO_2 bottom cladding layer with a thickness of 1.9 µm. The optical measurements were carried out using a cut-back method at 1550 nm wavelength for different lengths. Figure 3.13 (c) shows the optical field profile for the 4 µm width waveguide and fig. 3.13 (d) plots the measured output light power as a function of the waveguide length. The propagation loss was determined to be 10.1 dB/cm. The higher loss of this structure can be attributed to the unoptimized a-Si sputtering parameters. In order to reduce the loss, better hydrogen passivation of the dangling bond defects in the a-Si core is required as has been reported in literature [34]. Nevertheless,

the ability to sputter a-Si directly onto the developed sol-gel SiO_2 layer and optical loss measured demonstrates the sol-gel SiO_2's capability and potential to be used as a cladding layer for optical waveguides.

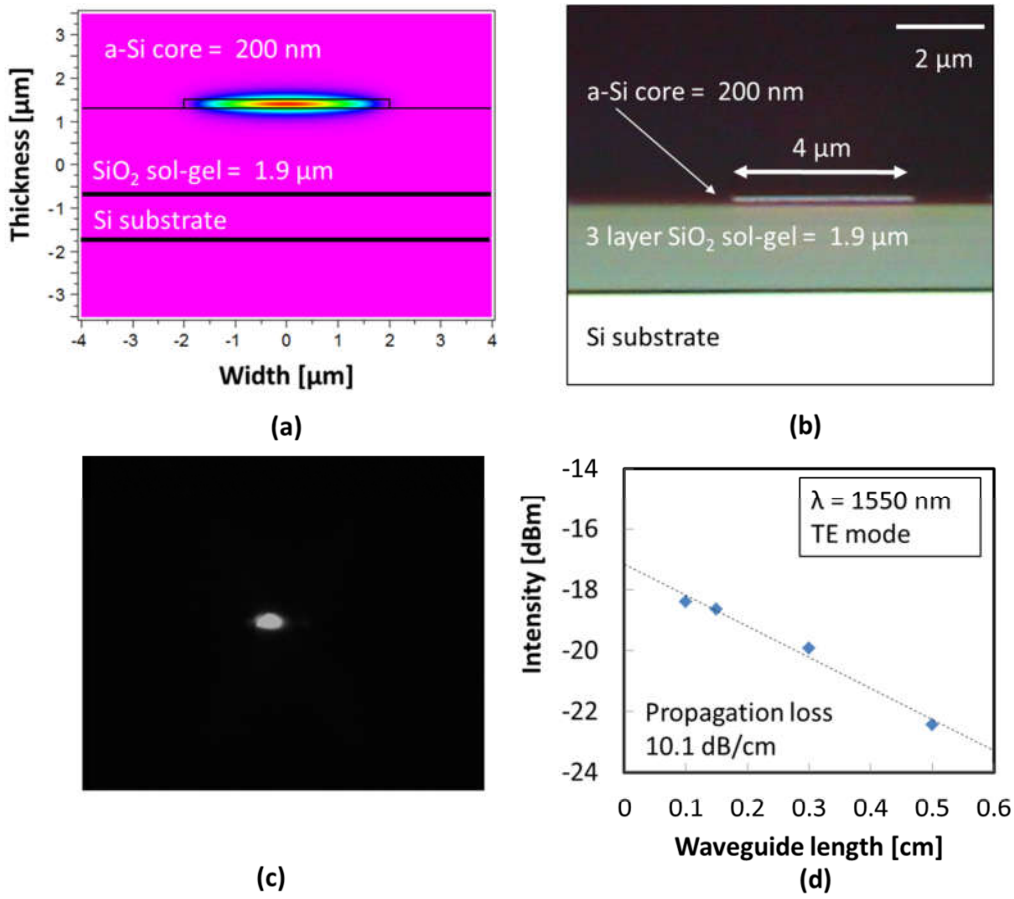


Fig. 3.13: Amorphous si core layer on sol-gel SiO_2 cladding layer waveguide: (a) simulation for a 200 nm a-Si core layer on 1.9 µm SiO_2 sol-gel cladding layer showing no leakage of light into the substrate, (b) facet view of fabricated 4 µm width a-Si waveguide on 3 layer sol-gel SiO_2 of 1.9 µm thickness, (c) optical field profile for the 4 µm width a-Si on sol-gel SiO_2 waveguide and (d) output light power for waveguides of different lengths with propagation loss of 10.1 dB/cm.

Our measured propagation loss of 10.1 dB/cm for sputtered a-Si is comparable to other reported values for a-Si waveguides which has been reported to be between 4.5 dB/cm [35] to 14 dB/cm [36]. By using PECVD hydrogenated amorphous silicon (a-Si:H), all dangling bonds are saturated with hydrogen and a low propagation loss of between 0.5 dB/cm to 2.0 dB/cm has been demonstrated [37]. Therefore, it is expected that by employing a similar a-Si:H core layer on top of our developed sol-gel SiO_2 cladding layer, a much lower loss is achievable.

3.7.2 Sputtered SiN as core layer

SiN is a material with a refractive index of 1.99. In this experiment, SiN was stacked onto the sol-gel SiO_2 using sputtering technique.

The SiN sputtering deposition parameters are:

Main pressure (Pa)	1.2×10^{-1}
Ar gas flow rate (sccm)	16.0
N_2 gas flow rate (sccm)	3.0
Plasma power (W)	500
RF power (W)	500
Sputtering time (mins)	35

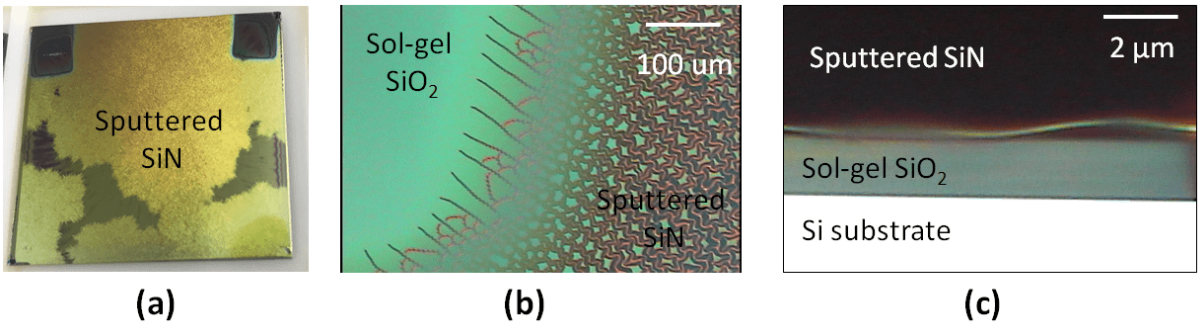


Fig. 3.14: Sputterd SiN on sol-gel SiO_2 where (a) whole sample of 3cm x 3cm sputtered SiN on top of sol-gel SiO_2 after 20 mins removed from sputterer, (b) top view of sputtered SiN layer showing buckling characteristics on sputtered SiN layer while sol-gel SiO_2 layer shows no damage and (c) side view of sputtered SiN layer showing buckling.

As shown in Fig. 3.14, the SiN layer undergoes compressive stress and this is evident from the buckling characteristics seen in Fig. 3.14 (b) and (c). The compressive stress in SiN has been reported to be up to 200 MPa while stress reduction techniques has been reported for PECVD deposited SiN [38] and this may be a possible option for stacking SiN on top of sol-gel SiO_2.

The Fig. 3.15 below shows the difference in characteristic between tensile stress as is seen during the development of the sol-gel SiO2 layer and compressive stress as is seen when depositing the SiN on top of the sol-gel SiO2 layer. Tensile stress which manifests itself in cracks and is seen in Fig. 3.15 (a) while compressive stress manifest itself in buckling or worm tracks as seen in Fig. 3.15 (b)

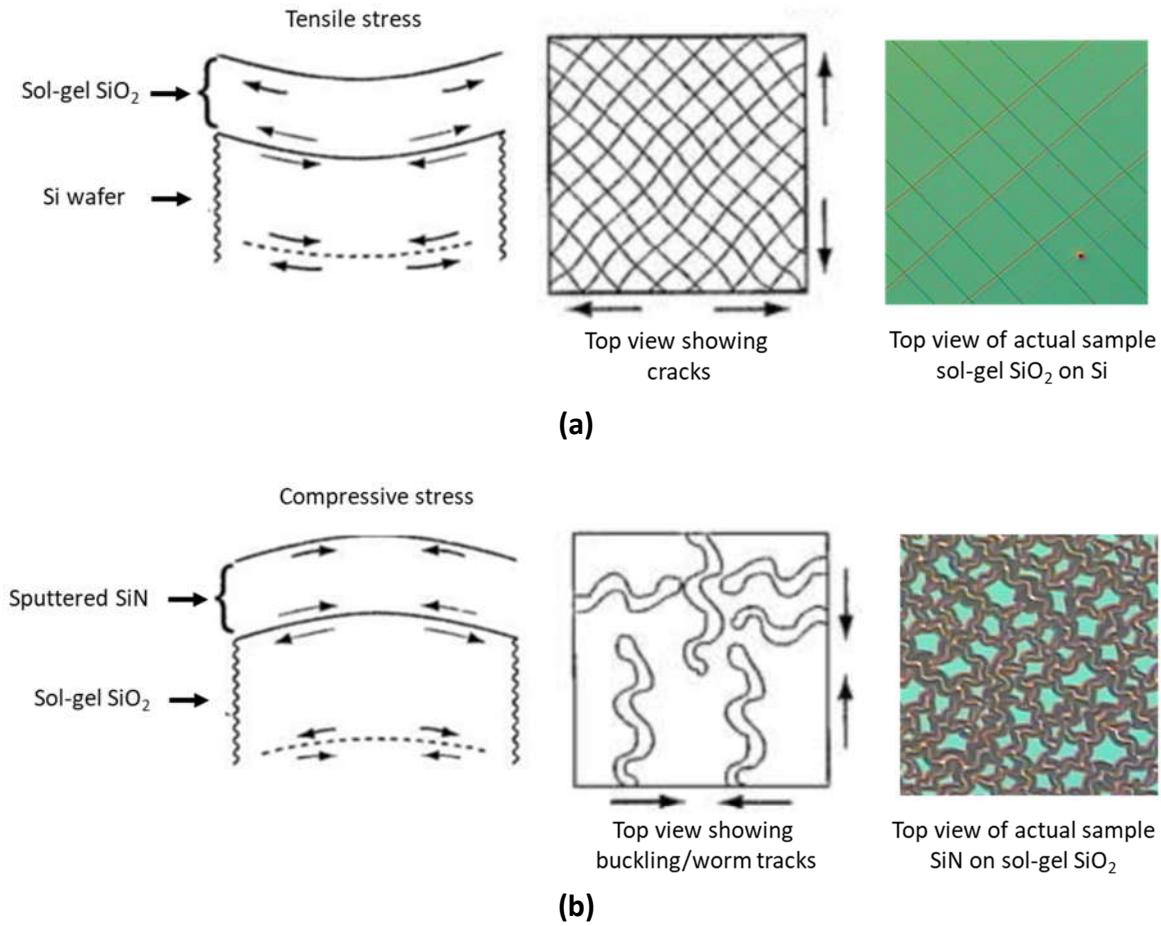


Fig 3.15: Comparison between (a) tensile stress seen during development of sol-gel SiO_2 which manifests in cracks against (b) compressive stress as seen during sputtering of SiN on top of sol-gel SiO_2 which manifests itself in buckling or worm tracks.

3.7.3 Sol-gel ZnO as core layer

ZnO is a material with high refractive index of 1.92 which has also been demonstrated as optical waveguide through sputtering deposition. For the sol-gel ZnO, the ZnO chemical precursor was procured from Kojunda Chemicals. The sol-gel Zn O was spin coated onto the sol-gel SiO_2 cladding layer at various spin coater rpm speeds and heated on a hot plate up to

350°C to stabilize the layer. For sol-gel ZnO, a number of published results have been presented. However, majority of the sol-gel ZnO layers were stacked directly onto glass or quartz substrates. In our work, we attempt to stack sol-gel ZnO onto sol-gel SiO_2 to develop an all sol-gel fabrication technique.

A review of sol-gel ZnO on the different substrates, the heat treatments applied and the obtained layer thickness are as follows in Table 3.5.

Table 3.5: Substrate, annealing parameters and obtained thickness for sol-gel ZnO

Author	Substrate type	1^{s} annealing treatment (°C)	2nd annealing treatment (°C)	ZnO thickness (nm)
Liu, et al. [39]	Glass	100	500	220
Kumar et al. [40]	Si	250	350-450	250
Bao et al. [41]	Quartz	300	450-600	300
Bole et al. [42]	Glass	300	300-425	275-375
Brenier et al. [43]	Si	80	250	20-60
Peterson et al. [44]	Si, quartz	300	700	180
Raoufi et al. [45]	Glass	250	300-500	500
Lin et al. [46]	Si, glass	300	450-550	280
Mridha et al. [47]	Glass	120	550	260
Dutta et al. [48]	Glass	350	550	36-247
Basak et al. [49]	Sapphire	120	550	300
Zhang et al. [50]	Si	120	600	434
Ohyama et al. [51]	Silica	300	600	100-260
Fujihara et al. [52]	Glass	400-500	400-500	200
Kokubun et al. [53]	Silica, Sapphire	90 300	500 600	150
Delgado et al. [54]	Glass	100	200-600	450
Ohya et al. [55]	Glass	110	600	11-33

In our experiments, we were unable to etch the ZnO layer either through dry etching or wet etching. Experiments conducted using the available SF_6, CHF_3

and C_3F_8 gasses did not etch the ZnO layer at all. For wet etching, a number of acids were trialled. HCl acid and acetic acid was found to not etch the layer while BHF etching removed the lower SiO_2 cladding layer before the ZnO layer could be etched. Due to this limitation, a ridge waveguide structure was designed to characterize the sol-gel ZnO layer. A ridge waveguide is a structure consisting of a bottom cladding layer, a core layer and an etched top rib cover layer as shown in Fig. 3.16 below. The refractive index of the core layer is higher than the bottom cladding and top cover layer thus confining light in the vertical direction. By adjusting the ridge width, *2a*, height of the rib over, *h*, and height of etched cover layer, *t*, light can be confined to within the ridge structure.

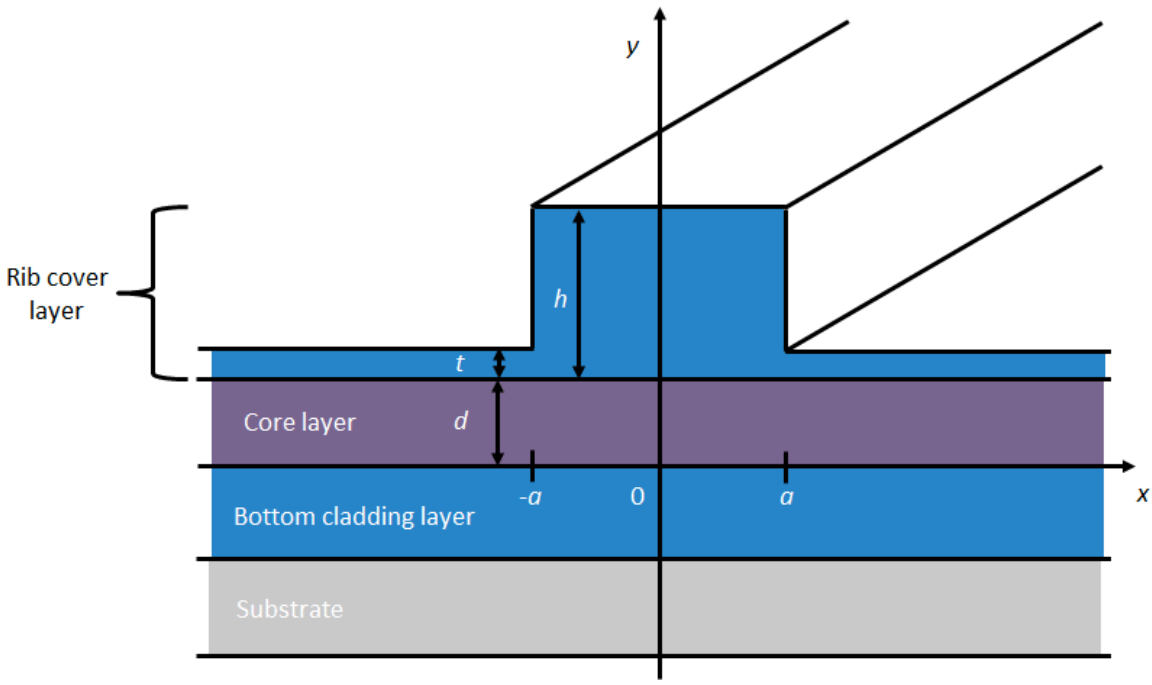


Fig. 3.16: Ridge waveguide structure with width of *2a*, core layer height of *d*, rib cover layer height of *h* and etched rib cover height of *t*.

The ridge waveguide structure is difficult to analyse by Mercatili's method or Kumar's method of division of the waveguide [56]. By following the work of Okamoto [57], in order to analyse the ridge waveguide structure, numerical methods should be used such as finite element method or the effective index method. The effective index method is as described in Appendix B following the work of Okamoto. Essentially, the effective refractive index for the area under the ridge is higher effective refractive index of the surrounding area as shown in Fig. 3.17 below where $n_{eff}(h) > n_{eff}(t)$.

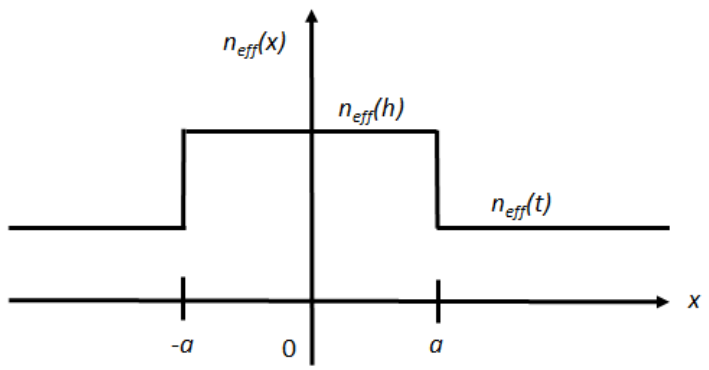


Fig. 3.17: Effective index distribution $n_{eff}(x)$ for area under the ridge *–a>x>a* and the surrounding area *x>a*, *x<-a*

Simulation of the all sol-gel structure was conducted as shown in Fig 3.18. For this simulation, the thickness of the core was set to 300 nm and the rib height was set to 0.5+*t* µm. The waveguide width was varied from 2 µm to 4 µm and the thickness of the etched top cover sol-gel, t, was varied from 0.2 µm to 0.6 µm. With a fixed rib height, *h*, our simulation has shown that the lateral confinement in the core layer is strongly affected by the thickness of the etched top cover layer.

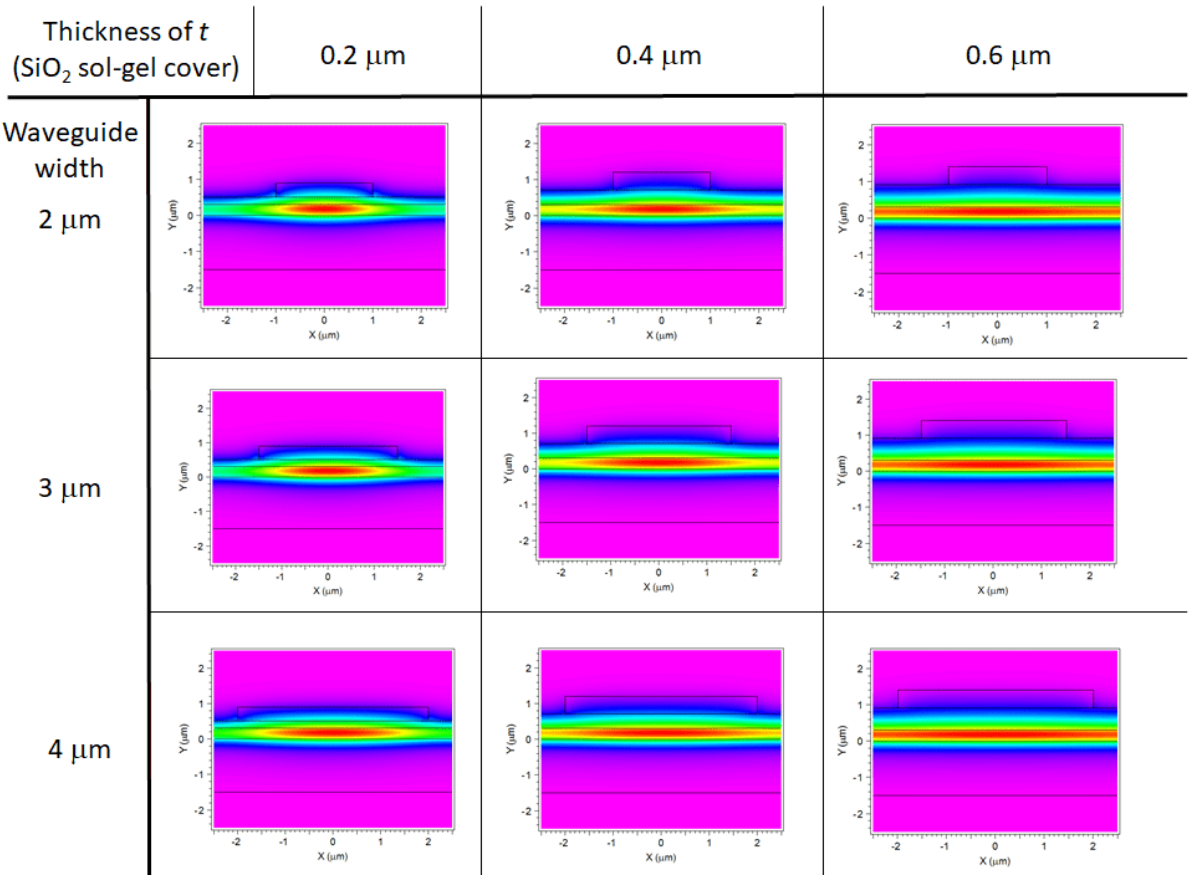


Fig. 3.18: Optical confinement for ridge waveguides with waveguide widths ranging from 2 µm to 4 µm and thickness of *t* (etched portion of top rib cover layer) ranging from 0.2 µm to 0.6 µm. Results show that optical confinement in the lateral direction is strongly dependent on the thickness, *t* of the etched SiO_2 sol-gel cover. Thickness of *t* at 0.6 µm show an almost slab waveguide characteristic with minimal lateral confinement.

The sol-gel SiO_2 layer was fabricated using the same recipe as previous described. For the sol-gel ZnO layer, it was spin coated directly on top the SiO_2 sol-gel layer. After spin coating, the sample was heated on a hot plate in order to stabilize the layer and was inserted into an annealing furnace and heated up to 500°C for 2 hours under vacuum condition. The thickness of the

sol-gel ZnO was found to be only around 150 nm for a single layer, therefore a second sol-gel ZnO layer was spin coated on top of the first layer and annealed using the same parameters. For the top cover layer, the same SiO_2 sol-gel recipe was again used. However, after the hot plate heating stage, the sample was coated in photoresist and waveguide patterns were defined using a mask aligner. The ridge waveguide structure was then etched using a CHF_3 based inductively coupled plasma (ICP). Lastly, the sample was annealed at 500°C for 2 hours under vacuum condition to densify the top SiO_2 sol-gel cover layer. A summary of the fabrication process is as described in Fig. 3.19. The sample was cleaved to different lengths and optical measurement was conducted using a 1.55 µm laser diode as a source. An optical power meter was used to measure the loss through the all sol-gel ridge waveguide structure.

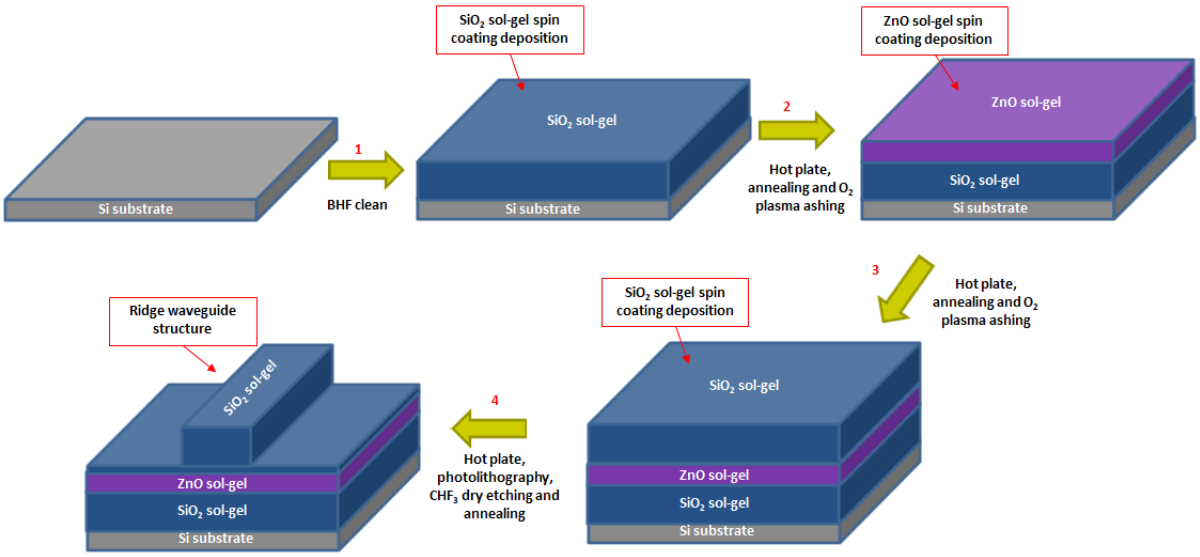
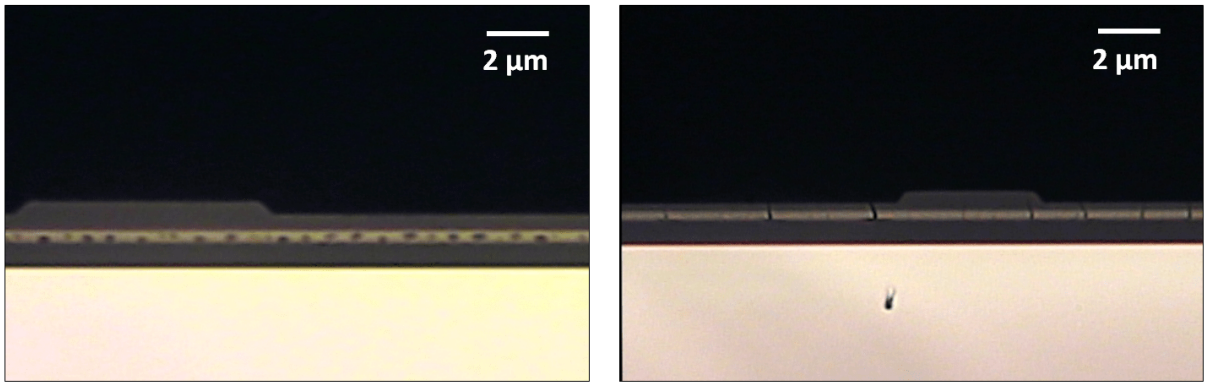


Fig. 3.19: Schematic of the all sol-gel fabrication process showing stacking of SiO_2 sol-gel bottom cladding layer, ZnO sol-gel core layer and SiO_2 sol-gel top cover layer to form the ridge waveguide structure.

The main issue observed with a sol-gel based fabrication technique is the appearance of cracks on the sol-gel layers due to a mismatch of thermal expansion co-efficient. Even though ZnO and SiO_2 sol-gel have a difference in thermal expansion co-efficient, by controlling the cooling down ramp during the annealing process we can minimize the appearance of cracks. Throughout the fabrication process of the all sol-gel ridge waveguide however, other issues were also observed such as described in Fig. 3.20 below. Figure 3.20 (a) shows bubbles forming in the sol-gel ZnO core layer. We believe that the bubbles were due to a residue or polymer layer forming between the ZnO layers which prevents complete solvent evaporation. Experiments conducted to remove this residue layer using the available dry etching or wet etching technique did not give any positive results and the bubbles were still present when stacking multi-layer sol-gel ZnO. Therefore, in order to mitigate the appearance of these bubbles, a single ZnO spin coating step was conducted with a lower spin coating parameter. A downside of this is that the ZnO core layer thickness was limited to 200 nm. Similarly another issue seen in Fig 3.20 (b) shows vertical cracks that originate from between the bottom SiO_2 and ZnO core layer. In order to minimize these vertical cracks of the ZnO core layer, the hot plate heating up stage was increased to 300°C for 2 hours in order to remove the solvent from the layer. Cooling down ramp of the annealing stage for sol-gel ZnO was also set to 1°C/min which aided in reducing the appearance of cracks.



(a) (b)

Fig. 3.20: Issues observed during fabrication of an all sol-gel ridge waveguide which includes (a) bubbles forming within the ZnO core sol-gel layer, (b) vertical cracks origination from the interface between ZnO core sol-gel and SiO_2 bottom sol-gel layer.

Due to the optimization of the fabrication process required to reduce peeling and cracking, a final ridge waveguide structure with the dimensions as shown in Fig. 3.21 (a) was obtained. The SiO_2 bottom cladding sol-gel layer thickness obtained was 0.7 µm, the ZnO core sol-gel layer thickness was 200 nm and the top SiO_2 cover sol-gel thickness of the ridge waveguide was 0.7 µm.

The ridge waveguides were cleaved into samples of 1 mm, 1.5 mm and 3 mm lengths and the optical loss measurements was conducted. An example of the optical field profile obtained for a 3 µm wide ridge waveguide with a 1.5 mm length is as shown in Fig. 3.21 (b) below. Figure 3.20 (c) shows the measured power output from the ridge waveguides with lengths from 1 mm to 3 mm with an average loss α, of 9.6 dB/mm.

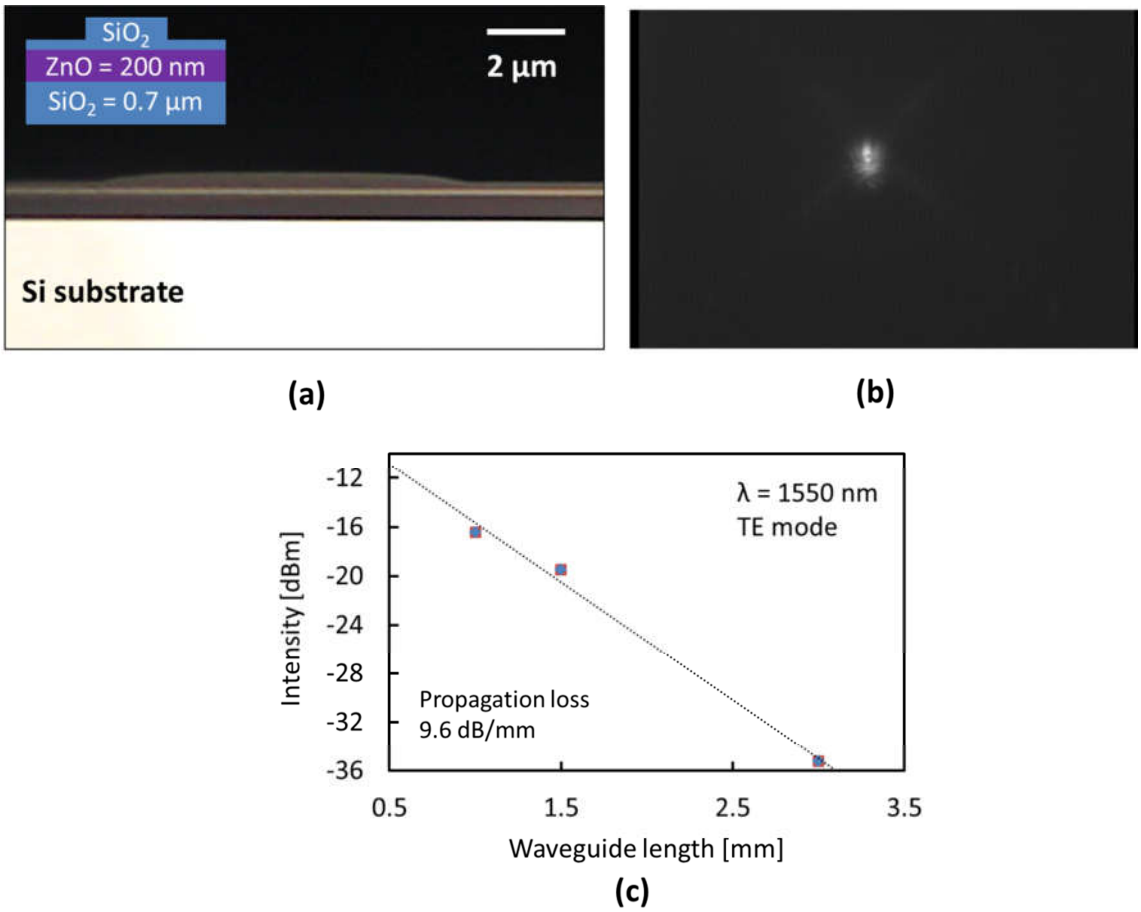


Fig. 3.21: Figures of (a) fabricated all sol-gel ridge waveguide with an SiO_2 bottom sol-gel layer of 0.7 µm, ZnO core sol-gel layer of 200 nm and SiO_2 top cladding sol-gel layer of 0.7 µm on a bulk Si substrate, (b) the optical field profile from the end facet of a 1.5 mm length ridge waveguide and (c) measured power for different waveguide lengths with an average loss of α = 9.6 dB/mm.

For analysis of a ridge waveguide structure, numerical methods such as finite element method and effective index method can be utilized. For the effective index method, the area under the ridge is determined to have a higher refractive index compared to the areas surrounding it. By following the work of Okamoto [57], the dispersion equation can be obtained by;

$$u\tan(u) = \frac{n_{eff}^2(h)}{n_{eff}^2(t)} w \tag{3.9}$$

$$u = ka\sqrt{n_{eff}^2(h) - \left(\frac{\beta}{k}\right)^2} \tag{3.10}$$

$$w = ka\sqrt{\left(\frac{\beta}{k}\right)^2 - n_{eff}^2(t)} \tag{3.11}$$

where n_{eff} (h) is the effective refractive index under the ridge and n_{eff} (t) is the effective refractive index under the surrounding area. The electric field profile can then be determined.

The electric field profile for the ridge waveguide is simulated as shown in Fig. 3.22. Figure 3.22 (a) shows the electric field profile for the current fabrication dimensions showing 17.6% of the optical light absorbed into the Si substrate which causes the high loss currently seen. In order to reduce the % of light absorbed into the Si substrate to below 1%, two possible solutions exists. The first shown in fig 3.22 (b) is by increasing the bottom SiO_2 layer significantly to 3.8 µm thickness. Another solution is shown in fig 3.21(c) where the ZnO core layer thickness is increased to 500 nm and the bottom SiO_2 layer is increased slightly to 2.5 µm. Figure 3.22 (d) indicates the electric field profile for the current fabrication method and for these two scenarios.

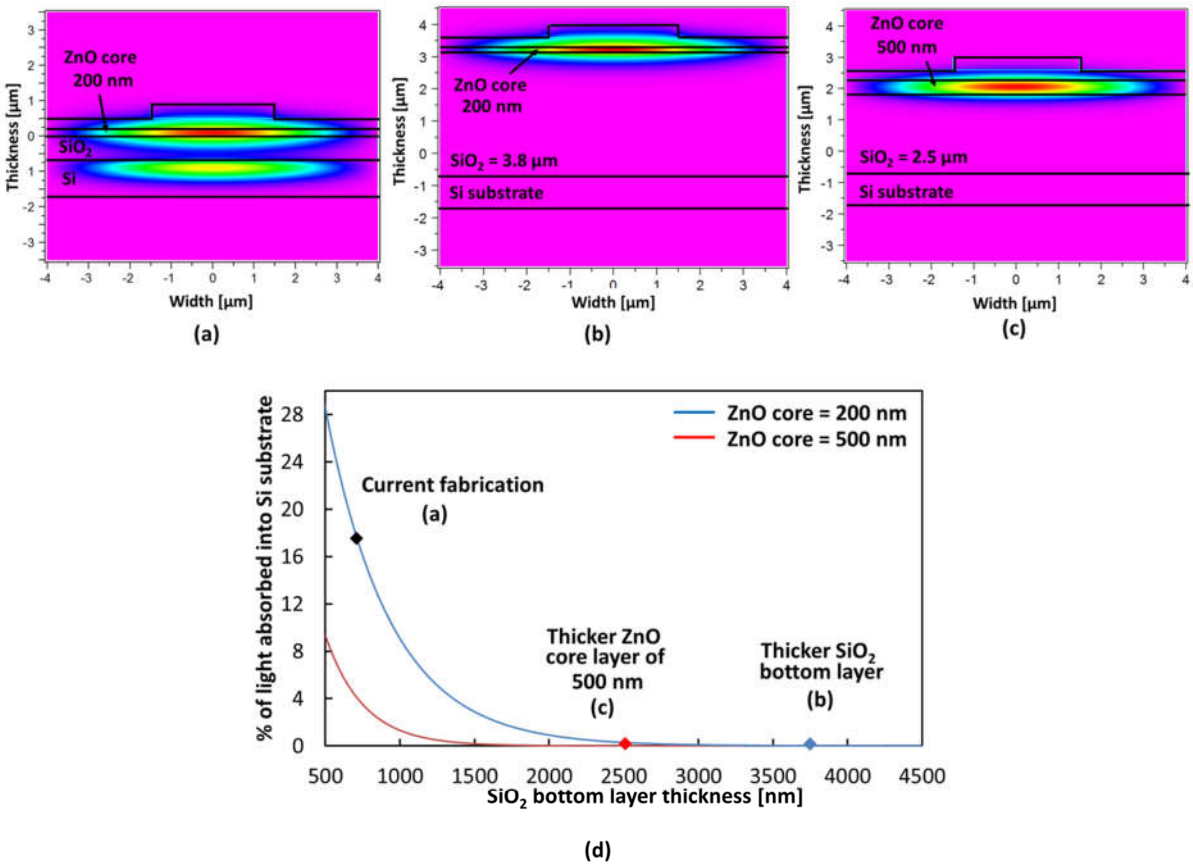
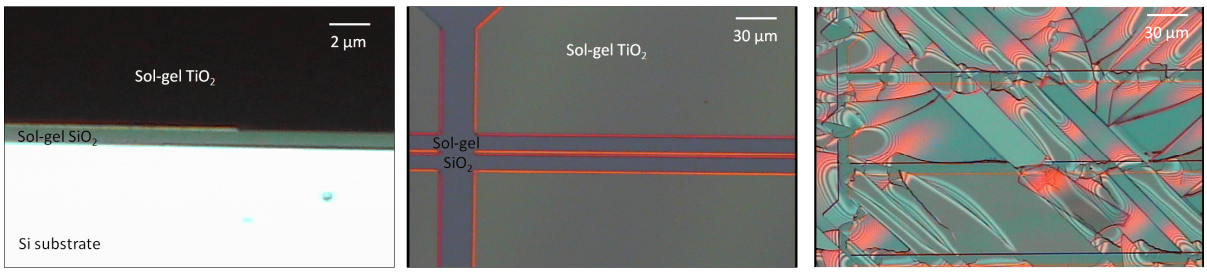


Fig. 3.22: Simulation results based on the dimensions of (a) current fabricated all sol-gel ridge waveguide showing the optical field leaking from the ZnO core layer into the Si substrate, and possible solutions to overcome this issue by (b) increasing the thickness of the bottom SiO_2 sol-gel cladding layer to 2.0 µm or by (c) increasing the thickness of the core ZnO sol-gel layer to 500 nm and bottom SiO_2 layer to 1.0 µm. Graph (d) shows the comparison between the % of light absorbed into the Si substrate at these 3 different scenarios with higher % of light absorbed by the Si indicating higher loss through the waveguide.

3.7.4 Sol-gel TiO_2 as core layer

TiO_2 is a material with high refractive index of 2.43 which has been demonstrated in literature as optical waveguides mainly through the sputtering deposition process. In our work, we experiment by using sol-gel TiO_2. The TiO_2 chemical precursor used was procured from Kojunda Chemicals. The sol-gel TiO_2 was spin coated onto the sol-gel SiO_2 cladding layer at 1000 rpm spin coating speed and heated on the hot plate to 145°C to stabilize the layer. The sample was then annealed up to 500°C, however in all of our experiments, the TiO_2 layer would crack and delaminate from the SiO_2 layer during this annealing process. The mechanism for the crack and delamination was determined to be due to the large difference in thermal expansion coefficients between the sol-gel SiO_2 (0.55×10^{-6}/K) and sol-gel TiO_2 (10.2×10^{-6}/K) layers.

In order to alleviate the stress that causes cracks during the annealing process, etching of the TiO_2 layer was thought to be able to provide stress relief similar as to that reported in literature for other materials [58]. Etching of TiO_2 was able to be conducted by using a BHF solution as is shown in Fig. 3.22 below after the TiO_2 layer was heated on the hot plate but before the annealing process. During this stage, the TiO_2 layer has not fully densified yet, thus it is able to be etched. Despite being fully etched down, it was still found that the cracks and peeling would occur during the annealing process.



(a) (b) (c)

Fig. 3.23: Experiments with TiO_2 as the core layer on top of SiO_2 sol-gel: (a) <60 nm sol-get TiO_2 layer on top of sol-gel SiO_2 layer, (b) top view of etched sol-gel TiO_2 layer, and (c) the same etched sample after the annealing process.

Figure 3.23 (a) shows the side view of an etched TiO_2 layer of <60nm thickness on top of the sol-gel SiO_2 layer. The etching process using BHF was conducted after the hot plate annealing stage where the TiO_2 layer was heated up to 145°C to stabilize after spin coating. Figure 3.23 (b) shows the top view of the TiO_2 sample before annealing while Fig. 3.23 (c) shows the cracks and delamination that occurs after annealing at 500°C. Literature for sol-gel TiO_2 layers have demonstrated that for optical waveguides, sol-gel TiO_2 have to be annealed between 500°C - 900°C in order to crystalize the TiO_2 layer for it to be usable as an optical waveguide core layer [59]. Because of the cracks and delamination that occurs in our processing due to the difference in thermal expansion coefficients, the sol-gel TiO_2 was found to not be suitable to be used the core layer on top of the sol-gel SiO_2 cladding layer.

3. 8. Conclusion

We have developed a sol-gel deposition scheme with the ability to stack multiple layers of sol-gel SiO_2 onto an Si substrate to achieve greater than 0.8 µm thickness. The main issue of peeling and cracks of the multi-layer stacked sol-gel SiO_2 layers were overcome by a double annealing process at 500°C for complete solvent evaporation, O_2 plasma ashing to remove the polymer layer and a short BHF dip for surface conditioning. A relatively thick sol-gel SiO_2 layer thickness of greater than 3 µm was achieved by six layers of spin coating deposition. The refractive index was determined to be 1.42. To assess its suitability as a cladding layer, an a-Si core layer was sputtered directly onto the 1.9 µm SiO_2 sol-gel cladding layer to form an optical waveguide with a propagation loss of 10.1 dB/cm measured at 1550 nm wavelength. Resistivity measurements were found to be greater than $1x10^9$ Ω. Furthermore, different core layer materials of sputtered SiN, sol-gel TiO_2 and sol-gel ZnO were also trialled to assess the feasibility of stacking these materials on top of the developed multi-layer sol-gel SiO_2. These results demonstrates that the developed multi-layer stacking scheme of sol-gel SiO_2 layers is suitable to realize cladding and passivation layers for optical waveguides in conjunction with different core materials on an Si substrate.

3. 9. References

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Chapter 4: Conclusions and outlook

4. 1. Conclusions

As outlined in chapter 1, the photonic integrated circuit is one of the main schemes proposed to improve energy efficiency in the information and communications technology field. Much progress has been achieved for active and passive photonic devices; however the lack of an efficient on-chip light source is still the main roadblock towards achieving a full photonic integrated circuit. Preliminary research has shown that Ge has the potential to fulfil this role. Although being an indirect bandgap material Ge, band engineering has enabled an electrically pumped laser source at 1550 nm to be achieved. The fabrication of Ge in order to fully realize its full potential has been less researched. Therefore, in this study we research on the accurate dry etching of Ge to fabricate precise width and dimensional control of Ge waveguides and for future photonic devices. Another aspect that has been mentioned in chapter 1 is the advancement of space division multiplexing (SDM) through multi-core fibres (MCFs) to achieve higher data transmission capabilities. Issues arise however on how to interface between planar photonic circuits and the 3D cross section of MCFs and one of the methods to achieve this is through multi-layer stacking using sol-gel for optical waveguides. In this study we also research on the possibility for a multi-layer sol-gel fabrication technique for optical waveguides.

In chapter 2, numerical analysis was conducted to identify the required thickness for a Ge-on-Si and GeOI structure to support a single mode waveguide. The minimum thickness of the substrate to support >99.9% optical confinement was also determined. FEM was then used to identify the minimum width of the optical waveguides. This was then translated into the required etching depth for fabrication. In the fabrication of Ge, dry etching using CHF_3 based ICP was developed for accurate etching. The developed fabrication process achieved an almost vertical sidewall angle of 85° while maintaining a relatively high 5:1 selectivity ratio towards normal photoresist. This enables almost a 100% accurate etched waveguide width.

In chapter 3, the issues, mechanism and fabrication method to realize multi-layer stacking of sol-gel SiO_2 for optical waveguide cladding and passivation layers was discussed. A new double annealing and O_2 plasma fabrication process was developed to eliminate the issues of cracks and peeling that was seen during multi-layer stacking of sol-gel SiO_2. A relatively thick sol-gel SiO_2 layer thickness of greater than 3 µm was achieved with refractive index of 1.42. Resistivity measurements were found to be greater than 6.6×10^{13} Ω. Furthermore, different core layer was sputtered directly onto the SiO_2 sol-gel cladding layer to form an optical waveguide with a-Si core layer having a propagation loss of 10.1 dB/cm measured at 1550 nm wavelength. These results demonstrates that the developed multi-layer stacking scheme of sol-gel SiO_2 layers is suitable to realize cladding and passivation layers for optical waveguides in conjunction with different core materials on an Si substrate.

4. 2. Outlook

We hope that the work here will help to propel the field of photonic integrated circuit in the future to overcome the need for greater energy efficiency and greater data transmission.

It is expected that the higher accuracy attainable by using CHF_3 based ICP dry etching to etch Ge will translate into better performance for both active and passive Ge photonic devices. Similarly, the capability to fabricate a multi-layer sol-gel SiO_2 technique for optical waveguides can facilitate interfacing between planar photonic circuits and MCFs. The capability to stack multi-layer sol-gel SiO_2 to achieve any thickness required for cladding layers along with the high electrical isolation as passivation layers shows promise for integrating optical devices such as waveguides together with electronic devices. Therefore, with these two fabrication results obtained, we believe that the future of photonic integrated circuits is bright indeed.

Appendix A: Analytical method for a three layer slab waveguide

This section elaborates on the analysis for a three layer optical waveguide to determine the effective refractive index, the electrical field and optical confinement by following the work of T. Tamir [1]. Figure A.1 illustrates a three layer slab optical waveguide with the refractive index of n_1 for the substrate, n_2 for the core film and n_3 for the cover with respect to *x*, *y*, and *z* directions. The structure is uniform in the *y* and *z* directions. The thickness of the core film is from 0 to W.

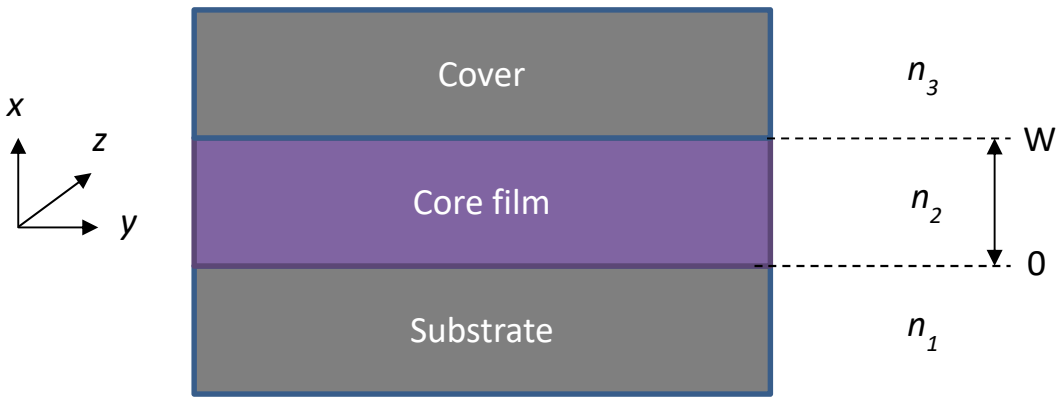

Fig. A.1: Schematic for a three layer slab waveguide structure

The refractive index in the core film has a higher refractive index and it is sandwiched between the substrate and cover layers that have a lower refractive index.

The substrate and the cover may have the same refractive, $n_1=n_3$ or it may have a different refractive index $n_1 \neq n_3$.

$$n_2 > n_1 \text{ and } n_2 > n_3 \tag{A.1}$$

Since the tangential field components are connected at the boundary interface between the film and the substrate, and the film and the cover, we can start with Helmholtz equations which are for uniform layers. Also, since the structure is uniform in the *y* direction, it can be assumed that $\frac{d}{dy} = 0$. Therefore, the equation for the electric field **E** is:

$$\frac{d^2\mathbf{E}}{dx^2} + k_0^2\left(\varepsilon_r - n_{\text{eff}}^2\right)\mathbf{E} = 0 \tag{A.2}$$

Similarly, for the magnetic field, **H**, the equation is:

$$\frac{d^2\mathbf{H}}{dx^2} + k_0^2\left(\varepsilon_r - n_{eff}^2\right)\mathbf{H} = 0 \tag{A.3}$$

For the three layer slab optical waveguide, there are two modes that propagates through it. The transverse electric mode (TE mode) and the transvers magnetic mode (TM).

The basics originate by deriving the wave equation from Maxwell's equations:

$$\boldsymbol{\nabla} \times \mathbf{E} = -j\omega\mu_0\mathbf{H} \tag{A.4}$$

$$\boldsymbol{\nabla} \times \mathbf{H} = -j\omega\varepsilon_0\varepsilon_r\mathbf{E} \tag{A.5}$$

Where the *x*, *y* and *z* component for the electric field are represented by:

$$\frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z} = -j\omega\mu_0 H_x \tag{A.6}$$

$$\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x} = -j\omega\mu_0 H_y \tag{A.7}$$

$$\frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y} = -j\omega\mu_0 H_z \tag{A.8}$$

Similarly, the components for the magnetic field are represented by:

$$\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} = -j\omega\varepsilon_0\varepsilon_r E_x \tag{A.9}$$

$$\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} = -j\omega\varepsilon_0\varepsilon_r E_y \tag{A.10}$$

$$\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} = -j\omega\varepsilon_0\varepsilon_r E_z \tag{A.11}$$

For all of these equations, it is assumed that the relative permeability $\mu_r = 1$and that $\mu = \mu_r\mu_0 = \mu_0$. Also, since the structure is uniform in the *z* propagation direction, the derivative with respect to the *z* direction $\partial/\partial z$, can be replaced by $-j\beta$. The effective refractive index from Eq. A.2 can also be expressed as $n_{\text{eff}} = \beta/k_0$, where k_0 is the wave number is vacuum.

The analysis can then be differentiated into TE and TM modes.

A.1 TE mode

For TE mode, the electric field is not in the longitudinal direction, $E_z = 0$ but the electric field is in the transverse direction where $E_y \neq 0$. Since the structure is uniform in the y direction, ${}^{\partial}/_{\partial y} = 0$.

Substituting this into Eq. A8 results in ${}^{\partial \mathrm{H_y}}/_{\partial x} = 0$. What this basically means is that H_y is constant and it can be assumed that $H_y = 0$. Furthermore, we can substitute $E_z = H_y = 0$ into Eq. A7 and this results in ${}^{\partial E_x}/_{\partial z} = 0$, which means that $E_x = 0$. Therefore we can simplify it into:

$$E_x = E_z = H_y = 0 \tag{A.12}$$

When substituting $H_x = -(\beta/\omega\mu_0)E_y$, which was derived from Eq. A.6 and $H_z = (j/\omega\mu_0)\,\partial E_y/\partial x$ which was derived from Eq. A.8 into Eq. A.10, the following wave equations for the principle Electric field component E_y is obtained:

$$\frac{\partial^2 E_y}{\partial x^2} + k_0^2\left(\varepsilon_r - n_{\mathrm{eff}}^2\right)E_y = 0 \tag{A.13}$$

where $k_0 = \omega\sqrt{\varepsilon_0\mu_0}$

A.2 Effective refractive index for TE mode.

For the substrate, core film and cover regions, the principle electric field component E_y can be expressed as:

Substrate: $E_y = C_1 exp(\gamma_1 x)$ where $\gamma_1 = k_0\sqrt{n_{\text{eff}}^2 - n_1^2}$ (A.14)

Core film: $E_y = C_2 \cos(\gamma_2 x + \alpha)$ where $\gamma_2 = k_0\sqrt{n_2^2 - n_{\text{eff}}^2}$ (A.15)

Cover: $E_y = C_3 \exp[-\gamma_3(x - W)]$ where $\gamma_3 = k_0\sqrt{n_{\text{eff}}^2 - n_3^2}$ (A.16)

In these equations, there are 4 unknown constants; n_{eff}, C_1, C_2 and C_3 and therefore 4 equations are required to determine the effective refractive index, n_{eff}. To obtain these 4 equations, the following boundary conditions are imposed on the tangential electric field component E_y and the tangential magnetic field component H_z at boundary of $x = 0$ and at $x = W$.

The tangential magnetic field component H_z is then given by:

$$H_z = \frac{-1}{j\omega\mu_0}\frac{\partial E_y}{\partial x} \quad \text{(A.17)}$$

Where in all 3 regions are defined as:

Substrate: $H_z(x) = -\frac{\gamma_1}{j\omega\mu_0} C_1 exp(\gamma_1 x)$ (A.18)

Core film: $H_z(x) = -\frac{\gamma_2}{j\omega\mu_0} C_2 \sin(\gamma_2 x + \alpha)$ (A.19)

Cover: $H_z(x) = -\frac{\gamma_3}{j\omega\mu_0} C_3 exp[-\gamma_3(x - W)]$ (A.20)

One boundary condition statement that holds true is that the tangential electric field components as well as the tangential magnetic field components are equal at the interfaces between adjacent layers. Therefore, the boundary conditions on these field components at $x = 0$ can be expressed as:

$$E_{y1}(0) = E_{y2}(0) \quad \text{(A.21)}$$

$$H_{z1}(0) = H_{z2}(0) \quad \text{(A.22)}$$

Similarly, at $x = W$, the equations can be expressed as:

$$E_{y2}(0) = E_{y3}(0) \quad \text{(A.23)}$$

$$H_{z2}(0) = H_{z3}(0) \quad \text{(A.24)}$$

And therefore, the 4 resulting equations are:

$$C_1 = C_2 \cos\alpha \tag{A.25}$$

$$-\gamma_1 C_1 = \gamma_2 C_2 \sin\alpha \tag{A.26}$$

$$C_2 \cos(\gamma_2 W + \alpha) = C_3 \tag{A.27}$$

$$-\gamma_2 C_2 \sin(\gamma_2 W + \alpha) = -\gamma_3 C_3 \tag{A.28}$$

From here, dividing Eq. A.26 by Eq. A.25, the following is obtained:

$$\alpha = -\tan^{-1}\left(\frac{\gamma_1}{\gamma_2}\right) + q_1\pi \text{ where } (q_1 = 0,1,2,\ldots) \tag{A.29}$$

On the other hand, dividing Eq. A.28 by Eq. A.27, the following is obtained:

$$\gamma_2 W = \tan^{-1}\left(\frac{\gamma_3}{\gamma_2}\right) - \alpha + q_2\pi \quad \text{where } (q_2 = 0,1,2,\ldots) \tag{A.30}$$

Substituting α from Eq. A.29 into Eq. A.30, the resulting equation is achieved:

$$\gamma_2 W = \tan^{-1}\left(\frac{\gamma_1}{\gamma_2}\right) + \tan^{-1}\left(\frac{\gamma_3}{\gamma_2}\right) + q\pi \text{ where } (q = 0,1,2,\ldots) \tag{A.31}$$

By using the following:

$$\tan^{-1}\left(\frac{y}{x}\right) = \frac{\pi}{2} - \tan^{-1}\left(\frac{x}{y}\right) \tag{A.32}$$

Eq. A.31 can be rewritten into:

$$\gamma_2 W = -\tan^{-1}\left(\frac{\gamma_2}{\gamma_1}\right) - \tan^{-1}\left(\frac{\gamma_2}{\gamma_3}\right) + (q+1)\pi \text{ where } (q = 0,1,2,\ldots) \qquad \text{(A.33)}$$

A.3 TM mode

For TM mode, the magnetic field is not in the longitudinal direction, $H_z = 0$ but the magnetic field is in the transverse direction where $H_y \neq 0$. Since the structure is uniform in the y direction, ${}^{\partial}/_{\partial y} = 0$.

Substituting this into Eq. A.8 results in ${}^{\partial \mathrm{E_y}}/_{\partial x} = 0$. What this basically means is that E_y is constant and it can be assumed that $E_y = 0$. Furthermore, we can substitute $H_z = E_y = 0$ into Eq. A.7 and this results in ${}^{\partial H_x}/_{\partial z} = 0$, which means that $H_x = 0$. Therefore we can simplify it into:

$$H_x = H_z = E_y = 0 \qquad \text{(A.34)}$$

When substituting $E_x = -(\beta/\omega\varepsilon_0\varepsilon_r)H_y$, which was derived from Eq. A.9 and $E_z = -(j/\omega\varepsilon_0\varepsilon_r)\,\partial H_y/\partial x$ which was derived from Eq. A.11 into Eq. A.7, the following wave equations for the principle Electric field component H_y is obtained:

$$\frac{\partial^2 H_y}{\partial x^2} + k_0^2\left(\varepsilon_r - n_{\mathrm{eff}}^2\right)H_y = 0 \qquad \text{(A.35)}$$

A.4 Effective refractive index for TM mode.

For the substrate, core film and cover regions, the principle magnetic field component H_y can be expressed as:

Substrate: $H_y = C_1 exp(\gamma_1 x)$ where $\gamma_1 = k_0\sqrt{n_{\text{eff}}^2 - n_1^2}$ (A.36)

Core film: $H_y = C_2 \cos(\gamma_2 x + \alpha)$ where $\gamma_2 = k_0\sqrt{n_2^2 - n_{\text{eff}}^2}$ (A.37)

Cover: $H_y = C_3 \exp[-\gamma_3(x - W)]$ where $\gamma_3 = k_0\sqrt{n_{\text{eff}}^2 - n_3^2}$ (A.38)

Similarly, in these equations, there are 4 unknown constants; n_{eff}, C_1, C_2 and C_3 and therefore 4 equations are required to determine the effective refractive index, n_{eff}. To obtain these 4 equations, the following boundary conditions are imposed on the tangential magnetic field component H_y and the tangential electric field component E_z at boundary of $x = 0$ and at $x = W$. The tangential electric field component E_z is then given by:

$$E_z = \frac{1}{j\omega\varepsilon_0\varepsilon_r}\frac{\partial H_y}{\partial x} \quad \text{(A.39)}$$

Where in all 3 regions are defined as:

Substrate: $E_z(x) = \frac{\gamma_1}{j\omega\varepsilon_0\varepsilon_r} C_1 exp(\gamma_1 x)$ (A.40)

Core film: $E_z(x) = -\frac{\gamma_2}{j\omega\varepsilon_0\varepsilon_r} C_2 \sin(\gamma_2 x + \alpha)$ (A.41)

Cover: $E_z(x) = \frac{\gamma_3}{j\omega\varepsilon_0\varepsilon_r} C_3 exp[-\gamma_3(x - W)]$ (A.42)

One boundary condition statement that holds true is that the tangential magnetic field components as well as the tangential electric field components are equal at the interfaces between adjacent layers.

Therefore, the boundary conditions on these field components at $x = 0$ can be expressed as:

$$C_1 = C_2 \cos\alpha \tag{A.43}$$

$$-\frac{\gamma_1}{\varepsilon_{r1}} C_1 = \frac{\gamma_1}{\varepsilon_{r2}} C_2 \sin\alpha \tag{A.44}$$

$$C_2 \cos(\gamma_2 W + \alpha) = C_3 \tag{A.45}$$

$$-\frac{\gamma_2}{\varepsilon_{r2}} C_2 \sin(\gamma_2 W + \alpha) = -\frac{\gamma_2}{\varepsilon_{r2}} C_3 \tag{A.46}$$

Dividing Eq. A.44 by Eq. A.43, the following is obtained:

$$\alpha = -\tan^{-1}\left(\frac{\varepsilon_{r2}}{\varepsilon_{r1}}\frac{\gamma_1}{\gamma_2}\right) + q_1\pi \qquad \text{where } (q_1 = 0,1,2,\ldots) \tag{A.47}$$

On the other hand, dividing Eq. A.46 by Eq. A.45, the following is obtained:

$$\gamma_2 W = \tan^{-1}\left(\frac{\varepsilon_{r2}}{\varepsilon_{r3}}\frac{\gamma_3}{\gamma_2}\right) - \alpha + q_2\pi \qquad \text{where } (q_2 = 0,1,2,\ldots) \tag{A.48}$$

Substituting α from Eq. A.47 into Eq. A.48, the resulting equation is achieved:

$$\gamma_2 W = \tan^{-1}\left(\frac{\varepsilon_{r2}}{\varepsilon_{r3}}\frac{\gamma_3}{\gamma_2}\right) + \tan^{-1}\left(\frac{\varepsilon_{r2}}{\varepsilon_{r1}}\frac{\gamma_1}{\gamma_2}\right) + q\pi \text{ where } (q = 0,1,2,\ldots) \tag{A.49}$$

By using Eq. A.32, the following is obtained:

$$\gamma_2 W = -\tan^{-1}\left(\frac{\varepsilon_{r1}}{\varepsilon_{r2}}\frac{\gamma_2}{\gamma_1}\right) - \tan^{-1}\left(\frac{\varepsilon_{r3}}{\varepsilon_{r2}}\frac{\gamma_2}{\gamma_2}\right) + (q+1)\pi \text{ where } (q = 0,1,2,\ldots) \quad \text{(A.50)}$$

Therefore, when comparing the Eq. A.31 and A.32 obtained for the TE mode with the Eq. A.49 and A.50 for the TM mode, it can be seen that the equations for the TM mode contains the ratio of the relative permittivities of the adjacent layers.

References

[1] T. Tamir, "*Guided-Wave Optoelectronics*," 1st ed., vol. 26. Springer Berlin Heidelberg, 1988.

Appendix B: Effective index method for ridge waveguides

This section elaborates on the analysis for a ridge waveguide by using the effective index method to determine the dispersion equation. by following the work of K. Okamoto [1]. Figure B.1 illustrates a ridge waveguide structure with the refractive index of n_s for the substrate, n_c for the core film, n_r for the rib cover layer and n_a for the air cover with respect to *x*, *y*, and *z* directions. The structure is uniform in the *z* direction. The width of the waveguide is from –*a* to *a*, the thickness of the core layer is *d* and the rib cover layer consists of two parts which is the rib area height, *h* and the etched portion of the rib cover layer with height *t*.

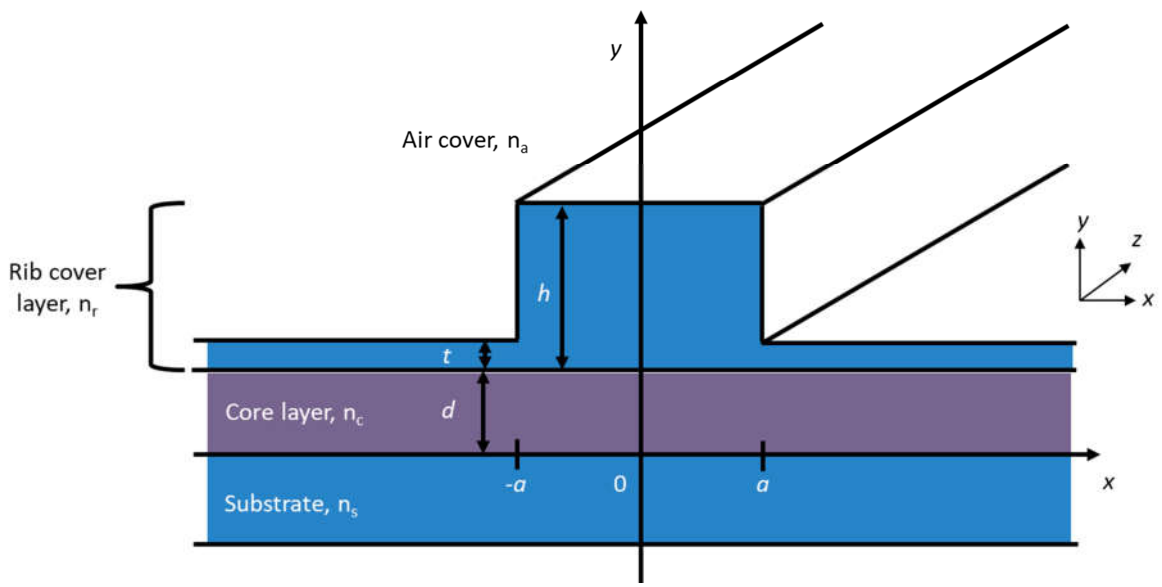

Fig. B.1: Schematic for a ridge waveguide structure

The refractive index in the core film has a higher refractive index and it is sandwiched between the substrate and cover layers that have a lower refractive index. For this, we assume that the substrate and the rib cover has the same refractive index, n_s=n_r.

$$n_c > n_s \text{ and } n_c > n_r \tag{B.1}$$

From the slab waveguide analysis in Appendix A, the wave equation and electromagnetic field can be represented as

$$\frac{d^2\boldsymbol{H_y}}{dx^2} + \frac{d^2\boldsymbol{H_y}}{dy^2} + [k^2n^2(x,y) - \beta^2]H_y = 0 \tag{B.2}$$

Similarly, for the effective index method, the electromagnetic field can be stated as separate variables in the x and y direction

$$\boldsymbol{H_y}(x,y) = X(x)Y(y) \tag{B.3}$$

Therefore, if we substitute Eq. B.3 into B.2, and dividing it by XY, the following equation is obtained.

$$\frac{1}{X}\frac{d^2\mathbf{X}}{dx^2} + \frac{1}{Y}\frac{d^2\mathbf{Y}}{dy^2} + [k^2n^2(x,y) - \beta^2] = 0 \tag{B.5}$$

From fig. B.1, we can deduce that the value $k^2 n_{eff}^2(x)$ is independent of the y-direction and can be added to and subtracted from Eq. B.5 to form two independent equations.

$$\frac{1}{Y}\frac{d^2\mathbf{Y}}{dy^2} + \left[k^2 n^2(x,y) - k^2 n_{eff}^2(x)\right] = 0 \qquad \text{(B.6)}$$

$$\frac{1}{X}\frac{d^2\mathbf{X}}{dx^2} + \left[k^2 n_{eff}^2(x) - \beta^2\right] = 0 \qquad \text{(B.7)}$$

This can be represented as a variation of the actual refractive index profile in fig. B.2 below:

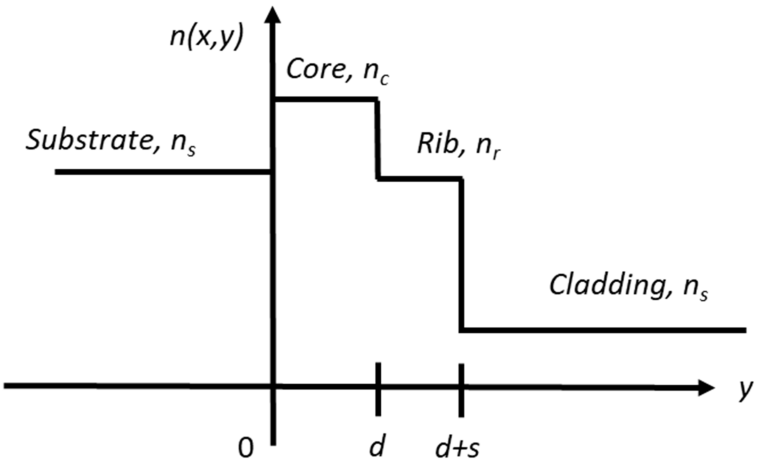

Fig. B.2: Refractive index profile from the substrate, core, rib and air cover layer

For the refractive index profile, the value *s* in fig. B.2 above is either the height of the rib, *h* or of the etched rib area, *t* from fig. B.1.

$$s = \begin{cases} h & 0 \leq |x| \leq a \\ t & |x| > a \end{cases} \tag{B.8}$$

From this, we can determine the effective refractive index distribution, $n_{eef}(x)$.

The continuous boundary conditions at the interface at y=0,y=d and y=d+s is indicated by $H_z \propto \frac{\partial H_y}{\partial y}$. Thus, this can be interpreted as a four-layer slab waveguide as shown in fig. B.2. For a four-layer slab waveguide, the dispersion equation is represented as:

$$\sin(\kappa d - 2\phi) = \sin(\kappa d) e^{-2(\sigma s + \psi)} \tag{B.9}$$

where each of these parameters are defined as:

$$\phi = tan^{-1}\left(\frac{\sigma}{\kappa}\right) \tag{B.10}$$

$$\psi = tanh^{-1}\left(\frac{\sigma}{\kappa}\right) \tag{B.11}$$

$$\kappa = k\sqrt{n_c^2 - n_{eff}^2} \tag{B.12}$$

$$\sigma = k\sqrt{n_{eff}^2 - n_s^2} \tag{B.13}$$

$$\gamma = k\sqrt{n_{\text{eff}}^2 - n_a^2} \tag{B.14}$$

Therefore, by using Eq. B.9 and the height of the rib as $s = h(0 \leq |x| \leq a)$, this gives the effective refractive index n_{eff}(h) for the area under the rib. As for when $s = t(|x| > a)$, this gives the effective refractive index n_{eff}(t). When can visualize the effective refractive index distribution n_{eff}(x) as shown in fig. B.3 below as a function of both n_{eff}(h) and n_{eef}(t).

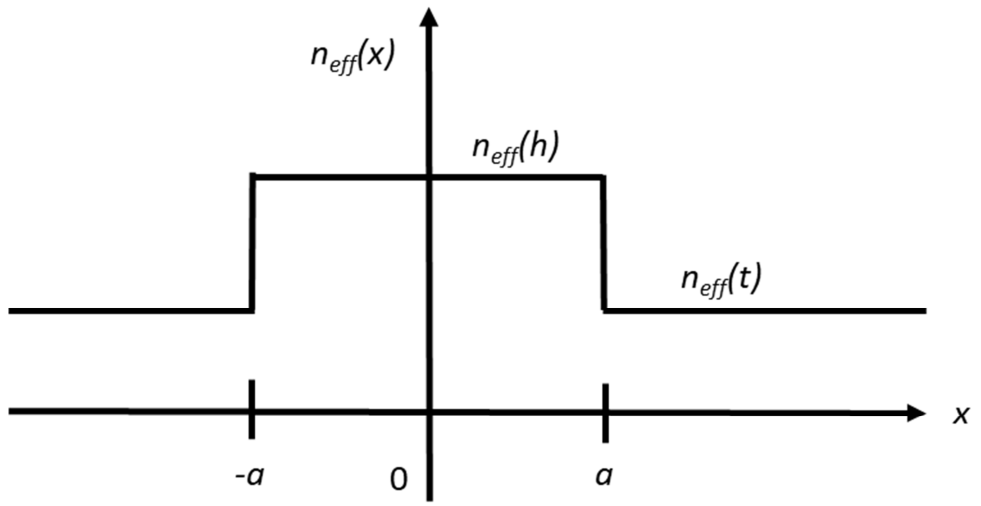

Fig. B.3: Effective index distribution n_{eff}(x) as both n_{eff}(h) and n_{eff}(t)

Eq. B.7 can then be solved by analysing fig. B.3 as a symmetrical three-layer slab waveguide. The boundary condition at x = -a and a should be continuous and that $E_z \propto \left(\frac{1}{n^2}\right)\frac{\partial H_y}{\partial x}$. Therefore, at x = -a and a, $\left(\frac{1}{n^2}\right)X$ should also be continuous.

Under these boundary conditions, the dispersion equation can be obtained as

$$u\tan(u) = \frac{n_{eff}^2(h)}{n_{eff}^2(t)}w \tag{B.15}$$

where

$$u = ka\sqrt{n_{eff}^2(h) - \left(\frac{\beta}{k}\right)^2} \tag{B.16}$$

$$w = ka\sqrt{\left(\frac{\beta}{k}\right)^2 - n_{eff}^2(t)} \tag{B.17}$$

References

[1] K. Okamoto, *Fundamentals of Optical Waveguides*, 2nd ed. Elsevier, 2006.

Appendix C: Derivation of coupled mode equations based on perturbation theory

This section elaborates on the derivation of the coupled mode equations based on the perturbation theory. A number of works has already been presented on the derivation of coupled mode theory [1],[2],[3]. In this appendix, we follow the work of Katsunari Okamoto [4] for the derivation of coupled mode equations based on the perturbation theory. In an axially uniform optical waveguide, a number of propagation modes exists. These modes are specific to each waveguide, and they satisfy the orthogonality conditions between each modes.

The schematic for a coupled waveguide system is as shown in fig. C.1 where the two waveguides with refractive index n_1 are separated by a core separation with refractive index n_0. When two waveguides are brought close to each other, the optical modes of each waveguide either couple or interfere with each other. When the electromagnetic field distribution after mode coupling do not differ substantially from those before mode coupling, the propagation characteristics of the coupled waveguides can be analysed by the perturbation theory.

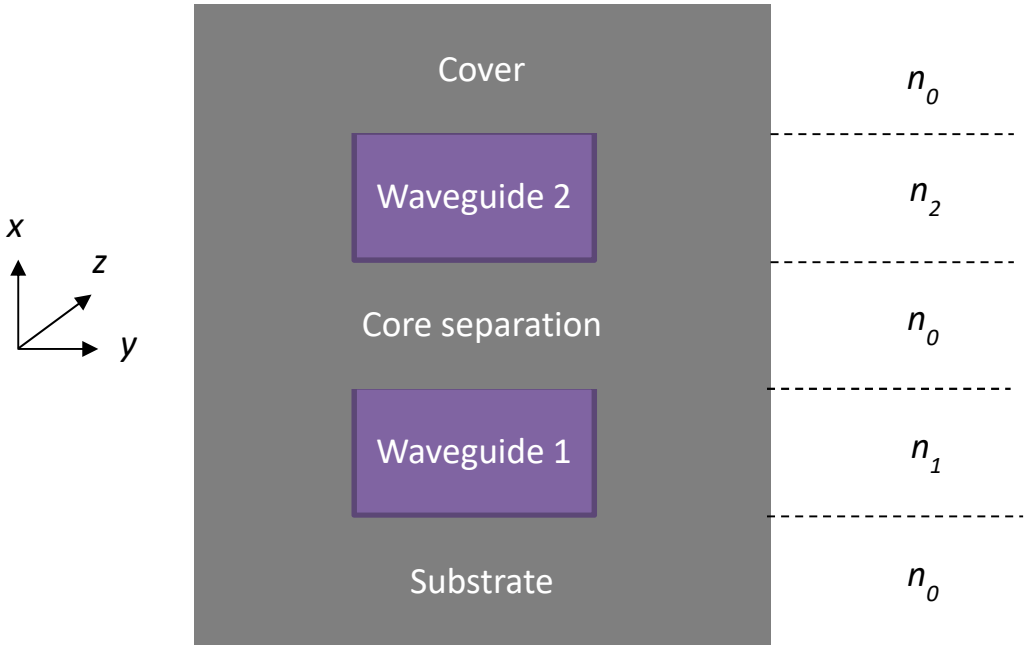

Fig. C.1: Schematic for a coupled waveguide

We can denote the eigen modes in each optical waveguide before mode coupling as $\tilde{E}_p, \tilde{H}_p$ where (p=1,2), and they satisfy the Maxwell equation as:

$$\begin{cases} \nabla \times \tilde{\mathbf{E}}_p = -j\omega\mu_0\tilde{\mathbf{H}}_p \\ \nabla \times \tilde{\mathbf{H}}_p = j\omega\varepsilon_0 N_p^2\tilde{\mathbf{E}}_p \end{cases} \quad \text{where (p=1,2)} \qquad \text{(C.1)}$$

Where $N_p^2(x,y)$ represents the refractive index distribution of each waveguide. The electromagnetic fields of the coupled waveguide can be expressed as the sum of the eigen modes in each waveguide as:

$$\begin{cases} \tilde{\mathbf{E}} = A(z)\tilde{\mathbf{E}}_1 + B(z)\tilde{\mathbf{E}}_2 \\ \tilde{\mathbf{H}} = A(z)\tilde{\mathbf{H}}_1 + B(z)\tilde{\mathbf{H}}_2 \end{cases} \qquad \text{(C.2)}$$

In this case, the electromagnetic fields in the coupled waveguide should also satisfy Maxwell's equations. When substituting Eq. C.1 into Eq. C.2, the following is obtained:

$$\begin{cases} \nabla \times \tilde{\mathbf{E}} = -j\omega\mu_0\tilde{\mathbf{H}} \\ \nabla \times \tilde{\mathbf{H}} = j\omega\varepsilon_0 N^2\tilde{\mathbf{E}} \end{cases} \tag{C.3}$$

And by using the Eq. C.1 and the following vector formula:

$$\nabla \times (A\mathbf{E}) = A\nabla \times \mathbf{E} + \nabla \mathrm{A} \times \mathbf{E} = A\nabla \times \mathbf{E} + \frac{dA}{dz}\mathbf{u_z} \times \mathbf{E} \tag{C.4}$$

The following relations can be obtained:

$$\left(\mathbf{u_z} \times \tilde{\mathbf{E}}_\mathbf{1}\right)\frac{dA}{dz} + \left(\mathbf{u_z} \times \tilde{\mathbf{E}}_\mathbf{2}\right)\frac{dB}{dz} = 0 \tag{C.5}$$

$$\begin{gathered} \left(\mathbf{u_z} \times \tilde{\mathbf{H}}_\mathbf{1}\right)\frac{dA}{dz} - j\omega\varepsilon_0(N^2 - N_1^2)A\tilde{\mathbf{E}}_\mathbf{1} + \left(\mathbf{u_z} \times \tilde{\mathbf{H}}_\mathbf{2}\right)\frac{dB}{dz} \\ -j\omega\varepsilon_0(N^2 - N_2^2)B\tilde{\mathbf{E}}_\mathbf{2} = 0 \end{gathered} \tag{C.6}$$

In these equations, $N^2(x, y)$ represents the refractive index distribution for the entire coupled waveguide.

Substituting Eq. C.4 and C.5 into the following integral equations:

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left[\tilde{\mathbf{E}}_1^* \cdot (Eq.B.4) - \tilde{\mathbf{H}}_1^* \cdot (Eq.B.5)\right]dxdy = 0 \tag{C.7}$$

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left[\tilde{\mathbf{E}}_2^* \cdot (Eq.B.4) - \tilde{\mathbf{H}}_2^* \cdot (Eq.B.5)\right]dxdy = 0 \tag{C.8}$$

We can obtain the following:

$$\frac{dA}{dz}+\frac{dB}{dz}\frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_1^*\times\tilde{\mathbf{H}}_2+\tilde{\mathbf{E}}_2\times\tilde{\mathbf{H}}_1^*\right)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_1^*\times\tilde{\mathbf{H}}_1+\tilde{\mathbf{E}}_1\times\tilde{\mathbf{H}}_1^*\right)dxdy}$$
$$+jA\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_1^2)\tilde{\mathbf{E}}_1^*\cdot\tilde{\mathbf{E}}_{\mathbf{1}}dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_1^*\times\tilde{\mathbf{H}}_1+\tilde{\mathbf{E}}_1\times\tilde{\mathbf{H}}_1^*\right)dxdy}$$
$$+jB\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_2^2)\tilde{\mathbf{E}}_1^*\cdot\tilde{\mathbf{E}}_{\mathbf{2}}dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_1^*\times\tilde{\mathbf{H}}_1+\tilde{\mathbf{E}}_1\times\tilde{\mathbf{H}}_1^*\right)dxdy}=0 \tag{C.9}$$

$$\frac{dB}{dz}+\frac{dA}{dz}\frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_2^*\times\tilde{\mathbf{H}}_1+\tilde{\mathbf{E}}_1\times\tilde{\mathbf{H}}_2^*\right)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_2^*\times\tilde{\mathbf{H}}_2+\tilde{\mathbf{E}}_2\times\tilde{\mathbf{H}}_2^*\right)dxdy}$$
$$+jA\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_1^2)\tilde{\mathbf{E}}_2^*\cdot\tilde{\mathbf{E}}_{\mathbf{1}}dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_2^*\times\tilde{\mathbf{H}}_2+\tilde{\mathbf{E}}_2\times\tilde{\mathbf{H}}_2^*\right)dxdy}$$
$$+jB\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_2^2)\tilde{\mathbf{E}}_2^*\cdot\tilde{\mathbf{E}}_{\mathbf{2}}dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z}\cdot\left(\tilde{\mathbf{E}}_2^*\times\tilde{\mathbf{H}}_2+\tilde{\mathbf{E}}_2\times\tilde{\mathbf{H}}_2^*\right)dxdy}=0 \tag{C.10}$$

From here, we can separate the transverse and the axial dependencies of the electromagnetic fields:

$$\begin{cases}\tilde{\mathbf{E}}_p=\mathbf{E}_p exp\left(-j\beta_p z\right)\\ \tilde{\mathbf{H}}_p=\mathbf{H}_p exp\left(-j\beta_p z\right)\end{cases}\text{ where (p=1,2)} \tag{C.11}$$

When we substitute Eq. C.10 into Eq. C.8 and Eq. C.9, the following is obtained:

$$\frac{dA}{dz} + c_{12}\frac{dB}{dz}exp[-j(\beta_2 - \beta_1)z] + j\chi_1 A + j\kappa_{12}Bexp[-j(\beta_2 - \beta_1)z] = 0 \tag{C.12}$$

$$\frac{dB}{dz} + c_{21}\frac{dA}{dz}exp[+j(\beta_2 - \beta_1)z] + j\chi_2 B + j\kappa_{21}Aexp[+j(\beta_2 - \beta_1)z] = 0 \tag{C.13}$$

where

$$\kappa_{pq} = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2 - N_q^2)\mathbf{E}_p^* \cdot \mathbf{E}_q dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z} \cdot (\mathbf{E}_p^* \times \mathbf{H}_p + \mathbf{E}_p \times \mathbf{H}_p^*)dxdy} \tag{C.14}$$

$$c_{pq} = \frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z} \cdot (\mathbf{E}_p^* \times \mathbf{H}_q + \mathbf{E}_q \times \mathbf{H}_p^*)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z} \cdot (\mathbf{E}_p^* \times \mathbf{H}_p + \mathbf{E}_p \times \mathbf{H}_p^*)dxdy} \tag{C.15}$$

$$\chi_p = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2 - N_p^2)\mathbf{E}_p^* \cdot \mathbf{E}_q dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u_z} \cdot (\mathbf{E}_p^* \times \mathbf{H}_p + \mathbf{E}_p \times \mathbf{H}_p^*)dxdy} \tag{C.16}$$

where the $(p, q) = (1,2)$ or $(2,1)$ respectively.

The definition of κ_{pq} is the mode coupling coefficient of the directional coupler. The definition of c_{pq} can be described as where If we consider a waveguide configuration shown in fig. C.1, the waveguide 1 only exists in the region of z < 0 and waveguide 2 in z ≥ 0. Therefore, when the eigen mode (**E₁**,

H₁) of waveguide 1 propagates from the negative z direction to z=0, the electromagnetic field in the cladding excites the eigen mode (**E₂**, **H₂**) of waveguide 2 at point z=0. This excitation efficiency is considered to be c_{12}. Therefore, c_{pq} basically represents the butt coupling coefficient between two waveguides.

When we compare the magnitude of κ_{pq} and χ_p for the case of when p=1 and q=2, and when we take into account that the actual value of $(N^2 - N_2^2)$ in waveguide 1 equals $(n_1^2 - n_0^2)$ and it is zero in all of the cladding and core separation areas. Therefore, the integration of κ_{12} is carried out only in the inside core region of waveguide 1. It should also be noted that the electric field of waveguide 2, $\mathbf{E}_2$ inside of waveguide 1 is very small at this point when compared to $\mathbf{E}_1$, that is $|E_2| = \eta|E_1|$. The magnitude of the integral term of κ_{12} in the numerator is about $(n_1^2 - n_0^2)\eta$. The integral of χ_p in Eq. C.16 is carried out in waveguide 2, where the refractive index difference $(N^2 - N_1^2)$ is also not zero. The magnitude of the integral term of χ_1 in the numerator is about $(n_1^2 - n_0^2)\eta^2$, and this is because the electric field strength of $\mathbf{E}_1$ in waveguide 2 is about η. And therefore, based on this comparison, we can conclude that χ_p is around η times smaller than κ_{pq}. Therefore, in this case the value of χ_p can be neglected when the two waveguides are sufficiently separated and $\eta \ll 1$, since χ_p is much smaller than κ_{pq}. In most conventional analysis of directional couplers, c_{pq} and χ_p are On the contrary, if the two waveguides are very close to each other, the value of c_{pq} and χ_p cannot be neglected.

The optical power carried by the eigen mode in the waveguide $p(p = 1,2)$ is described in the equation below:

$$P_p = \frac{1}{2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left(\mathbf{E}_p \times \mathbf{H}_p^*\right) \cdot \mathbf{u}_z dxdy \quad \text{where } p(p = 1,2) \tag{C.17}$$

From this equation, we can determine that the denominators of Eq. C.14-C.15 are equal to $4P_p$ and from here we can assume that the eigen modes in both waveguides are normalized to satisfy the following condition:

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left(\mathbf{E}_p^* \times \mathbf{H}_p + \mathbf{E}_p \times \mathbf{H}_p^*\right) \cdot \mathbf{u}_z dxdy = 4P_p = 1 \tag{C.18}$$

$$\text{where } p(p = 1,2)$$

From Eq. C15, we know that:

$$c_{21} = c_{12}^* \tag{C.19}$$

And from Eq. B16:

$$\chi_p = \chi_p^* \qquad \text{where } p(p = 1,2) \tag{C.20}$$

Here, we can express the difference of the propagation constants between waveguide 1 and 2 as:

$$\delta = \frac{\beta_2 - \beta_1}{2} \tag{C.21}$$

And the optical power in the entire coupled waveguide structure is expressed as:

$$P = \frac{1}{2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left(\tilde{\mathbf{E}} \times \tilde{\mathbf{H}}\right) \cdot \mathbf{u}_z dxdy \tag{C.22}$$

Substituting Eq. C.3 and C.10 into Eq. C.22 and the following is obtained:

$$P = \frac{1}{2}[|A|^2 + |B|^2 + A^* B c_{12} exp(-j2\delta z) + AB^* c_{12}^* \exp(j2\delta z)] \quad \text{(C.23)}$$

The Eqs. C.15, C.18 and C.19 are used in the derivation of Eq. C.23 above.

One assumption is that the waveguides are loss less and therefore, the optical power remains constant:

$$\frac{dP}{dz} = 0 \quad \text{(C.24)}$$

Substituting Eqs. C.12 and C.13 into Eq. C.24 above, the following is obtained:

$$jA^* B(\kappa_{21}^* - \kappa_{12} - 2\delta c_{12}) exp(-j2\delta z) - jAB^*(\kappa_{21} - \kappa_{12}^* - 2\delta c_{12}^*) exp(j2\delta z) = 0 \quad \text{(C.25)}$$

And since the power is independent of z, the following is obtained:

$$\kappa_{21} = \kappa_{12}^* + 2\delta c_{12}^* \quad \text{(C.26)}$$

In most cases, conventional analysis indicates the reciprocity of the coupling coefficients expressed by $\kappa_{21} = \kappa_{12}^*$, and since c_{12}^* is assumed to be 0. However, this is only valid if the propagation constants of the two waveguides are the same, or that the two waveguides are sufficiently separated. However, if these are not met, then the right hand side of Eq. C.26 cannot be neglected.

The derivation of the coupling mode equations can be derived from Eq. C.12 and C.13 where we can obtain:

$$\frac{dA}{dz} = -j\kappa_a B exp(-j2\delta z) + j\alpha_a A \tag{C.27}$$

Similarly, from Eq. C.12 and C.13, we can also obtain:

$$\frac{dB}{dz} = -j\kappa_b A exp(2\delta z) + j\alpha_b B \tag{C.28}$$

From Eq. C.27 and C.28, the parameters, κ_a, κ_b, α_a and α_b are defined as:

$$\kappa_a = \frac{\kappa_{12} - c_{12}\chi_2}{1-|c_{12}|^2} \tag{C.29a}$$

$$\kappa_b = \frac{\kappa_{12} - c_{12}\chi_1}{1-|c_{12}|^2} \tag{C.29b}$$

$$\alpha_a = \frac{\kappa_{21}c_{12} - \chi_1}{1-|c_{12}|^2} \tag{C.30a}$$

$$\alpha_b = \frac{\kappa_{12}c_{12}^* - \chi_2}{1-|c_{12}|^2} \tag{C.30b}$$

When assuming that $c_{pq} = \chi_p = 0$ where (p,q) = (1,2), the Eq. C.27 and C.28 can be re-written as:

$$\frac{dA}{dz} = -j\kappa_{12} B exp[-j(\beta_2 - \beta_1)z] \tag{C.32}$$

$$\frac{dB}{dz} = -j\kappa_{21} A exp[+j(\beta_2 - \beta_1)z] \tag{C.33}$$

Where κ_{pq}can be obtained from Eq. C.14. In most directional couplers, $\kappa_{pq}$is real and therefore the reciprocity of the coupling coefficients can be expressed as:

$$\kappa = \kappa_{12} = \kappa_{21} \tag{C.34}$$

References

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Appendix D: Coupled mode theory for coupled waveguides

In this section, the application of multi-layer stacking for the interface between the photonic integrated circuit and a 3D structure such as a multi-core fibre are discussed. An overview of the coupled mode theory is described here and simulation results are presented in order to realize a vertical coupled waveguide.

D. 1. Coupled waveguides

One of the basic elements used as a building block for optical devices is a system of coupled waveguides [1]. The physical representation model for a coupled waveguide consists of two or more waveguides placed in close proximity to one another. These waveguides may be parallel to each other or may have variable separations. The waveguides may also be subjected to changes in the refractive index due to gratings, tapers, nonlinearities and loss or gain along the waveguide axes. The changes in refractive index may be caused by imperfections on the material processing and device fabrication and in most cases; the effects of these imperfection are undesirable and will adversely affect the performance of the coupled waveguide. In other instances, changes in the refractive index may be created on purpose for reflecting, switching and modulating the light in these waveguides. The

coupled mode theory deals with the lightwave interactions between these two waveguides and a large number of work have been presented over the years [2][3][4].

If two waveguide are brought close to each other such as shown in fig. D.1, the optical modes of each waveguide either couple or interfere with each other. In this work, a number of assumptions are defined. The coupled waveguides are parallel and are assumed to be identical to each other and have a constant refractive index. The thickness of each waveguide is designed to support only a single fundamental TE mode. Similarly, the distance between these two parallel waveguides are assumed to be constant with a constant refractive index as well.

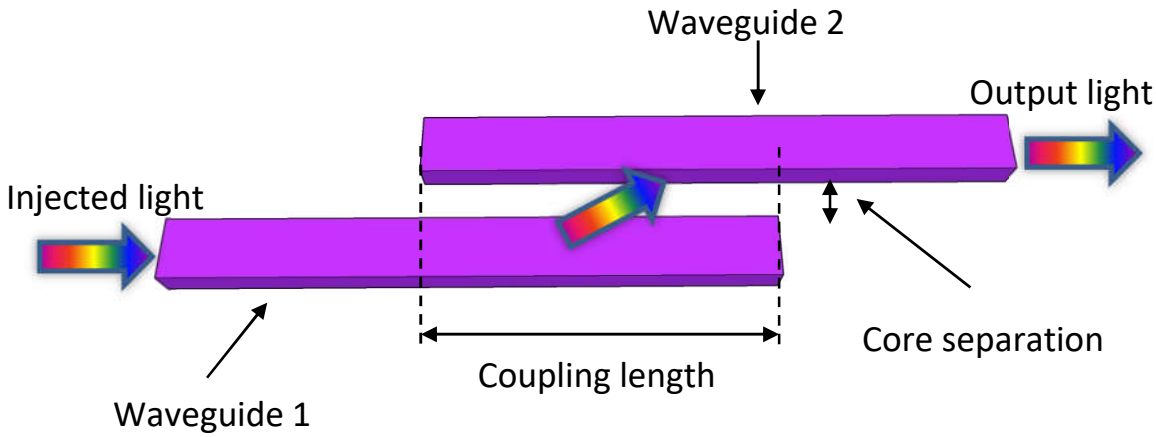

Fig. D.1: Two parallel waveguides with refractive index N_1 and N_2, a core separation between the two waveguides and coupling length.

D. 2. Coupled mode theory: Coupling coefficient and coupling length

Following the work of Okamoto [5], analysis using the perturbation method yields 3 parameters for the coupling between two parallel waveguides. The derivations of coupled mode equations based on the perturbation theory can be found in Appendix B and the results obtained are:

$$\kappa_{pq} = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2 - N_q^2)E_p^* \cdot E_q dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} u_z \cdot (E_p^* \times H_p + E_p \times H_p^*)dxdy} \tag{D.1}$$

$$c_{pq} = \frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} u_z \cdot (E_p^* \times H_q + E_q \times H_p^*)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} u_z \cdot (E_p^* \times H_p + E_p \times H_p^*)dxdy} \tag{D.2}$$

$$\chi_{pq} = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2 - N_p^2)E_p^* \cdot E_p dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} u_z \cdot (E_p^* \times H_p + E_p \times H_p^*)dxdy} \tag{D.3}$$

where *p* and *q* are either (*p,q*) = (waveguide 1, waveguide 2) or (waveguide 2, waveguide 1) respectively. *N* is the effective refractive index, while *Np* and *Nq* are the refractive index of waveguide 1 and 2. Similarly, *E* and *H* are the electric and magnetic fields of the respective waveguides.

κ_{pq} is the mode coupling coefficient and is very important for the calculation of the coupling length and the reflectivity for directional couplers.

c_{pq} is the butt coupling coefficient while the magnitude for χ_{pq} is much smaller than κ_{pq}. Therefore, in most conventional analyses of the directional coupler, c_{pq} and χ_{pq} are neglected and assumed to be $c_{pq} = \chi_{pq} = 0$.

For the coupling coefficient of TE mode in a directional coupler consisting of symmetrical waveguides, the coupling coefficient κ is expressed as

$$\kappa = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty} \left(N^2 - N_2^2\right) E_1^* \cdot E_2 dx}{\int_{-\infty}^{\infty} u_z \cdot (E_1^* \times H_1 + E_1 \times H_1^*) dx} \tag{D.4}$$

The electromagnetic field component of the TE mode is expressed as

$E_x = H_y = 0$ and $H_x = -(\beta/\omega\mu_0)E_y$. and therefore, the following equalities are defined:

$$u_z \cdot (E_1^* \times H_1 + E_1 \times H_1^*) = \frac{2\beta}{\omega\mu_0} \left|E_{1y}\right|^2 \tag{D.5a}$$

$$E_1^* \cdot E_2 = E_{1y}^* \cdot E_{2y} \tag{D.5b}$$

And since $(N^2 - N_2^2)$ is zero outside of waveguide 1, the integration of κ needs to be done only within waveguide 1.

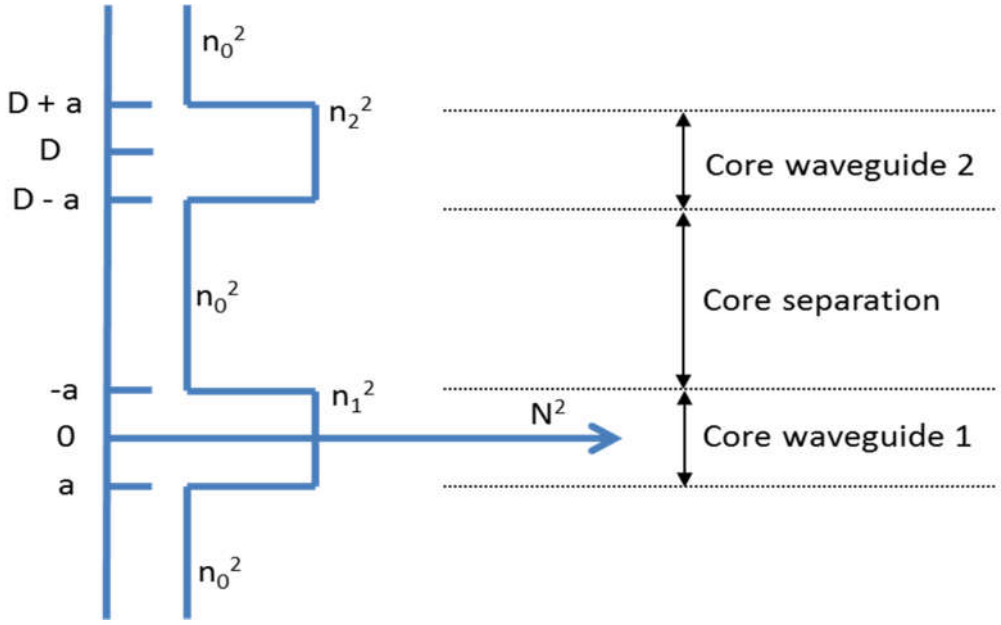

Fig. D.2: Schematic for waveguide 1 and 2 with equal dimension, *a* and the core separation, *D*. The refractive index of core waveguide 1 and 2 are assumed to be identical (N_1=N_2) and the core separation and cladding layers also have the same refractive index (N_0)

The origin of the x-axis is taken at the centre of waveguide 1, as shown in Fig. D.2 above and the core separation is denoted by D. Substituting equation D.5 into D.4, the following equation is obtained.

$$\kappa = \frac{\omega\varepsilon_0\left(N^2 - N_2^2\right)\int_{-a}^{a} E_{1y}^{*}\cdot E_{2y}dx}{\frac{2\beta}{\omega\mu_0}\int_{-\infty}^{\infty}\left|E_{1y}\right|^2 dx} \qquad \text{(D.6)}$$

The electric field components in the slab waveguides 1 and 2 are given by Eq. D.7 and D.8:

$$E_{1y} = \begin{cases} A\cos\left(\frac{u}{a}x\right) & (|x| \leq a) \\ A\cos(u)\, exp\left[-\frac{w}{a}(|x| - a)\right] & (|x| > a) \end{cases} \quad \text{(D.7)}$$

$$E_{2y} = A\cos(u)\, exp\left[\frac{w}{a}(x - D + a)\right] \; (|x| \leq a) \quad \text{(D.8)}$$

Substituting the Eq. D.7 and D.8 into Eq. D.6 and using the eigenvalue equation for TE mode, of the form;

$$w = u\tan(u) \quad \text{(D.9)}$$

Eq. D.6 reduces to

$$\kappa = \frac{k^2}{\beta}(n_1^2 - n_0^2)\frac{u^2w^2}{(1+w)v^4} exp\left[-\frac{w}{a}(D - 2a)\right] \quad \text{(D.10)}$$

The equation can be then be further rewritten by using $\beta \cong kn_1$ and $(n_1^2 - n_0^2) = 2n_1^2\Delta$ to achieve:

$$\kappa = \frac{\sqrt{2\Delta}}{a}\frac{u^2w^2}{(1+w)v^3} exp\left[-\frac{w}{a}(D - 2a)\right] \quad \text{(D.11)}$$

where Δ is a function of the difference in refractive index, D is the distance between the two waveguides and 2a is the thickness or width of the waveguides.

Therefore, based on this equation, the coupling length where 100% power coupling occurs is given by:

$$L_c = \frac{\pi}{2\kappa} \quad \text{(D.12)}$$

Based on equation D.11, we can see that the two main factors that affect the coupling coefficient κ and the coupling length, L_c are:

1. The refractive index of the waveguide core, cladding and core separation.

2. The dimensions of the waveguides and the core spacing between them.

The same principles are applied to a multi-layer stacked waveguide in order to determine the coupling coefficient and the coupling length and the simulation results are discussed in the following section.

D. 3. Multi-layer vertically coupled waveguides

In order to realize a coupled waveguide, two parallel waveguides must be fabricated with a specific core dimensions and core separation. To realize this in the vertical plane, the cladding, core and core separation layers must be stacked on top of each other as shown in the Fig. D.3.

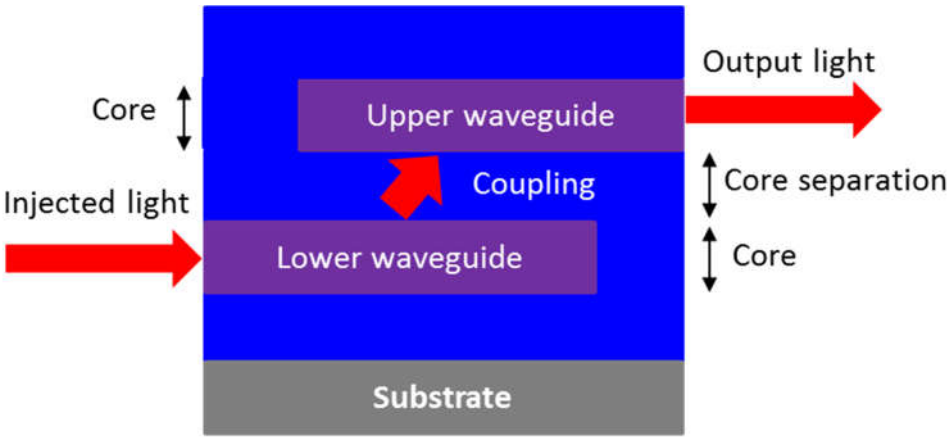

Fig. D.3: Schematic for a vertical coupled waveguide where the injected light enters the lower waveguide, undergoes coupling and exits the upper waveguide

In this work, the upper and lower core waveguides are defined with a refractive index of 1.92 and the cladding and core separation layers have a refractive index of 1.44. Both of the upper and lower core waveguides have a thickness of 300nm and the core separation layer has a thickness of 1.5μm. By using an injected light of 1550 nm, this gives the calculated κ=0.0277μm^{-1}. Therefore, the coupling length of this coupler as obtained from Eq. 2.12 is $L_c = 56.6$ μm.

The coupling waveguides are simulated by using beam propagation method (BPM) and the results are as shown below in Fig. D.4.

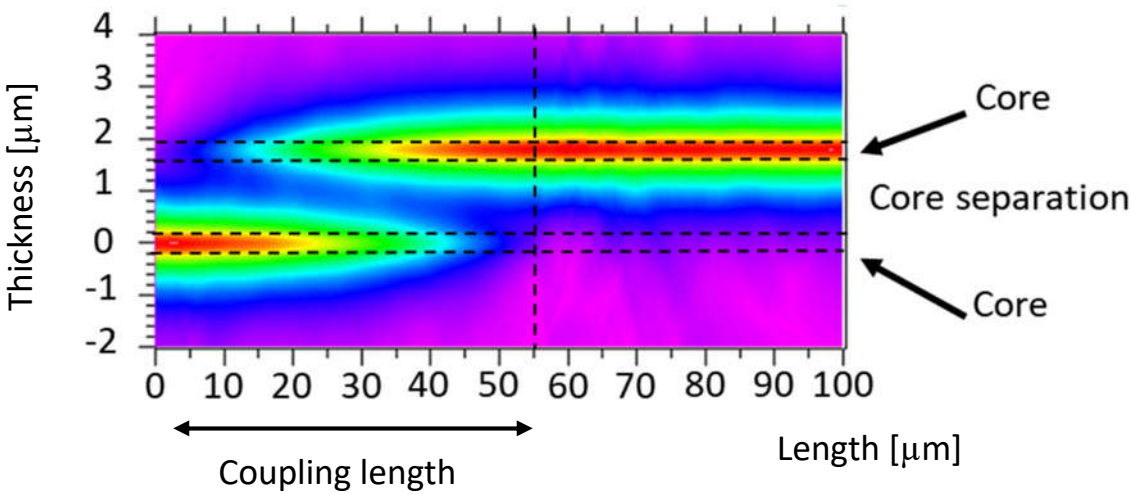

Fig. D.4: BPM simulation results for a coupled waveguide with core thickness of 300 nm and core separation of 1.5 μm. The coupling length is determined to be around 55 μm.

D. 4. Fabrication tolerances for coupled waveguide

As previously stated in section D.1, variations during the fabrication process can have an effect on the performance of the coupling waveguide. Also, based on equation D.12, the dimensions of the waveguide as well as the separation between them influence the coupling coefficient.

One of the issues faced with fabricating a vertical coupling waveguide is the capability to control the thickness of each layer. Therefore, if there are variations in the thickness of each layer, the coupling effect changes. In this section we analyse the effect of a change in the thickness of core as well as the thickness of the core separation layer on the power output and the coupling between the two waveguides.

In the first scenario, we vary the thickness of each core from 150 nm to 450 nm. The simulation results show that in order to have >90% coupling from the lower waveguide to the upper waveguide, the thickness of each core can only be within a ±60 nm tolerance as shown in Fig. D.5. On the other hand, the coupling efficiency show that even if core thickness ranges from 150 nm to 450 nm, the coupling efficiency is still greater than 2dB as seen in Fig D.6.

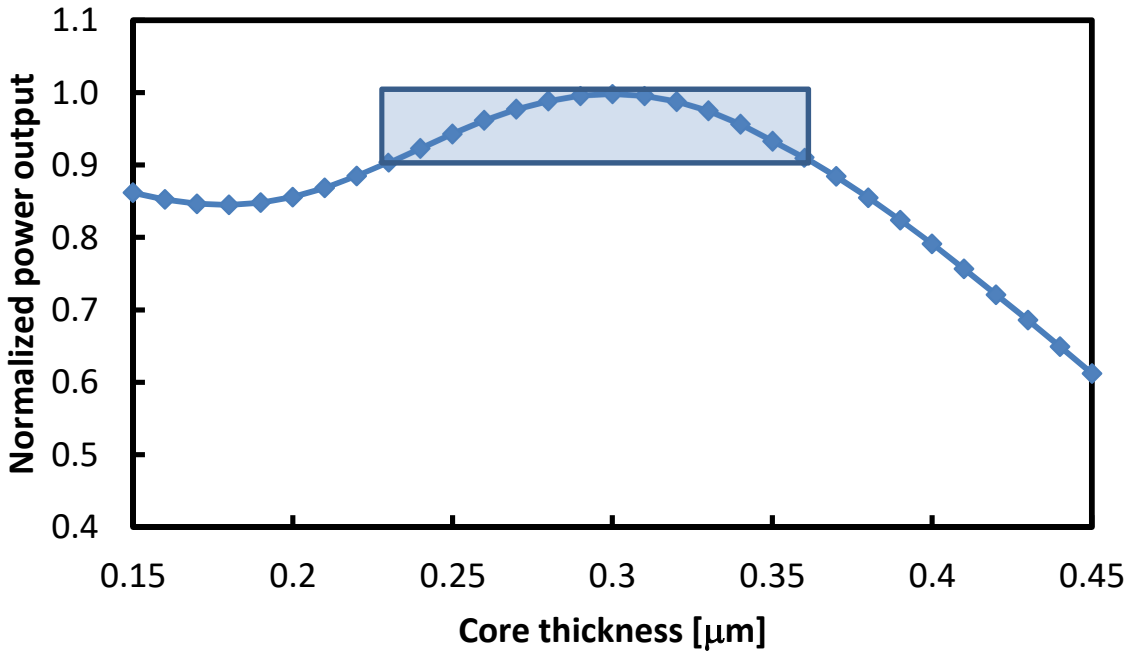

Fig. D.5: Normalized power output of the upper waveguide when the core thickness is varied from 150 nm to 450 nm. The blue highlighted area indicate >90% normalized power output of the upper waveguide.

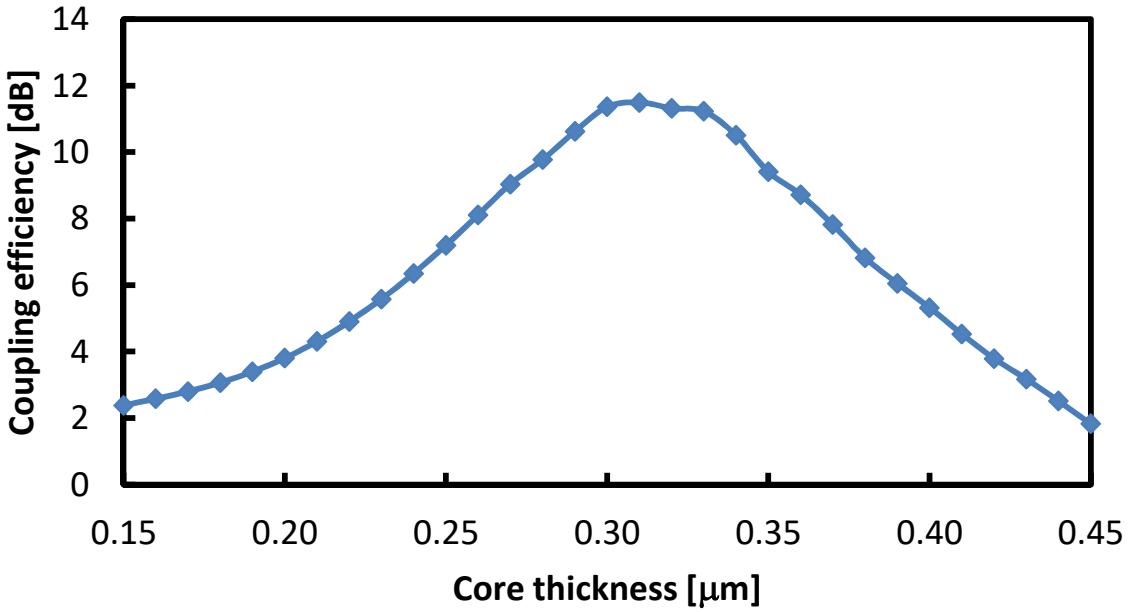

Fig. D.6: Coupling efficiency (dB) when the core thickness is varied from 150 nm to 450 nm.

In the second scenario, we vary the thickness of the core separation layer from 1.0 μm to 2.5 μm and the simulation results show that for >80% power coupling, the fabrication tolerance allows for a core separation thickness to vary from 1.32 μm to 1.72 μm as shown in Fig. D.7 below. Similarly, the coupling efficiency as shown in Fig. D.8 indicate that the coupling efficiency is lower than zero for if the thickness goes thinner than 1.25 μm or thicker than 1.9 μm. Therefore, the fabrication tolerance of ±0.2 μm is acceptable for fabricating the core separation layer.

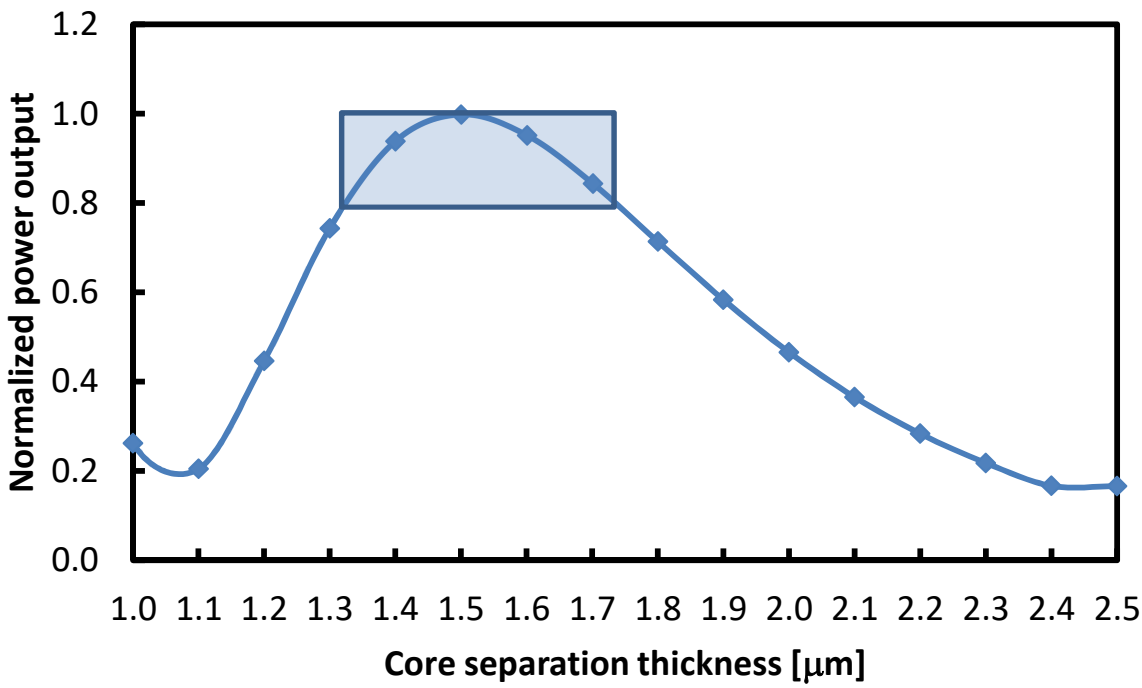

Fig. D.7: Normalized power output of the upper waveguide when the core separation thickness is varied from 1.0 μm to 2.5 μm. The blue highlighted area indicate >80% power output of the upper waveguide.

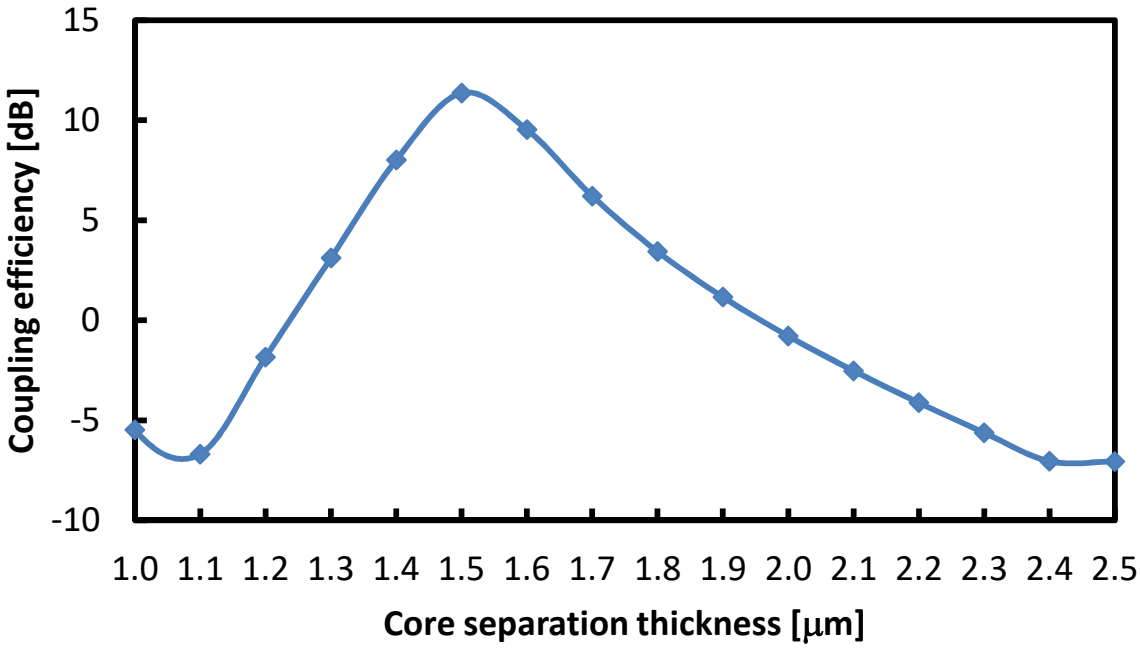

Fig. D.8: Coupling efficiency (dB) when the core separation thickness is varied from 1.0 μm to 2.5 μm.

One assumption that is held throughout the simulation process is that each layer is consistent throughout the entire waveguide. In actuality, this may not be the exact case during the fabrication process. Imperfections such as cracks, voids, and diffusion of one layer into the other can have an adverse effect on the performance of the vertical coupler and will reduce the coupling efficiency further. Some of the imperfections seen during the fabrication process and methods to overcome them are described in detail in the next chapter.

D. 5. Conclusion

In conclusion, in this chapter we have shown an overview of the coupled mode theory for the coupling waveguide. Calculation and simulation done through BPM have shown a coupling length of around 55 μm is achieved for our designed dimensions. Further simulation data show that the fabrication tolerance for variations in both the core thickness and the core separation thickness where data indicates that >90% power coupling can be achieved if the core thickness is kept within a ±60 nm tolerance. For variation in the core separation, a ±200 nm fabrication tolerance is acceptable for a >80% power coupling. The lower size of the design can enable it to be integrated with other photonic devices in a photonic integrated circuit. It is expected that by making use of the multi-layer sol-gel SiO_2 fabrication technique in conjunction with a suitable core material, a vertical coupling waveguide can be achieved.

D. 6. References

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List of abbreviations

Si	Silicon
Ge	Germanium
GaAs	Gallium arsenide
GaN	Galium nitride
N_2	Nitrogen
SiO_2	Silicon dioxide
ZnO	Zinc oxide
TiO_2	Titanium oxide
GeO_2	Germanium oxide
CMOS	Complementary metal oxide semiconductor
III-V	Materials from group III and group V in the periodic table
TE	Transverse electric
TM	Transverse magnetic
SOI	Silicon-on-insulator
GeOI	Germanium-on-insulator
CVD	Chemical vapour deposition
PECVD	Plasma enhanced chemical vapour deposition
MBE	Molecular beam epitaxy
ALD	Atomic layer deposition
SDM	Space division multiplexing

MCF	Multi-core fibre
ICP	Inductively coupled plasma
SF_6	Sulfur hexafluoride
CHF_3	Triflurometh ane
SDM	Space division multiplexing
C_3F_8	Perfluoropropane
MCF	Multi-core fibre
SEM	Scanning electron microsope
TEOS	Tetraethyl orthosilicate
MTES	Methyltriethoxysilane
BHF	Buffered hydrofluoric acid
TLM	Transfer length method

List of symbols

V	Normalized frequency
κ	Dispersion relation
h	Thickness of waveguide core or cladding layer
n_f	Refractive index of film core
n_s	Refractive index of substrate or cladding layer
n_{eff}	Effective refractive index
σ_i	Intrinsic stress
E_s / E_f	Young's modulus of substrate / film
t_s / t_f	Thickness of substrate / film
υ_s / υ_f	Poisson's ratio of substrate / film
$\Delta \frac{1}{r}$	Difference in curvature of the substrate before and after stacking of top layer
$\in_m$	Mismatch of thermal expansion coefficient of layer versus the substrate
M_s / M_f	Ratio of elastic modulus and Poission's ratio of substrate / film
ω	Work of adhesion
A	Hamaker constant
β	Lateral geometry of sample
a_0^n	Geometry of sample